SY22812B

High Frequency QR Flyback Controller with Valley Lockout and E-mode GaN FET Driver

General Description

The SY22812B is a high frequency quasi-resonant (QR) flyback controller designed for PD adaptors and quick chargers. It can drive enhancement GaN FETs directly, and can deliver 240W output power over a wide output voltage range. The 25kHz–300kHz switching frequency allows for reduced transformer and capacitor sizes.

The SY22812B operates using peak current control. It provides a QR mode in which the GaN FET can be turned on at a valley point to reduce switching loss, especially under high input voltages.

In conventional QR flyback solutions, the valley number always varies between 1 and 2 or 3 and 5, which increases V_O ripple and creates audible noise. The SY22812B uses a proprietary circuit to lock the valley number between 1 and 6, for improved stability compared with other conventional QR solutions.

If the load decreases, SY22812B will enter discontinuous conduction mode (DCM) to reduce the switching frequency for higher efficiency. If the load is very light, the SY22812B will enter burst mode to reduce power loss.

The SY22812B provides comprehensive functions to ensure reliable operation, including: HV startup, X capacitor discharge, brown-out protection, output and VCC overvoltage protection (OVP), output undervoltage protection (UVP), internal and external overtemperature protection (OTP), and open-loop protection (OLP).

It is recommended to use the SY23434 as a secondary side Synchronous Rectifier (SR) controller in conjunction with the SY22812B so that Zero Voltage Switching (ZVS) operation can be achieved for higher efficiency.

The SY22812B is available in a SSOP9 package.

Features

- DCM+QR Combined Operating Mode
- Direct Enhancement-Mode (E-mode) GaN FET Driver
- Programmable Gate Driver Current
- 140V Internal LDO on VCCH input pin
- Switching Frequency Range: 25kHz–300kHz
- Automatic Valley Lockout from 1 to 6 cycles
- Low Frequency Burst (1kHz)
- Frequency Modulation to Reduce EMI Noise (Configurable using ZCS Resistor)
- Internal Soft-Start
- Integrated 700V HV Startup
- Brown-In/Out Protections
- X Capacitor Discharge Protection
- Programmable Output OVP and UVP
- Current Sense Resistor Short Protection
- Internal and External OTP
- Compact Package: SSOP9

Applications

- AC/DC Adapters
- PD Adapters
- Quick Chargers

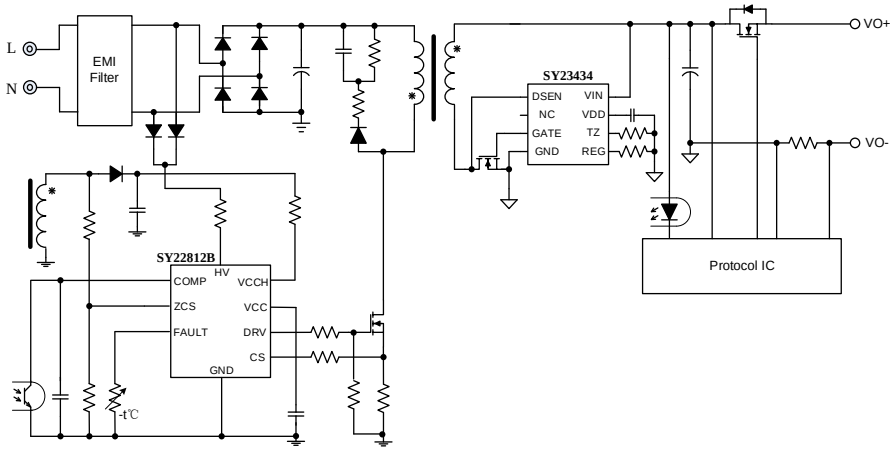


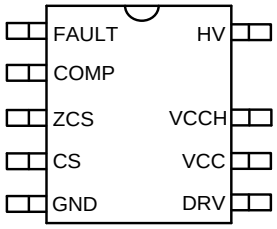
Figure 1. Typical Application Circuit using Synchronous Rectification (SR)

Ordering Information

Ordering Part Number	Package type	Top Mark
SY22812BFVP	SSOP9 RoHS-Compliant and Halogen-Free	**AAGMxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	FAULT	External OTP and V_{OUT} OVP pin.
2	COMP	Compensation voltage of secondary side, connected to an optocoupler.
3	ZCS	Output voltage, input voltage, and QR valley detection pin.
4	CS	Inductor current sensing pin.
5	GND	Ground pin.
6	DRV	Programmable GaN FET gate drive pin.
7	VCC	Power supply pin.
8	VCCH	High voltage power supply pin.
9	HV	HV startup, brown-in/out, X capacitor discharge detection pin.

Block Diagram

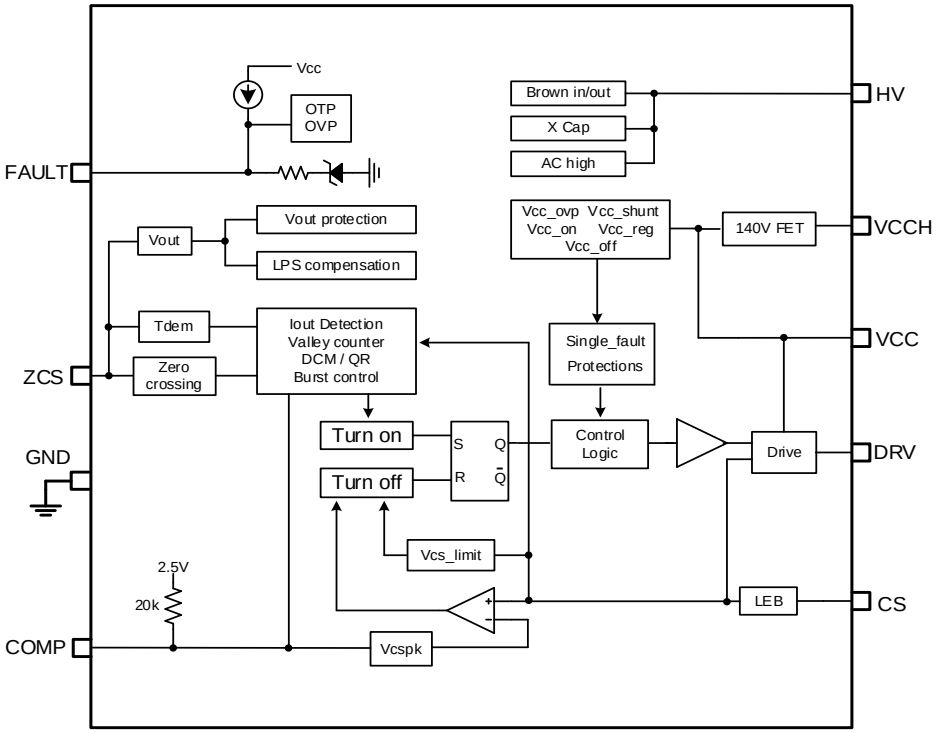


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
HV	-0.3	700	V
VCC	-0.3	30	
VCCH	-0.3	140	
DRV	-0.3	8	
CS, COMP, FAULT	-0.3	4	
ZCS	-1 (Note 1)	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-60	150	
Note1, Dynamic ZCS Negative Voltage in 50μs Duration		-1	V
Note1, Dynamic ZCS Negative Current in 50μs Duration		-2	mA
Human Body Model ESD (HV Pin and VCCH Pin) per ESDA/JEDEC JS-001-2017 (Note 3)		±1	kV
Human Body Model ESD (All Pins Except HV Pin and VCCH Pin) per ESDA/JEDEC JS-001-2017 (Note 3)		±2	kV
Charged Device Model ESD per JS-002-2018 (Note3)		±500	V
Latch-Up Test per JEDEC78E (Note 3)		±100	mA
MSL Rating		3	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		158	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		30	
PD Power Dissipation TA = 25°C		0.79	W

Recommended Operating Conditions

Parameter	Min	Max	Unit
HV	-0.3	700	V
VCC	8	25	
VCCH	9	140	
DRV	4	6	
CS	-0.3	0.5	
ZCS	-0.3	3.0	
COMP	-0.3	2.5	
FAULT	-0.3	3.0	
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	85	°C

Electrical Characteristics

(V_{VCC} = 13V (Note 3), T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
HV	HV Current to Charge VCC	$I_{HV\_CHARGE1}$	V_{HV} = 100V_{DC}, VCC = 0V	0.15	0.3	0.55	mA
			V_{HV} = 100V_{DC}, VCC = 3V	2.6	4.0	5.4	mA
	Current to Discharge X Cap (Note 5)	I_{HV_XCAP}			2.0		mA
	High or Low Voltage Detection	$HV_{TH\_AC\_HIGH}$		200	218	236	V
	AC Low Debounce Time	$t_{AC\_LOW\_DBC}$			40		ms
	Debounce Time to Detect AC Unplug	t_{UNPLUG_DBC}			100		ms
	BO Threshold	HV_{TH_BO}		89	95	103	V
	BI Threshold	HV_{TH_BI}			105		V
	BO Debounce Time	t_{BO_DBC}			100		ms
	BI Debounce Time	t_{BI_DBC}			200		μs
VCC	VCC Turn-On Threshold	V_{CC_ON}	V_{CC} rising	18	20	22	V
	VCC Turn-Off Threshold	V_{CC_OFF}	V_{CC} falling	6.5	7.0	7.5	V
	VCC Short Threshold	$V_{CC\_SHORT\_TH}$		0.5	0.7	0.8	V
	VCCH Regulation Threshold	V_{CC_REG}		10	11	12	V
	VCCH Regulation Hysteresis	V_{CC_REGHYS}			2.0		V
	Protection Timer after Error Trigger	t_{ERROR}			1.0		s
	VCC OVP Threshold	V_{CC_OVP}	V_{VCC} rising	26.4	28.0	29.6	V
	VCC OVP Debounce Cycles	N_{VCCOVP_DBC}			4		
	VCC Shunt Threshold	V_{CC_SHUNT}		25	27	29	V
	VCC Shunt Current Capability	I_{VCC_SHUNT}	VCC > $V_{CC,\ SHUNT}$		10		mA
	Normal Operation Current Consumption	$I_{CC\_OPERATING}$	C_L = open, f_{SW} = 50kHz		1.2		mA
	Standby Current Consumption	$I_{CC\_STANDBY}$	V_{COMP} < $V_{TH\_SLEEP\_IN}$	280	400	520	μA
VCCH	Maximum Voltage	$VCCH_{BV}$		140			V
CS	Maximum Peak Current Limit Threshold if Secondary Side Short	V_{CS_MAX}		685	720	755	mV
	Leading Edge Blanking for V_{CS_MAX}	t_{CS_LEB1}			150		ns

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Delay Time from V_{CS_MAX} to PWM Off	t_{CSMAX_DELAY}			30		ns
	V_{CS_MAX} Debounce Cycles	N_{VCSMAX_DBC}			4		
	V_{CS} Limit	V_{CS_LIMIT1}	AC Low	475	500	525	mV
	V_{CS} Limit	V_{CS_LIMIT2}	AC High	425	450	475	mV
	Leading Edge Blanking Time for V_{PK} Control and V_{CS_LIMIT}	t_{CS_LEB2}			250		ns
	Delay Time from V_{CS_LIMIT} to DRV Falling	t_{CS_DELAY2}			30		ns
	Delay Time from V_{PK} Control to DRV Falling	t_{CS_DELAY3}			30		ns
	V_{CS} Minimum in DCM Mode	V_{CSMIN_DCM}		85	100	115	mV
	Soft-Start Time	t_{SST}			10		ms
	QR Mode Frequency of Modulation	$f_{MODULATION\_QR}$			4		kHz
	V_{CSPK} Modulation Amplitude in QR Mode	$V_{QR\_MODULATION1}$	Valley = 1–3		20		mV
			Valley = 4–6		30		mV
	CS Short-Circuit Protection	V_{CS_SHORT}	t_{ON} = 6.2μs		60		mV
ZCS	OVP Threshold Voltage	V_{ZCS_OVP}		2.36	2.50	2.64	V
	OVP Threshold Voltage Debounce Cycles	N_{ZCSOVP_DBC}			4		
	UVP Threshold Voltage of V_{OUT}	V_{ZCS_UVP}			150		mV
	UVP Threshold Voltage Debounce Time	$t_{VOUTUVP\_DBC}$			20		ms
	Maximum Value of Off Blanking Time	t_{ZCSLEB_MAX}		1.65	2.3	2.95	μs
	Minimum Value of Off Blanking Time	t_{ZCSLEB_MIN}		0.65	0.9	1.3	μs
	Maximum Off-Time	t_{OFF_MAX}		90	120	150	μs
	Zero-Cross Point Detect	V_{ZCS_ZERO}			0		mV
	QR Turn-On Delay Time	$t_{ZCS\_ONDELAY}$			100		ns
Fault	Current Source for OTP Detection	I_{OTP}		42.5	45	47.5	μA
	OTP Threshold	V_{OTP_TH}		0.37	0.4	0.43	V
	OTP Exit Threshold	$V_{OTPEXIT\_TH}$			0.43		V
	Clamp Diode for OVP	$V_{OVPDIODE}$		1.00	1.20	1.40	V
	Capability of Clamp	$I_{RFAULTOVP}$			1		mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Diode for OVP						
	OVP Threshold	V_{OVP_TH}			2.5		V
	Debounce Time to Trigger OTP/OVP	$T_{FAULTOTP/OVP\_DBC}$	$V_{FAULT} < V_{OTP\_TH}$ $V_{FAULT} > V_{OVP\_TH}$		200		μs
COMP	Internal Pullup Voltage Source	V_{COMP_PULLUP}		2.2	2.5	2.8	V
	Internal Pullup Resistor	R_{COMP_PULLUP}			20		kΩ
	V_{CS_LIMIT} Point	V_{COMP_LIMIT}			1.9		V
	QR Mode to DCM Change Threshold	V_{COMPTH_DCM}			1.0		V
	Hysteresis of QR Mode to DCM	V_{COMPTH_DCMHYS}			0.1		V
	Minimum Switching Frequency Threshold	V_{COMP_FMIN}		0.55	0.7	0.85	V
	Enter Burst Mode Threshold	$V_{COMP\_BURSTIN}$	V_{COMP} falling	0.19	0.25	0.31	V
	Exit Burst Mode Threshold	$V_{COMP\_BURSTOUT}$	V_{COMP} increasing		0.45		V
	Start PWM Threshold in Burst Mode	$V_{COMP\_BURSTSTART}$	V_{COMP} increasing		0.35		V
	Burst Frequency	$V_{COMP\_BURSTFREQ}$			1		kHz
	OLP Threshold	V_{COMP_OLP}	V_{COMP} rising	1.95	2.2	2.45	V
DRV	High Voltage Clamp	V_{DRV-CS_CLAMP}		5.5	5.8	6.1	V
	Programmable Driver Current	I_{DRV}	DVR-GND: 43kΩ		5		mA
			DVR-GND: 22kΩ		10		mA
			DVR-GND: 10kΩ		20		mA
			DVR-GND: < 2kΩ		Not supported		
	Sink Current	I_{DRV_SINK}			600		mA
	t_{ON_MAX}	t_{ON_MAX}		14	20	26	μs
	Frequency Limit in DCM Mode	f_{LIMIT_DCM}			75		kHz
	Frequency Minimum in DCM Mode	f_{MIN_DCM}		20	25	32	kHz
	DCM Mode Modulation Frequency	$f_{MODULATION\_DCM}$			250		Hz
	Minimum Valley Number in QR Mode	$VALLEY_{NUMBER}$	HV < 218V	1		6	
			HV > 218V	1		6	
Internal OTP	OTP Threshold	$T_{OVP\_SHUNTDOWN}$			150		°C
	Recovery Threshold	$T_{OVP\_RECOVERY}$			130		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.
Note 3: Meets ESDA/JEDEC JS-001-2017 and JEDEC78E.
Note 4: Production tested at 25˚C. Limits are guaranteed by design, test or statistical correlation.
Note 5: Increase VCC pin voltage gradually higher than V_{CC_ON} voltage, then reduce it to 13V.

Detailed Description

HV Startup and Power Supply

The HV pin charges the VCC capacitor at AC power-on. When VCC voltage rises above the startup threshold, the HV circuits will be turned off to reduce power loss.

HV will charge the VCC and VCCH pins together during AC power-on. The suggested value for the VCCH and VCC capacitors are 10μF and 1μF, respectively which enables a small total solution size.

In situations when the device enters protection mode, the PWM operation is stopped for a t_{ERROR} time. Because of the power consumption during t_{ERROR}, the VCC and VCCH capacitor voltages will drop. When VCC falls to V_{CC_REG}, HV circuitry is enabled again to charge the capacitors until VCC > (V_{CC_REG} + V_{CC_REGHYS}). After t_{ERROR}, the internal logic will be reset, and a restart sequence is initiated.

QR Mode (Automatically Selected Valley Number between 1 and 6)

In QR mode, PWM turns on at the valley point of the GaN FET drain voltage. This improves EMI and efficiency. V_{CSPK} is controlled by V_{COMP}, and the valley number is controlled by the output load. When V_{COMP} is higher than (V_{COMP_THDCM} + V_{COMPTH_DCMHYS}), QR mode is enabled and on the 6th valley number. As the load increases, the valley number decreases in one-step increments until it reaches the minimum value.

Valley Detect

The waveform in Figure 3 shows the valley detection method. When the falling edge of the zero-crossing voltage appears at the ZCS pin, the SY22812B will turn on the GaN FET after a delay.

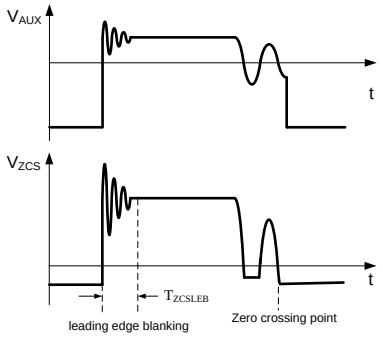


Figure 3. Valley Detection

Noise is present at the ZCS pin when the GaN FET turns off, which may affect valley detection. The SY22812B uses a blanking time to avoid noise interference, which is described in the Output OVP and UVP section.

DCM Mode

When V_{COMP} is lower than V_{COMPTH_DCM}, DCM mode is enabled. In DCM mode, V_{CSPK} and the switching frequency is controlled by V_{COMP}. PWM turns on instantly at f_{SW} and does not wait for the valley point. As load decreases, frequency first decreases from $f_{LIMIT,DCM}$ to $f_{MIN,DCM}$, and the part operates in PFM mode to maintain high efficiency. When the frequency has decreased to $F_{MIN,\ DCM}$ and load continues decreasing, V_{CSPK} begins decreasing to keep constant output voltage.

Burst Mode

When frequency and V_{CSPK} have all decreased to respective minimum values, if the output load continues decreasing, V_{COMP} will be lower than $V_{COMP\_BURSTIN}$. In this case the device starts operating in Burst mode. PWM will start when V_{COMP} is higher than $V_{COMP\_BURSTSTART}$. The PWM number of switching cycles is controlled by t_{BURST} in order to keep burst frequency lower than the set value. PWM operation will continue until the set number cycles are completed. PWM then stops and waits for the next rising edge of $V_{COMP\_BURSTSTART}$. With this method, the burst frequency is low and audible noise is reduced.

When V_{COMP} is higher than $V_{COMP\_BURSTOUT}$, the SY22812B will enter DCM mode.

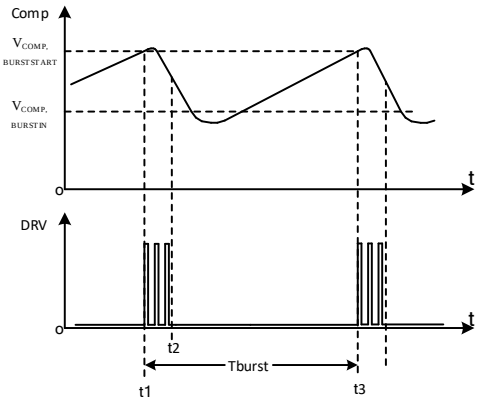


Figure 4. Quiet Burst

VCCH Power Supply

In order to simplify external circuits, the SY22812B includes an internal LDO connected to the VCCH pin with a maximum voltage of up to 140V. When VCC is lower than V_{CC_REG}, VCCH will charge the VCC capacitor through an internal circuit. When VCC is higher than (V_{CC_REG} + V_{CC_REGHYS}), VCCH will stop charging.

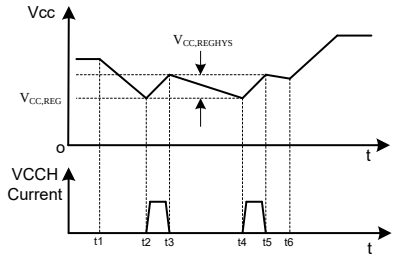


Figure 5 VCCH Charge Function

If high efficiency is important and slightly increasing the BOM cost is acceptable, two windings can be used to reduce VCC loss. As shown in Figure 6, if V_{OUT} is low, Na3 voltage is too low and VCCH charges VCC. If V_{OUT} is high, Na3 voltage is high enough and VCCH will be floating. A resistor and Zener diode in parallel with C11, can be used to clamp the high voltage coming from Na1's leakage inductance. The recommended value for R25 is 1kΩ. D25's clamp voltage should be higher than Na1 voltage and lower than C11 rated voltage.

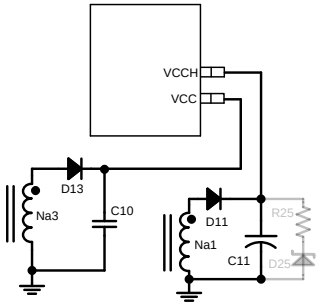


Figure 6. Typical Circuit for High Efficiency Application

Figure 7 shows a single winding solution. The recommended value for C10 is 1μF. The parallel resistor and Zener diode for C11 are not needed.

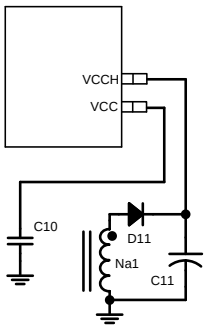


Figure 7. Typical Circuit for One Winding Application

During the X capacitor discharge process, C10 voltage may be charged to V_{CC_SHUNT}. In this case, a 35V capacitor voltage rating is recommended.

X Capacitor and Frequency Modulation Configuration using the ZCS Resistor

The frequency modulation and X capacitor discharge functions can be selected using the ZCS resistor. When X capacitor is enabled, HV should be connected to the AC line via two diodes. When the X capacitor is disabled, HV can be connected to V_{BUS} to eliminate the diodes and reduce solution cost.

ZCS resistors configuration:

ZCS Pulldown (R8)	X Capacitor Function	Frequency Modulation
15-16kΩ ±1%	Disabled	Disabled
8.2kΩ ±1%	Enabled	Disabled
4.3kΩ ±1%	Disabled	Enabled
2.0-2.2kΩ ±1%	Enabled	Enabled

The ZCS_OVP threshold is 2.50V. With R8 selected, R7 can be calculated according to V_{OUT_OVP} and Na/Ns. The resistor R4, in series with CS should be adjusted as well. If I_{OUT_OLP} (Selected by customer) increases according to V_{AC} rising, the value of R4 should be increased for more compensation.

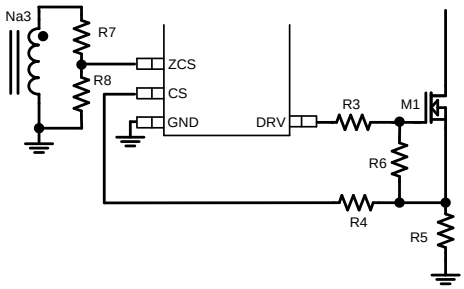


Figure 8. X Capacitor and Frequency Modulation using ZCS Resistor

Programmable Drive Current

During turn-on, the SY22812B uses constant current to charge the input M1 capacitance, Cgs, and improve EMI performance. During turn-off, the DRV pin will be pulled down quickly to reduce turn-off loss. Traditional drive resistors and diodes are not required. R3 is used to make slight adjustments to the turn-off speed. The recommended value of R3 is 5Ω–20Ω.

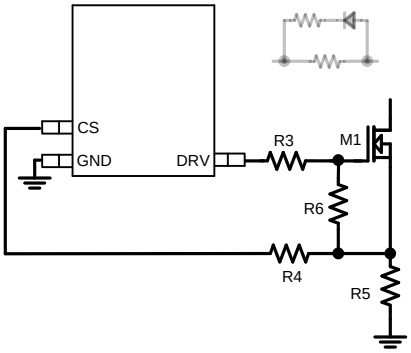


Figure 9. Drive Circuit of GaN FET

At turn-on, the constant current value can be selected using R6 based on the table below:

R6	Constant Current
10kΩ	20mA
22kΩ	10mA
43kΩ	5mA
<2kΩ	Not Supported

The device enters protection mode for R6 values below 2Kohm where PWM switching is disabled.

Using a lower current, the GaN turn-on speed will be slower and EMI performance will be better. R6 value is measured during startup, and the current value is fixed until the following startup.

Frequency Modulation

In QR mode, the SY22812B adds a triangle voltage on V_{CS} for frequency modulation. If the valley number is between 1 and 3, the modulation amplitude is set to 20mV. If the valley number is between 4 and 6, the modulation amplitude is set to 30mV in order to obtain an effective range of frequency modulation.

Soft-Start

At startup, when V_{COMP} rises to $V_{COMP\_BURSTSTART}$, PWM operation starts and V_{CS} increases from the minimum value linearly. Under heavy load or V_{OUT} short conditions, soft-start will terminate after T_{SST}. Under light load or no-load conditions, when the V_{CS} value determined by V_{COMP} is lower than the value determined by soft-start, soft-start will terminate and V_{COMP} will control V_{CS}.

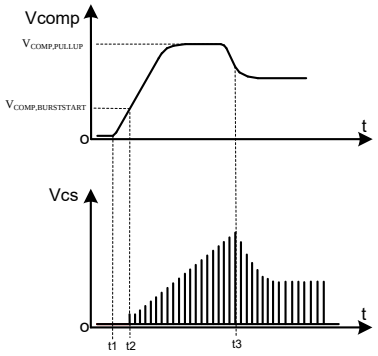


Figure 11. Soft-Start Process

Under startup or V_{OUT} short conditions, V_{OUT} and ZCS are very low. If ZCS cannot detect an effective valley signal, t_{OFF_MAX} will be enabled. This is helpful to reduce deep CCM switching and reduce the voltage stress on the SR MOSFET V_{DS}.

V_{CS_LIMIT}

After t_{CS_LEB2} in every cycle, when V_{CS} is higher than V_{CS_LIMIT}, PWM will turn off immediately. The decision is made cycle by cycle and won't affect next cycle's PWM on time.

V_{CS_MAX}

Under normal operating conditions, V_{CS_LIMIT} can limit GaN peak current and provide sufficient protection. When the transformer winding or the secondary diode short circuits, the current slope is very high and the transformer will enter saturation state. The current can rise to a much higher level during t_{CS_LEB2}.

The SY22812B can detect V_{CS} after t_{CS_LEB1}, which is shorter than t_{CS_LEB2}. If V_{CS} is higher than V_{CS_MAX} for four consecutive cycles, PWM operation stops and the timer starts. After t_{ERROR}, the logic is reset and a restart is triggered, with HV charging VCC to V_{CC_ON}.

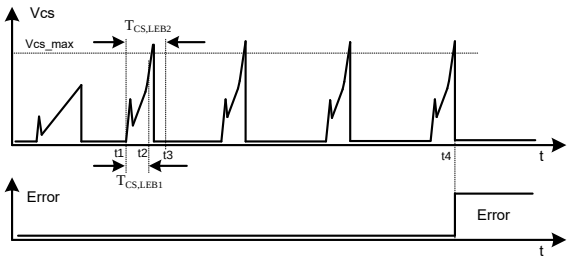


Figure 12. V_{CS_MAX} Process

Brown-In and Brown-Out

When input voltage is lower than 90V AC, current and heat dissipation on the transformer and primary GaN FET are very high. The SY22812B provides brown-in (BI) and brown-out (BO) protections to protect the power supply. Brown-in and brown-out are defined as follows:

- BI: HV voltage is higher than $HV_{TH,BI}$ and lasts for $t_{BI,DBC}$.
- BO: HV voltage is lower than $HV_{TH,BO}$ and lasts for $t_{BO,DBC}$.

After a BO event, PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

X Capacitor Discharge

Under light load, when the charger is unplugged from the AC source, there may be remaining high voltage on the input terminals, which can represent a safety concern.

The SY22812B uses the HV pin to discharge the X capacitor. HV is connected to the AC side through R1, D1, and D3. The recommended R1 value is 5kΩ–10kΩ, which protects against surge voltages on the AC line.

If there is no HV rising edge for continuous time t_{UNPLUG_DBC}, an AC unplug condition is detected and PWM stops. HV sources an I_{HV_XCAP} current to the VCC pin. As a result, VCC rises to V_{CC_SHUNT} and HV falls linearly. When VCC becomes lower than V_{CC_OFF}, the discharge stops.

The voltage rating of the VCC capacitor should be higher than V_{CC_SHUNT}. A 35V voltage rating is recommended.

During X capacitor discharge, when a rising edge on HV (indicating AC re-plug) is detected, the discharge is terminated immediately. The t_{ERROR} timer continues. During t_{ERROR}, HV keeps VCC between V_{CC_REG} and (V_{CC_REG} + V_{CC_REGHYS}). After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

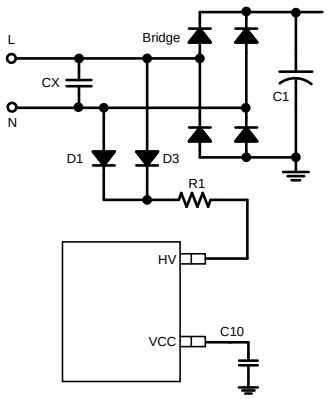


Figure 13. X Capacitor Discharge Circuit

Figure 14 shows the discharge waveforms:

- At t1, AC unplug occurs.
- At t2, AC unplug is confirmed. PWM stops and HV sources current to VCC.
- At t3, VCC rises to V_{CC_SHUNT}.
- At t4, X capacitor discharge current is lower than VCC dissipation and VCC begins falling.
- At t5, VCC is lower than V_{CC_OFF} and the discharge stops.

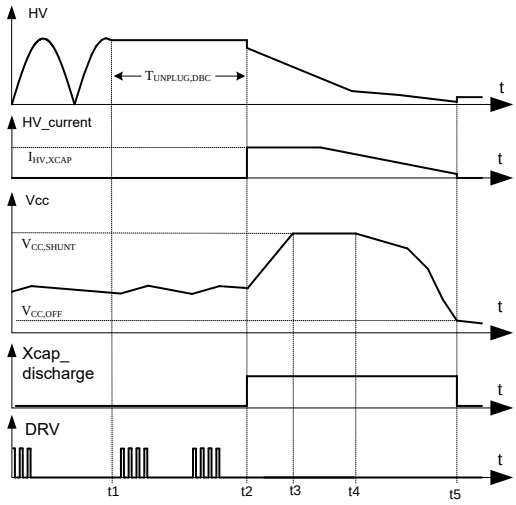


Figure 14. X Capacitor Discharge Waveforms

Output OVP and UVP

The SY22812B detects the output voltage through the ZCS pin and provides output overvoltage protection (OVP) and undervoltage protection (UVP). When the primary GaN FET turns off, there is a parasitic resonance on AUX winding. The SY22812B uses blanking time to avoid false triggering. Blanking time is adaptive according to V_{CSPK}. When V_{CSPK} is below 200mV, primary current is low and energy stored in leakage inductance is also low. Parasitic resonance on auxiliary winding will be shorter, and blanking time is also shorter. Blanking time increases to the maximum value as V_{CSPK} rises to 500mV.

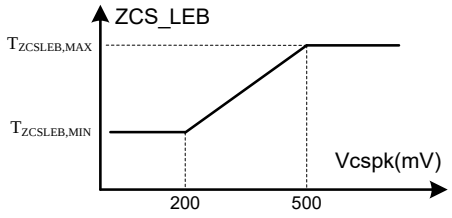


Figure 15. ZCS Blanking Time

When ZCS voltage is higher than V_{ZCS_OVP} for N_{ZCSOVP_DBC} cycles, ZCS_OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

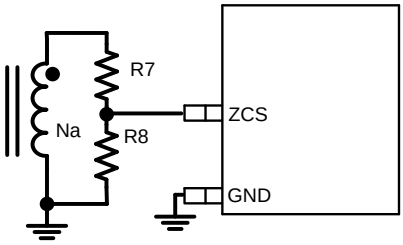


Figure 16. ZCS OVP Setting

Output OVP threshold is calculated as follows:

$$V_{OUT\_OVP} = V_{ZCS\_OVP} \times \frac{R7 + R8}{R8} \times \frac{Ns}{Na}$$

When ZCS voltage is lower than V_{ZCS_UVP} continuously for a $t_{VOUTUVP\_DBC}$ period, ZCS_UVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

Note: The pulldown resistor R8 value should be selected first, based on use of the X capacitor and frequency modulation settings. Then, R7 should be calculated according to the above equation. UVP is used to avoid continuous operation under V_{OUT} short circuit conditions and is not mandatory for the design.

VCC OVP

The SY22812B provides VCC overvoltage protection (OVP) to protect the IC from abnormal high voltage caused by an open feedback loop or improper N_A winding. When VCC rises to V_{CC_SHUNT} and external power current capability is higher than the shunt ability, VCC can continue rising.

VCC is continuously monitored. If VCC is higher than V_{CC_OVP} for four continuous cycles, VCC OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

If the error condition still exists after restart, the IC will operate in hiccup mode.

Open-Loop Protection

If the output is short-circuited, the optocoupler circuit is open, or the load increases too much, V_{COMP} will increase. When V_{COMP} is higher than V_{COMP_OLP} and lasts for t_{OLP_DBC}, open-loop protection (OLP) is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

FAULT OTP and OVP

The FAULT pin can be used for detecting OVP and overtemperature protection (OTP) conditions. During normal operation, the current of I_{OTP} is clamped by D12. D12's clamp voltage is selected to be between the OTP threshold and OVP threshold. Therefore, neither protection is triggered.

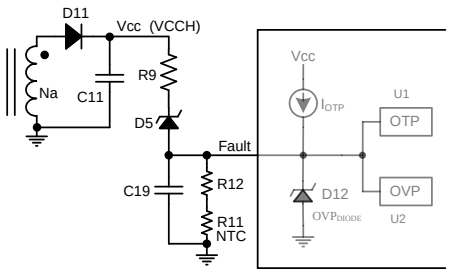


Figure 17 Fault OTP and OVP

Under error conditions, VCC or VCCH will rise. In this case if D5 also fails, the pullup current might be higher than D12's clamp ability and the FAULT pin voltage will increase. When the FAULT pin is higher than V_{OVP_TH} and lasts for $T_{FAULTOTP/OVP\_DBC}$, FAULT OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

R11 is a negative temperature coefficient (NTC) resistor. As temperature rises, R11 resistance falls. When R11 resistance is low enough, there will be no current flowing into D12 and the I_{OTP} current will flow into R11. As I_{OTP} does not change, FAULT voltage will fall along with R11 resistance. When FAULT voltage is lower than V_{OTP_TH}, FAULT OTP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}. After restart, the FAULT pin is monitored, and PWM will not begin until FAULT voltage is higher than $V_{OTPEXIT\_TH}$.

R9 is used to limit the current flowing into the FAULT pin. The OVP threshold is primarily decided by D5 breakdown voltage. R12 is used to adjust the OTP threshold. C19 is used to filter noise, with a recommended value of 100pF.

CS Pin Short Circuit

During t_{ON} of every PWM cycle, V_{CS} is sampled every 4μs and compared with V_{CS_SHORT}. If $V_{CS} < V_{CS\_SHORT}$, short-circuit protection is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

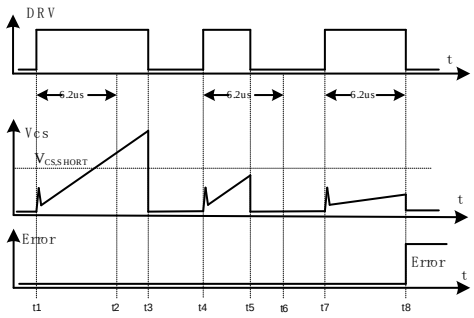


Figure 18. CS Short Protection

Figure 18 shows the short-protection logic:

- At t2, V_{CS} is higher than V_{CS_SHORT}. No protection.
- At t5, the 6.2μs timer has not expired. No comparison is needed. No protection.
- At t8, V_{CS} is lower than V_{CS_SHORT} at 6.2μs mark. Protection is triggered.

Internal OTP

The SY22812B continuously monitors the die temperature during normal operating. When the die temperature rises above the OTP threshold, PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

Design Guide

BUS Capacitor Calculation

Generally, bulk capacitor CBUS is selected according to the following rules:

- No PFC: 1.5–1.8uF per watt (Output power).
- With PFC: 0.5–0.8uF per watt (Output power).

Minimum BUS Voltage Calculation

Minimum BUS voltage appears when input voltage V_{AC} is lowest and output current reaches its rated value. When there is no power factor correction (PFC) circuit before the flyback, minimum BUS voltage is calculated as follows:

$$V_{BUS\_MIN} = \sqrt{2V_{IN\_MIN}^2 - \frac{P_O(1-K_{CH})}{\eta C_{BUS} f_o}}$$

where KCH is the BUS capacitor charge coefficient (generally KCH is set to 0.2–0.3), η is conversion efficiency, and f_o is the AC input frequency.

When selecting the necessary capacitors, the following aspects have to be considered: The actual capacitance for aluminum capacitors is only 85-90% of nominal value and component tolerance has to be taken into account.

The following examples are helpful for fast selection and can be used as a reference.

For a 30W solution, with no boost PFC circuit. Bus nominal capacitance is 27 + 27μF. V_{BUS_MIN} is as follows:

Output Power	30W	35W	40W	45W
AC90V 50Hz	86V	80V	75V	68V
AC90V 60Hz	93V	87V	83V	78V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

For a 66W solution, no boost PFC circuit. Under full load 20V, 3.3A, V_{BUS_MIN} is as follows:

Bus Nominal Capacitance	82+22 μF	82+10μ F	82μF	68μF
AC90V 50Hz	82V	78V	72V	60V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

For a 140W solution, boost + flyback topology. Output is 28V, 5A. Bus nominal capacitance is 39+39uF.

At AC90V 50Hz, boost PFC outputs DC240V. V_{BUS} is 222V(min) to 253V(max). Ripple is 31V.

At AC176V 50Hz, boost PFC outputs DC350V. V_{BUS} is 338V(min) to 362V(max). Ripple is 24V.

Transformer Parameters Calculation

1. Primary/secondary turns ratio: N_{PS}

N_{PS} is limited by voltage stress on the primary GaN FET:

$$N_{PS} \le \frac{V_{MOS\_BR}K_{DR} - \sqrt{2}V_{IN\_MAX} - \Delta V_{SN}}{V_O + V_{D\_F}}$$

where V_{MOS_BR} is the breakdown voltage of the primary GaN FET; KDR is the V_{DS} de-rating factor of the power MOS; $V_{IN,MAX}$ is always AC264V; V_{D_F} is the forward voltage of the secondary rectification diode (If SR is used on the secondary side, use V_{D_F} = 0); ΔVSN is the voltage spike at primary GaN turn-off. A starting value of 50V can be used for the calculation.

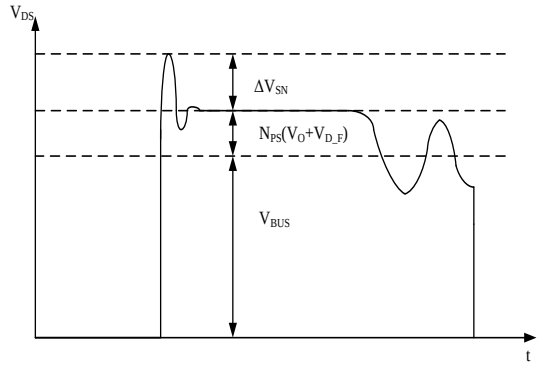


Figure 19. Primary V_{DS} Waveform

After N_{PS} is determined, the reflected voltage can be calculated as follows:

$$V_{OR} = N_{PS} \times (V_O + V_{D\_F})$$

2. Primary Inductance: LP

The SY22812B provides operates in QR and DCM modes (CCM is not available). The transformer primary inductance is mainly related to switching frequency. With V_{BUS} being at its minimum value, L_P can be calculated as follows:

$$L_P = \frac{1}{2 \times F_{SW\_MIN} \times V_O \times I_O \times} \times \left(\frac{V_{BUS\_MIN} \times V_{OR}}{V_{BUS\_MIN} + V_{OR}}\right)^2$$

where V_O is the output voltage and the unit is V; N_{PS} is the primary/secondary turns ratio; V_{BUS_MIN} is the minimum voltage after the bridge (V); f_{SW_MIN} is the frequency at V_{BUS_MIN} (kHz); I_O is the output current (A); L_P is the primary inductance (mH).

In the parameters, V_O, N_{PS}, V_{BUS_MIN} and I_O have been determined. Only F_{SW_MIN} needs to be selected. When f_{SW_MIN} is higher, L_P will be lower. The frequency for AC230V designs will also be higher.

For a typical application, f_{SW_MIN} is approximately 100kHz-130kHz, at V_{BUS_MIN} (usually 80V-90V). Then, frequency at V_{BUS_MAX} (370V) is approximately 160kHz-220kHz.

3. Turns of primary winding: N_P

(a) Select the magnetic core, confirm the effective core area (AE)

(b) Select B_{MAX} for the magnetic core (0.32T–0.36T)

(c) Calculate primary R_{CS} (preliminary):

$$R_{CS} = \frac{V_{CS\_LIMIT} \times N_{PS} \times V_{BUS\_MIN}}{2 \times I_{OUT\_OLP} \times (V_{OR} + V_{BUS\_MIN})}$$

Where V_{CS_LIMIT} is 0.5V and I_{OUT_OLP} is the overload protection threshold, which is selected based on the maximum current that the converter needs to deliver. For example when the maximum current required is 3A, a value of 3.5A can be used for I_{OUT_OLP}

(d) Calculate maximum primary peak current

$$I_{PPK\_MAX} = \frac{V_{CS.LIMIT}}{R_{CS}}$$

(e) Calculate primary turns: N_P

$$N_P = \frac{L_P \times I_{PPK\_MAX}}{B_{MAX} \times A_E}$$

4. Turns of secondary winding: NS

$$N_S = \frac{N_P}{N_{PS}}$$

In the actual design, F_{SW_MIN} is difficult to determine. If a random value is selected, later calculations may be difficult and this may be unsuitable to the transformer bobbin. The following flow is suggested, for reduced number of iterations and predictable results:

1. Select transformer and AE
2. Determine winding width of the bobbin
3. Select N_S wire gauge
4. Determine N_S
5. Determine V_{OR} and N_{PS}
6. Calculate N_P
7. Select N_P wire gauge
8. Calculate R_{CS}
9. Calculate I_{PPK_MAX}
10. Determine B_{MAX}
11. Calculate L_P

With this procedure, f_{SW_MIN} is not an input parameter. When L_P is calculated, the switching frequency f_{SW} is determined as well. This will always lead to a satisfactory design, and efficiency will always be close to optimal for a given transformer.

5) Turns of auxiliary winding: N_A

For fast charge applications, V_{OUT} range is wide. Turns of AUX winding should take V_{OUT_MAX} and V_{OUT_MIN} into consideration.

Increasing efficiency is possible by using two AUX windings if a slight increase in BOM cost is acceptable.

- AUXL can supply V_{CC} at V_{OUT_MAX}.
- $18V < \frac{V_{OUT\_MAX}}{N_S} \times N_{AUXL} < 22V$

- AUXH can supply V_{CC} at V_{OUT_MIN}.
- $10V < \frac{V_{OUT\_MIN}}{N_S} \times N_{AUXH} < 14V$

In low-cost applications, one winding is enough, which is AUXH. The number of turns for the AUXH winding is the same as N_{AUXH} in the above formula.

Secondary Rectifier MOSFET Selection

Under the conditions of V_{BUS_MAX} and V_{OUT_OVP}, the reverse voltage of the secondary rectification MOSFET will reach its maximum level. The maximum voltage (ignoring the voltage spike when the primary MOSFET is turned on) is calculated as follows:

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP}$$

Maximum instantaneous forward current is calculated as follows:

$$I_{SPK\_MAX} = I_{PPK\_MAX} \times N_{PS}$$

For a 66W (20V, 3.3A) solution, BSC098N10NS5 is recommended, which has 100V, 8.2mΩ (V_{GS} = 10V) ratings.

For a 90W (20V, 4.5A) solution, BSC0805LS is recommended, which has 100V, 6.0mΩ (V_{GS} = 10V) ratings.

For a 120W (20V, 6.0A) solution, two MOSFETs in parallel are recommended, primarily for heat dissipation. Using two BSC098N10NS5, which is 100V, 8.2mΩ (V_{GS} = 10V) ratings.

Ensure that the MOSFET selected can handle the dissipated heat without exceeding the target acceptable temperature increase. Validate the design performing temperature measurements under worst case load and ambient temperature conditions.

Layout Considerations

Follow these PCB layout guidelines for optimal performance and EMI considerations:

Signals are grouped in two categories:

- Switching nodes: primary drain/AUX/core; secondary drain/AUX/core.
- Important signal nodes (easy to be disturbed):
  - Primary: V_{CS}, FAULT, comp, ZCS, f_{MAX} etc.
  - Secondary: REG, TZ (TZ pin of SY23434), feedback loop, etc.
- To guarantee normal operation, important signal nodes should be far away from switching nodes. If PCB routing is difficult, static nodes should be used as shielding between switching and signal nodes. Static nodes can be V_{BUS}, GND, VCC, VCCH, V_{OUT}, SGND, etc.
- In order to optimize EMI performance, switching nodes on the PCB layout should be as small as possible. Switching nodes should not be selected for heat sinking, such as GaN drain.
- In order to obtain good EMI performance, the main current loop should be as small as possible.
  - Current path during t_{ON}: bus capacitor → transformer → GaN → R_{CS} → GND → bus capacitor
  - Current path during t_{OFF} time: transformer → SR_MOS → C_{OUT} → GND → transformer
  - Current in leakage inductance and snubber circuit
  - Drive loop of primary and secondary MOSFETs
- Place these components near SY22812B:
  - Fault capacitor, comp capacitor, f_{MAX} resistor, CS resistor (in series), VCC capacitor.
  - ZCS pullup resistor should be placed near the AUX pin of the transformer, and pulldown resistor should be near the ZCS pin.
- The REG and TZ resistors, V_{DD} and V_{IN} capacitors should be close to SY23434.
- GND routing is as follows:
  - SY22812B's GND should be connected to RCS_GND in order to get accurate V_{CS} signal.
- Because $V_{GS(TH)}$ of the GaN FET may be as low as 1.2V, it can easily be falsely triggered by noise.
  - Connect IC_GND to RCS_GND directly.
  - Keep the drive loop as small as possible.

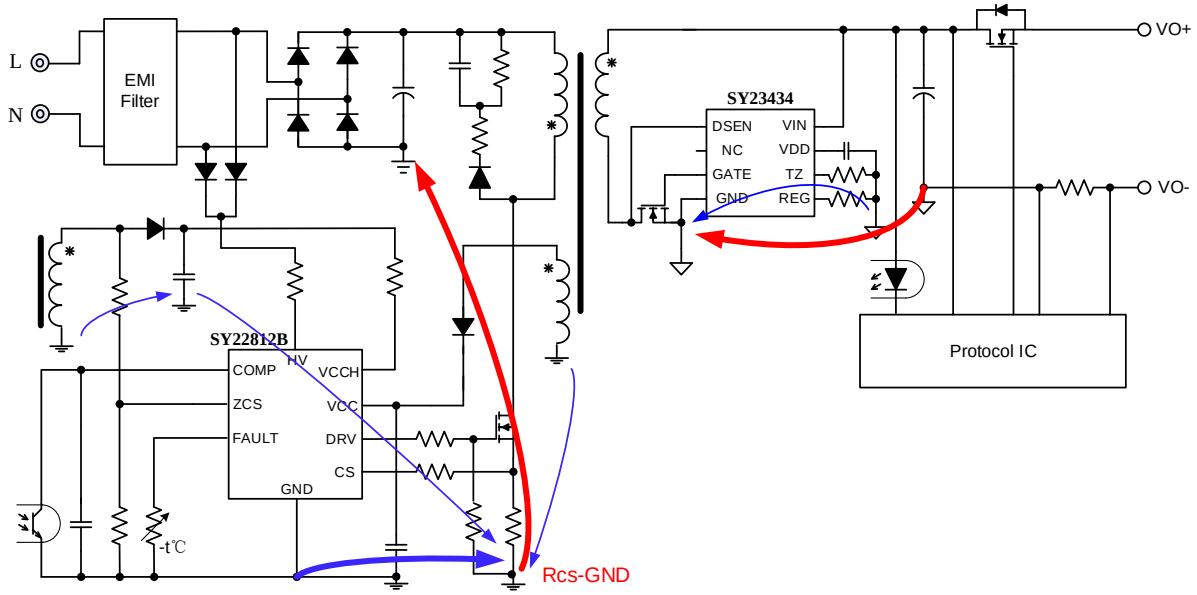


Figure 20. Recommended PCB Layout

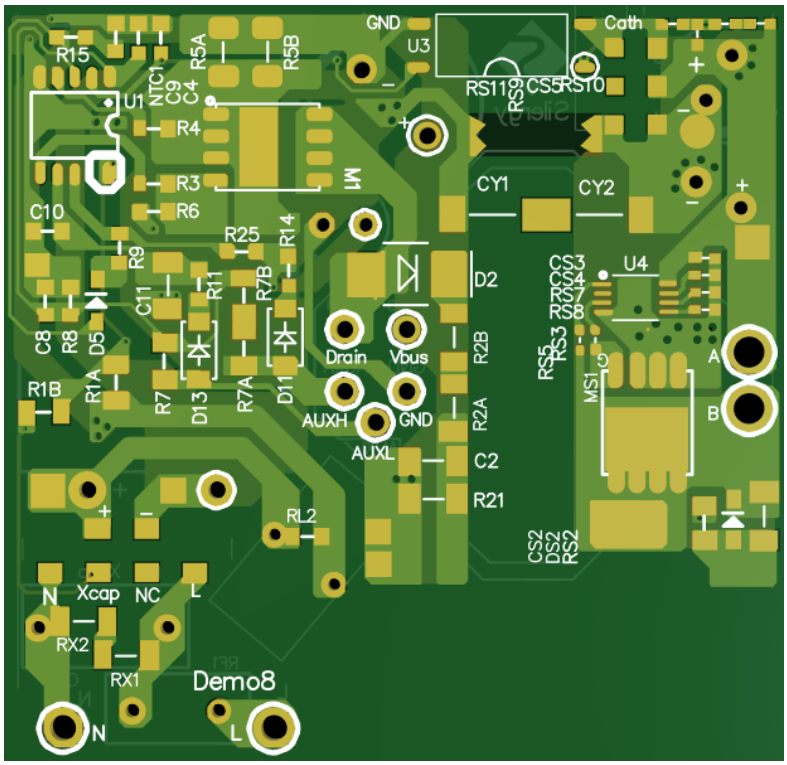


Figure 21. Bottom layer of recommend PCB layout.

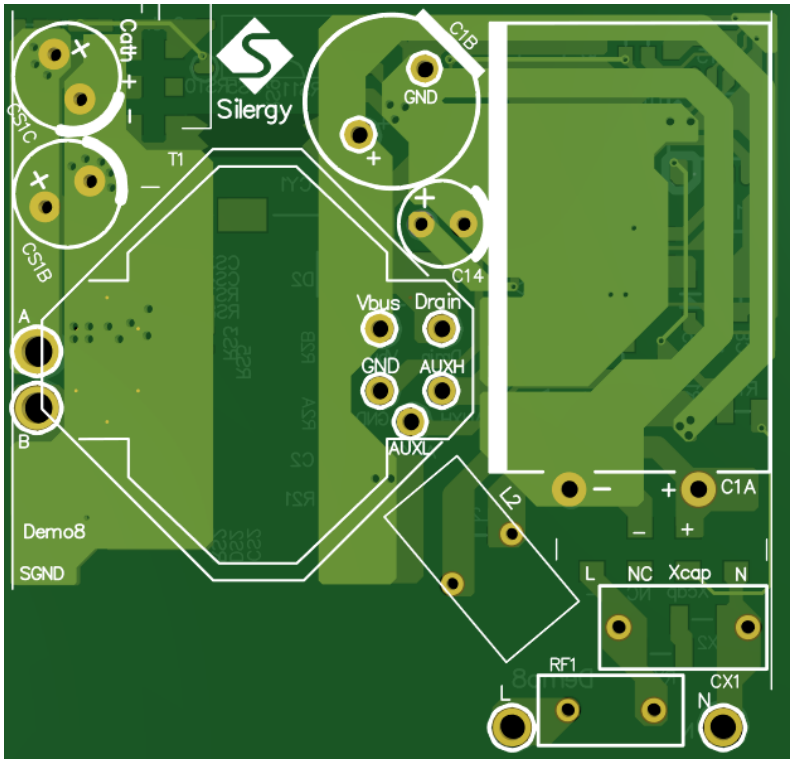


Figure 22. Top layer of recommend PCB layout.

Design Example

A step-by-step design example of a typical application is shown below.

Input/output specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	90V–264V
Rated output power	P_O	66W
Rated output voltage	V_O	5V–20V
Output OVP level	V_{O_OVP}	24V
Rated output current	I_O	3.3A
OLP	I_{OLP}	4.04A
Efficiency	η	93%

Preset parameters

Parameter	Symbol	Value
Breakdown voltage of power MOS	V_{MOS_BR}	650V
V_{DS} de-rating factor of power MOS	K_{DR}	90%
Spike on V_{DS} at power MOS turn-off	ΔV_{SN}	70V
BUS capacitor charge coefficient	K_{CH}	0.2
Secondary diode forward voltage drop	V_{D_R}	0V (SR)
Transformer effective Ae (RM8)	A_E	62 mm²

1. BUS capacitor selection

Select BUS capacitor: C_{BUS} = 104μF (1.57uF/W)

2. Minimum BUS voltage calculation

BUS capacitor charge coefficient: K_{CH} = 0.2

$$V_{BUS\_MIN} = \sqrt{2V_{IN\_MIN}^2 - \frac{P_O(1-K_{CH})}{\eta C_{BUS} f_o}} = \sqrt{2\times 90^2 - \frac{66\times(1-0.2)}{93\%\times 104u\times 60}} = 84V$$

3. Transformer design

(a) Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS} \le \frac{V_{MOS\_BR}K_{DR} - \sqrt{2}V_{IN\_MAX} - \Delta V_{SN}}{V_O + V_{D\_F}} = \frac{650\times 0.9 - \sqrt{2}\times 264 - 70}{20+0} = 7.1$$

N_{PS} is selected as: N_{PS} = 6.25, Reflected voltage V_{OR} = 6.25×20V = 125V.

(b) Calculate L_P of the transformer: Select f_{SW_MIN} = 110kHz

$$L_P = \frac{1}{2\times F_{SW\_MIN}\times V_O\times I_O\times}\times\left(\frac{V_{BUS\_MIN}\times V_{OR}}{V_{BUS\_MIN}+V_{OR}}\right)^2 = \frac{1}{2\times 110kHz\times 20V\times 3.3A}\times\left(\frac{84\times 125}{84+125}\right)^2 = 0.174mH$$

(c) Calculate R_{CS}: In normal operation, V_{REF_OCP} = 0.85V.

$$R_{CS} = \frac{V_{CS\_LIMIT}\times N_{PS}\times V_{BUS\_MIN}}{2\times I_{OUT\_OLP}\times(V_{OR}+V_{BUS\_MIN})} = \frac{0.5\times 6.25\times 84}{2\times 4.04\times(125+84)} = 0.155ohm$$

(d) Calculate maximum primary peak current:

$$I_{PPK\_MAX} = \frac{V_{CS.LIMITL}}{R_{CS}} = \frac{0.50}{0.155} = 3.23A$$

(e) Calculate primary winding turns N_P: B_{MAX} = 0.354T

$$N_P = \frac{L_P \times I_{PPK\_MAX}}{B_{MAX} \times A_E} = \frac{170uH \times 3.23A}{0.354T \times 62mm^2} = 25ts$$

(f) Calculate secondary winding turns N_S:

$$N_S = \frac{N_P}{N_{PS}} = \frac{25}{6.25} = 4$$

(g) Calculate auxiliary winding turns N_{AUXL} = 4ts: V_{OUT_MAX} = 20V

$$18V < \frac{V_{OUT\_MAX}}{N_S} \times N_{AUXL} < 22V, \quad , \quad 3.6 < N_{AUXL} < 4.4$$

Calculate auxiliary winding turns N_{AUXH} = 10ts: V_{OUT_MIN} = 5V

$$10V < \frac{V_{OUT\_MIN}}{N_S} \times N_{AUXL} < 14V, \quad , \quad 8 < N_{AUXH} < 11.2$$

4. Secondary diode selection

(a) Maximum reverse voltage calculation:

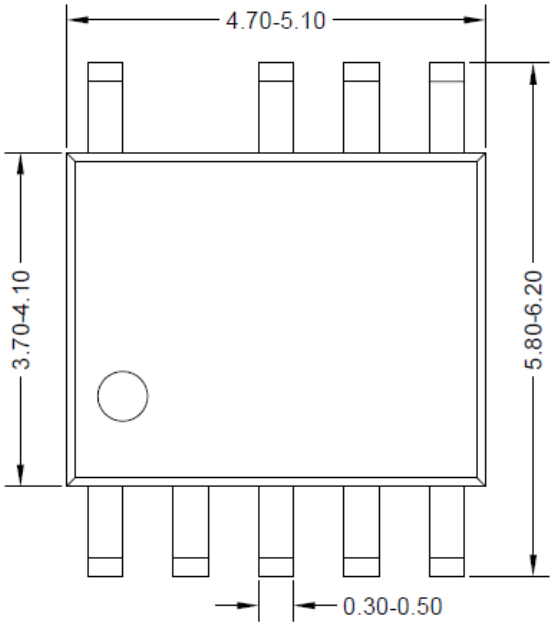
$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP} = \frac{\sqrt{2} \times 264}{6.25} + 24 = 84V$$

Considering the voltage spike, reverse voltage rating is recommended to be 100V–120V.

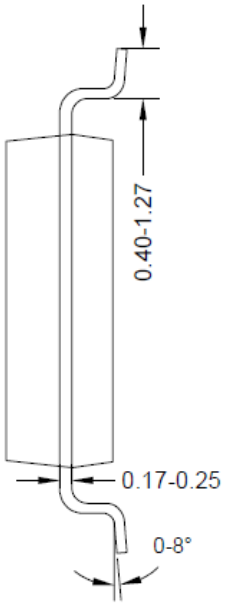
(b) Maximum instantaneous forward current:

$$I_{SPK\_MAX} = I_{PPK\_MAX} \times N_{PS} = 2.45A \times 6.25 = 15.3A$$

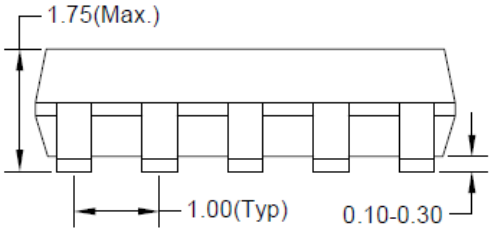
SSOP9 Package Outline Drawing



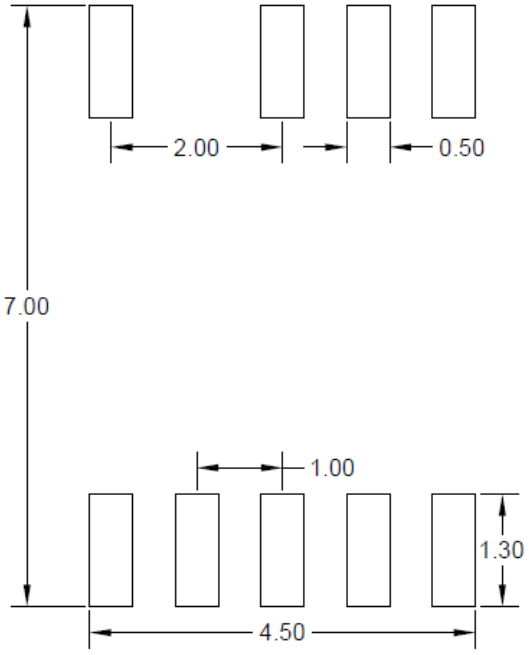
Top View



Side View



Front View

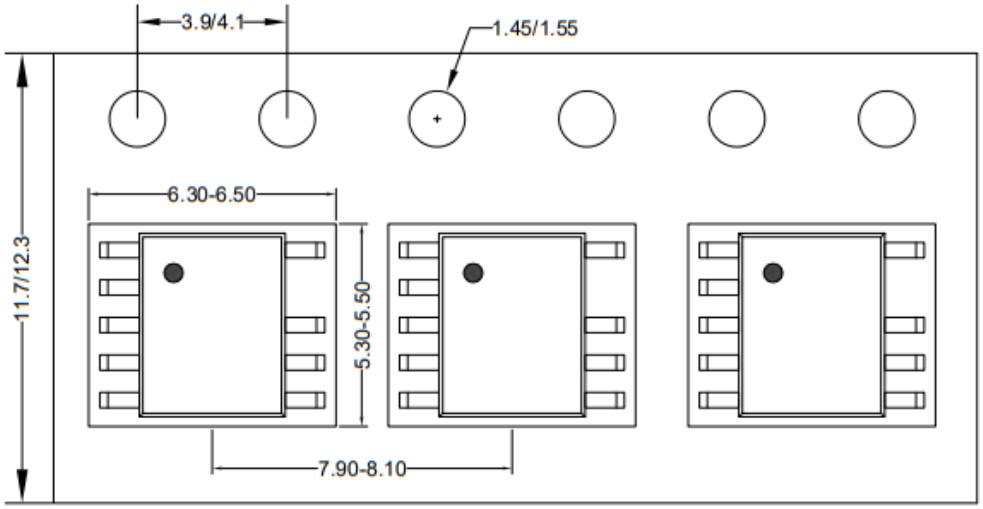


Recommended PCB Layout
(Reference Only)

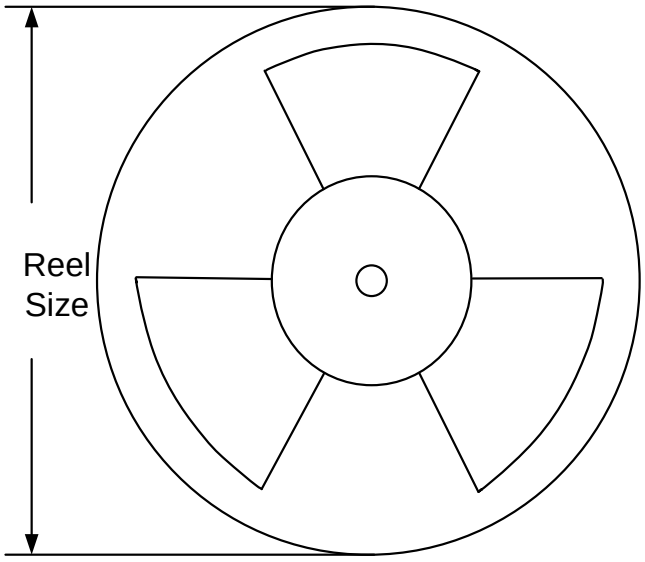
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

1. Tape Orientation



2. Carrier Tape and Reel specification for packages



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
SSOP9	12	8	13"	400	400	4000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
March 30，2024	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com