

### General Description

The SY21286 is a high efficiency synchronous buck converter operating over a wide input voltage range of 4.5V to 24V and capable of delivering up to 6A current. It integrates low  $R_{DS(ON)}$  top and bottom MOSFETs to minimize the conduction loss. It operates at a pseudo-constant frequency of 500kHz, to enable the use of small size inductor and capacitors. The SY21286 also integrates a bypass switch which allows the VCC to be powered by external 3.3V power supply and further reduces the power consumption of the entire system.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY21286 provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection, to guarantee safe operation in all operating conditions.

### Features

- Low  $R_{DS(ON)}$  for Internal MOSFETs: 28m $\Omega$  Top, 16m $\Omega$  Bottom
- Wide Input Voltage Range: 4.5V ~ 24V
- Adjustable Output Voltage: 0.6V ~ 2.5V
- 6A Continuous Output Current Capability
- 500kHz Pseudo-Constant Frequency
- $\pm 1\%$  Internal Reference Voltage
- Internal 0.6ms Soft-Start Limits the Inrush Current
- Constant On-Time and Ripple-Based Control
- Excellent Dynamic Performance
- Integrated 1.2 $\Omega$  Bypass Switch
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Adjustable Valley Current Limit Threshold by ILMT Pin
- Cycle-by-Cycle Peak and Valley Current Limit Protection
- Latch-Off Mode Output Under Voltage Protection
- Latch-Off Mode Output Over Voltage Protection
- Latch-Off Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact package: QFN2.5x2.5-16

### Applications

- LCD-TV/Net-TV/3D-TV
- Set Top Box
- Notebook
- High Power AP

### Typical Application

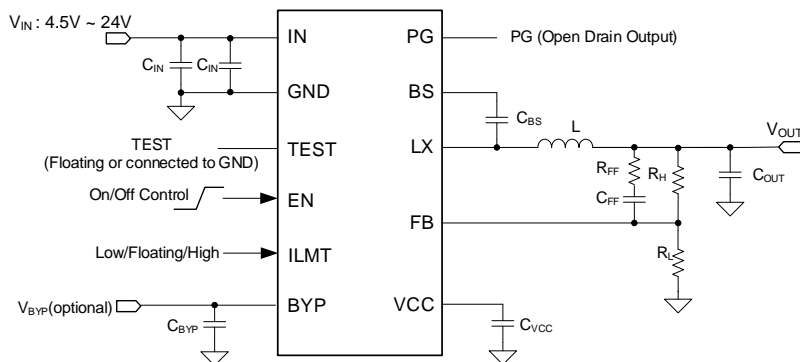


Figure1. Schematic Diagram

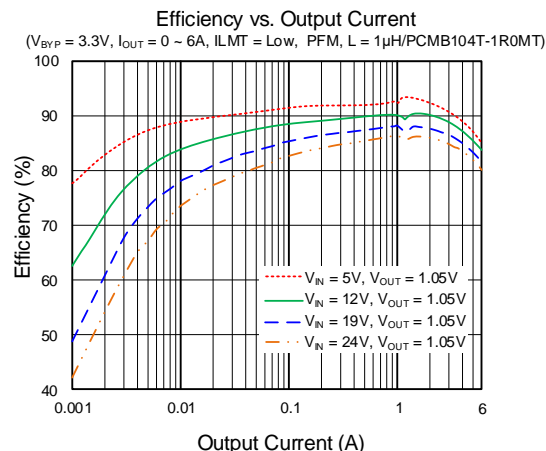


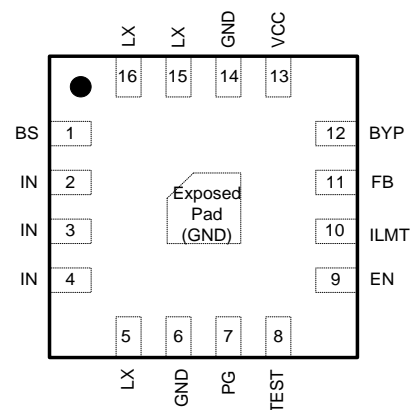
Figure2. Buck Efficiency vs. Output Current

## Ordering Information

Ordering Number	Package type	Top Mark
SY21286RHC	QFN2.5x2.5-16 RoHS Compliant and Halogen Free	GBMxyz

*x = year code, y = week code, z = lot number code*

## Pinout (top view)



## Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
2, 3, 4	IN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
5, 15, 16	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6, 14, EP	GND	Ground pin.
7	PG	Power good indicator pin. PG pin should be connected to $V_{IN}$ or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
8	TEST	For factory use only. Leave this pin floating or connect it to GND in application.
9	EN	Enable control pin of the buck converter. Pull high to turn on. Pull low to turn off. Do not leave this pin floating. The pin is also used for controlling the operation mode of the buck converter under light load condition after its output is within the regulated range. When its voltage is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode. When its voltage is higher than 2.2V, the buck converter operates in pulse-frequency modulation mode.
10	ILMT	Valley current limit threshold selection pin. See table 1.
11	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$ .
12	BYP	External 3.3V bypass power supply input pin. Decouple this pin to ground with a 1μF ceramic capacitor. Make one good RC filter for BYP input if the 3.3V external power rail has significant ripple. Leave this pin floating or connect this pin to the ground if it is not used.
13	VCC	Internal 3.3V LDO output pin. Power supply for the internal analog circuits. Decouple this pin to ground with at least a 2.2μF ceramic capacitor.

## Block Diagram

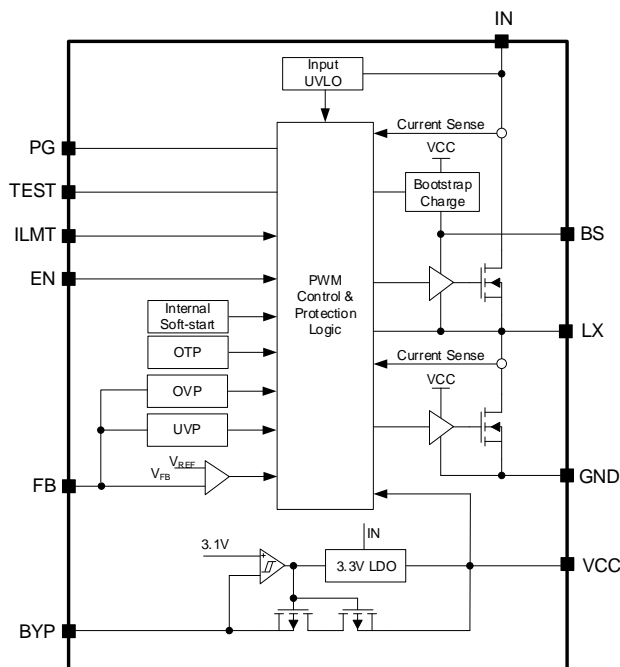


Figure3. Block Diagram

## Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	28	V
IN-LX, LX, PG, EN, TEST	-0.3	26	
BS-LX, VCC, ILMT, FB	-0.3	4	
BYP	-0.3	6	
LX, 10ns Duration	-5	29	
LX, 20ns Duration	-1	28	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

## Thermal Information

Parameter (Note2)	Typ	Unit
$\theta_{JA}$ Junction-to-Ambient Thermal Resistance	33	°C/W
$\theta_{JC}$ Junction-to-Case Thermal Resistance	5.5	
$P_D$ Power Dissipation $T_A = 25^\circ\text{C}$	3	W

## Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
Input Voltage	4.5	24	V
Output Voltage	0.6	2.5	
Continuous Output Current		6	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $C_{OUT} = 66\mu F$ ,  $C_{FF} = 220pF$ ,  $R_{FF} = 1k\Omega$ ,  $T_J = 25^\circ C$ ,  $I_{OUT} = 1A$  unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	$V_{IN}$		4.5		24	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	$V_{IN}$ rising			4.4	
	UVLO Hysteresis	$V_{IN,HYS}$			0.5		
	Quiescent Current 1	$I_{Q1}$	EN = High, $V_{BYP} = 0V$ , $V_{OUT} = V_{SET} \times 105\%$		190	240	$\mu A$
	Quiescent Current 2	$I_{Q2}$	EN = High, $V_{BYP} = 3.3V$ , $V_{OUT} = V_{SET} \times 105\%$		50	75	
	Shutdown Current	$I_{SHDN}$	EN = Low		5	9	
Output	Voltage Range	$V_{OUT}$		0.6		2.5	V
	Feedback Reference Voltage	$V_{REF}$		0.594	0.600	0.606	
	FB Input Current	$I_{FB}$	$V_{FB} = 1V$	-50		50	nA
	Discharge Current	$I_{DIS}$	$V_{OUT} = 1.2V$		40		mA
	Soft-Start Time	$t_{SS}$	$V_{OUT}$ from 0% to 100% $V_{SET}$ (Note4)		0.6		ms
	OVP Threshold	$V_{OVP}$	$V_{FB}$ rising	117	120	123	% $V_{REF}$
	OVP Hysteresis	$V_{OVP,HYS}$			5		
	OVP Delay Time	$t_{OVP,DLY}$	(Note4)		30		$\mu s$
	UVP Threshold	$V_{UVP}$	$V_{FB}$ falling	55	60	65	% $V_{REF}$
	UVP Delay Time	$t_{UVP,DLY}$	(Note4)		200		$\mu s$
MOSFETs	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			28		m $\Omega$
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			16		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$			17.5		A
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$	ILMT = Low	6		9	
			ILMT = Floating	8		12	
			ILMT = High	3.5		5.5	
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$	USM mode	2.4	3		
Enable (EN)	Input Voltage High	$V_{EN,H}$		1			V
	Input Voltage Low	$V_{EN,L}$				0.4	
	EN Voltage for Ultra-sonic Mode	$V_{EN,USM}$		1		1.6	
	EN Voltage for PFM Mode	$V_{EN,PFM}$		2.2		$V_{IN}$	
	De-Glitch Time	$t_{EN,DG}$	(Note4)		40		$\mu s$
ILMT	Input Voltage High	$V_{ILMT,H}$	(Note4)	$V_{CC} - 0.8$			V
	Input Voltage Low	$V_{ILMT,L}$	(Note4)			0.4	
Frequency	Switching Frequency	$f_{SW}$	$V_{OUT} = 1.2V$ , CCM	410	500	590	kHz
	Ultra-sonic Mode Frequency	$f_{USM}$	USM mode, $I_{OUT} = 0A$	20			

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Minimum On-Time	$t_{ON,MIN}$			50		ns
	Minimum Off-Time	$t_{OFF,MIN}$			200		
Power Good (PG)	Rising Threshold	$V_{PG,R}$	$V_{FB}$ rising (good)	86	90	94	% $V_{REF}$
	Falling Threshold	$V_{PG,F}$	$V_{FB}$ falling (not good)	81	85	89	
	Delay Time	$t_{PG,R}$	Low to high (Note4)		200		$\mu s$
		$t_{PG,F}$	High to low (Note4)		30		
		$t_{PG,OFF}$	IC shuts down (Note4)			0.5	
	Low Voltage	$V_{PG,LOW}$	$V_{FB} = 0V$ , $I_{PG} = 5mA$			0.4	V
VCC	Output Voltage	$V_{CC}$	VCC adds 1mA load		3.37		
BYP	$R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.2		$\Omega$
	Turn on Voltage	$V_{BYP}$		2.97	3.1		V
	Turn on Hysteresis	$V_{BYP,HYS}$			0.2		
	OVP Voltage	$V_{BYP,OVP}$			120		% $V_{CC}$
OTP	Temperature	$T_{OTP}$	$T_J$ rising (Note4)		150		$^{\circ}C$
	Temperature Hysteresis	$T_{OTP,HYS}$	$T_J$ falling (Note4)		15		

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** Package thermal resistance is measured in the natural convection at  $T_A = 25^{\circ}C$  on a 8.5cmx8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

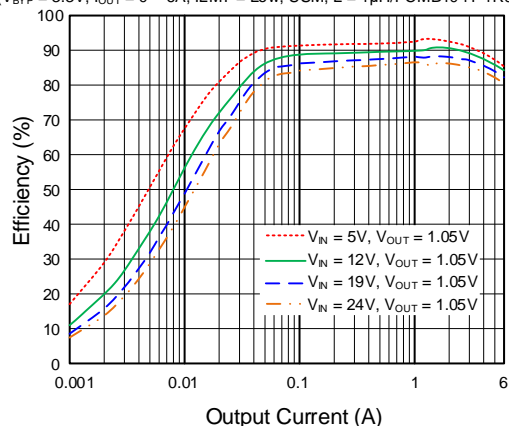
**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** Guaranteed by design.

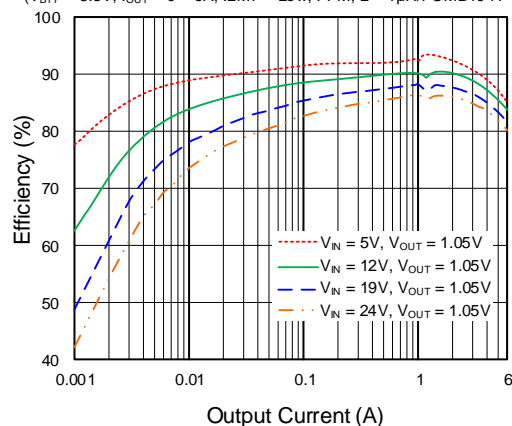
## Typical Performance Characteristics

( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1.05\text{V}$ ,  $L = 1\mu\text{H}$ ,  $C_{OUT} = 66\mu\text{F}$ ,  $C_{FF} = 220\text{pF}$ ,  $R_{FF} = 1\text{k}\Omega$ , unless otherwise noted)

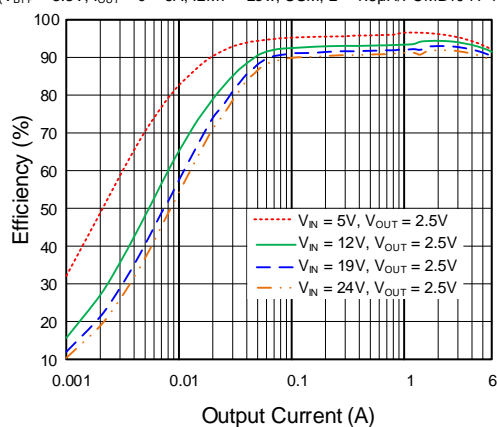
Efficiency vs. Output Current  
( $V_{BYP} = 3.3\text{V}$ ,  $I_{OUT} = 0 \sim 6\text{A}$ ,  $ILMT = \text{Low}$ ,  $USM$ ,  $L = 1\mu\text{H}/\text{PCMB104T-1R0MT}$ )



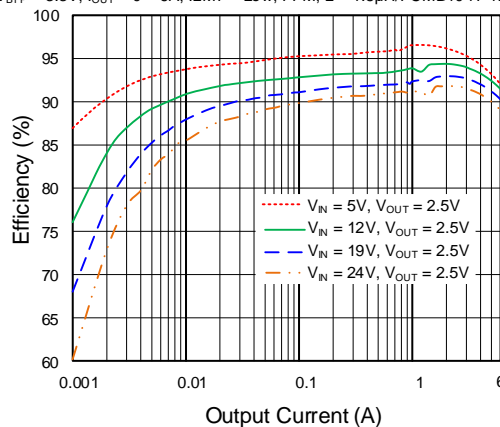
Efficiency vs. Output Current  
( $V_{BYP} = 3.3\text{V}$ ,  $I_{OUT} = 0 \sim 6\text{A}$ ,  $ILMT = \text{Low}$ ,  $PFM$ ,  $L = 1\mu\text{H}/\text{PCMB104T-1R0MT}$ )



Efficiency vs. Output Current  
( $V_{BYP} = 3.3\text{V}$ ,  $I_{OUT} = 0 \sim 6\text{A}$ ,  $ILMT = \text{Low}$ ,  $USM$ ,  $L = 1.5\mu\text{H}/\text{PCMB104T-1R5MS}$ )

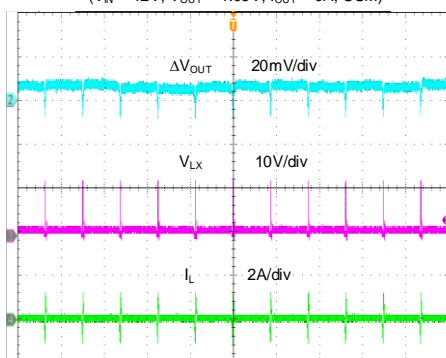


Efficiency vs. Output Current  
( $V_{BYP} = 3.3\text{V}$ ,  $I_{OUT} = 0 \sim 6\text{A}$ ,  $ILMT = \text{Low}$ ,  $PFM$ ,  $L = 1.5\mu\text{H}/\text{PCMB104T-1R5MS}$ )



### Output Ripple

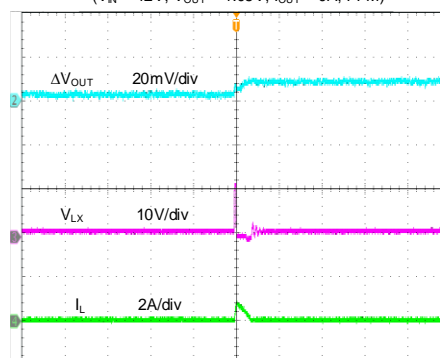
( $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1.05\text{V}$ ,  $I_{OUT} = 0\text{A}$ ,  $USM$ )



Time (40μs/div)

### Output Ripple

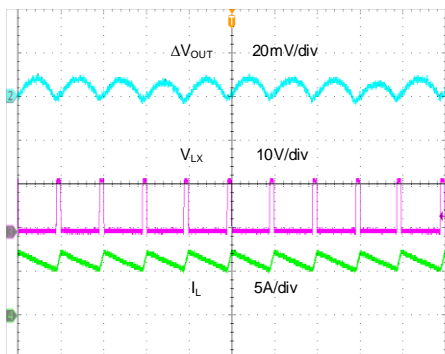
( $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1.05\text{V}$ ,  $I_{OUT} = 0\text{A}$ ,  $PFM$ )



Time (2μs/div)

## Output Ripple

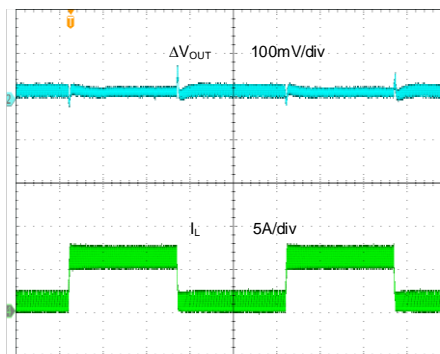
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A$ )



Time (2μs/div)

## Load Transient

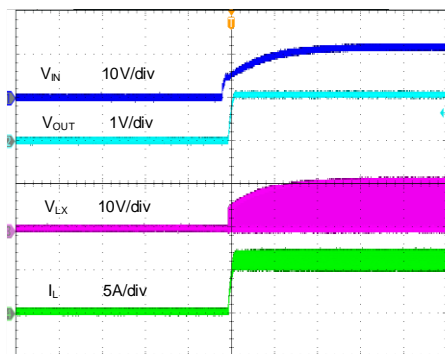
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 0.6 - 6A$ , PFM)



Time (200μs/div)

## Startup from $V_{IN}$

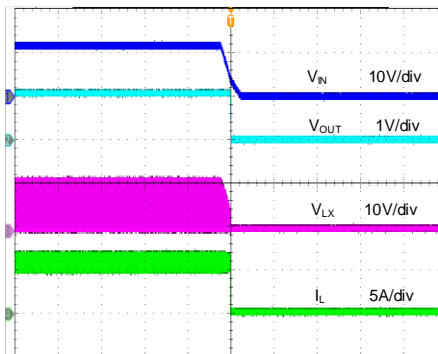
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A$ )



Time (4ms/div)

## Shutdown from $V_{IN}$

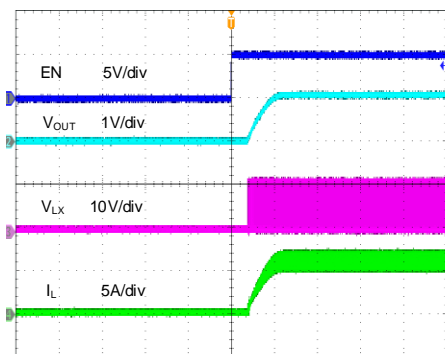
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A$ )



Time (4ms/div)

## Startup from EN

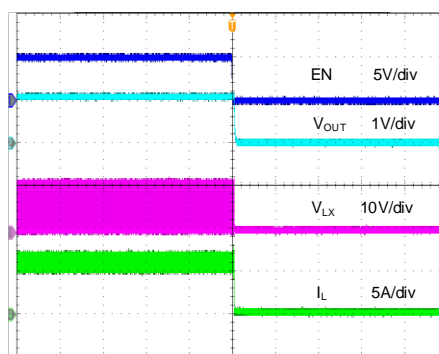
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A$ )



Time (800μs/div)

## Shutdown from EN

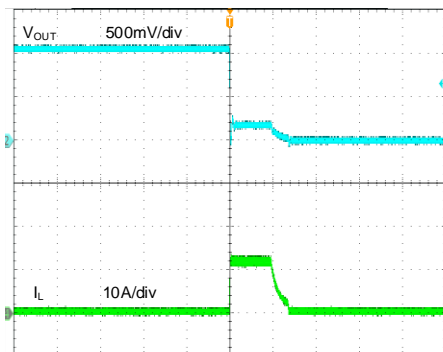
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A$ )



Time (800μs/div)

## Short Circuit Protection

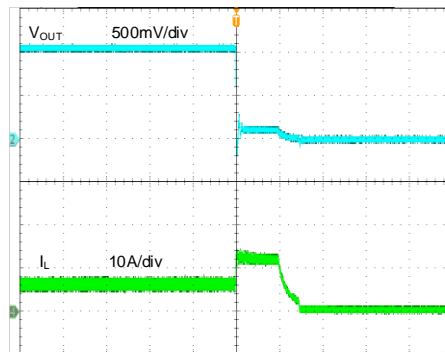
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 0A \sim$  Short,  $ILMT = Low$ )



Time (200 $\mu$ s/div)

## Short Circuit Protection

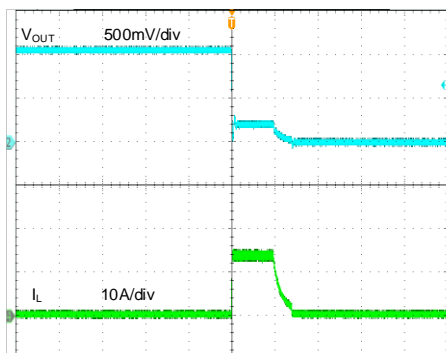
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A \sim$  Short,  $ILMT = Low$ )



Time (200 $\mu$ s/div)

## Short Circuit Protection

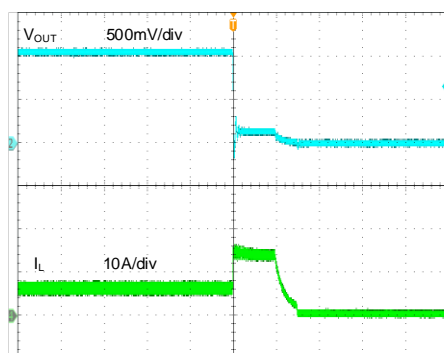
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 0A \sim$  Short,  $ILMT = Floating$ )



Time (200 $\mu$ s/div)

## Short Circuit Protection

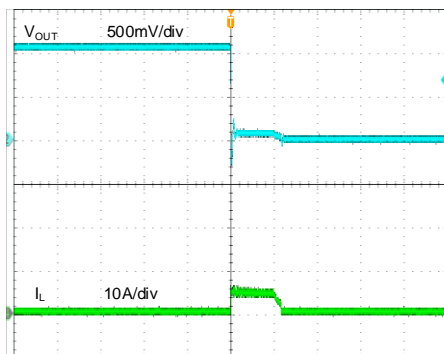
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 6A \sim$  Short,  $ILMT = Floating$ )



Time (200 $\mu$ s/div)

## Short Circuit Protection

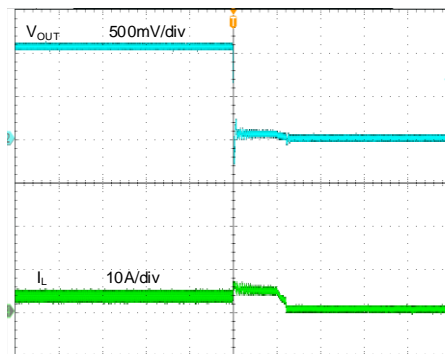
( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 0A \sim$  Short,  $ILMT = High$ )



Time (200 $\mu$ s/div)

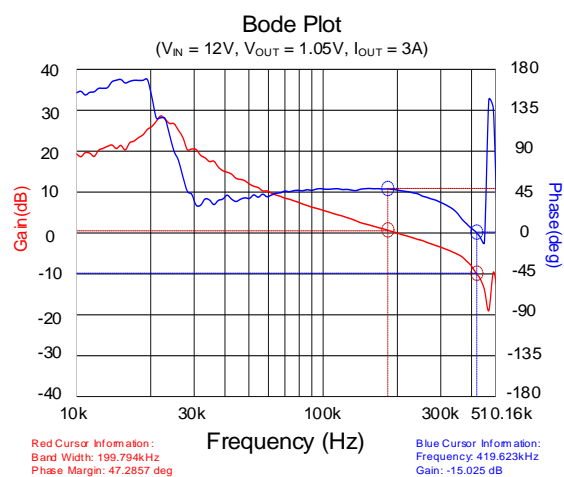
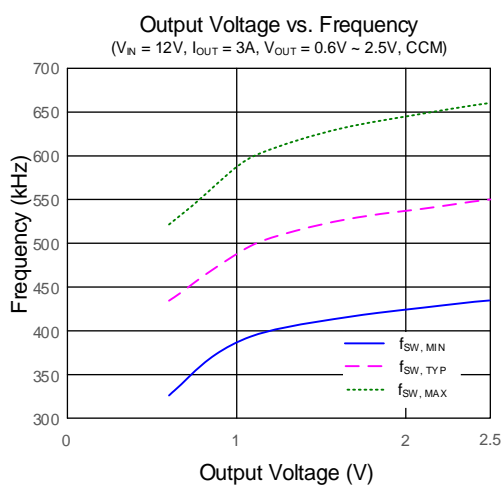
## Short Circuit Protection

( $V_{IN} = 12V$ ,  $V_{OUT} = 1.05V$ ,  $I_{OUT} = 3A \sim$  Short,  $ILMT = High$ )



Time (200 $\mu$ s/div)





## Detailed Description

### General Features

#### Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time ( $t_{ON}$ ) is a “fixed” voltage ratio,

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

For example, considering that a hypothetical converter targets 1.2V output from a 12V input at 500kHz, the target on-time is

$$\frac{1.2V}{12V} \times \frac{1}{500kHz} = 200ns$$

Each  $t_{ON}$  pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one  $t_{ON}$  period, a minimum off-time ( $t_{OFF,MIN}$ ) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

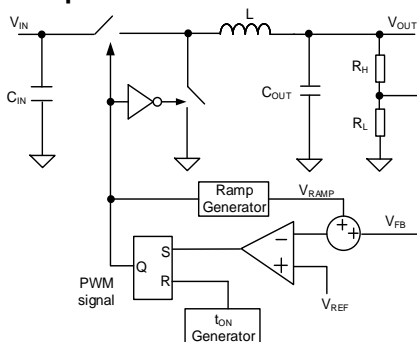
In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

#### Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

The device can support 2.5V maximum output voltage even when the input voltage is as low as 4.5V, across the entire junction temperature range of  $-40^{\circ}C \sim 125^{\circ}C$ .

#### Instant-PWM Operation



Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the  $t_{ON}$  duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the  $t_{ON}$  pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the  $t_{ON}$  pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the  $t_{ON}$  period. At the end of the  $t_{ON}$  period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients,  $t_{ON}$  can be retrigged with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time ( $t_{DEAD}$ ) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as well as between turning the bottom MOSFET off and the top MOSFET on.

#### Light Load Operation Mode Selection

PFM or USM light load operation is selected using the EN pin. EN is a dual purpose input serving as the buck converter enable pin but also as mode selection pin to control operation mode of the buck converter under light load conditions, after its output is within the regulated range. If the voltage on this pin is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode (USM). If the voltage on this pin is higher than 2.2V, the buck converter operates using pulse-frequency modulation (PFM) mode.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \quad (1)$$

the current through the bottom MOSFET will ramp to near zero before the next  $t_{ON}$  time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another  $t_{ON}$  until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next  $t_{ON}$  cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

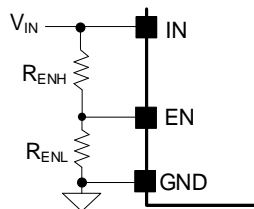
If USM light load operation is selected, the control loop keeps the switching frequency above the audible frequency range, even under deep light load or null load conditions.

## Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input undervoltage lockout protection.

The device remains in a low current state and LX switching actions are inhibited until  $V_{IN}$  exceeds the UVLO rising threshold. At that time, if EN is high, the device starts operating. If  $V_{IN}$  falls below  $V_{IN,UVLO}$  less than the input UVLO hysteresis, LX node switching actions will again be suppressed.

Increasing the default input UVLO threshold can be implemented using an external resistor divider connected to EN.



## EN Control

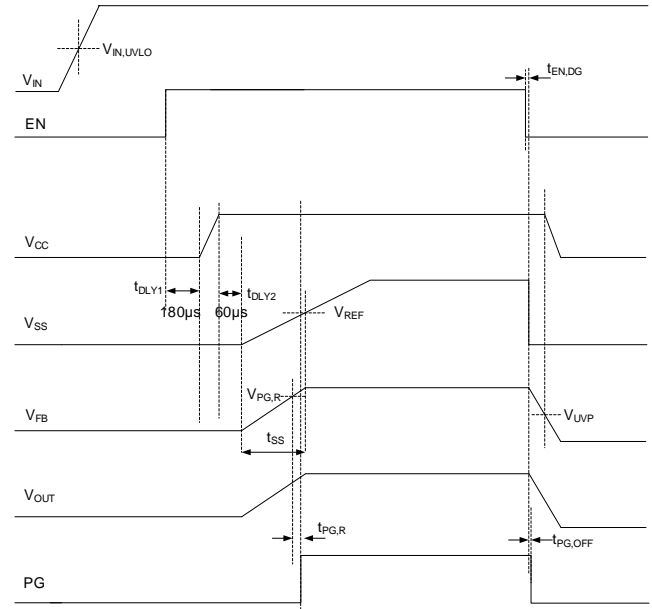
The EN input is a high-voltage capable input with logic-compatible threshold. EN logic high is defined as a voltage higher than 1V, and a logic low as a voltage lower

than 0.4V. When the device is turned off, the shutdown current  $I_{SHDN}$  is below 9μA.

It is not recommended to connect EN pin to  $V_{IN}$  or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used for EN pin in this case.

## Startup and Shutdown

The device incorporates an internal soft-start circuit to smoothly ramp the buck converter output to the desired voltage whenever it is enabled. Internally, the soft-start circuit clamps the output at zero and then allows the output to rise to the desired voltage over approximately 0.6ms, which avoids high current flow and transients during startup. The startup and shutdown sequence are shown below:



After  $V_{IN}$  exceeds the UVLO rising threshold, the VCC is turned on after the delay time  $t_{DLY1}$  if EN is high, the buck converter is turned on after another delay time  $t_{DLY2}$  after VCC voltage is set up. When the output voltage is 90% of the regulated value, PG is set to the high-impedance state after the delay time  $t_{PG,R}$ .

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage  $V_{SS}$  exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

## PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than  $V_{PG,R}$  and less than  $V_{OVP}$  for at least

the power good delay time (low to high), PG will be set to high-impedance state.

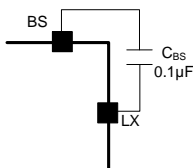
PG should be connected to  $V_{IN}$  or another voltage source through a resistor (e.g., 100k $\Omega$ ). After  $V_{IN}$  rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage  $V_{FB}$  reaches  $V_{PG,R}$ , PG is set to high-impedance state after a delay time of 200 $\mu$ s (typ.). When  $V_{FB}$  drops to  $V_{PG,F}$ , or rises above  $V_{OVP}$  for the OVP delay time, PG is driven low after a delay time of 30 $\mu$ s (typ.).

## Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low  $V_{IN}$  or EN, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOSFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 40mA for  $V_{OUT} = 1.2V$ . The discharge MOSFET is not active outside of these shutdown conditions.

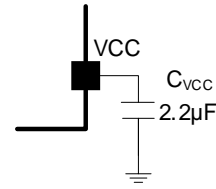
## External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a 0.1 $\mu$ F low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.



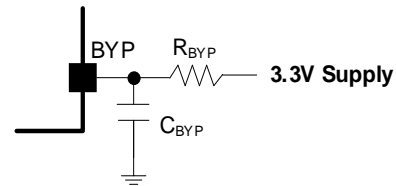
## VCC Output

The device integrates a high performance, low drop-out linear regulator 3.3V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. Once the input voltage exceeds its own UVLO (rising) threshold, and EN is high, VCC is turned on and supplied power by  $V_{IN}$ . After the BYP voltage exceeds BYP turn on voltage, the internal LDO regulator will be turned off and the bypass switch will be turned on so that VCC output can switch to BYP voltage to reduce power consumption. Connect a 2.2 $\mu$ F low ESR ceramic capacitor from VCC to GND. Make sure the loop formed by the VCC capacitor is shorter than the loop for the BYP capacitor, if there is placement conflict between them.



## BYP Input

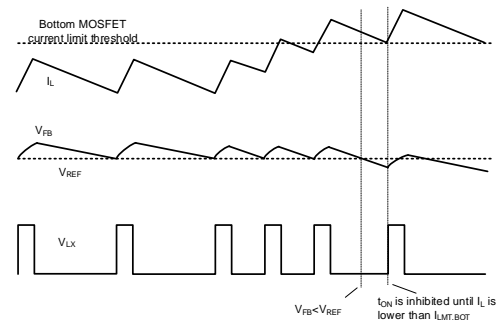
When a 3.3V external power supply is connected to the BYP, the internal LDO is automatically turned off. The overall efficiency may be improved by using an external power supply. Connect a 1 $\mu$ F low ESR ceramic capacitor from BYP pin to GND. Using an external low pass filter consisting of a small value resistor  $R_{BYP}$  and a ceramic capacitor  $C_{BYP}$  is recommended for applications where the external power rail has significant ripple. Connect the pin to GND or leave floating if not used.



## Fault Protection Modes

### Output Current Limit

The buck converter features cycle-by-cycle "valley" current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold,  $t_{ON}$  is inhibited until the current returns back to below the threshold.



The device supports programmable valley current limit threshold. Pull ILMT pin low, floating or high for 3 gears successively increasing valley current limit threshold. When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

ILMT Gears	$I_{LMT,BOT}$	Recommended Table
ILMT = Low	$\geq 6A$	Pull ILMT to GND by $\leq 10k\Omega$ Resistor
ILMT = Floating	$\geq 8A$	ILMT pin floating
ILMT = High	$\geq 3.5A$	Pull ILMT to VCC by $\leq 10k\Omega$ Resistor

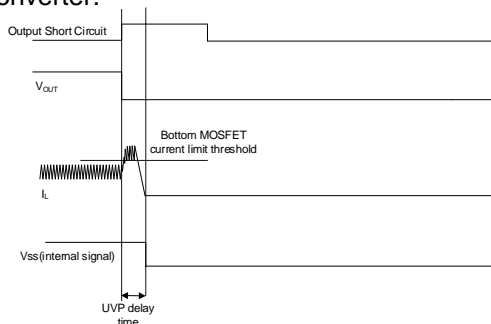
Table1: Programmable Valley Current Limit

The valley current limit protection limits the inductor current, but the OCP itself is a non-latched protection. When the load current is higher than the bottom MOSFET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. When the feedback voltage falls below the under voltage protection (UVP) threshold, and continues for the UVP delay time, the buck converter will be disabled and enter latch-off state. Independent from this mechanism, the over temperature protection may also be triggered under the over current condition and the buck converter will be disabled and enter latch-off state.

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the  $t_{ON}$  time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on.  $t_{ON}$  can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

## Output Under Voltage Protection (UVP)

If  $V_{OUT} < \sim 60\%$  of the regulated value for approximately 200 $\mu s$  occurring when the output short circuit or the load current is much higher than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the buck converter will be disabled and set to a latch-off state. Cycle EN input to re-enable the buck converter.



## Output Over Voltage Protection (OVP)

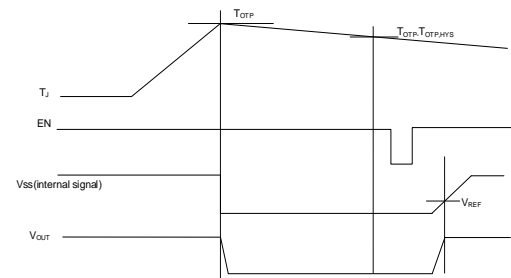
The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the top MOSFET naturally remains off and different actions are taken depending on the operation mode.

When operating in PFM light load mode, if the feedback voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. If the feedback voltage doesn't exceed the OVP threshold, the LX node switching actions will be resumed when the combined feedback and ramp signals become lower than the reference voltage. If the feedback voltage exceeds the over voltage protection threshold for the OVP delay time, the output over voltage protection (OVP) will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN input to re-enable the buck converter.

When operating in USM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold for the OVP delay time, the protection will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN input to re-enable the buck converter. False OVP triggers may happen under USM light load conditions, if the inductance value is chosen too low.

## Over Temperature Protection (OTP)

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects the junction temperature exceeds 150°C, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled and enter a latch off status. In this case the VCC is not disabled. Cycle EN input to re-enable the buck converter after the junction temperature cools down about 15°C. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.



## Design Procedure

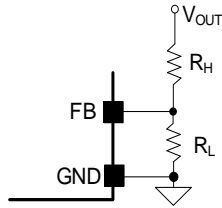
### Feedback Resistor Divider Selection

Choose  $R_H$  and  $R_L$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_H$  and  $R_L$ . A value of between 10k $\Omega$  and 1M $\Omega$  is strongly recommended for both resistors. If  $V_{SET}$  is 1.2V,  $R_H =$



100kΩ is chosen, then using following equation,  $R_L$  can be calculated to be 100kΩ.

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_H$$



## Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at  $D = 0.5$ , then

$$I_{CIN\_RMS\_MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE\_CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at  $D = 0.5$ , then

$$V_{CIN\_RIPPLE\_CAP\_MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10μF X5R capacitor is sufficient. Place the ceramic input capacitor as close to the device's IN and GND pin as possible.

## Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the LX node.

The buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off between efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. Choosing higher inductance value inductors tend to have higher DCR and will slow down transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current ( $\Delta I_L$ ) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductance value by selecting the input and output voltages, the operating frequency ( $f_{SW}$ ), the maximum output current ( $I_{OUT\_MAX}$ ) and estimating a  $\Delta I_L$  as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current ( $\Delta I_L$ ) and required peak current inductor current  $I_{L\_PEAK}$ .

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of  $I_{L\_PEAK}$ .

If USM light load operation is selected, make sure the inductance value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Selecting low loss ferrite materials is recommended.

## Inductor Design Example

Consider a typical design for a buck converter providing 1.2V<sub>OUT</sub> at 6A from 12V<sub>IN</sub>, operating at 500kHz and using target inductor ripple current ( $\Delta I_L$ ) of 40% or 2.4A.

First, determine the approximate inductance value:

$$L = \frac{1.2V \times (12V - 1.2V)}{12V \times 500kHz \times 2.4A} = 0.9\mu H$$

Next, select the nearest standard inductance value, in this case 1 $\mu$ H, and calculate the resulting inductor ripple current ( $\Delta I_L$ ):

$$\Delta I_L = \frac{1.2V \times (12V - 1.2V)}{12V \times 500kHz \times 1\mu H} = 2.16A$$

$$I_{L,PEAK} = 6A + \frac{2.16A}{2} = 7.08A$$

The resulting 2.16A ripple current is 2.16A/6A is ~36%, which is within the 20% ~ 50% target.

$$I_{L,PEAK,RVS} = \frac{2.16A}{2} = 1.08A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting  $I_{L,PEAK}$  of 7.08A.

## Output Capacitor Selection

The buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

## Steady State Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple ( $\Delta I_L$ ) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE, ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE, CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with  $\Delta I_L = 2.16A$  using three 22 $\mu$ F ceramic capacitors, each with an ESR of ~6m $\Omega$  for parallel total of 66 $\mu$ F and 2m $\Omega$  ESR.

$$V_{RIPPLE, ESR} = 2.16A \times 2m\Omega = 4.32mV$$

$$V_{RIPPLE, CAP} = \frac{2.16A}{8 \times 66\mu F \times 500kHz} = 8.18mV$$

Total ripple = 12.50mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150 $\mu$ F 40m $\Omega$  POS cap, the above result is

$$V_{RIPPLE, ESR} = 2.16A \times 40m\Omega = 86.40mV$$

$$V_{RIPPLE, CAP} = \frac{2.16A}{8 \times 150\mu F \times 500kHz} = 3.60mV$$

Total ripple = 90.00mV.

## Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, for good performance specific considerations must be addressed, especially when using small ceramic capacitors which have low capacitance at low output voltages, which results in insufficient stored energy for load transients. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of +/- 3A,  $V_{ESR} = +/- 3A \times 2m\Omega = +/- 6mV$ . The POS capacitor result with the same load transient,  $V_{ESR} = +/- 3A \times 40m\Omega = +/- 120mV$ .

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty cycle factor. During a fast load transient, the maximum duty cycle of the buck converter is a function of  $t_{ON}$  and the  $t_{OFF,MIN}$ , as the control scheme is designed to rapidly ramp the inductor current by grouping together many  $t_{ON}$  pulses in this case. The maximum duty factor  $D_{MAX}$  may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = - \frac{L \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 3A load increase using the ceramic capacitor case when  $V_{IN} = 12V$ . At  $V_{OUT} = 1.2V$ , the result is  $t_{ON} = 200ns$ ,  $t_{OFF,MIN} = 200ns$ ,  $D_{MAX} = 200 / (200 + 200) = 0.5$  and

$$V_{UNDERSHOOT,CAP} = - \frac{1\mu H \times (3A)^2}{2 \times 66\mu F \times (12V \times 0.5 - 1.2V)} = -14.2mV$$

Using the POS capacitor in the above example, the result is:

$$V_{UNDERSHOOT,CAP} = -\frac{1\mu H \times (3A)^2}{2 \times 150\mu F \times (12V \times 0.5 - 1.2V)} = -6.25mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 3A load decrease using the ceramic capacitor case above. At  $V_{OUT} = 1.2V$  the result is

$$V_{OVERSHOOT,CAP} = \frac{1\mu H \times (3A)^2}{2 \times 66\mu F \times 1.2V} = 56.82mV$$

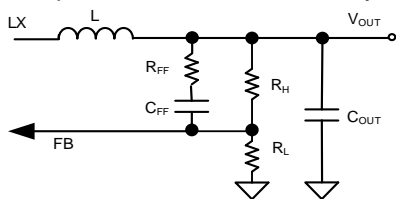
Using the POS capacitor in the above example, the result is:

$$V_{OVERSHOOT,CAP} = \frac{1\mu H \times (3A)^2}{2 \times 150\mu F \times 1.2V} = 25.00mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application. If the system requirements are not met, recalculate with a different configuration.

## Load Transient Considerations

The device uses the COT ripple-based control strategy to achieve good stability and fast transient response. In applications with high step load current, adding an RC network  $R_{FF}$  and  $C_{FF}$  between the OUT capacitors and the FB pin may further speed up the load transient response.  $R_{FF} = 1k\Omega$  and  $C_{FF} = 220pF$  have been shown to perform well in most applications. Increasing  $C_{FF}$  will speed up the load transient response if there is no stability issue.



Note: For  $C_{OUT} > 500\mu F$  and when the minimum load current is low, use feedforward values of  $R_{FF} = 1k\Omega$  and  $C_{FF} = 2.2nF$  to provide sufficient ripple to FB node for low output ripple and good transient behavior.

## Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the

surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where,  $T_{J,MAX}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is  $125^\circ C$ . The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For the QFN2.5x2.5-16 package the thermal resistance  $\theta_{JA}$  is  $33^\circ C/W$  when measured on a standard Silergy  $8.5cm \times 8.5cm$  size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz copper traces connected to each device pin and very large, unbroken 1-oz internal power and ground planes.

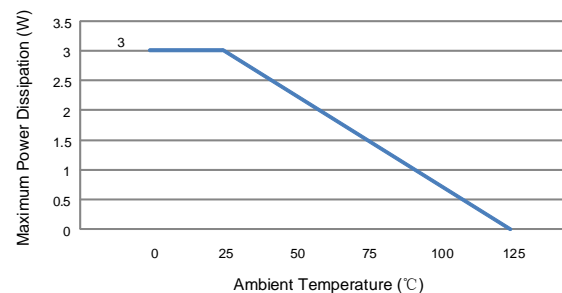
Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at  $T_A = 25^\circ C$  may be calculated by the following formula:

$$P_{D,MAX} = \frac{125^\circ C - 25^\circ C}{33^\circ C/W} = 3W$$

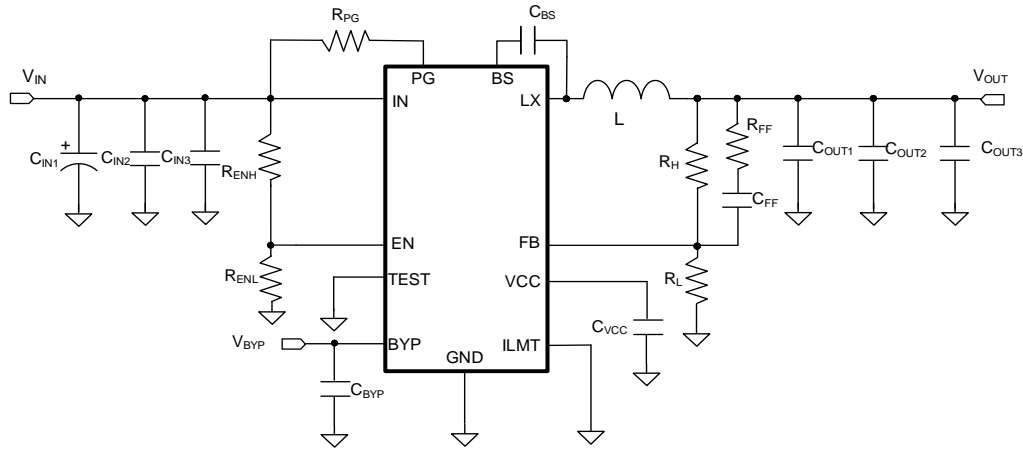
The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J,MAX}$  and thermal resistance  $\theta_{JA}$ . Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

Maximum Power Derating Curve





## Application Schematic ( $V_{OUT} = 1.05V$ )



## BOM List

Designator	Description	Part Number	Manufacturer
C <sub>IN1</sub>	47μF/50V, Electrolytic Cap		
C <sub>IN2</sub>	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mpRata
C <sub>IN3</sub> , C <sub>BS</sub>	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mpRata
C <sub>OUT1</sub> , C <sub>OUT2</sub> , C <sub>OUT3</sub>	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mpRata
C <sub>VCC</sub>	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mpRata
C <sub>BYB</sub>	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	mpRata
C <sub>FF</sub>	220pF/50V/C0G,0603	GRM1885C1H221JA01D	mpRata
L	1.0μH/18A, inductor	PCMB104T-1R0MT	CYNTEC
R <sub>ENH</sub>	10kΩ, 1%, 0603		
R <sub>ENL</sub>	1MΩ, 1%, 0603		
R <sub>H</sub> , R <sub>PG</sub>	100kΩ, 1%, 0603		
R <sub>L</sub>	133kΩ, 1%, 0603		
R <sub>FF</sub>	1kΩ, 1%, 0603		

## Recommend Component Values for Typical Applications

V <sub>OUT</sub> (V)	R <sub>H</sub> (kΩ)	R <sub>L</sub> (kΩ)	C <sub>FF</sub> (pF)	L/Part Number	C <sub>OUT</sub>
1.05	100	133	220	1.0μH/PCMB104T-1R0MT	22μF×3/16V, 1206, X5R
1.2	100	100	220	1.0μH/PCMB104T-1R0MT	22μF×3/16V, 1206, X5R
1.8	100	49.9	220	1.5μH/PCMB104T-1R5MS	22μF×3/16V, 1206, X5R
2.5	100	31.6	220	1.5μH/PCMB104T-1R5MS	22μF×3/16V, 1206, X5R

## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

**Input Capacitors:** Place the input capacitor close to IN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the IN and GND using a wide copper pour. A 0.1 $\mu$ F input ceramic capacitor is recommended to reduce the high-frequency noise.

**Output Capacitors:** Ensure that the C<sub>OUT</sub> negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

**VCC Capacitor:** Place the VCC capacitor close to VCC using a short, direct copper trace to the nearest GND pin (pin 14).

**BYP Capacitor:** Place the BYP capacitor close to BYP using a short, direct copper trace to the nearest device GND pin (pin 14) if bypass function is used. It is recommended to make one good RC filter for BYP input if the 3.3V external power ripple is large.

**Feedback Network:** Place the feedback components (R<sub>H</sub>, R<sub>L</sub>, R<sub>FF</sub> and C<sub>FF</sub>) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Use a Kelvin connection for the feedback sampling point at C<sub>OUT</sub> rather than the inductor output terminal.

**LX Connection:** Keep LX area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance. Wide LX copper trace between pin 5 and pin 15, 16 should be used to improve efficiency.

**BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C<sub>BS</sub>) as short as possible.

**Control Signals:** It is not recommended to connect control signals to V<sub>IN</sub> or another voltage source directly. A resistor in a range of 1k $\Omega$  to 1M $\Omega$  should be used if they are pulled high.

**GND Vias:** Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place four GND vias on it for heat dissipation.

**PCB Board:** A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper area as wide as possible. Middle1 layer should be used as a GND layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

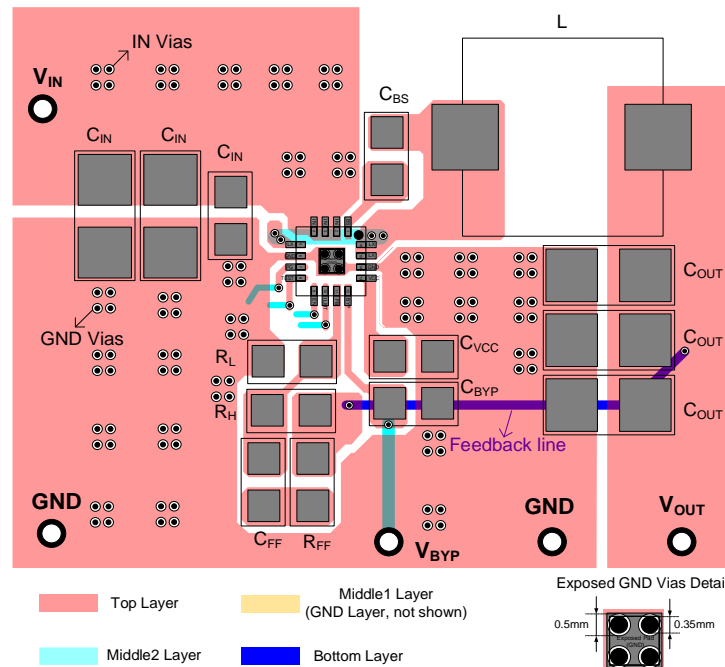
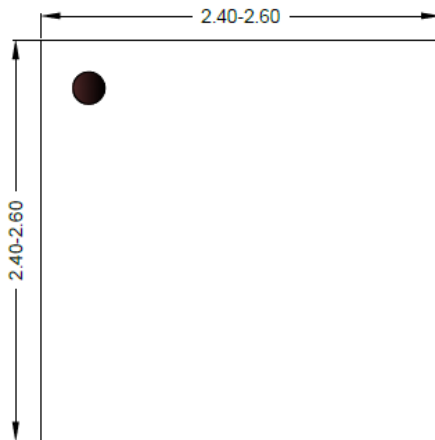
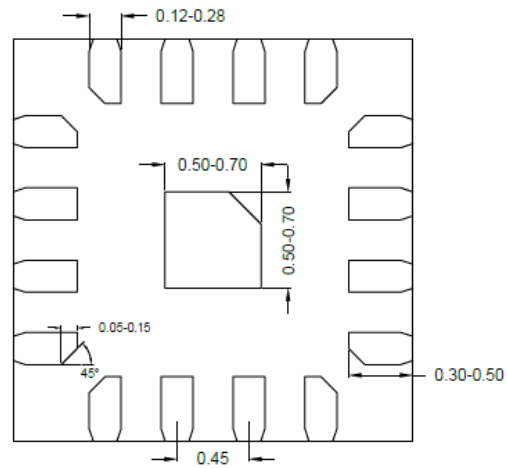


Figure4. PCB Layout Suggestion

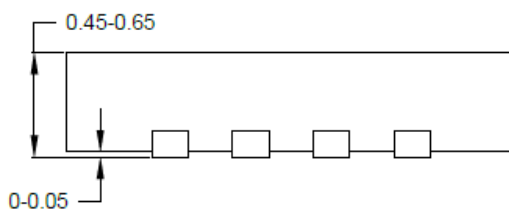
## QFN2.5×2.5-16 Package Outline Drawing



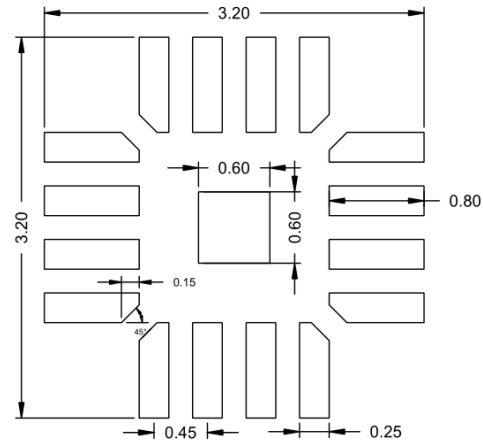
Top view



Bottom view



Side view

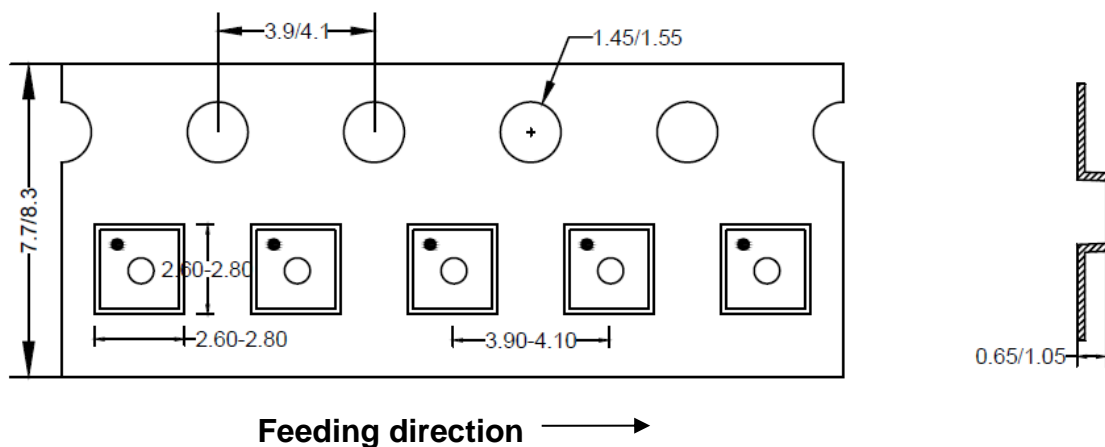


Recommended PCB layout  
(Reference only)

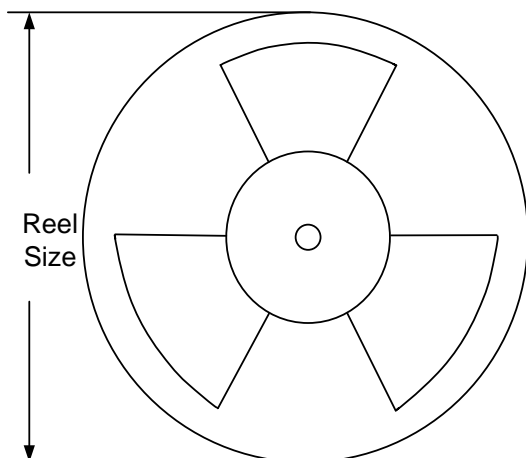
**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Tape and Reel Information

### 1. QFN2.5x2.5 tape orientation



### 2. Carrier Tape and Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5x2.5	8	4	7"	400	160	3000

### 3. Others: NA

**Revision History**

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
May.17, 2024	1.0	Initial Release	-

### IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: [www.silergy.com](http://www.silergy.com)

© 2024 Silergy Corp.

**All Rights Reserved.**