SQ82100

20-Output PCIe Gen1 to Gen6 Clock Buffer

General Description

The SQ82100 is a 20-output ultra-low additive phase jitter PCIe Gen1 to Gen6 clock buffer. The 20-channel low power differential HCSL reference output clocks can be used for SAS, SATA, and other applications. It provides integrated termination resistors for 85Ω output transmission lines. The OE_N pins, combined with SMBus enable bits and a 3-wire side-band interface, control any channel output clock, enabling or disabling it.

If SBEN is set to high, the SBI enables or disables the output. If SBEN is set to low, the data input pins (OE[512]_N, SDATA, SCLK, and PWRGD/PWRDN_N) feature a power-down tolerant design, allowing these signals to be driven when the SQ82100 is powered down.

Applications

- Servers
- Computing
- PCI Express (PCIe 1.0 ~ 6.0)

Features

- Supports 3.3V Power Supplies
- Differential Additive Phase Jitter: PCIe Gen6 <10fs RMS
- Differential Additive Phase Jitter: PCIe Gen5 <20fs RMS
- Differential Additive Phase Jitter: DB2000QL <30fs RMS
- Differential Additive Phase Jitter: PCIe Gen4 <30fs RMS
- Fully Compliant with Intel DB2000QL Specifications
- 20 Low-Power Push-Pull LP-HCSL PCIe Outputs
- Supports Clock Frequencies from 1MHz to 400MHz
- Maximum Output-to-Output Skew: 50ps
- Embedded Low Dropout (LDO) Voltage Regulator
- Embedded Series Termination Resistors for 85Ω Differential Transmission Line
- Power Down Tolerant (PDT) On Digital Input Pins
- Transparent for Spread Spectrum Clock
- Eight OE Pins
- SMBus Interface
- Side-Band Interface (SBI)

Typical Application

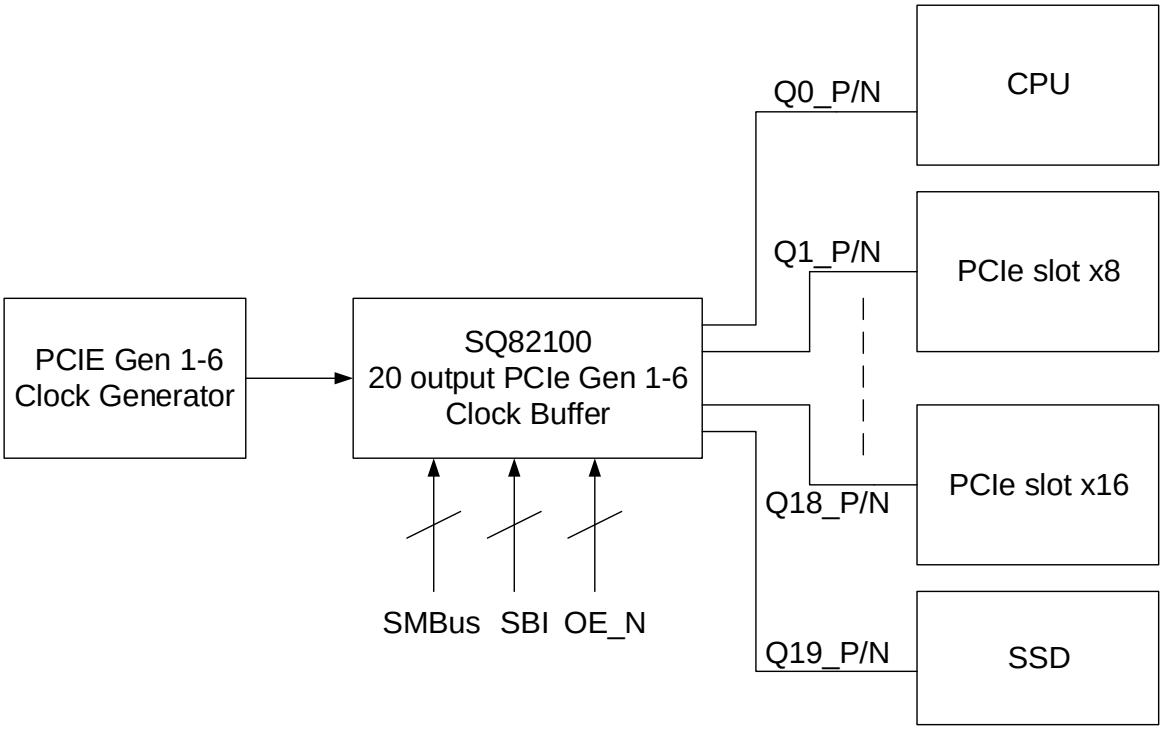


Figure 1. Typical Application Circuit

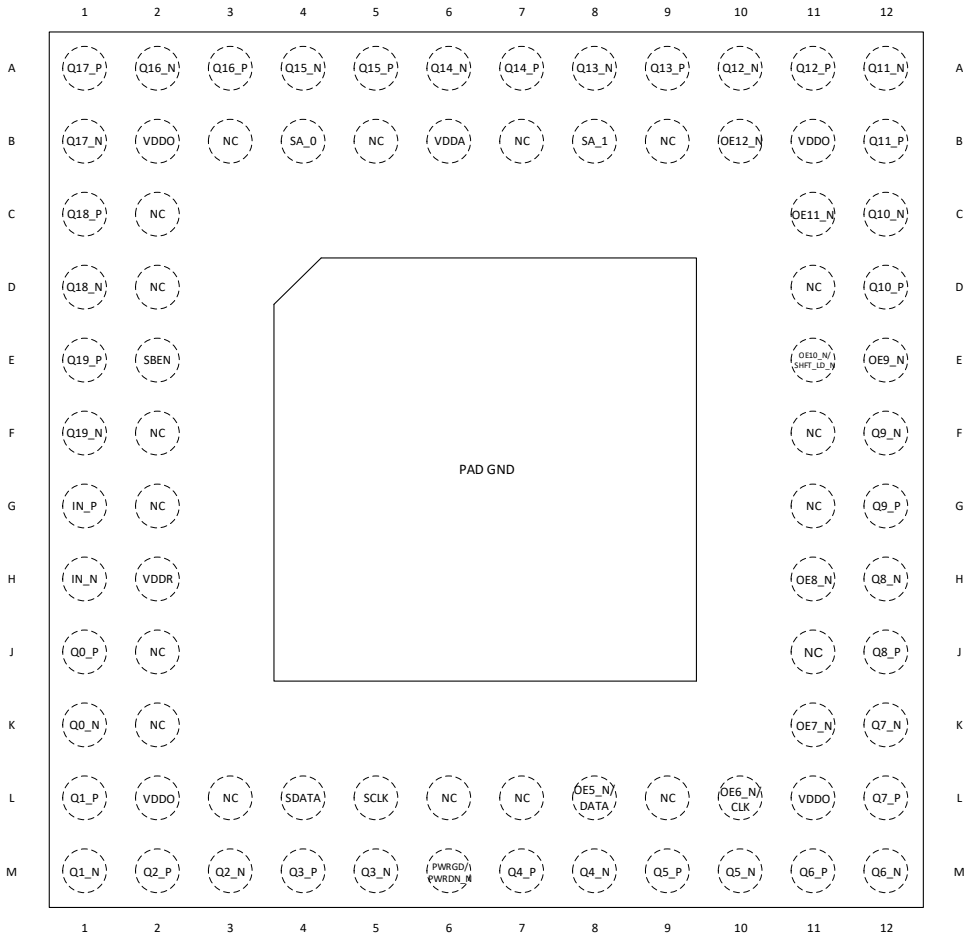
Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ82100EDQ	AQFN6×6-80	**GQF*xyz***

Device code: GQF

x=year code, y=week code, z=lot number code

Pinout (Top View)



(AQFN6×6-80)

Pin Description

Pin No.	Pin Name	Type		Description
A1	Q17_P	Output	HCSL	Differential true clock output.
A2	Q16_N	Output	HCSL	Differential complementary clock output.
A3	Q16_P	Output	HCSL	Differential true clock output.
A4	Q15_N	Output	HCSL	Differential complementary clock output.
A5	Q15_P	Output	HCSL	Differential true clock output.
A6	Q14_N	Output	HCSL	Differential complementary clock output.
A7	Q14_P	Output	HCSL	Differential true clock output.
A8	Q13_N	Output	HCSL	Differential complementary clock output.
A9	Q13_P	Output	HCSL	Differential true clock output.
A10	Q12_N	Output	HCSL	Differential complementary clock output.
A11	Q12_P	Output	HCSL	Differential true clock output.
A12	Q11_N	Output	HCSL	Differential complementary clock output.
B1	Q17_N	Output	HCSL	Differential complementary clock output.
B2	VDDO	Power		Nominal 3.3V power supply for outputs.
B3	NC			No connect.
B4	SA_0	Input	CMOS	SMBus address bit. A tri-level input that operates with the SA_1 pin, if present, to decode SMBus addresses. It includes internal pullup/down resistors to bias to VDDA/2.
B5	NC			No connect.
B6	VDDA	Power		Nominal 3.3V power supply for analog block.
B7	NC			No connect.
B8	SA_1	Input	CMOS	SMBus address bit. A tri-level input that operates with the SA_0 pin, if present, to decode SMBus addresses. It includes internal pullup/down resistors to bias to VDDA/2.
B9	NC			No connect.
B10	OE12_N	Input	CMOS	Active low input for enabling Q12 pair. 1 = disable outputs, 0 = enable outputs. The pin features an internal pulldown and power-down tolerant inputs.
B11	VDDO	Power		Nominal 3.3V power supply for outputs.
B12	Q11_P	Output	HCSL	Differential true clock output.
C1	Q18_P	Output	HCSL	Differential true clock output.
C2	NC			No connect.
C11	OE11_N	Input	CMOS	Active low input for enabling Q11 pair. 1 = disable outputs, 0 = enable outputs. The pin features an internal pulldown and power-down tolerant inputs.
C12	Q10_N	Output	HCSL	Differential complementary clock output.

D1	Q18_N	Output	HCSL	Differential complementary clock output.
D2	NC			No connect.
D11	NC			No connect.
D12	Q10_P	Output	HCSL	Differential true clock output.
E1	Q19_P	Output	HCSL	Differential true clock output.
E2	SBEN	Input	CMOS	SBEN enables either the OE pin and SMBus or the side-band interface for controlling output enables. Features power-down tolerant inputs. SBEN=0, OE pins and SMBus enable bits are enabled, Side-Band interface is disabled. SBEN=1, OE pins and SMBus enable bits are disabled, Side-Band interface is enabled.
E11	OE10_N/SHFT_LD_N	Input	CMOS	Active low input for enabling output 10 or SHFT_LD_N pin for the Side-Band Interface. This pin has an internal pulldown and is powerdown tolerant. When SBEN=0, OE mode, OE10_N/SHFT_LD_N =1, disable output 10, OE10_N/SHFT_LD_N =0, enable output 10. When SBEN=1, Side-Band Mode: OE10_N/SHFT_LD_N =1, enable Side-Band Interface shift register, OE10_N/SHFT_LD_N =0, disable Side-Band Interface shift register. Transfers Side-Band shift register into output register on the falling edge.
E12	OE9_N	Input	CMOS	Active low input for enabling Q9 pair. Power down tolerant inputs. OE9_N =1, disable output 9, OE9_N =0, enable output 9.
F1	Q19_N	Output	HCSL	Differential complementary clock output.
F2	NC			No connect.
F11	NC			No connect.
F12	Q9_N	Output	HCSL	Differential complementary clock output.
G1	IN_P	Input	HCSL	Differential true clock input.
G2	NC			No connect.
G11	NC			No connect.
G12	Q9_P	Output	HCSL	Differential true clock output.
H1	IN_N	Input	HCSL	Differential complementary clock input.
H2	VDDR	Power		Nominal 3.3V power supply for input clock circuits.
H11	OE8_N	Input	CMOS	Active low input for enabling Q8 pair. Power down tolerant inputs. OE8_N =1, disable output 8, OE8_N =0, enable output 8.
H12	Q8_N	Output	HCSL	Differential complementary clock output.
J1	Q0_P	Output	HCSL	Differential true clock output.
J2	NC			No connect.

J11	NC			No connect.
J12	Q8_P	Output	HCSL	Differential true clock output.
K1	Q0_N	Output	HCSL	Differential complementary clock output.
K2	NC			No connect.
K11	OE7_N	Input	CMOS	Active low input for enabling Q7 pair. This input is power down tolerant. OE7_N =1, disable output 7, OE7_N =0, enable output 7.
K12	Q7_N	Output	HCSL	Differential complementary clock output.
L1	Q1_P	Output	HCSL	Differential true clock output.
L2	VDDO	Power		Nominal 3.3V power supply for outputs.
L3	NC			No connect.
L4	SDATA	I/O	CMOS	SMBus data pin. Power down tolerant inputs.
L5	SCLK	Input	CMOS	SMBus clock pin. Power down tolerant inputs.
L6	NC			No connect.
L7	NC			No connect.
L8	OE5_N/DATA	Input	CMOS	Active low input for enabling output 5 or the data pin for the Side-Band Interface. This pin features an internal pulldown. This input is power down tolerant. When SBEN=0, OE mode, OE5_N/DATA is OE pin. OE5_N/DATA =1, disable output 5, OE5_N/DATA =0, enable output 5. When SBEN=1, Side-Band Mode: OE5_N/DATA is SBI data pin.
L9	NC			No connect.
L10	OE6_N/CLK	Input	CMOS	Active low input for enabling output 6 or the clock pin for the Side-Band Interface shift register. This pin has an internal pulldown and is power down tolerant. When SBEN=0, OE mode, OE6_N/CLK is OE pin. OE6_N/CLK =1, disable output 6, OE6_N/CLK =0, enable output 6. When SBEN=1, Side-Band Mode, OE6_N/CLK is the SMB clock pin. Clocks data into the Side-Band Interface shift register on the OE6_N/CLK rising edge.
L11	VDDO	Power		Nominal 3.3V power supply for outputs.
L12	Q7_P	Output	HCSL	Differential true clock output.
M1	Q1_N	Output	HCSL	Differential complementary clock output.
M2	Q2_P	Output	HCSL	Differential true clock output.
M3	Q2_N	Output	HCSL	Differential complementary clock output.
M4	Q3_P	Output	HCSL	Differential true clock output.
M5	Q3_N	Output	HCSL	Differential complementary clock output.

M6	PWRGD/ PWRDN_ N	Input	CMOS	The input signals the device to sample latched inputs and start up on the first high assertion. This pin includes an internal pulldown resistor and is power down tolerant. PWRGD/PWRDN_N = 0, power down mode, PWRGD/PWRDN_N = 1, Exit power down mode.
M7	Q4_P	Output	HCSL	Differential true clock output.
M8	Q4_N	Output	HCSL	Differential complementary clock output.
M9	Q5_P	Output	HCSL	Differential true clock output.
M10	Q5_N	Output	HCSL	Differential complementary clock output.
M11	Q6_P	Output	HCSL	Differential true clock output.
M12	Q6_N	Output	HCSL	Differential complementary clock output.
EPAD	Power			Connect to ground.

Functional Block Diagram

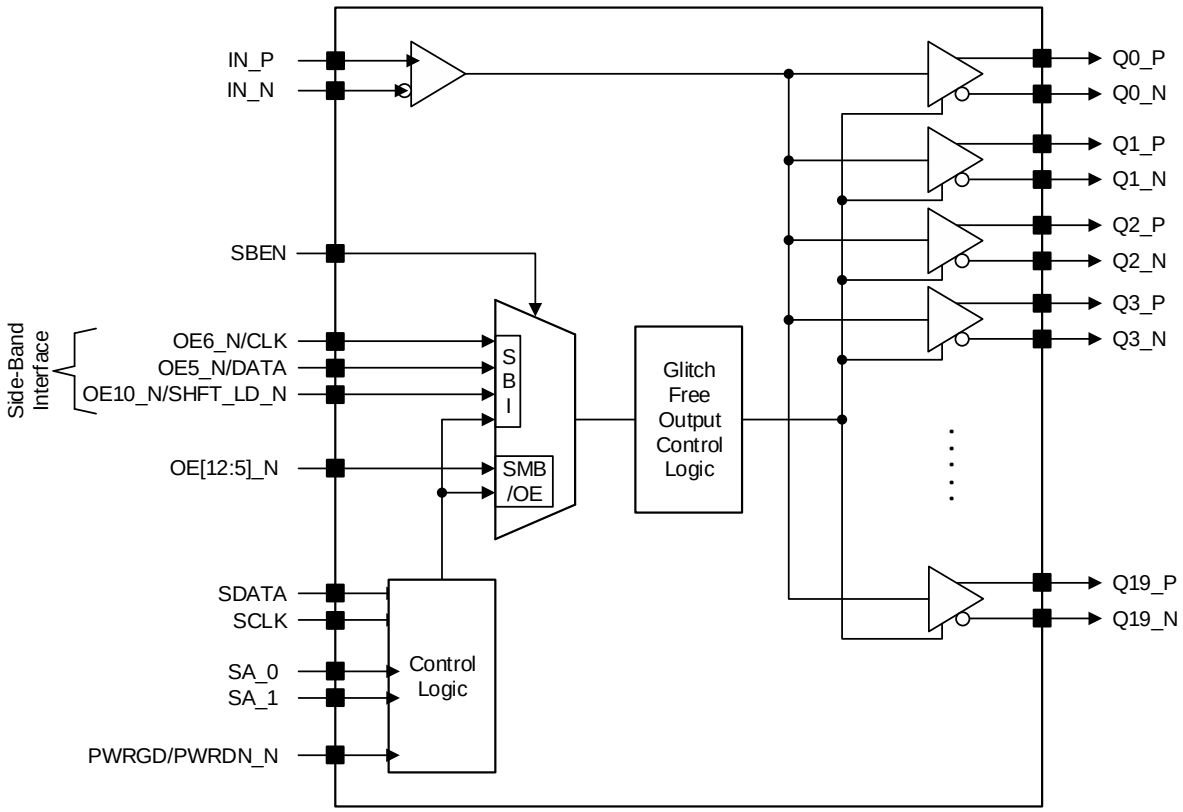


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
VDDA, VDDO, VDDR		-0.5	4	V
Clock Input IN_P/N Pins		-0.5	2.5	V
VIN Input Control Pins		-0.5	VDDA+0.5	V
Junction Temperature, Operating		-40	125	°C
Storage Temperature		-65	150	°C
V_{ESD} Electrostatic Discharge	Human-body Model (HBM)	± 2500		V
	Charged Device Model (CDM)	± 750		V

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	24	°C/W
θ_{JB} Junction-to-Board Thermal Resistance	9	
θ_{JC} Junction-to-Case (Top) Thermal Resistance	23.2	
θ_{JC} Junction-to-Case (Bottom) Thermal Resistance	2.5	
Ψ_{JT} Junction-to-Top Characterization Parameter	0.6	
P_D Power Dissipation T_A = 25°C	0.66	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Operation Ambient Temperature Range	-40	85	°C
Operation Junction Temperature Range	-40	125	°C
Core Supply Voltage Range (VDDA, VDDR)	3.135	3.465	V
Output Supply Voltage Range(VDDO)	3.135	3.465	V

Electrical Characteristics

(VDDA=VDDR=VDDO =3.3V.schmatatic of Figure 10, . T_A = -40°C to 85°C,tycal value are at T_A = 25°C, unless otherwise specified (Note4))

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	V_{DD}	VDDA,VDDR,VDDO	3.135	3.3	3.465	V
Power Supply Current	I_{DD}	VDDA+VDDR+VDDO All outputs active at 100MHz,CL=2pF		200	220	mA
Power Supply Power Down Current	I_{DD_PD}	VDDA+VDDR+VDDO. All outputs disable. PWRGD/PWRDN_N=0.		2.7	5	mA
Ambient Temperature	T_A	Industrial grade	–40		85	°C
SMBus						
Input High Voltage	V_{IH}	SA_0,SA_1. Single-ended tri-level inputs	2.4		V_{DD}+0.3	V
Input Mid Voltage	V_{IM}	SA_0,SA_1. Single-ended tri-level inputs	1.3	$0.5V_{DD}$	1.8	V
Input Low Voltage	V_{IL}	SA_0,SA_1. Single-ended tri-level inputs	-0.3		0.8	V
Internal Pullup Resistance	R_{PU}	SA_0,SA_1. Single-ended tri-level inputs	150	220	290	kΩ
Internal Pulldown Resistance	R_{DN}	SA_0,SA_1. Single-ended tri-level inputs	150	220	290	kΩ
Input High Current	I_{IH}	SA_0,SA_1.Single-ended tri-level inputs, V_{IN} = V_{DD}	10	15	20	µA
Input Low Current	I_{IL}	SA_0,SA_1.Single-ended tri-level inputs, V_{IN} = 0V	-20	-15	-10	µA
Pin Inductance (Note 5)	L_{PIN}	SCLK,SDATA.			7	nH
Nominal Bus Voltage	V_{DDSMB}	SCLK,SDATA.	2.7		3.6	V
SMBus Input High Voltage	V_{IHSMB}	SCLK,SDATA. V_{DDSMB} = 3.3V	2		V_{DDSMB}	V
SMBus Input Low Voltage	V_{ILSMB}	SCLK,SDATA. V_{DDSMB} = 3.3V			0.8	V
SMBus Sink Current	$I_{SMBSINK}$	SCLK,SDATA. at V_{OLSMB}	4			mA
SMBus Output Low Voltage	V_{OLSMB}	SCLK,SDATA. at $I_{SMBSINK}$			0.4	V
SMBus Operating Frequency (Note 5)	f_{MAXSMB}	SCLK,SDATA. Maximum frequency			400	kHz
SMBus Rise Time (Note 5)	t_{RMSB}	SCLK,SDATA. (Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)		800		ns
SMBus Fall Time (Note 5)	t_{FMSB}	SCLK,SDATA. (Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)		10		ns
Digital Control						
Input High Voltage	V_{IH}	PWRGD/PWRDN_P, OEx_N,SBEN. Single-ended inputs.	2		V_{DD}+0.3	V

Input Low Voltage	V_{IL}	PWRGD/PWRDN_P, OEx_N,SBEN. Single-ended inputs.	-0.3		0.8	V
Input High Current	I_{IH}	PWRGD/PWRDN_P, OEx_N,SBEN. Single-ended inputs with pull down resistor. $V_{IN} = V_{DD}$	20	30	40	µA
Input Capacitance (Note 5)	C_{IN}	PWRGD/PWRDN_P, OEx_N,SBEN. Single-ended inputs.	1.5		5	pF
Rise/ Fall Time of Input (Note 5)	t_{RF}	PWRGD/PWRDN_P, OEx_N,SBEN. Single-ended inputs.			5	ns
HCSL Input						
Input Frequency (Note 5)	f_{IN}	IN_P,IN_N. Differential frequency	1	100	400	MHz
Diff. Input Swing Voltage (Note 5)	V_{SWING}	IN_P,IN_N. Peak to peak value (V_{IHDIF}-V_{ILDIF})	200			mV
Common Mode Voltage (Note 5)	V_{COM}	IN_P,IN_N.	100		900	mV
Diff. Input Slew Rate (Note 5)	dv/dt	IN_P,IN_N.	0.7			V/ns
Single-end Input Leakage Current	I_{IN_P}	IN_P,IN_N. $V_{IN\_P} = V_{DD}$, $V_{IN\_N} = 0V$	60		120	µA
Single-end Input Leakage Current	I_{IN_N}	IN_P,IN_N. VIN_N = VDD, VIN_P= 0V	10		22	uA
Diff. Input Duty Cycle (Note 5)	t_{DC}	IN_P,IN_N. Measured differentially	45		55	%
HCSL Output						
Maximum Output Voltage (Note 5)	V_{MAX}	Qx_P,QxN (x=0~19).Measurement on single-ended signal using absolute value	660	780	900	mV
Minimum Output Voltage (Note 5)	V_{MIN}	Qx_P,QxN (x=0~19).	-150	-20	150	mV
Absolute Crossing Point Voltage (Note 5)	V_{cross} absolute	Qx_P,QxN (x=0~19).	250		550	mV
Relative Crossing Point Voltage (Note 5)	V_{cross} relative	Qx_P,QxN (x=0~19).			140	mV
Output Frequency (Note 5)	f_{OUT}	Qx_P,QxN (x=0~19).		100	400	MHz
Slew Rate (Note 5)	t_{RF}	Qx_P,QxN (x=0~19).Scope averaging enabled, 10-inch trace. Measured using ±150mV window around differential 0V.	2	3	4	V/ns
Slew Rate Matching (Note 5)	Dt_{RF}	Qx_P,QxN (x=0~19).Scope averaging enabled, 10-inch trace. Measured using ±75mV window around Crossing Point			20	%
Output Skew (Note 5)	t_{SKEW}	Qx_P,QxN (x=0~19).Averaging enabled, VT = 50%			50	ps
Diff. Output Duty Cycle (Note 5)	t_{DC}	Qx_P,QxN (x=0~19).Measured differentially	45		55	%
Duty Cycle Distortion (Note 5)	DC Distortion	Qx_P,QxN (x=0~19).Measured differentially at 100 MHz	-0.5		0.5	%
Propagation Delay (Note 5)	t_{pd}	Qx_P,QxN (x=0~19). Input to Output delay.		2	3	ns

Output Enable Latency(Note 5)	t_{OELAT}	Qx_P,QxN starts after OEx_N assertion (x=0~19) Qx_P,QxN stops after OEx_N de-assertion (x=0~19)		5	10	clocks
PD_N De-assertion (Note 5)	t_{PDLAT}	Qx_P,QxN (x=0~19). Differential outputs enable after PWRGD/PWRDN_N de-assertion		20	300	µs
Output Stabilization(Note 5)	t_{STAB}	Qx_P,QxN (x=0~19). From power up and after input clock stabilization or after PWRGD/PWRDN_N de-assertion to 1st clock		0.3	1.8	ms
Output differential Impedance	Z_{diff}	Qx_P,QxN (x=0~19). Output impedance.	81	85	89	Ω
Side-Band Interface (Note5)						
Side-Band Clock Period	t_{PERIOD}	OE6_N/CLK as SBI Clock Period	40			ns
SHFT Setup Time	t_{SETUP}	OE10_N/SHFT_LD_N as SBI SHFT setup time to CLK rising edge	10			ns
Data Setup Time	t_{DSETUP}	OE5_N/DATA as SBI DATA setup time to CLK rising edge	5			ns
Data Hold Time	t_{DHOLD}	OE5_N/DATA as SBI DATA hold time after CLK rising edge	2			ns
Delay Time	t_{DELAY}	Qx_P,QxN (x=0~19).Delay from OE6_N/CLK rising edge to LD_N falling edge	10			ns
LD_N Delay	t_{LD}	Qx_P,QxN (x=0~19).Delay OE10_N/SHFT_LD_N falling edge to next output configuration taking effect	4		10	clocks
CLK Slew Rate	t_{RF}	OE6_N/CLK as SBI CLK input between 20% to 80%	0.7	1	4	V/ns
PCIe Common Clock (CC) Architecture Jitter (Note5)						
Additive Integrated Phase Jitter (RMS)	t_{jPHASE}	PCIe Gen 2 Low Band, 10kHz < f <1.5MHz (PLL BW 5-16MHz or 8-5MHz, CDR = 5MHz)		0.02	0.003	ps
		PCIe Gen 2 High Band, 1.5MHz < f <Nyquist (50MHz); (PLL BW 5-16MHz or 8-5MHz, CDR = 5MHz)		0.06	0.09	ps
		PCIe Gen 3 (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.025	0.035	ps
		PCIe Gen 4 (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.025	0.035	ps
		PCIe Gen 5 (PLL BW of 500k to 1.8MHz. CDR =20MHz)		0.011	0.016	ps
		PCIe Gen 6 (PLL BW of 500k to 1MHz. CDR =10MHz)		0.005	0.008	ps
		100MHz (12kHz to 20MHz)		55	90	fs
		156.25MHz (12kHz to 20MHz)		50	90	fs
		100MHz, apply DB2000Q filter, see Figure 6		17	20	fs

PCIe Independent Reference Clock Architecture Jitter (Note5)						
Additive Integrated Phase Jitter (RMS)	t_{jPHASE}	PCIe Gen 3 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.035	0.045	ps
		PCIe Gen 4 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.035	0.045	ps
		PCIe Gen 4 SRNS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0.025	0.035	ps
		PCIe Gen 5 SRIS (PLL BW 1.8MHz, CDR= 20MHz)		0.01	0.015	ps
		PCIe Gen 5 SRNS (PLL BW 1.8MHz, CDR= 20MHz)		0.01	0.015	ps
		PCIe Gen 6 SRIS (PLL BW 1MHz, CDR= 10MHz)		0.008	0.011	ps
		PCIe Gen 6 SRNS (PLL BW 1MHz, CDR= 10MHz)		0.008	0.011	ps

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured with natural convection and chip mounted on highly effective four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25°C$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Register Maps

Byte 0: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Q19_OE	Q19 output enable	RW	1	Low/Low	Enable
5	Q18_OE	Q18 output enable	RW	1	Low/Low	Enable
4	Q17_OE	Q17 output enable	RW	1	Low/Low	Enable
3	Q16_OE	Q16 output enable	RW	1	Low/Low	Enable
2	Reserved			0		
1	Reserved			0		
0	Reserved			0		

Byte 1: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q7_OE	Q7 output enable	RW	1	Low/Low	OE7_N control
6	Q6_OE	Q6 output enable	RW	1	Low/Low	OE6_N control
5	Q5_OE	Q5 output enable	RW	1	Low/Low	OE5_N control
4	Q4_OE	Q4 output enable	RW	1	Low/Low	Enable
3	Q3_OE	Q3 output enable	RW	1	Low/Low	Enable
2	Q2_OE	Q2 output enable	RW	1	Low/Low	Enable
1	Q1_OE	Q1 output enable	RW	1	Low/Low	Enable
0	Q0_OE	Q0 output enable	RW	1	Low/Low	Enable

Byte 2: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q15_OE	Q15 output enable	RW	1	Low/Low	Enable
6	Q14_OE	Q14 output enable	RW	1	Low/Low	Enable
5	Q13_OE	Q13 output enable	RW	1	Low/Low	Enable
4	Q12_OE	Q12 output enable	RW	1	Low/Low	OE12_N control
3	Q11_OE	Q11 output enable	RW	1	Low/Low	OE11_N control
2	Q10_OE	Q10 output enable	RW	1	Low/Low	OE10_N control
1	Q9_OE	Q9 output enable	RW	1	Low/Low	OE9_N control
0	Q8_OE	Q8 output enable	RW	1	Low/Low	OE8_N control

Byte 3: OE_N Pin Realtime Readback Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1

7	OE12_N	Realtime Readback of OE12_N	R	Realtime	OE12_N=Low	OE12_N=High
6	OE11_N	Realtime Readback of OE11_N	R	Realtime	OE11_N=Low	OE11_N=High
5	OE10_N	Realtime Readback of OE10_N	R	Realtime	OE10_N=Low	OE10_N=High
4	OE9_N	Realtime Readback of OE9_N	R	Realtime	OE9_N=Low	OE9_N=High
3	OE8_N	Realtime Readback of OE8_N	R	Realtime	OE8_N=Low	OE8_N=High
2	OE7_N	Realtime Readback of OE7_N	R	Realtime	OE7_N=Low	OE7_N=High
1	OE6_N	Realtime Readback of OE6_N	R	Realtime	OE6_N=Low	OE6_N=High
0	OE5_N	Realtime Readback of OE5_N	R	Realtime	OE5_N=Low	OE5_N=High

Byte 4: SBEN

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:1	Reserved			0		
0	RB_SBEN	Readback of SBEN	R	Realtime	SBEN=Low	SBEN=High

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	Revision ID = 0001	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Vendor ID = 0100	
2	PVID2		R	0		
1	PVID1		R	1		
0	PVID0		R	1		

Byte 6: Device Type/Device ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DID7	Device ID	R	1		
6	DID6		R	1		
5	DID5		R	0		
4	DID4		R	0		
3	DID3		R	1		
2	DID2		R	0		
1	DID1		R	1		
0	DID0		R	0		

Byte 7: Byte Count Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back; the default is 8 bytes.	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Byte 8: Side-Band Mask Register only when SBEN=1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Mask7	Mask off Side-Band Disable	RW	0	The Side-Band shift register may disable the output.	Ensures the output is enabled regardless of the Side-Band shift register value.
6	Mask6	Mask off Side-Band Disable	RW	0		
5	Mask5	Mask off Side-Band Disable	RW	0		
4	Mask4	Mask off Side-Band Disable	RW	0		
3	Mask3	Mask off Side-Band Disable	RW	0		
2	Mask2	Mask off Side-Band Disable	RW	0		
1	Mask1	Mask off Side-Band Disable	RW	0		
0	Mask0	Mask off Side-Band Disable	RW	0		

Byte 9: Side-Band Mask Register only when SBEN=1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Mask15	Mask off Side-Band Disable	RW	0	The Side-Band shift register may disable the output.	Ensures the output is enabled regardless of the Side-Band shift register value.
6	Mask14	Mask off Side-Band Disable	RW	0		
5	Mask13	Mask off Side-Band Disable	RW	0		
4	Mask12	Mask off Side-Band Disable	RW	0		
3	Mask11	Mask off Side-Band Disable	RW	0		
2	Mask10	Mask off Side-Band Disable	RW	0		
1	Mask9	Mask off Side-Band Disable	RW	0		
0	Mask8	Mask off Side-Band Disable	RW	0		

Byte 10: Side-Band Mask Register only when SBEN=1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		

4	Reserved			0		
3	Mask19	Mask off Side-Band Disable	RW	0	The Side-Band shift register may disable the output.	Ensures the output is enabled regardless of the Side-Band shift register value.
2	Mask18	Mask off Side-Band Disable	RW	0		
1	Mask17	Mask off Side-Band Disable	RW	0		
0	Mask16	Mask off Side-Band Disable	RW	0		

Byte 11: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q19	Impedance selection of Q19	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
6	Z1_Q19		RW	0		
5	Reserved			0		
4	Z0_Q18	Impedance selection of Q18	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
3	Z1_Q18		RW	0		
2	Reserved			0		
1	Z0_Q17	Impedance selection of Q17	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
0	Z1_Q17		RW	0		

Byte 12: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q16	Impedance selection of Q16	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
5	Z1_Q16		RW	0		
4	Reserved			0		
3	Z0_Q15	Impedance selection of Q15	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
2	Z1_Q15		RW	0		
1	Reserved			0		
0	Reserved			0		

Byte 13: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q14	Impedance selection of Q14	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
6	Z1_Q14		RW	0		
5	Reserved			0		
4	Z0_Q13	Impedance selection of Q13	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
3	Z1_Q13		RW	0		
2	Reserved			0		
1	Z0_Q12	Impedance selection of Q12	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
0	Z1_Q12		RW	0		

Byte 14: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q11	Impedance selection of Q11	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
5	Z1_Q11		RW	0		
4	Reserved			0		
3	Z0_Q10	Impedance selection of Q10	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
2	Z1_Q10		RW	0		
1	Reserved			0		
0	Reserved			0		

Byte 15: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q9	Impedance selection of Q9	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
6	Z1_Q9		RW	0		
5	Reserved			0		
4	Z0_Q8	Impedance selection of Q8	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
3	Z1_Q8		RW	0		
2	Reserved			0		
1	Z0_Q7	Impedance selection of Q7	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
0	Z1_Q7		RW	0		

Byte 16: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q6	Impedance selection of Q6	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
5	Z1_Q6		RW	0		
4	Reserved			0		
3	Z0_Q5	Impedance selection of Q5	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
2	Z1_Q5		RW	0		
1	Reserved			0		
0	Reserved			0		

Byte 17: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q4	Impedance selection of Q4	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
6	Z1_Q4		RW	0		

5	Reserved			0		
4	Z0_Q3	Impedance selection of Q3	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
3	Z1_Q3		RW	0		
2	Reserved			0		
1	Z0_Q2	Impedance selection of Q2	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	

Byte 18: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q1	Impedance selection of Q1	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
5	Z1_Q1		RW	0		
4	Reserved			0		
3	Z0_Q0	Impedance selection of Q0	RW	0	00 or 11 = Nominal 01=-5%, 10=+5%	
2	Z1_Q0		RW	0		
1	Reserved			0		
0	Reserved			0		

Byte 19: Reserved

Byte 20: Stop State Configuration Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	VSW[2]	Global differential output swing control	RW	1	Default=750mV 0.3V-1.0V 100mV/Step	
6	VSW[1]		RW	0		
5	VSW[0]		RW	1		
4	Reserved			0		
3	Reserved			0		
2	Reserved			1		
1	STOPST[1]	Differential Stop Mode State	RW	0	00=Low/Low; 10=High/Low 01=HiZ/HiZ; 11=Low/High	
0	STOPST[0]		RW	0		

Byte 21: Power down Restore Configuration Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	Reserved			0		
3	PD_RESTORE_N	Save configuration in power down mode	RW	1	Config cleared	Config saved

2	Reserved			0		
1	Reserved			0		
0	Reserved			0		

SMBus Address Selection Table

SA_1	SA_0	Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

SMBus Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	……	8 bits	1 bit	1 bit
Start bit	SMBus Address	W(0)	Ack	Start Register Address	Ack	Total Writing Bytes Quantity	Ack	First Byte	Ack	……	Last Byte	Ack	Stop bit

SMBus Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	……	8 bits	1 bit	1 bit
Start bit	SMBus Address	W(0)	Ack	Reading Register Address	Ack	Repeat Start bit	SMBus Address	R(1)	Ack	Total Reading Bytes Quantity	Ack	First Reading Byte	Ack	……	Last Reading Data Byte	NAck	Stop bit

Output Control - SBEN=0

Inputs		OE_N Pins and Register Bits		Side-Band Interface		
PWRGD/ PWRDN_N	IN_P/IN_N	SMBus Enable Bit	OE_N Pin	MASKx Byte[10:8]	Dx	Q_P/Q_N [19:0]
0	X	X	X	X	X	Low/Low
1	Running	0	X	X	X	Low/Low
		1	0	X	X	Running
		1	1	X	X	Low/Low
1	Stopped	1	0	X	X	Stopped
		1	1	X	X	Low/Low

Output Control - SBEN=1

Inputs	OE_N Pins and Register Bits	Side-Band Interface	

PWRGD/ PWRDN_N	IN_P/IN_N	SMBus Enable Bit	OE_N Pin	MASKx Byte[10:8]	Dx	Q_P/Q_N [19:0]
0	X	X	X	X	X	Low/Low
1	Running	X	X	0	0	Low/Low
		X	X	0	1	Running
		X	X	1	X	Running
1	Stopped	X	X	0	0	Low/Low
		X	X	0	1	Stopped
		X	X	1	X	Stopped

Detailed Description

Output Enable Control on SQ82100

The SQ82100 offers two methods for enabling and disabling the 20-channel output clock. The first method uses the OE_N pins, and SMBus output enable bits. The second method is controlled by the side-band interface (SBI), a simple 3-wire serial interface. Both interfaces cannot operate simultaneously; the logic level of the SBEN pin determines the active interface. If SBEN is set to high, the SBI is enabled. If SBEN is set to low, the traditional OE_N pin and SMBus output are enabled as the interface.

The enable or disable synchronization logic for those two methods can ensure that the output enable bits are glitch-free at startup.

Traditional Method

Outputs 5 through 12 have dedicated output enable pins, and each of the 20 outputs has dedicated SMBus output enable bits in Byte0, Byte1, and Byte2 of the SMBus registers.

Side-Band Interface

As shown in Figure 3, the second method of the Side-Band Interface (SBI) is achieved via the pins of SBI_DATA (OE5_N/DATA), SBI_CLK (OE6_N/CLK) and SHFT_LD_N (OE10_N/SHFT_LD_N). When the OE10_N/SHFT_LD_N pin is high, OE5_N/DATA will be shifted into the shift register on the rising edge of OE6_N/CLK, and then the shift registers will be loaded into the Output Register on the falling edge of the OE10_N/SHFT_LD_N pin.

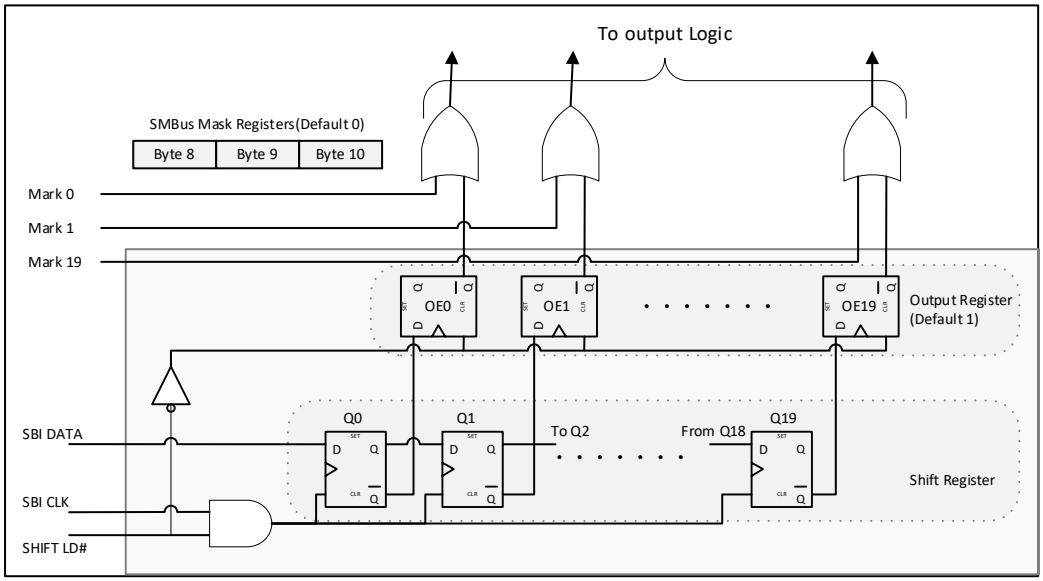


Figure 3. Side-Band Interface

In the SQ82100, only one output enable control interface (SBI or OE and SMBus) is active at a time. The SBEN pin selects the active interface and should not be changed during normal operation. If SBEN is set to low, the traditional OE_N pin/SMBus interface is enabled. If SBEN is set to high, the Side-Band Interface (SBI) is enabled. Bit 0 of read-back register Byte 4 indicates the active interface.

When the SBI is enabled, OE[7:9, 11,12]_N will be disabled. SBI_DATA, SBI_CLK, and SHFT_LD will be enabled on OE5_N/DATA, OE6_N/CLK and OE10_N/SHFT_LD_N pins. And SMBus registers for masking off the disable function of the shift register become active.

When the SBI is enabled and power is applied, the SBI remains active even if the PWRGD/PWRDN_N pin is set to low, indicating power-down mode. This allows loading the shift register into the output register before setting the PWRGD/PWRDN_N pin high to exit power-down mode. However, the mask registers cannot be accessed when PWRGD/PWRDN_N is low because they are used by the normal SMBus interface. Upon power-up, the mask registers default to 0, allowing the SBI shift register bits to disable their respective outputs. The output enable registers default to high, setting the outputs to the enabled state when powering up.

The respective output is enabled when a '1' is set in the mask register. This prevents accidentally disabling critical outputs when using the SBI. The shift order follows the order of the outputs (Q[19:0]), as shown in Figure 4. The first bit is shifted to enable Q19, and the last bit is shifted to enable Q0.

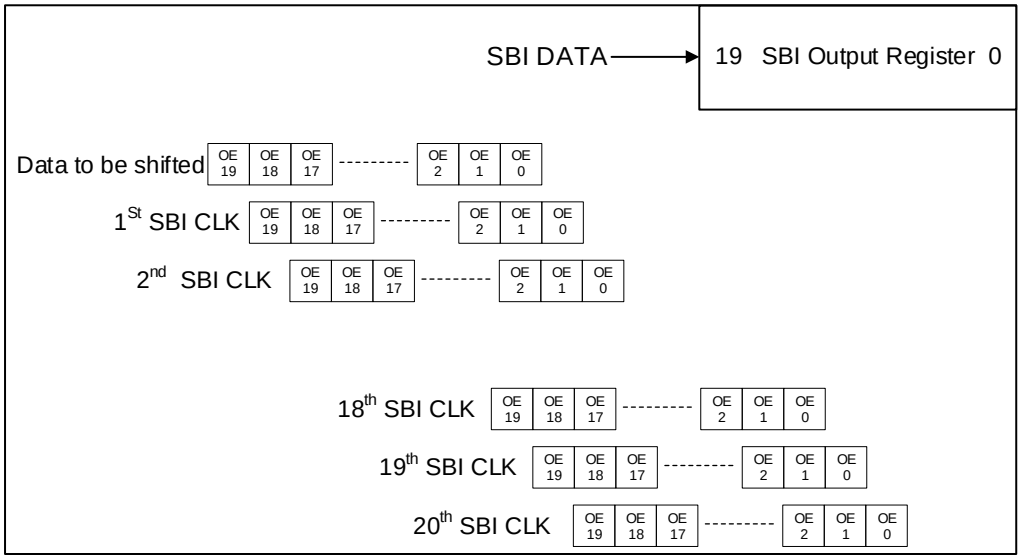


Figure 4. Side-Band Shift Order

The SBI interface supports clock rates up to 25MHz. Multiple devices may share SBI_DATA (OE5_N/DATA) and SBI_CLK (OE6_N/CLK) pins. Dedicating a SHFT_LD_N (OE10_N/SHFT_LD_N) pin to each device allows it be used as a chip-select pin. When the SHFT_LD_N pin is low, the SQ82100 will ignore any activity on the SBI_DATA (OE5_N/DATA) and SBI_CLK (OE6_N/CLK) pins. The sequence chart is shown in Figure 5.

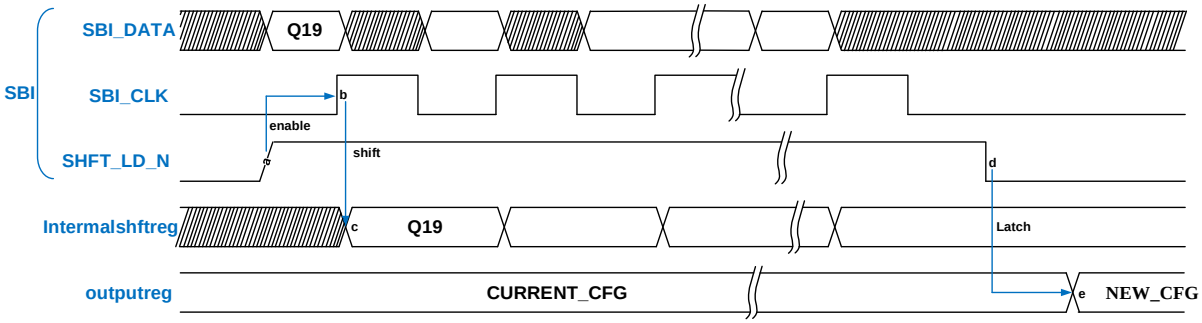


Figure 5. Side-Band Interface Functional Timing

Application and Implementation

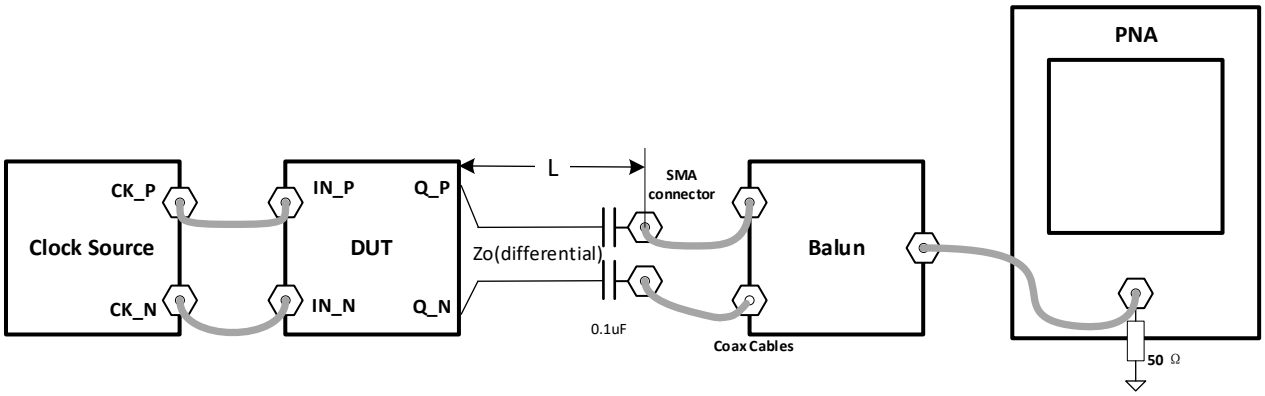


Figure 6. Test Setup for Additive Phase Jitter Measurement

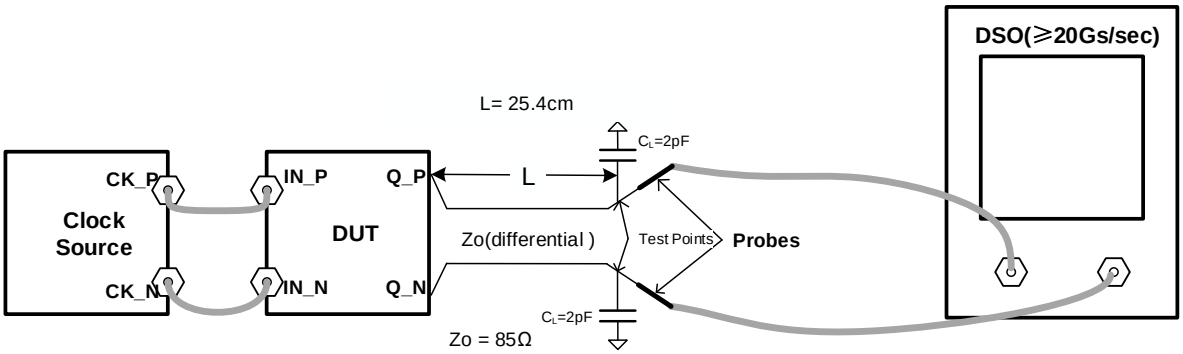


Figure 7. Test Setup for Clock Characteristics

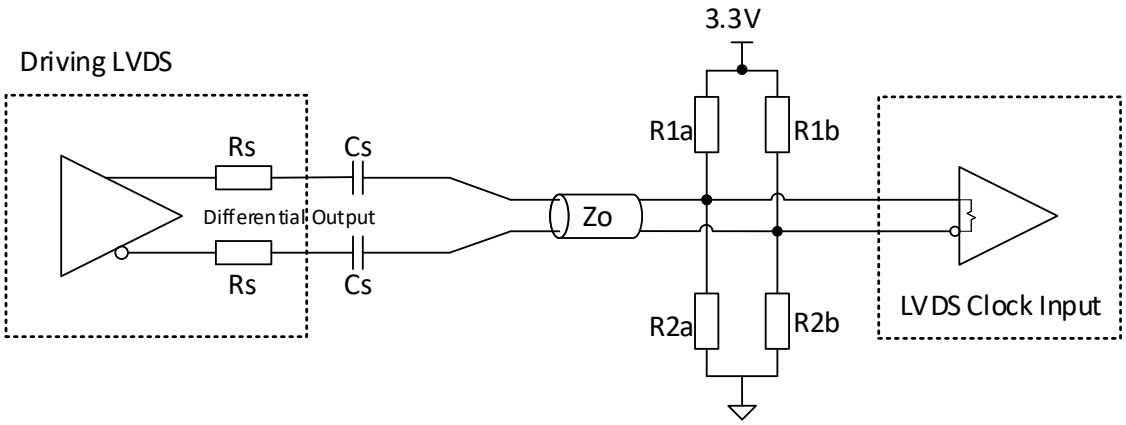


Figure 8. Differential Output Driving LVDS

Differential Output Terminations Driving LVDS (Z0 =85Ω)

Component	Receiver with Termination	Receiver without Termination	Unit
R_{1a}, R_{1b}	10k	130	Ω
R_{2a}, R_{2b}	5.6k	64	Ω
C_C	0.1	0.1	uF
V_{CM}	1.2	1.2	V

Phase Noise Plots

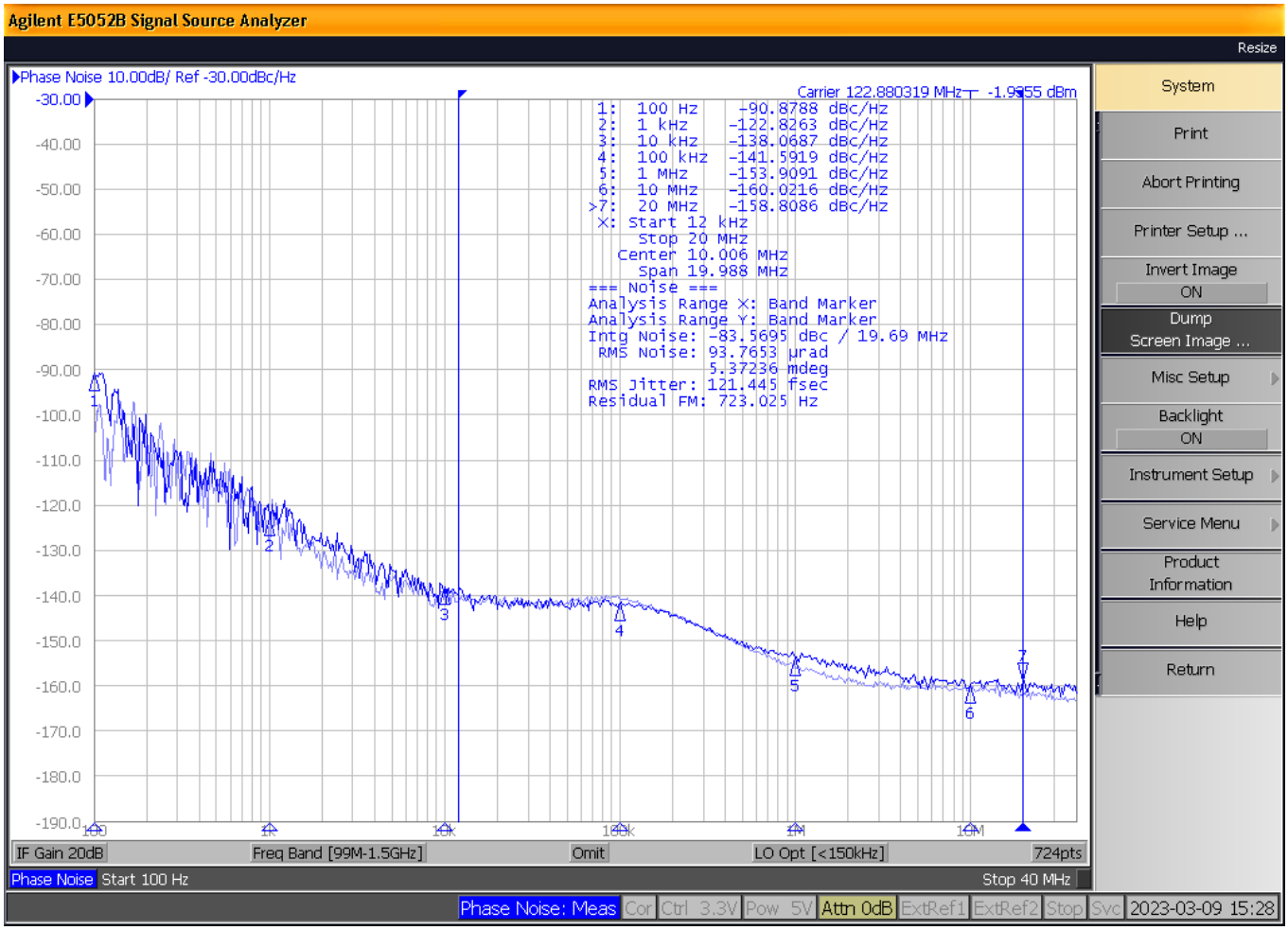


Figure 9. 122.88 MHz Input Phase Noise vs. Output Phase Noise. Additive Jitter 48fs

Application Schematic

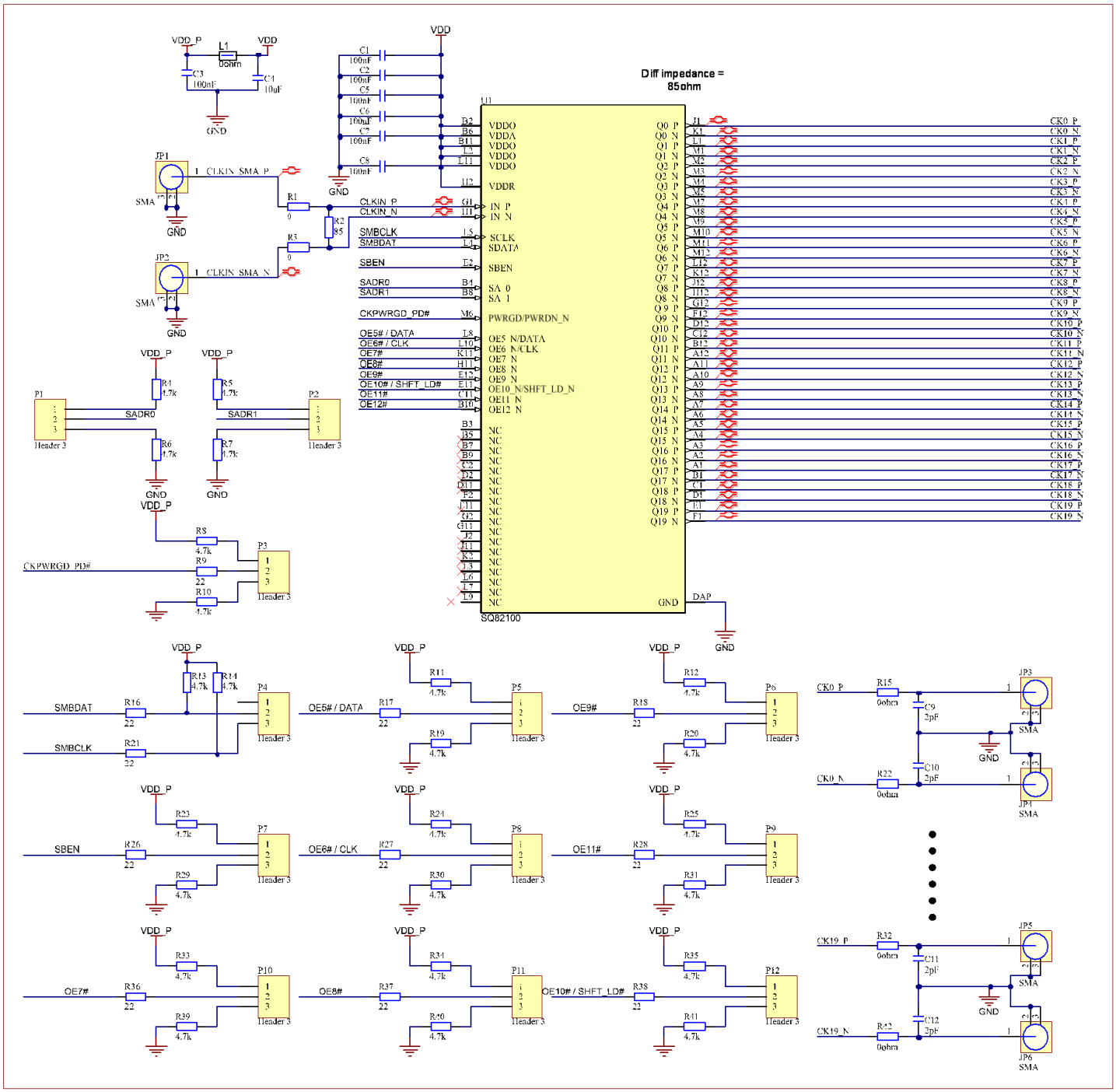


Figure 10. Application Schematic

BOM List

Designator	Description	Part Number	MFR
U1	20-Output PCIe Gen1 to Gen6 Clock Buffer, AQFN6x6-80	SQ82100EDQ	Silergy
C1, C2, C3, C5, C6, C7, C8	100nF ±10% 50V, 0603	GRM188R71H104K	muRata
C9, C10, C11, C12	2pF 50V ±0.1pF	GRM1885C1H2R0BA01D	muRata
C4	10μF ±10% 16V, 3216	TAJA106K016RNJ	Kyocera AVX
JP1, JP2, JP3, JP4, JP5, JP6	SMA, 5.35mm	SMA KHDC3	Eastsheep
L1	Ferrite Bead 30Ω at 100MHz ±25%, 0603	BLM18PG300SN1D	muRata
P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12	HDR1X3	Header 3	
R1, R3, R15, R22, R32, R42	0Ω ±5% 100mW, 0603	RC0603JR-070RL	YAGEO
R2	85Ω ±5% 100mW, 0603	RC0603JR-07080RL	YAGEO
R4, R5, R6, R7, R8, R10, R11, R12, R13, R14, R19, R20, R23, R24, R25, R29, R30, R31, R33, R34, R35, R39, R40, R41	4.7kΩ ±5% 100mW, 0603	RC0603FR-074K7L	YAGEO
R9, R16, R17, R18, R21, R26, R27, R28, R36, R37, R38	22Ω ±5% 100mW, 0603	RC0603JR-07022RL	YAGEO

Layout Guidelines

For optimal design, follow these PCB layout guidelines:

1. 0.1μF capacitors should be used as filters to reduce noise interference from the power supply. It is recommended that C1, C2, and C5 through C8 be placed as close to the power pins as possible.
2. Jumpers P1 through P12 can set up the related logic.
   - P1, P2, P4, and P7 are used for SMBus; details can be found in the Register Map.
   - P5, P8, and P12 are used for SBI; details can be found in the Side-Band Interface section.
   - Other jumpers control the logic to high or low.
3. SMA connectors of JP1 and JP2 are clock input connectors. R2 is used for matching the input clock impedance to 85Ω and should be placed as close to the clock input pins (G1, H1) as possible to avoid abnormal clock input.
4. The nets of CK0_P/N through CK19_P/N and the SMA connectors of JP3/4 through JP5/6 are clock outputs.
5. C9, C10, C11, and C12 simulate the test load with a 10-inch length trace on the PCB. The characteristic impedance of the differential input/output trace should be 85Ω on the PCB.

See Figure 10 for an example of an SQ82100 application schematic. The VCC is 3.3V.

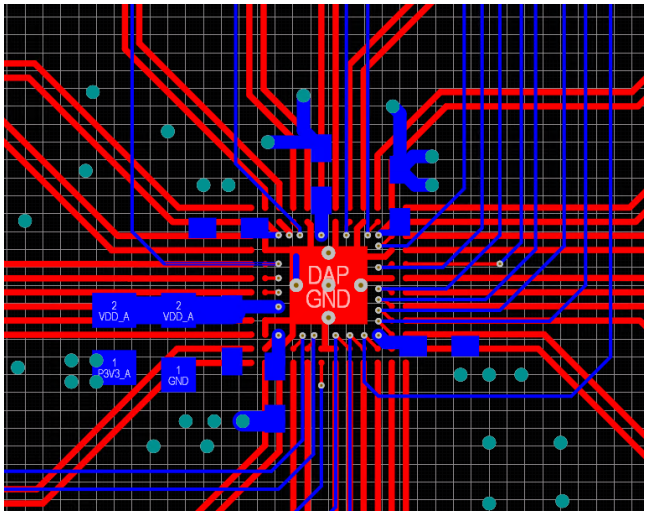
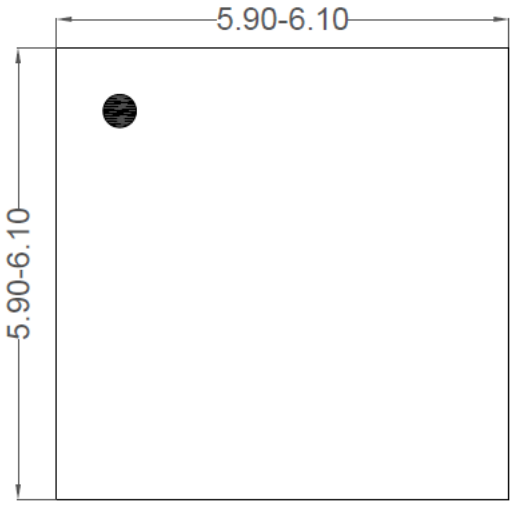
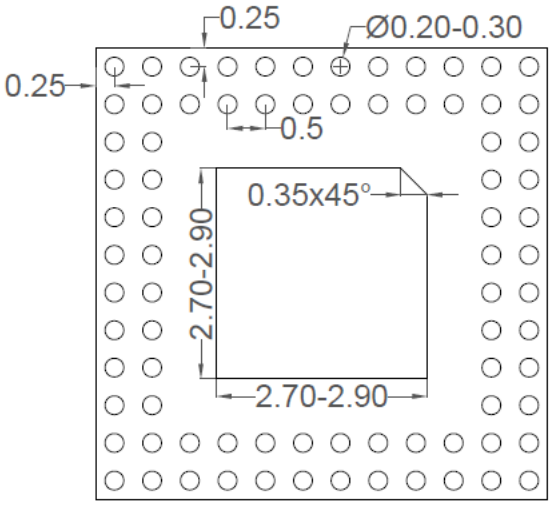


Figure 11. Layout Recommendation

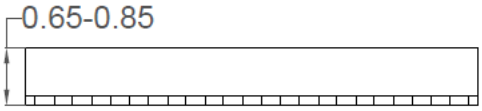
AQFN6x6-80 Package Outline Drawing



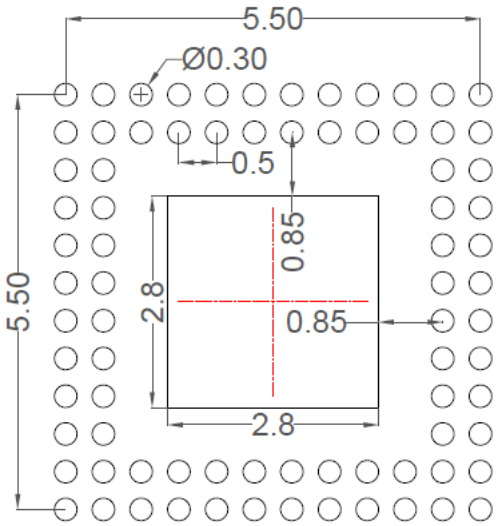
Top View



Bottom View



Front View

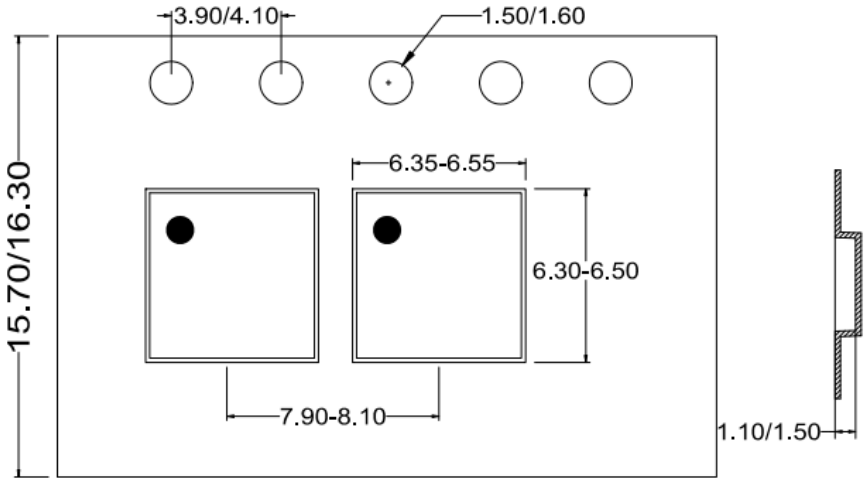


Recommended PCB Layout (Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

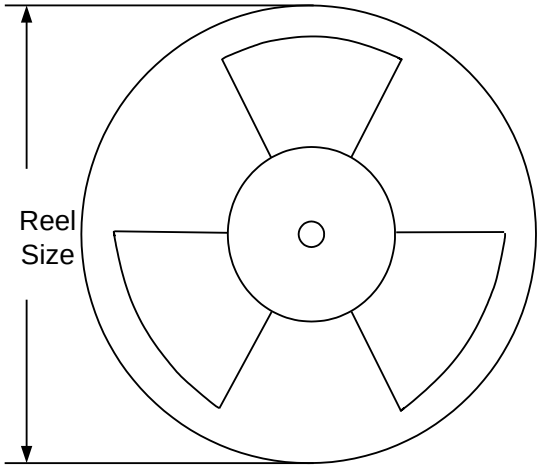
Tape and Reel Information

Tape dimensions and pin 1 orientation



Feeding direction ⟶

Reel dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
AQFN6x6-80	16	8	13"	400	400	2500

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
June 29, 2024	Revision 1.0	Initial Release

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