SA59400

High-Accuracy 12-bit Analog-to-Digital Converter with PGA, Internal Reference and Temperature Sensor

General Description

The SA59400 is a high-accuracy, low power analog-to-digital converter (ADC) featuring an integrated 12-bit high-speed ADC, a programmable gain amplifier (PGA), an oscillator, and a high-accuracy temperature sensor. The PGA provides input ranges from ±128mV to ±4.096V. Capable of performing conversions at data rates up to 4630 samples per second (SPS), the SA59400 enables high-resolution measurements of both small and large signals.

The SA59400 device integrates an input multiplexer (MUX) that supports the measurement of either two differential inputs or four single-ended inputs. An integrated high-accuracy temperature sensor can be used for system-level temperature monitoring or cold-junction compensation in thermocouple applications.

The SA59400 transfers data via a Serial Peripheral Interface (SPI™) and operates in continuous-conversion or single-shot modes. In single-shot mode, the device automatically powers down after a conversion, significantly reducing current consumption during idle periods.

The device has a wide power supply range from 2.7V to 5.5V. It is specified over the extended operating temperature range (–40°C to +125°C) and is available in an MSOP10 package. These features make it ideal for low-power, space-constrained sensor measurement applications.

Features

- Wide Supply Range: 2.7V to 5.5V
- Low Current Consumption:
  - Continuous Mode: 350μA
  - Single-Shot Mode: Automatic Power Down
- Programmable Data Rate: 120 SPS to 4630 SPS
- Single-Cycle Settling
- Internal Low Drift Voltage Reference
- Internal Temperature Sensor:
  - 3°C (Max) Error: -40°C to 125°C
- Internal Oscillator
- Internal PGA
- Two Differential or Four Single-Ended Inputs
- AEC-Q100 Grade 1 Qualified
- MSOP10 Package

Applications

- Battery Management Systems
- Automotive Sensors:
  - Thermocouples
  - Resistance Temperature Detectors (RTDs)
  - Electrochemical Gas Sensors
  - Particulate Matter Sensors

Typical Application

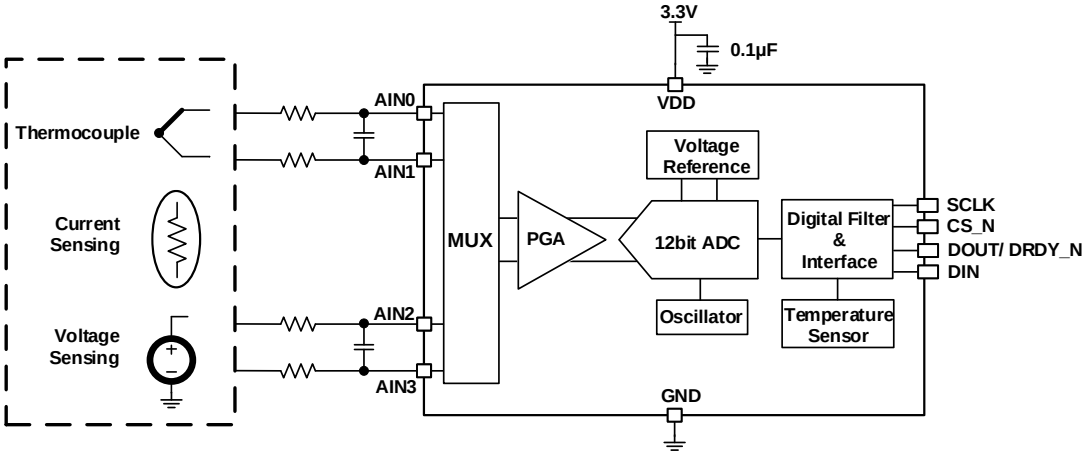


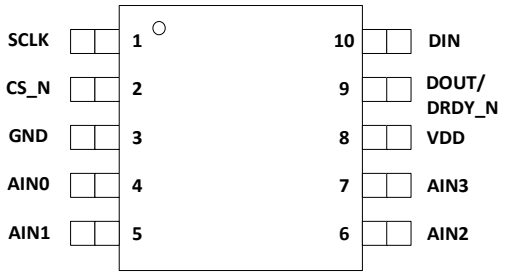
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SA59400FBP	MSOP10	**FQM*xyz***

Device code: FQM
x=year code, y=week code, z= lot number code

Pinout (Top View)



(MSOP10)

Pin Description

Pin No.	Pin Name	Pin Description
1	SCLK	Serial clock input.
2	CS_N	Chip select. Active low. Connect to GND if not in use.
3	GND	Ground.
4	AIN0	Analog input 0. Leave unconnected or tied to VDD if not in use.
5	AIN1	Analog input 1. Leave unconnected or tied to VDD if not in use.
6	AIN2	Analog input 2. Leave unconnected or tied to VDD if not in use.
7	AIN3	Analog input 3. Leave unconnected or tied to VDD if not in use.
8	VDD	Power supply. Connect a 100nF power supply decoupling capacitor to GND.
9	DOUT/DRDY_N	Serial data output combined with data ready. Active low.
10	DIN	Serial data input.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VDD	-0.3	6	V
AIN0/ AIN1/ AIN2/ AIN3	-0.3	VDD+ 0.3	
DIN/ DOUT/DRDY_N/ SCLK/ CS_N	-0.3	VDD+ 0.3	
Input current into any pin	-10	+10	mA
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 4000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	255	°C/W
θ_{JC} Junction-to-Case (top) Thermal Resistance	40	
P_D Power Dissipation T_A = 25°C	1.2	mW

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VDD	2.7	5.5	V
AIN0/ AIN1/ AIN2/ AIN3	0	VDD	V
DIN/ DOUT/DRDY_N/ SCLK/ CS_N	0	VDD	V
Operating Ambient Temperature Range	-40	125	°C

Electrical Characteristics

V_{VDD} = 3.3V, schematic of Figure 1, data rate (DR) = 120 SPS, T_A = 25°C, unless otherwise specified (Note 4).

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Analog Inputs (Note 5)						
Common-Mode Input Impedance		FSR = ±4.096V (Note 6), FSR = ±2.048V, FSR = ±1.024V, FSR = ±0.512V, FSR = ±0.256V, FSR = ±0.128V		100		MΩ
Differential Input Impedance		FSR = ±4.096V (Note 6)		800		kΩ
		FSR = ±2.048V, FSR = ±1.024V		500		
		FSR = ±0.512V		330		
		FSR = ±0.256V		200		
		FSR = ±0.128V		135		
System Performance						
Resolution		No missing codes	12			Bits
Data Rate	DR		120		4630	SPS
Data Rate Variation		All data rates	-10		+10	%
Integral Nonlinearity	INL	DR=128SPS, FSR = ±2.048V (Note 7)			±0.5	LSB
Offset Error	V_{OS}	FSR = ±2.048V, differential inputs		±0	±0.5	LSB
		FSR = ±2.048V, single-ended inputs		±0.25		LSB
Offset Drift		FSR = ±2.048V		0.002		LSB/°C
Offset Channel Match		Match between any two inputs		0.25		LSB
Gain Error (Note 8)		FSR = ±2.048V, T_A = 25°C		0.05	0.25	%
Gain Drift (Note 8,Note 9)		FSR = ±0.128V		7		ppm/°C
		FSR = ±2.048V		5	40	
		FSR = ±4.096V (Note 6)		5		
Gain Match (Note 8)		Match between any two gains		0.05	0.5	%
Gain Channel Match		Match between any two inputs		0.05	0.2	
Temperature Sensor						
Temperature Range			-40		+125	°C
Temperature Resolution				0.125		°C/LSB
Accuracy		T_A = –40°C to +125°C		0.5	±3	°C
		versus supply		0.125	±0.5	°C /V
Digital Input / Output						
High-level Input Voltage	V_{IH}		0.7V_{VDD}		V_{VDD}	V
Low-level Input Voltage	V_{IL}		V_{GND}		0.5	
Low-level Output Voltage	V_{OL}	I_{OL} = 3mA	V_{GND}		0.4	
Input Leakage, High	I_H	V_{IH} = 5.5V	-10		10	µA
Input Leakage, Low	I_L	V_{IL} = GND	-10		10	
Power Supply						
Operating Supply Range			2.7		5.5	V
Quiescent Current	I_Q	Operating, T_A = 25°C		350	440	µA
		Operating, T_A =–40°C to +125°C			520	
		Power down mode, T_A = 25°C		5	10	
		Power down mode, T_A =–40°C to +125°C			45	

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is mounted on low effective single-layer PCB and tested under still air.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested that T_A = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3V or 5.5V (whichever is smaller) must be applied to this device.

Note 7: Best-fit INL; covers 99% of full-scale.

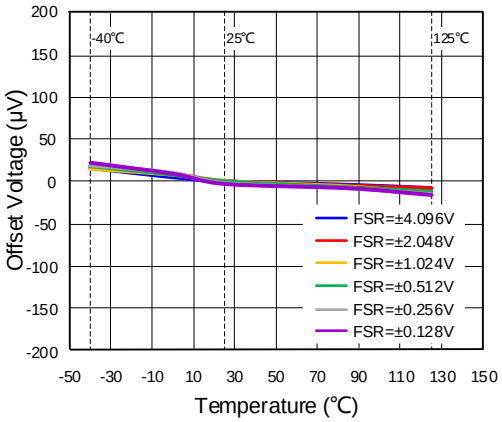
Note 8: Includes all errors from onboard PGA and voltage reference.

Note 9: Maximum value specified by characterization.

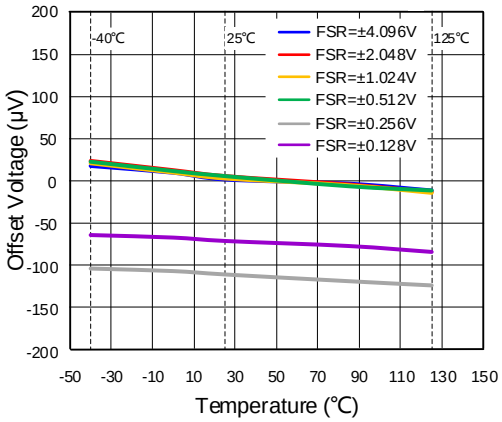
Typical Characteristics

At T_A = 25°C, V_{VDD} = 3.3V, data rate (DR) =120 SPS, and FSR = ±2.048 V (unless otherwise noted)

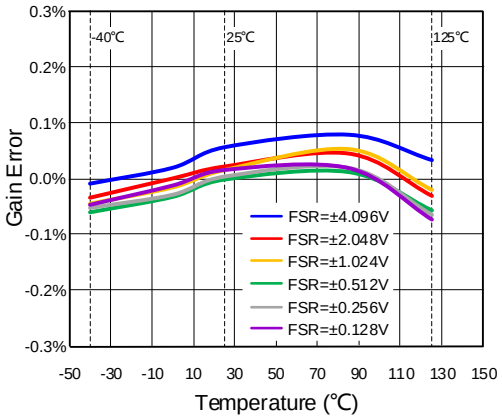
Differential Offset Voltage vs. Temperature



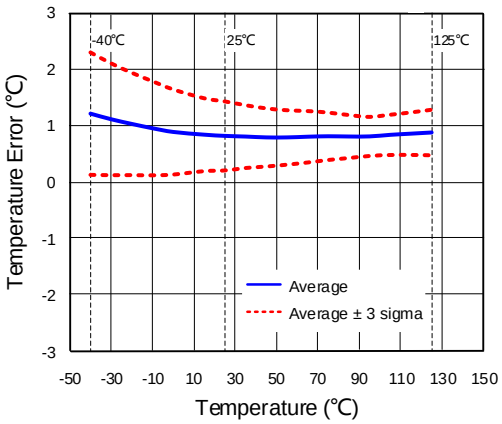
Single-Ended Offset Voltage vs. Temperature



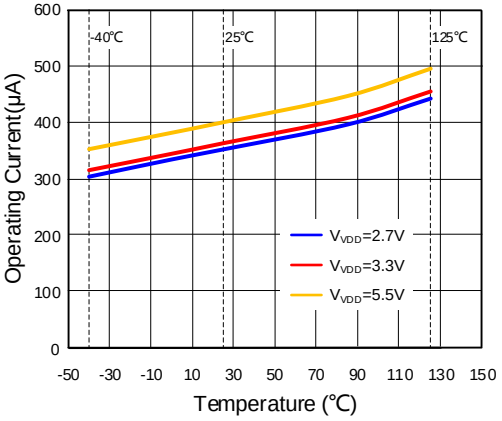
Gain Error vs. Temperature



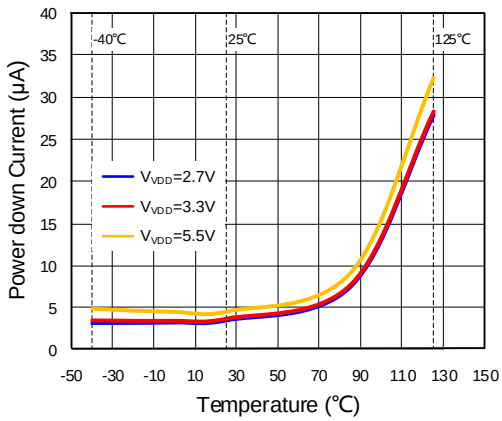
Temperature Sensor Error vs. Temperature



Operating Current vs. Temperature



Power down Current vs. Temperature



Detailed Description

Overview

The SA59400 is a precision, low power, delta-sigma (ΔΣ) analog-to-digital converter (ADC) that includes an internal reference voltage, a ΔΣ ADC core with a PGA, a clock oscillator, and an SPI. The PGA offers input ranges from ±128mV to ±4.096V. The device also integrates a highly linear and accurate temperature sensor. These features aim to enhance performance and minimize the need for external circuitry.

The SA59400 includes a differential, switched-capacitor ΔΣ modulator combined with a digital filter. The device ADC measures the VIN differential signal by calculating the difference between V (INP) and V (INN). This design significantly attenuates any common-mode signal. The internal voltage reference signal is first compared with the input signal. Then, the digital filter outputs a code proportional to the input voltage after receiving a high-speed bit stream from the modulator.

The SA59400 offers two conversion modes: continuous-conversion and single-shot. It can perform conversions at a data rate of up to 4630 samples per second (SPS), allowing the SA59400 to make high resolution measurements of both small and large signals. In continuous-conversion mode, the continuous conversion rate is the same as the programmed data rate, and the ADC automatically starts converting the input signal as soon as the last conversion is completed. The data reflects the most recently completed conversion and can be read anytime. In single-shot mode, the ADC converts the input signal on request and stores the value in the internal conversion register. Then, the device enters a power-down state. This mode significantly reduces power consumption in systems with long idle times between conversions or where only periodic conversions are required.

Functional Block Diagram

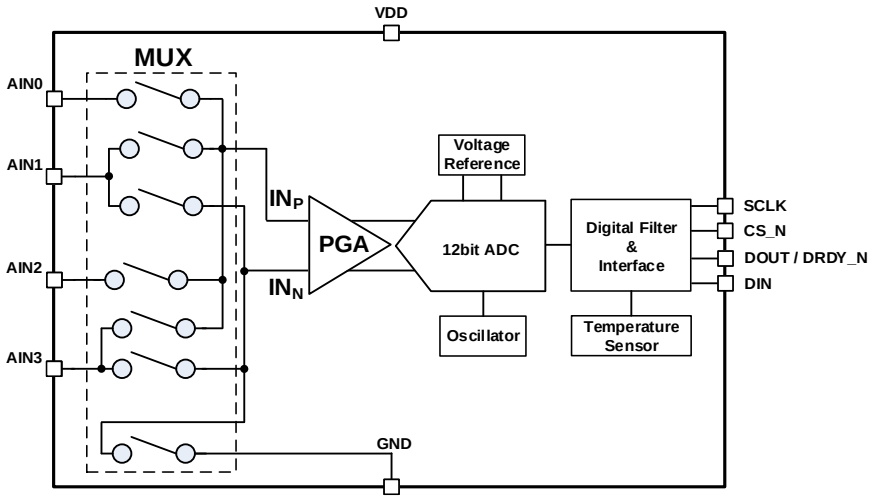


Figure 2. Block Diagram

Multiplexer

The SA59400 device includes an input multiplexer (MUX) that allows the measurement of either two differential or four single-ended signals. Additionally, AIN0, AIN1, and AIN2 can be measured differentially relative to AIN3. For single-ended signal measurements, the negative input of the ADC is internally connected to GND through a switch within the multiplexer. The multiplexer is configured using bits MUX[2:0] in the Config register.

When (V(INP) – V(INN)) < 0, the negative codes indicate negative differential signals. The device does not output negative codes when measuring single-ended inputs. Electrostatic discharge (ESD) diodes connected to VDD and GND protect the inputs of the SA59400 device. The absolute voltage at any input must be kept within the range of GND - 0.3V to VDD + 0.3V to prevent the ESD diodes from activating. If input pin voltages might exceed these conditions, it is advisable to use external Schottky diodes and series resistors to limit the input current to safe values, as specified in the Absolute Maximum Ratings.

Additionally, an external Schottky diode clamp is recommended if there is a potential to overdrive unused inputs. Overdriving unused inputs on the SA59400 device may influence the current conversion on other input pins.

Full-Scale Range (FSR) and LSB Size

The SA59400 is suitable for high accuracy and high-speed sensing applications, with a PGA implemented in front of the SA59400 ΔΣ ADC core. Configure the full-scale range by setting the bits PGA [2:0] in the Config register. It can be set to ±4.096V, ±2.048V, ±1.024V, ±0.512V, ±0.256V or ±0.128V.

Table 1 displays the Full-Scale Range (FSR) along with the corresponding Least Significant Bit (LSB) size, derived from the full-scale voltage using the formula provided below:

$$LSB = FSR / 2^{12}$$

Ensure that the analog input voltage does not exceed the limits specified in the Electrical Characteristics section. If the VDD exceeds 3.3V, the ±4.096V full-scale range permits input voltages up to the power supply level. The full-scale ADC output code cannot be obtained when the supply voltage is less than the full-scale range (for example, VDD = 3.3V and full-scale range = ±4.096V). This limitation results in a loss of some dynamic range.

Table 1. SA59400 Full-Scale Range and Corresponding LSB Size

FSR	LSB Size
±4.096V (Note)	2mV
±2.048V	1mV
±1.024V	0.5mV
±0.512V	0.25mV
±0.256V	0.125mV
±0.128V	0.0625mV

Note: This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to this device.

Temperature Sensor

Set bit TS_MODE = 1 in the Config register to operate the device in temperature sensor mode. The first 12 bits of the 16-bit conversion result indicate temperature in this mode. Byte 1, the most significant byte (MSB), is followed by Byte 2, the LSB. The data is output starting with the MSB. One LSB equals 0.125°C. Negative numbers are represented in binary two's-complement format, as shown in Table 2.

Table 2. 12-Bit Temperature Data Format

Temperature (°C)	Digital Output (Binary)	Hex
128	0 100 0000 0000	400
127.875	0 011 1111 1111	3FF
100	0 011 0010 0000	320
80	0 010 1000 0000	280
40	0 001 0100 0000	140
30	0 000 1111 0000	0F0
25	0 000 1100 1000	0C8
0.25	0 000 0000 0010	002
0	0 000 0000 0000	000
–0.25	1 111 1111 1110	FFE
–25	1 111 0011 1000	F38
–40	1 110 1100 0000	EC0

Converting Positive Temperatures

To convert positive temperatures to a digital data format:

1. Divide the temperature by the resolution.
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: 40°C / (0.125°C/LSB) = 320 = 140h = 0001 0100 0000

To convert a positive digital data format to temperatures:

1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0001 0100 0000 = 140h = 320 × (0.125°C / LSB) = 40°C

Converting Negative Temperatures

To convert negative temperatures to a digital data format:

1. Divide the absolute value of the temperature by the resolution and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the two's complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: |–25°C| / (0.125/count) = 200 = 0C8h = 0000 1100 1000
Twos complement format: 1111 0011 0111 + 1 = 1111 0011 1000

To convert a negative digital data format to temperature:

1. Generate the two's complement of the 12-bit, left-justified binary number of the temperature result (with MSB= 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

Example: 1111 0011 1000 has a two's complement of 0000 1100 1000 = 0000 1100 0111 + 1
Convert to temperature: 0000 1100 1000 = 0C8h = 200; 200 × (-0.125°C / LSB) = –25°C

Device Operating Modes

Reset and Power-Up

By default, the SA59400 enters power-down state at start-up. The device interface and digital blocks are active but do not perform data conversion. The initial power-down state of the SA59400 prevents systems with tight power-supply requirements from encountering a surge during power-up.

When the SA59400 powers up, the device is reset, and all bits in the Config register are set to their respective default settings.

Operating Modes

The SA59400 offers both continuous-conversion mode and single-shot mode. Use the MODE bit in the Config register to switch between these modes.

Continuous-Conversion Mode

When the MODE bit in the Config register is set to 0, the SA59400 will operate in continuous-conversion mode where a new conversion starts as soon as the previous one is completed. The conversion rate is configured using the DR field in the Cofig Register. Once the conversion is complete, the SA59400 will put the result in the Conversion register, and the ADC will automatically start a new conversion. The data reflects the most recently completed conversion and can be read anytime. Writing a 1 to the MODE bit in the Config register or resetting the device switches it to single-shot mode.

Single-Shot Mode and Power-Down

In single-shot mode (MODE bit set to 1), the ADC converts the input signal on request and stores the value in the internal conversion register. Then, the device enters a power-down state. This power-down state will be the default state for the SA59400 when it is first powered on. The device can still respond to commands even if it is powered down. The SA59400 will remain in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is set, the device will power up, reset the SS bit to 0, and start a single conversion. The device will power down again when conversion data is ready. Writing a 0 to the MODE bit in the Config register switches operation to continuous-conversion mode.

Duty Cycling for Low Power

Reducing the output data rate generally enhances the noise performance of the ΔΣ ADC in the SA59400 device, as more samples from the internal modulator are averaged to produce a conversion result. However, in applications where power consumption is critical, improving noise performance at low data rates may not be necessary. For such applications, the SA59400 supports duty cycling, which can achieve significant power savings by periodically requesting high data-rate readings while effectively operating at a lower data rate.

For example, in a power-down state, the SA59400, with a data rate set to 4630 SPS, can be operated by a microcontroller that triggers a single-shot conversion every 8.3ms (120 SPS). The conversion of 4630 SPS takes approximately 0.216ms, allowing the SA59400 to enter a power-down state for the remaining 8.1ms. The duty cycling rate is arbitrary and defined by the controller.

Programming

Serial Interface

The compatible serial interface for SPI can be configured with either four interface signals (CS_N, SCLK, DIN, and DOUT/DRDY_N) or three signals (SCLK, DIN, and DOUT/ DRDY_N, with CS_N tied low). The interface enables reading conversion data, read from and write to registers, and controlling the device operation.

Chip Select (CS_N)

The SA59400 facilitates SPI communication via the CS_N pin, which is beneficial when multiple devices are sharing a single serial bus. During serial communication, the CS_N pin remains low. Taking CS_N high resets the serial interface, disregards SCLK, and sets the DOUT/DRDY_N to a high-impedance state. In this state, DOUT/ DRDY_N cannot provide an indication of data readiness. In cases with multiple devices where monitoring of DOUT/DRDY_N is necessary, it is advisable to periodically lower CS_N. Consequently, the DOUT/DRDY_N pin either becomes low, signaling new data in the Conversion register ready for transfer, or remains high, indicating the absence of new data. Data can be transferred at any time without the risk of corruption. Upon initiating a transfer, the current data result locks into the output shift register and remains unchanged until the communication cycle completes, preventing data corruption.

Serial Clock (SCLK)

The serial clock pin (SCLK) is used to clock data on the DIN and DOUT/ DRDY_N pins into and out of the SA59400, which has a Schmitt-triggered input. Keep SCLK as clean as possible to prevent glitches from accidentally shifting the data even if the input has hysteresis. Keep SCLK low for 28ms to reset the serial interface, and the next SCLK pulse begins a new communication cycle. When the serial interface transmission is interrupted, using this timeout feature can recover communication. The SCLK signal should be kept low when the serial interface is idle.

Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the SA59400. On the SCLK falling edge, the device latches data present on DIN. The SA59400 does not drive the DIN pin.

Data Output and Data Ready (DOUT/DRDY_N)

The data output and data ready pin (DOUT/ DRDY_N) is used for reading conversion and register data, and needs to be used together with SCLK. DOUT/DRDY_N triggers a microcontroller to start reading data from the SA59400 and also indicates the completion of a conversion when new data is ready. When new data is ready, this pin transitions to a low level. Data from DOUT/DRDY_N is shifted out on the rising edge of SCLK. In continuous-conversion mode, if no data is retrieved, DOUT/DRDY_N will return to high 8μs before the next data-ready signal (DOUT/DRDY_N low). It is crucial to complete the data transfer before DOUT/DRDY_N reverts to high, as depicted in Figure 3.

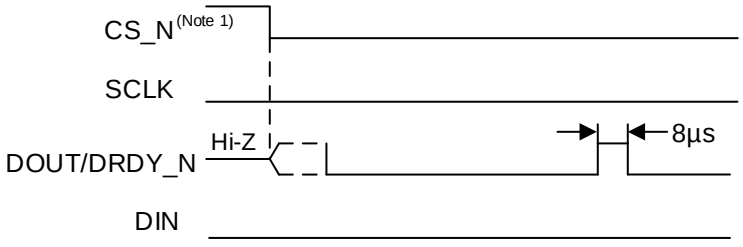


Figure 3. DOUT/DRDY_N Behavior without Data Retrieval in Continuous-Conversion Mode

Note: CS_N can remain low on the SA59400 if it is the sole device on the serial bus. When CS_N is low, DOUT/DRDY_N asserts low, indicating that new data is available.

By default, DOUT/DRDY_N is configured with a weak internal pull-up resistor when CS_N is high. This configuration helps minimize the risk of DOUT/DRDY_N floating near mid-supply and causing leakage current in the master device. The pull-

up resistor can be disabled by setting the PULL_UP_EN bit to 0 in the Config register, which places the device into a high-impedance state.

Data Format

The SA59400 delivers 12-bit data in binary two's complement format, which is left-justified within the 16-bit data word. A negative full-scale (–FS) input produces an output code of 8000h, and a positive full-scale (+FS) input produces an output code of 7FF0h. For signals that exceed full-scale, the output clips at these codes. Table summarizes the output codes for different input signals respectively.

Table 3. Input Signal vs Output Code

Input Signal, VIN (INP – INN)	Ideal Output Code
≥ +FS (2^{11} – 1) / 2^{11}	7FF0h
+FS / 2^{11}	0010h
0	0
–FS / 2^{11}	FFF0h
≤ –FS	8000h

Data Retrieval

For single-shot and continuous conversion modes, data is written to and read from the SA59400 similarly, without issuing any commands. The operating mode is selected via the MODE bit in the Config register.

When the SA59400 operates in single-shot mode (MODE bit set to 1), a new conversion will only start by writing a 1 to the SS bit.

When the SA59400 operates in continuous-conversion mode (MODE bit set to 0), even if CS_N is high, the device will be constantly starting new conversions.

Device data can be read at any time without risk of data corruption since the conversion data are buffered, with the current data retained until replaced by new conversion data. New conversion data readiness is signaled when DOUT/DRDY_N is asserted low, and the data is read by shifting out on DOUT/DRDY_N. The most significant bit (MSB) of the data (bit 15) is clocked out on the first rising edge of SCLK. Concurrently, as the conversion result is clocked out of DOUT/DRDY_N, new Config register data are latched on DIN at the falling edge of SCLK.

The SA59400 supports two types of complete data transmission cycles: 16 bits and 32 bits. The 16-bit cycle is applicable when the CS_N line can be controlled and is not permanently tied low. The 32-bit cycle facilitates the direct readback of Config register settings within the same data transmission cycle.

16-Bit Data Transmission Cycle

As shown in Figure 4, if there is no need to read back the Config register data, the SA59400 conversion data can be clocked out within a short 16-bit data transmission cycle. After the 16th SCLK cycle, take CS_N high to reset the SPI interface. Subsequently, lowering CS_N again initiates a new data transmission at the first rising edge of SCLK with the currently buffered conversion result. It is important to note that if DOUT/DRDY_N is high at the start of the data retrieval, the read will replicate the data from the previous transmission cycle. Conversely, if DOUT/DRDY_N is low at the beginning of data retrieval, this indicates that the conversion buffer has been updated with a new result.

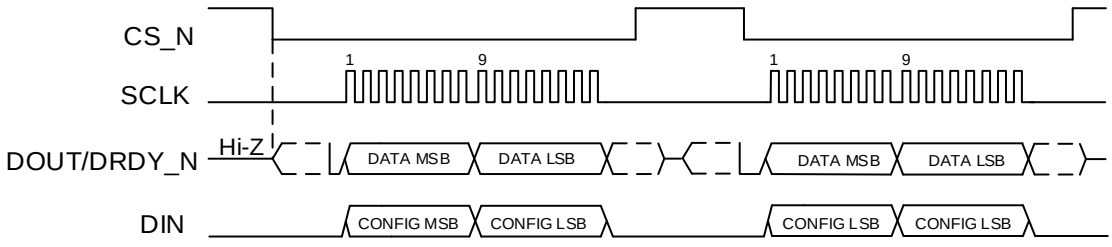


Figure 4. 16-Bit Data Transmission Cycle

32-Bit Data Transmission Cycle

The 32 bits allow direct readback of Config register settings in the same data transmission cycle. Figure shows the data in a 32-bit data transmission cycle has four bytes: two bytes for the conversion result and the other two bytes for the Config register readback. The device consistently reads the MSB first.

As shown in Figure , the same Config register setting is written twice during one transmission cycle. The Config register setting is read back in the last two bytes of the same cycle. As shown in Figure 6, the Config register is written once during the first half of the transmission cycle, maintaining the DIN pin either low or high in the second half. The data written in the initial two bytes of the 32-bit cycle is read back in the final two bytes of the same cycle.

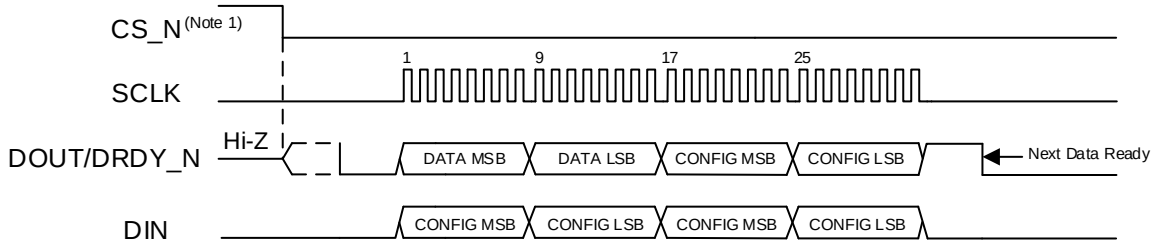


Figure 5. 32-Bit Data Transmission Cycle with Config Register Readback

Note: CS_N can remain low on the SA59400 if it is the sole device on the serial bus. When CS_N is low, DOUT/DRDY_N asserts low, indicating that new data is available.

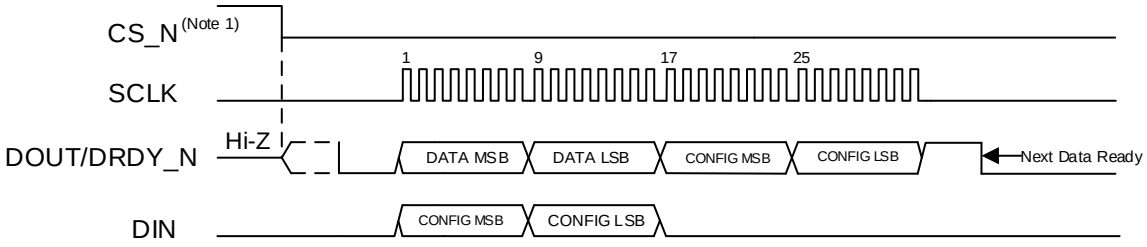


Figure 6. 32-Bit Data Transmission Cycle: DIN Held Low

Note: CS_N can remain low on the SA59400 if it is the sole device on the serial bus. When CS_N is low, DOUT/DRDY_N asserts low, indicating that new data is available.

Register Map

The SA59400 features two registers accessible via SPI: the Conversion register, which holds the result of the last conversion, and the Config register, which enables users to configure the operation of the SA59400 and check its status.

Conversion Register [reset = 0000h]

The 16-bit Conversion register of the SA59400 stores the result of the last conversion in binary two's complement format. Upon power-up, this register is cleared to 0 and stays at 0 until the first conversion is complete.

Figure 7. Conversion Register

15	14	13	12	11	10	9	8
D11	D10	D9	D8	D7	D6	D5	D4
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D3	D2	D1	D0	Reserved			
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	Reserved	R	0h	Always reads back 0h

Config Register [reset = 038Bh]

The 16-bit Config register of the SA59400 controls the operating mode, input selection, data rate, full-scale range, and temperature sensor mode.

Figure 8. Config Register

15	14	13	12	11	10	9	8
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-4h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			TS_MODE	PULL_UP_EN	NOP[1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SS	R/W	0h	**Single-shot conversion start** This bit initiates a single conversion. The SS bit can only be written while in the power-down state and has no effect during an ongoing conversion. When writing: 0 = No effect 1 = Starts a single conversion (only when in power-down state) Always reads back 0 (default).
14:12	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = INP is AIN0 and INN is AIN1 (default) 001 = INP is AIN0 and INN is AIN3 010 = INP is AIN1 and INN is AIN3 011 = INP is AIN2 and INN is AIN3 100 = INP is AIN0 and INN is GND

				101 = INP is AIN1 and INN is GND 110 = INP is AIN2 and INN is GND 111 = INP is AIN3 and INN is GND
11:9	PGA[2:0]	R/W	4h	SA59400 Programmable gain amplifier configuration These bits configure the programmable gain amplifier. 000 = FSR is ±4.096V (Note 1) 001 = FSR is ±2.048V (default) 010 = FSR is ±1.024V 011 = FSR is ±0.512V 100 = FSR is ±0.256V 101 = FSR is ±0.128V 110 = FSR is ±0.128V 111 = FSR is ±0.128V
8	MODE	R/W	1h	**Device operating mode** This bit controls the SA59400 operating mode. 0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data rate** These bits control the data rate setting. 000 = 120 SPS 001 = 241 SPS 010 = 475 SPS 011 = 919 SPS 100 = 1712 SPS (default) 101 = 2976 SPS 110 = 4630 SPS 111 = Not Used
4	TS_MODE	R/W	0h	**Temperature sensor mode** This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	**Pull-up enable** This bit enables a weak internal pull-up resistor on the DOUT/DRDY_N pin, but only when CS_N is high. An internal 400-kΩ resistor connects the bus line to the supply when enabled. If disabled, the DOUT/DRDY_N pin floats. 0 = Pull-up resistor disabled on DOUT/ DRDY_N pin 1 = Pull-up resistor enabled on DOUT/DRDY_N pin (default)
2:1	NOP[1:0]	R/W	1h	**No operation** The NOP[1:0] bits control whether data is written to the Config register. To write data to the Config register, the NOP[1:0] bits must be set to 01. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data. Do not update the contents of the Config register 01 = Valid data. Update the Config register (default) 10 = Invalid data. Do not update the contents of the Config register 11 = Invalid data. Do not update the contents of the Config register
0	Reserved	R	1h	**Reserved** Writing either 0 or 1 to this bit has no effect. Always reads back 1.

Note: This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3V to this device.

Application Schematic

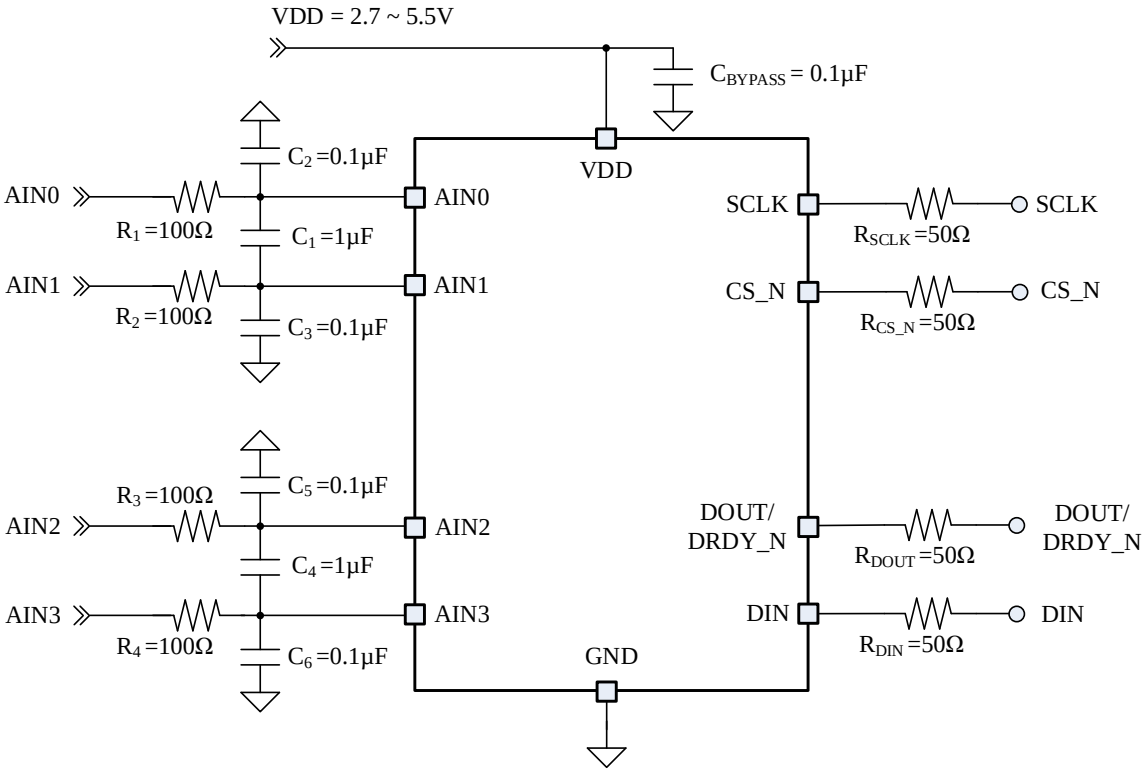


Figure 9. Schematic Diagram

BOM List

Designator	Description	Part Number	MFR
C_{BYPASS}	0.1µF/50V/X7R, 0603	GCJ188R71H104KA12D	muRata
R_1, R_2, R_3,R_4	100Ω, 1%, 0603		
R_{SCLK}, R_{CS_N}, R_{DOUT},R_{DIN}	50Ω, 1%, 0603		
C_1,C_4	1µF/50V/0603		
C_2, C_3, C_5, C_6	0.1µF/50V/0603		

PCB Layout Guide

For optimal design, follow these PCB layout guidelines:

1. Place a high-quality capacitor across the analog inputs with differential connections to enhance signal integrity.
2. Position a bypass capacitor (a 0.1μF MLCC is recommended) as close as possible to the VDD and GND pins.
3. Place series termination resistors R_{SCLK}, R_{DIN}, R_{DOUT}, R_{CS_N}, close to the output drivers (R_{DOUT} should be placed close to the ADC and the rest placed close to the microcontroller)

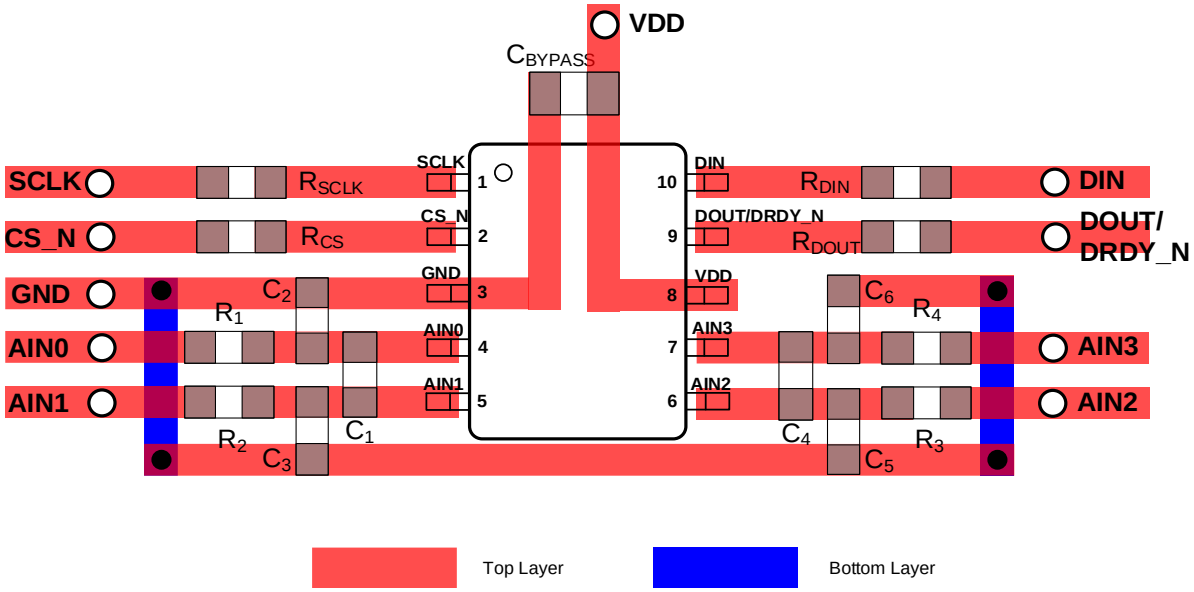
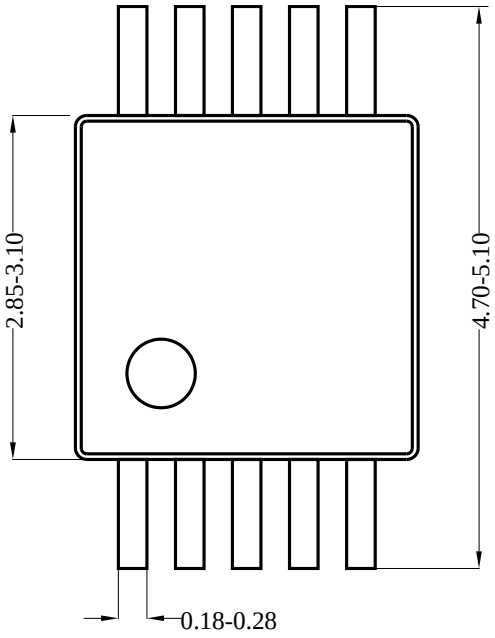
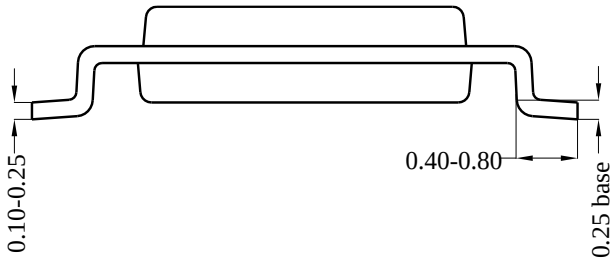


Figure 10. Layout Recommendation

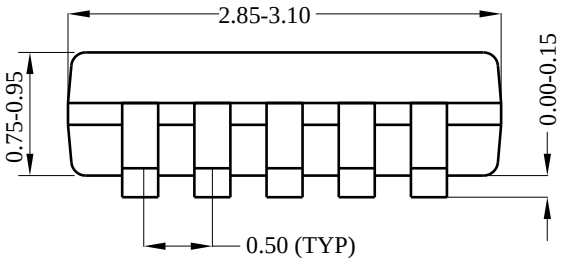
MSOP10 Package Outline & PCB Layout



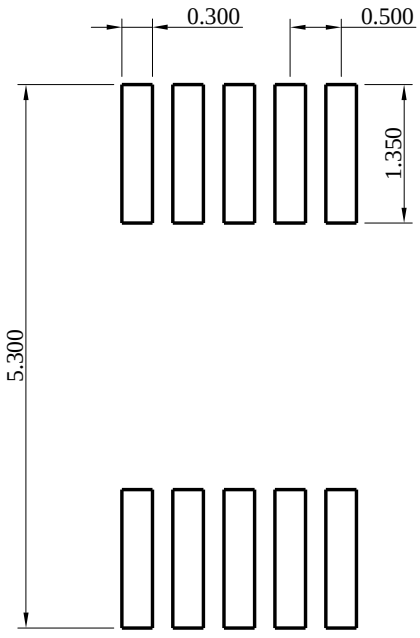
Top View



Side View



Front View

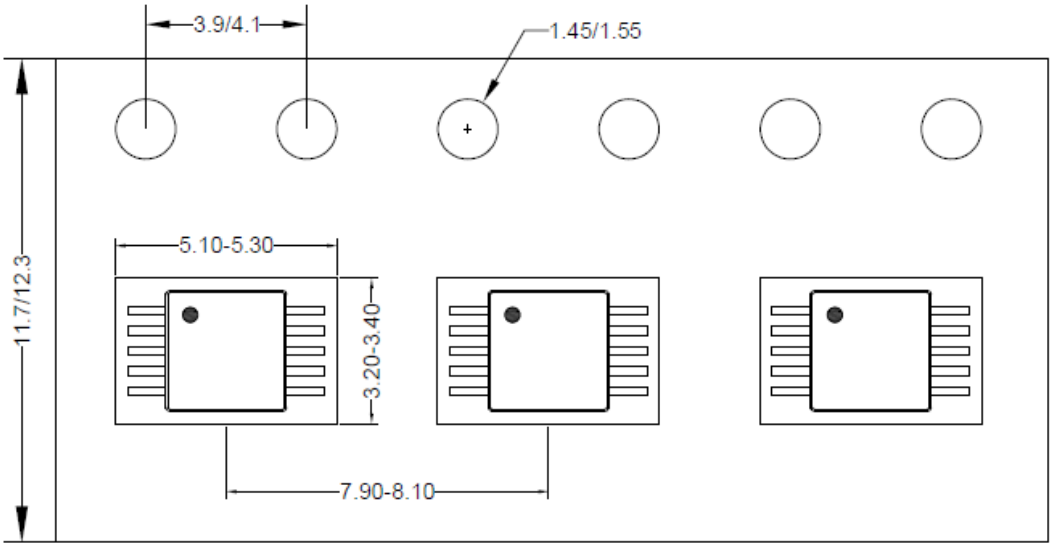


Recommended Pad Layout

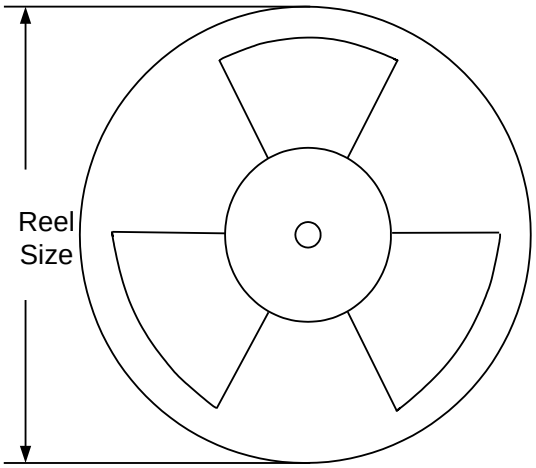
Note: All dimensions are in millimeters and exclude mold flash & metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Sept. 3, 2024	Revision 1.0	Initial Release

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