SQ76004B

High Efficiency, 4 A , 2.5V-6V Input Synchronous Step Down DC/DC converter

General Description

The SQ76004B is a step-down module converter with built-in power MOSFETs and inductor. The SQ76004B achieves 4A of continuous output current from a 2.5V to 6V input voltage with excellent load and line regulation. It provides accurate regulation for a variety of loads over T_J= -40°C to 125°C. The output voltage can be regulated as low as 0.6V. Only the input capacitors, the output capacitor and the FB resistor divider are needed to complete the design.

Features

- 2.5V to 6V Input Voltage Range
- 4A Continuous Output Current
- Accurate ±1% V_{REF} Voltage
- 2.4MHz Pseudo-constant switching frequency
- Internal Soft-Start Limits Inrush Current
- Power-Good Indicator
- 100% duty cycle operation
- Reliable Protection Modes:
  - Auto-retry Mode for UVLO and OTP.
  - Hiccup Mode for OCP
- Compact Package: QFN2.5×2.5-10
  Height: 1.25mm max
  MSL-1 Compliant

Applications

- Smart Phones
- Telecom Applications
- Optical Modules
- General POL Applications

Typical Application

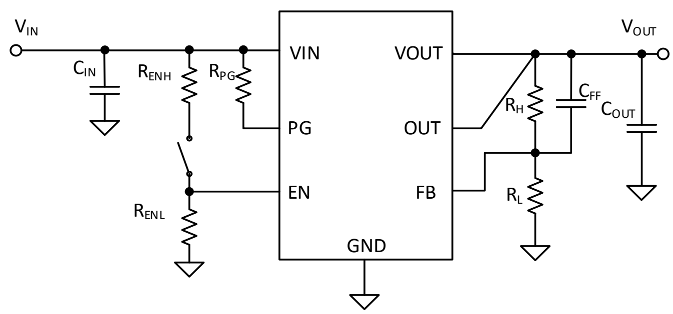


Figure 1. Application Circuit

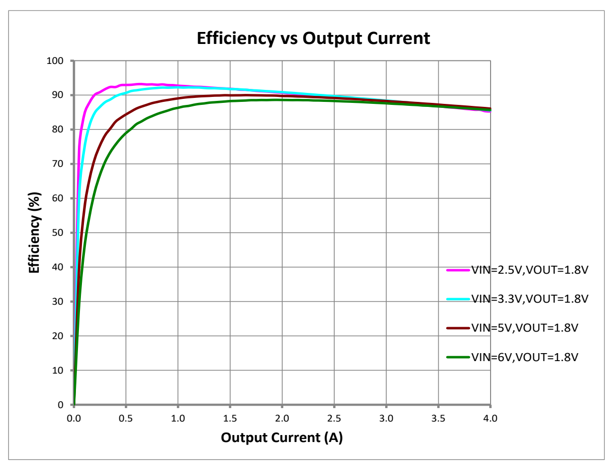
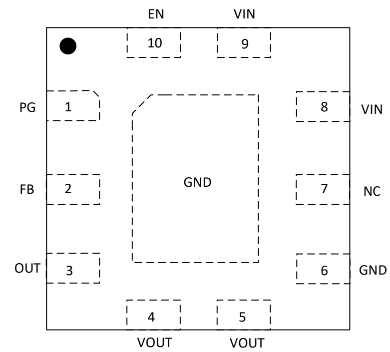


Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type
SQ76004BAKE	QFN2.5×2.5-10 RoHS-Compliant and Halogen-Free

Pinout (top view)



Pin No	Pin Name	Pin Description
1	PG	Power good open drain output pin. Connect to GND or leave floating if not used.
2	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
3	OUT	Output voltage feedback pin, connect to the output capacitor side.
4,5	VOUT	Output voltage pin. Decouple this pin to the GND pin with at least a 22μF×2 ceramic capacitor.
6	GND	Ground pin.
7	NC	Do not connect these pins to GND, to another pin, or to any other voltage. This pin must be soldered to an isolated pad.
8,9	VIN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
10	EN	Enable pin. Pull high to enable the device. Pull low to disable the device.

Block Diagram

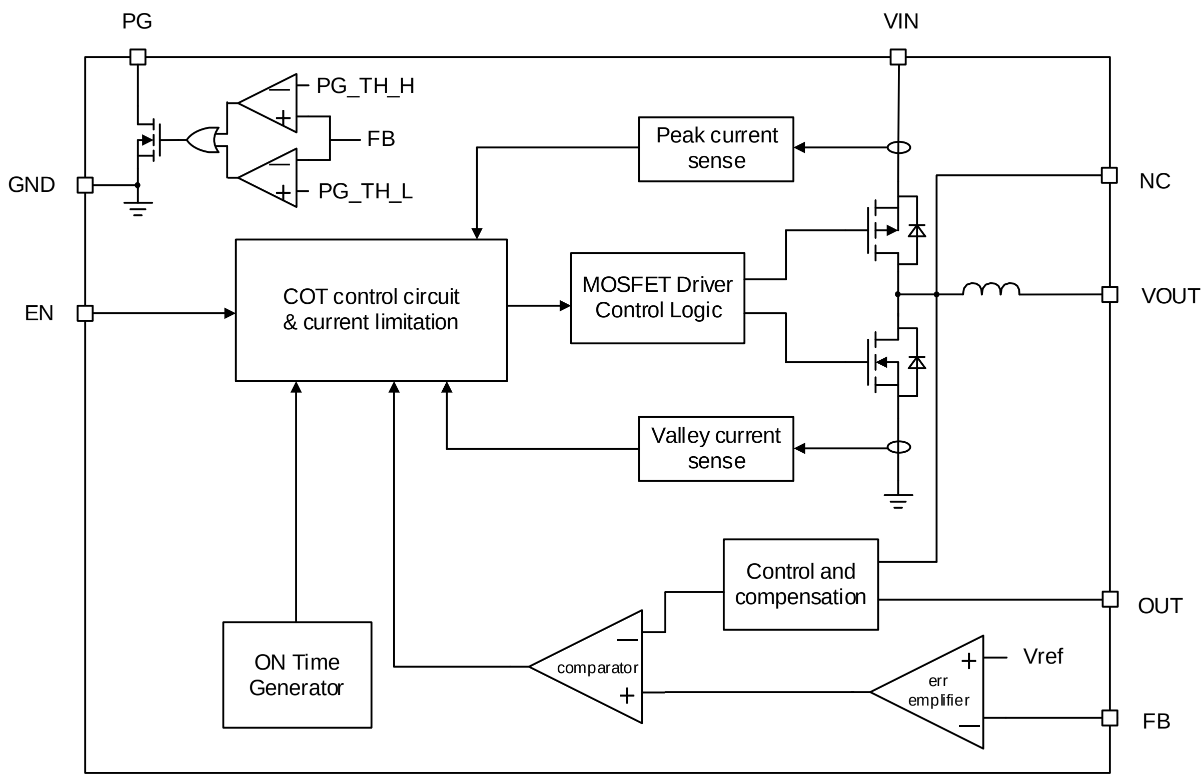


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	7	V
All Other Pins	-0.3	VIN + 0.3	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-55	125	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	27	°C/W
Ψ_{JB} Junction-to-Board Thermal Resistance	20	
P_D Power Dissipation T_A = 25°C	3.7	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.5	6	V
Output Voltage	0.6	V_{IN}	
Output Current	0	4	A

Electrical Characteristics

(V_{IN} = 3.3V, V_{OUT} =1.8V,C_{OUT} =2×22µF, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (Note 4). The values are guaranteed by test, design or statistical correlation, FB divider resistor accuracy = 0.5%, unless otherwise specified)

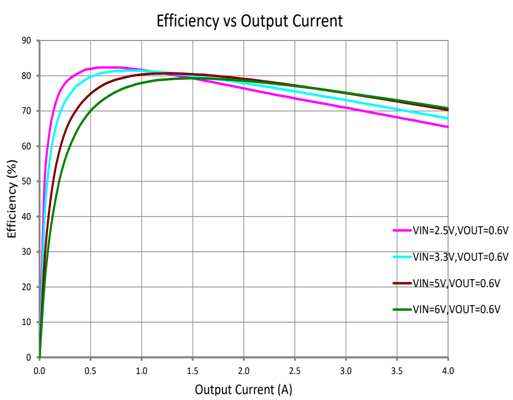
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Specifications	Input Voltage Range	V_{IN}		2.5		6	V
	Input UVLO Threshold (falling)	$V_{UVLO,FALLING}$	EN=V_{IN}	2	2.2	2.3	V
	UVLO, Hysteresis	V_{HYS}	V_{IN} falling		250		mV
	Input Current with No Load	I_{IN}	I_O=0A	10	16	30	mA
	Shutdown Current	I_{SHDN}			0.1	15	µA
Output Specifications	Feedback Reference Voltage	V_{VREF}		0.594	0.6	0.606	V
	Load Regulation(Note5)	ΔV_{LDR}	Io=0-3A			±1	%
	Line Regulation(Note5)	ΔV_{LNR}	V_{IN}=2.5-6V			±0.5	%
	Temperature Regulation(Note5)	ΔT_{TMR}	T_A=-40°C to 105°C			±2	%
	Bottom FET Valley Current Limit	$I_{LIM,BOT}$			5		A
	Rise Time	t_{RISE}	From EN high to 95% of V_{OUT} nominal	0	0.3	1	ms
General Specifications	Switching Frequency	f_{SW}		1.92	2.4	2.88	MHz
	Thermal Shutdown Temperature	T_{SD}			150		°C
	Thermal Shutdown Hysteresis	T_{HYS}			20		°C
	Maximum Duty Cycle (Note 5)	D_{MAX}		100			°C
	Min On Time(Note 5)	$t_{ON,MIN}$			50		ns
Signal Specifications	EN Pin Logic High Threshold (rising)	$V_{EN,H}$		1.0			V
	EN Pin Logic Low Threshold (falling)	$V_{EN,L}$				0.4	V
	EN Pull-down Resistance	R_{EN}	VIN=3.3V, EN=0.5V	300	400	500	kΩ
	Power Good Asserts Threshold	$V_{PG,ASSERTS}$	V_{OUT} rising	92	95	98	%
			V_{OUT} falling	85	88	91	%

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: θ_{JA} and Ψ_{JB} are based on a four-layer Silergy Evaluation Board (1.6mm thickness, 2OZ copper, 95% copper coverage) in the natural convection at T_A = 25°C. Junction temperature (T_J) refers to the hottest device, which is inductor temperature and case temperature (T_C) as well for this product. Board temperature (T_B) refers to the PCB point to the hottest IC pin with a 1mm distance on the same PCB surface layer.
Note 3: The device is not guaranteed to function outside its operating conditions.
Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.
Note 5: The values are guaranteed by design, not production testing.

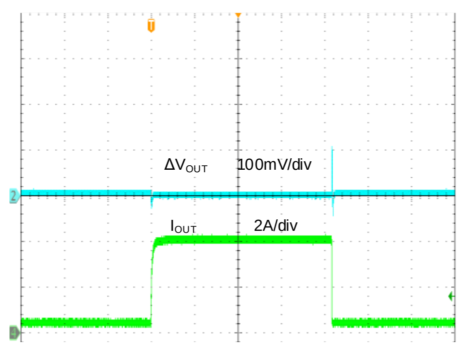
Typical Performance Characteristics

(C_{OUT} = 2×22µF, T_A = 25°C, resistor tolerance is ±1%, unless otherwise specified.)

V_{OUT}=0.6V

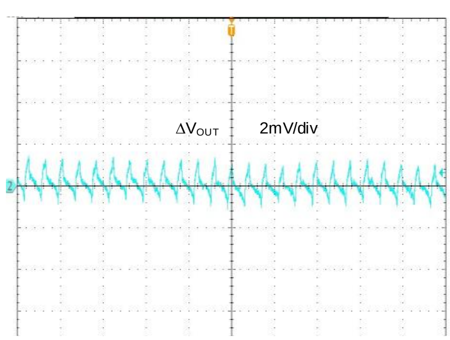


Load Transient
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=0.4~4A)



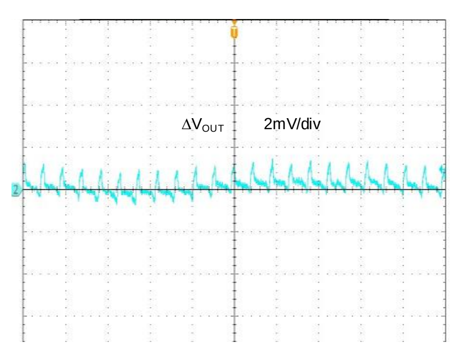
Time (200µs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=4A)



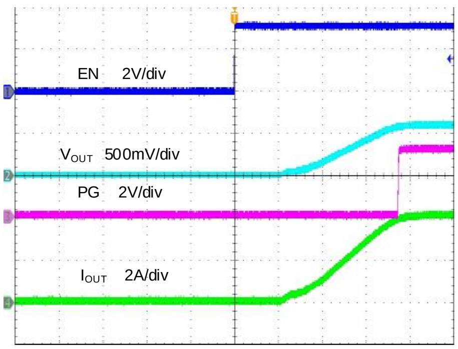
Time (1µs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=0A)



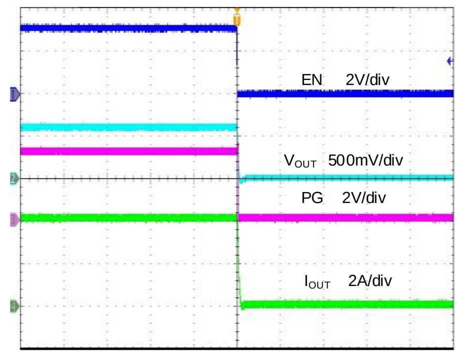
Time (1µs/div)

Startup from EN
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=4A)



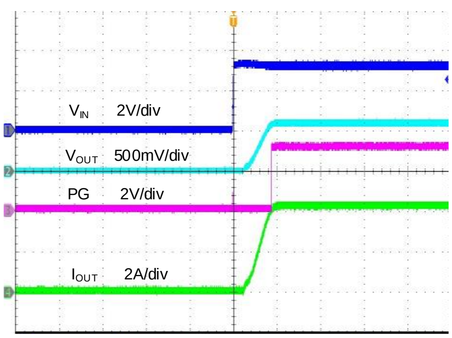
Time (200μs/div)

Shutdown from EN
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=4A)



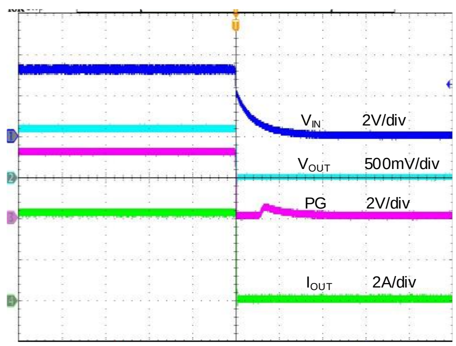
Time (200μs/div)

Startup from V_{IN}
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=4A)



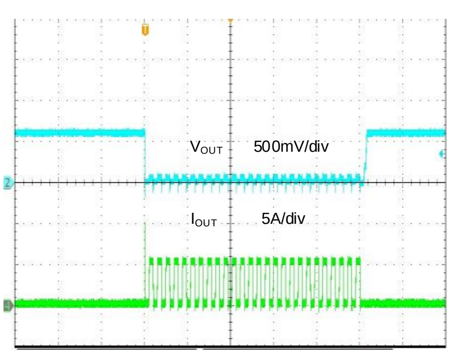
Time (800μs/div)

Shutdown from V_{IN}
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=4A)



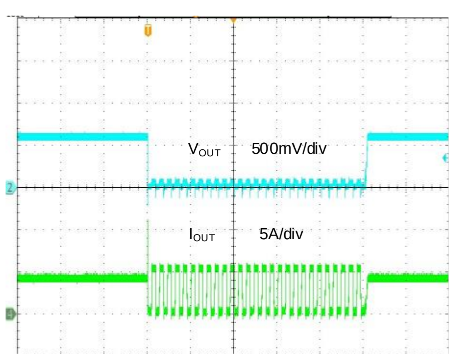
Time (800μs/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=0A-Short)



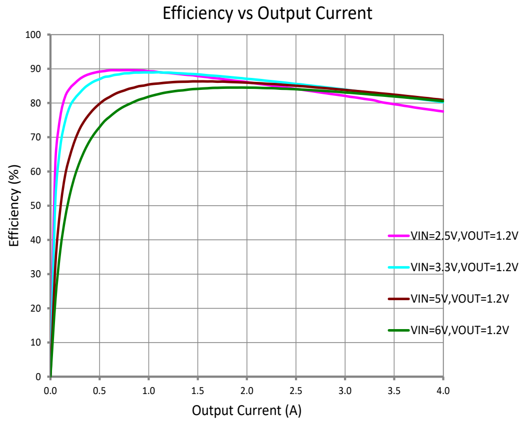
Time (10ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.6V, I_{OUT}=4A-Short)

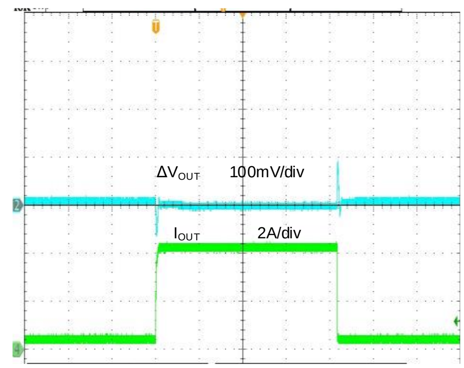


Time (10ms/div)

V_{OUT}=1.2V

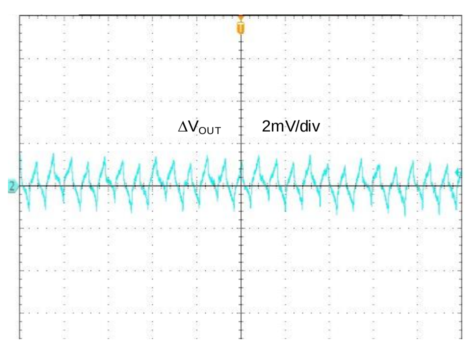


Load Transient
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.4~4A)



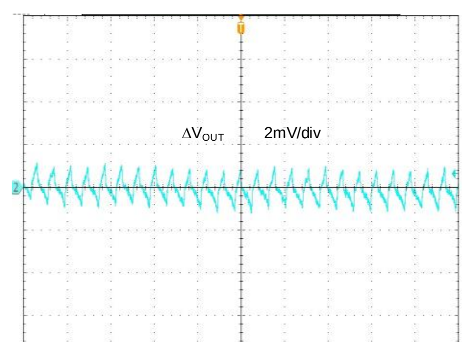
Time (200μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=4A)



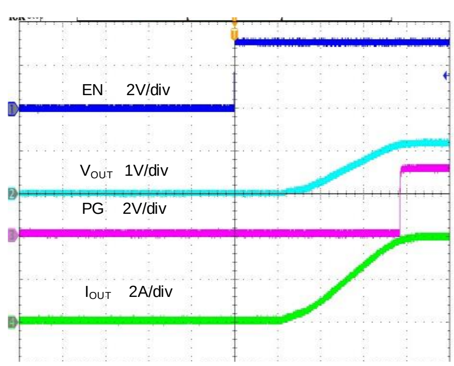
Time (1μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A)



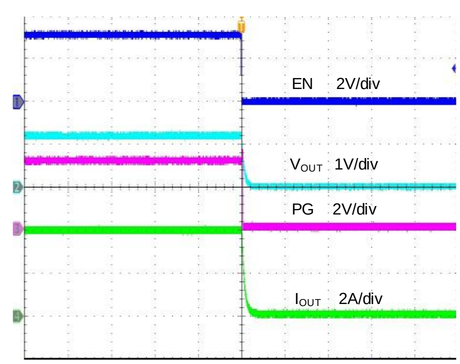
Time (1μs/div)

Startup from EN
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=4A)



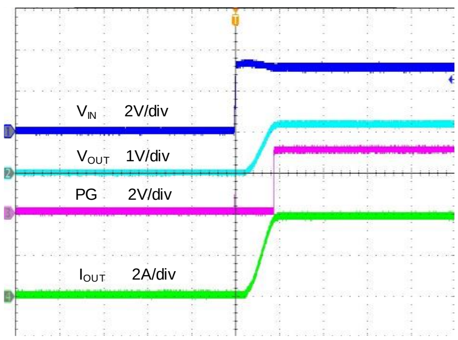
Time (200μs/div)

Shutdown from EN
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=4A)



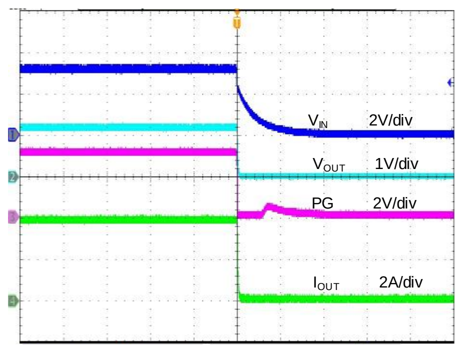
Time (200μs/div)

Startup from V_{IN}
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=4A)



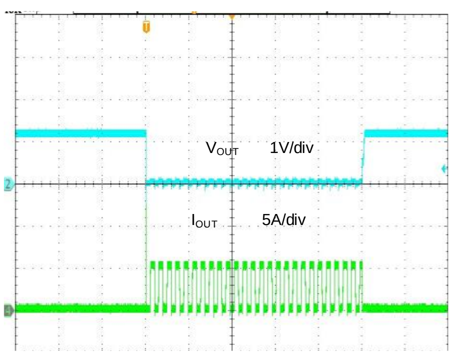
Time (800μs/div)

Shutdown from V_{IN}
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=4A)



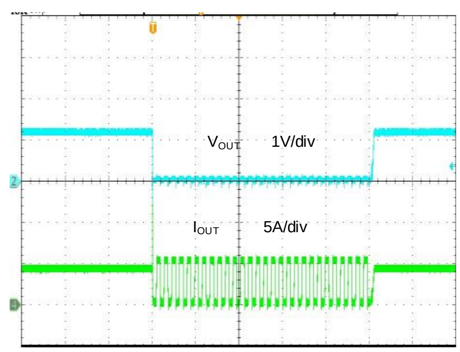
Time (800μs/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A-Short)



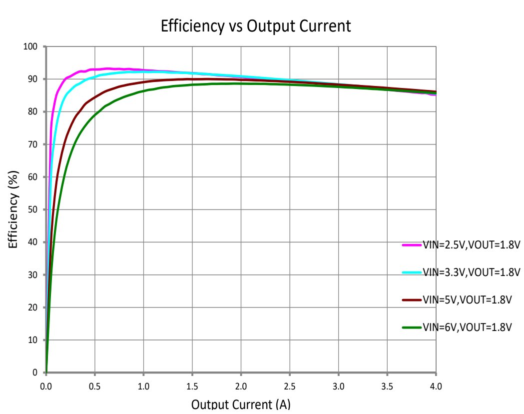
Time (10ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=4A-Short)

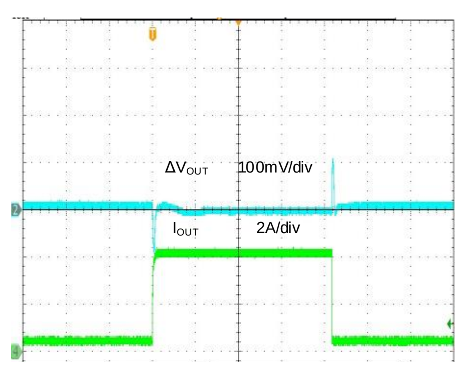


Time (10ms/div)

V_{OUT}=1.8V

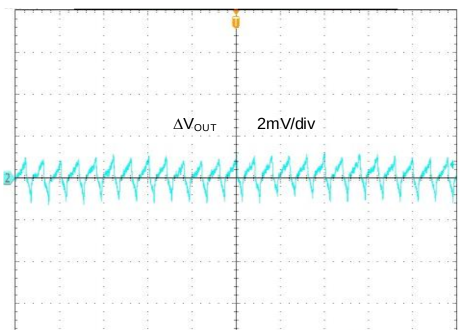


Load Transient
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=0.4~4A)



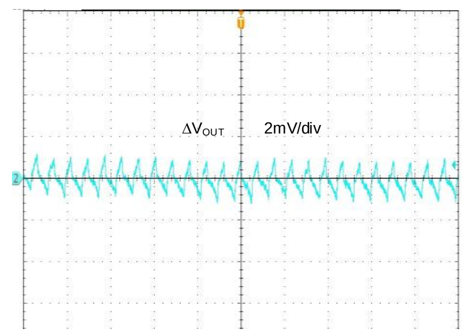
Time (200μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=4A)



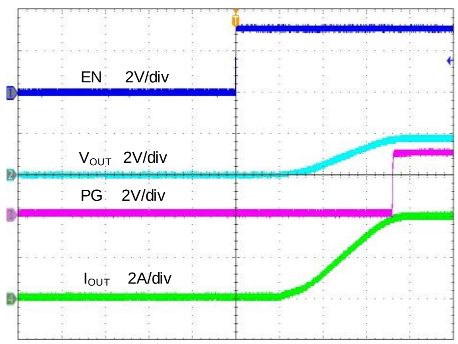
Time (1μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=0A)



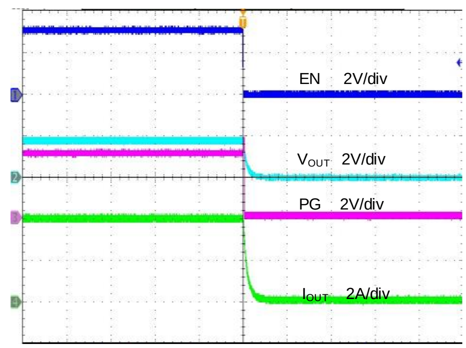
Time (1μs/div)

Startup from EN
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=4A)



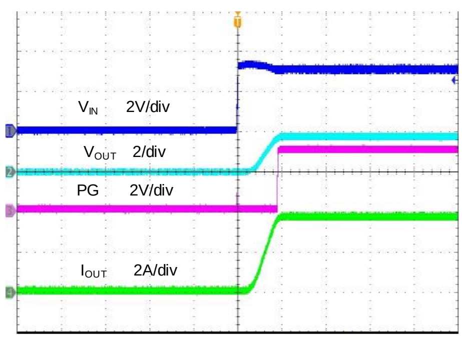
Time (200μs/div)

Shutdown from EN
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=4A)



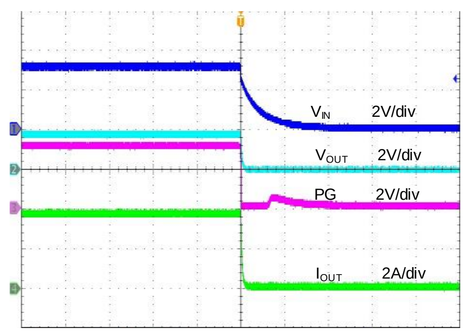
Time (200μs/div)

Startup from V_{IN}
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (800μs/div)

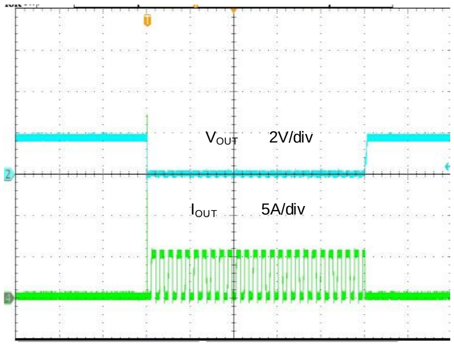
Shutdown from V_{IN}
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=4A)



Time (800μs/div)

Short Circuit Protection

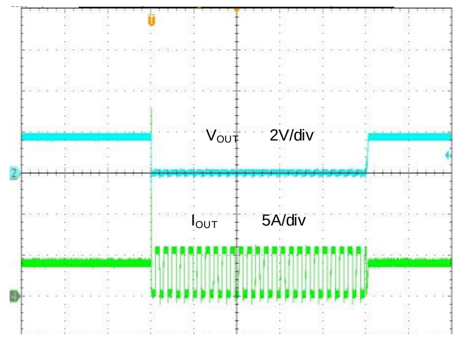
(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=0A-Short)



Time (10ms/div)

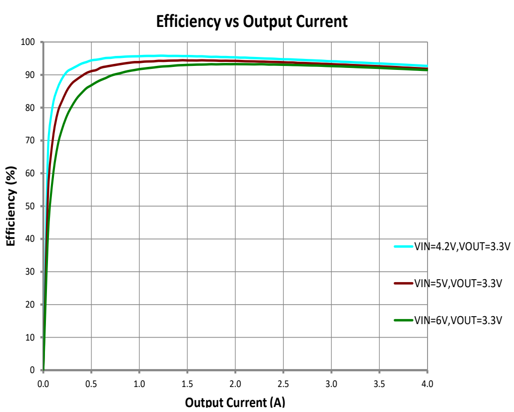
Short Circuit Protection

(V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=4A-Short)



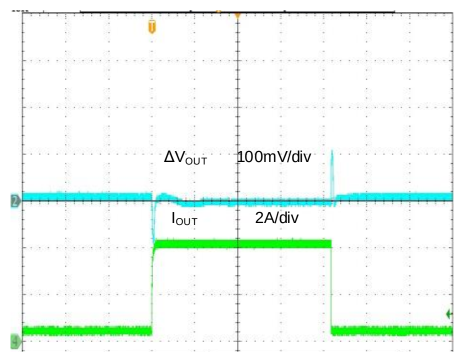
Time (10ms/div)

V_{OUT}=3.3V



Load Transient

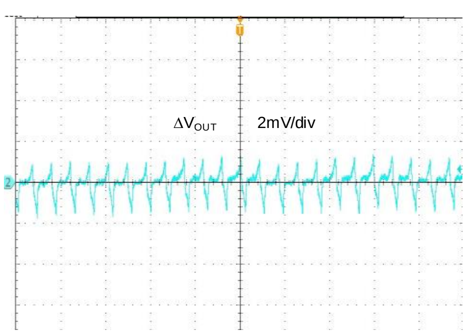
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.4~4A)



Time (200μs/div)

Output Ripple

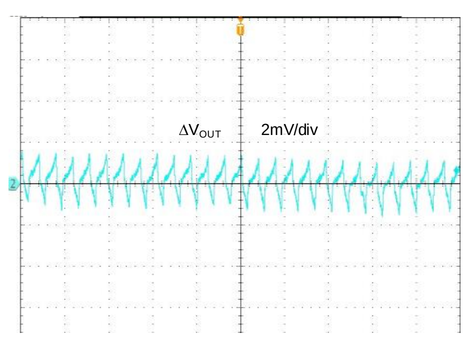
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A)



Time (1μs/div)

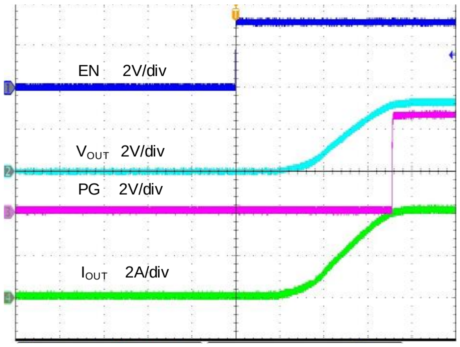
Output Ripple

(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A)



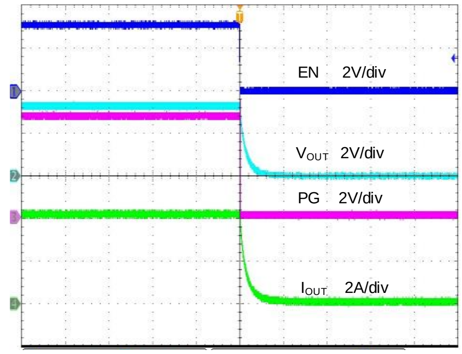
Time (1μs/div)

Startup from EN
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A)



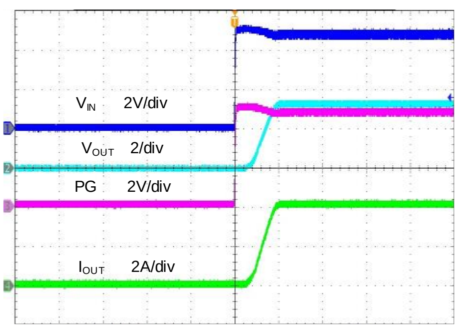
Time (200μs/div)

Shutdown from EN
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A)



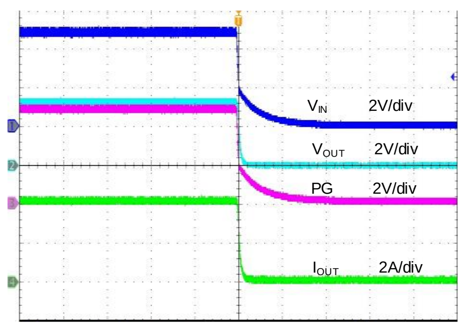
Time (200μs/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A)



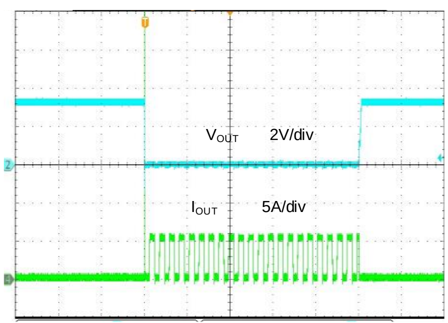
Time (800μs/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A)



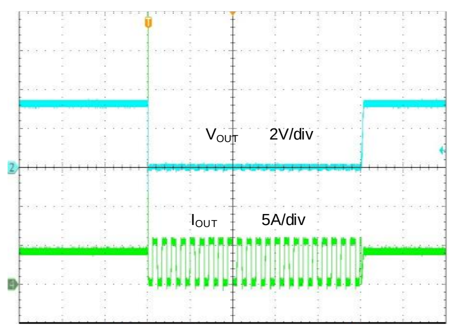
Time (800μs/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A-Short)



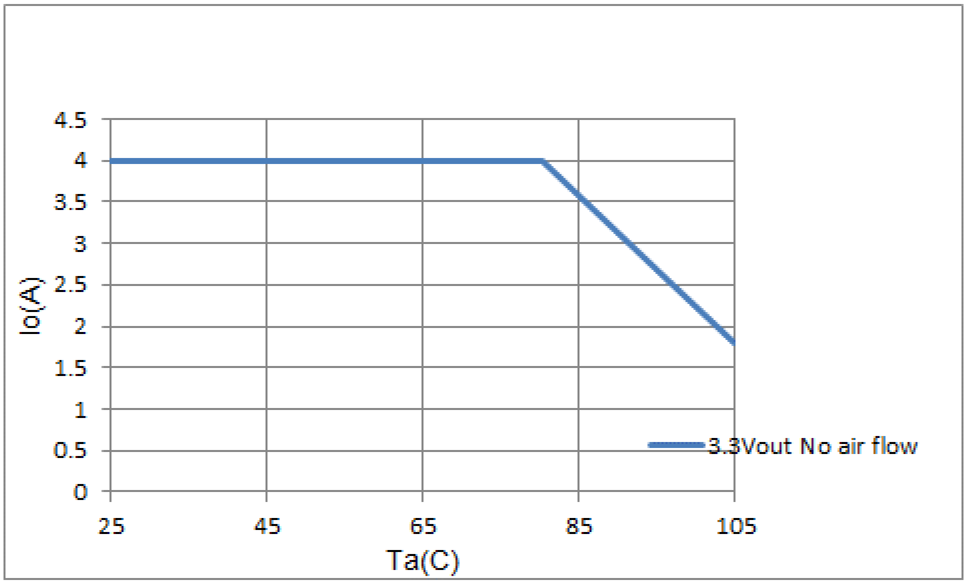
Time (10ms/div)

Short Circuit Protection
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A-Short)



Time (10ms/div)

Thermal Derating Curve @VIN=5V



1) TA: Air temperature, 0.5 inch above IC.
2) Based on a four-layer Silergy Evaluation Board in the natural convection.
3) The inductor temperature is not beyond 115℃ under this TD curve.
4) For customer’s specific application, the recommended inductor temperature limitation is 115℃.

Applications Information

The following paragraphs provide guidance on selecting the input capacitor C_{IN}, the output capacitor C_{OUT}, and the feedback resistors (R_H and R_L) to meet the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If R_H =100kΩ is chosen, then R_L can be calculated to be:

$$R_L = \frac{0.6 \times R_H}{V_{OUT} - 0.6}$$

Input Capacitor C_{IN}

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor with higher than 10V rating and greater than 10μF capacitance, Place this ceramic capacitor really close to the VIN and GND pins.
Care should be taken to minimize the loop area formed by C_{IN}, and VIN/GND pins.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required, to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMSMAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.
The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple equirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLECAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLECAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

Two typical X7R or better grade ceramic capacitors with higher than 10V rating and greater than 10μF capacitance are recommended for most applications. Place the capacitors really close to the VIN and GND pins, while minimizing the loop area formed by CIN, and VIN/GND pins. An additional 100 nF capacitor used to reduce high frequency noise is recommended to be used in parallel and placed closest to the VIN/GND pins.

Obtaining a good input ripple performance is dependent on selecting capacitors that can handle the RMS ripple current.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with higher than 6.3V rating and greater than 44μF capacitance. Place this ceramic capacitor really close to the VOUT and GND pins to minimize the loop area formed by C_{OUT}, and the VOUT/GND pins.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{sw}}$$

If the output capacitance is larger than 100μF (ceramic) or other type of capacitor (polymer, tantalum…) is used, please contact Silergy supporting team to get more assessment.

External Capacitor Recommendation

	Description	Vendor	PN
C_{IN}	10μF/16V/X7S ,0805	Murata	GRM21BC71C106KE11L
C_{OUT}	22μF/6.3V/X7T,0805	Murata	GRM21BD70J226ME44L

FCCM Mode

The SQ76004B operates in FCCM (Forced Continuous Inductor Current Mode). The low-side synchronous rectifier remains on until the next t_{ON} cycle, allowing continuous current flow through the inductor. This allows the device to maintain a relatively constant switching frequency over the output current range at the expense of reduced efficiency during light load operation.

Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If VFB is greater than VPG low threshold and less than VPG high threshold for at least the power good delay time (low to high), PG will be high-impedance. Otherwise, it is pulled low. PG allowable current should not exceed 10mA. Ensure that a proper resistor value with a value between 10kΩ~100kΩ is used. The pull-up resistor can be connected to any active voltage rail that ensures a proper voltage level for the device this pin is connected to.

Over Current Protection

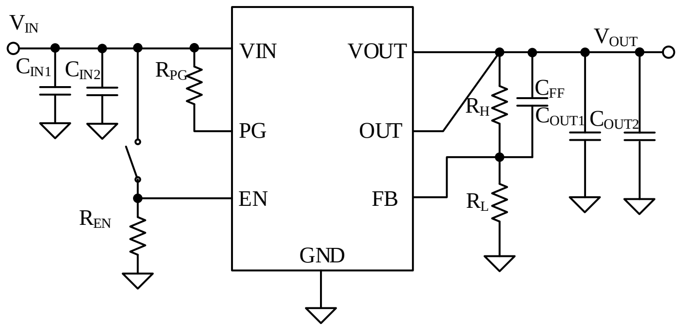
When the load current is increasing, as soon as the high side power MOSFET current gets higher than peak current limit threshold(~6A), the high side power MOSFET will turn off and the low side power MOSFET will turn on and stay on until the current going through it decreases below the valley current limit threshold(~5A). If the load current continues to increase, the output voltage will drop. When the output voltage drops to below 20% of the target the output, the Under Voltage Protection (UVP) is triggered and the device stops switching for a period of 1ms (typ.). A soft-start is initiated after the hiccup time and the device will attempt to restart. Normal operation is resumed if the overcurrent condition is removed.

The UVP fault detection is disabled during the startup sequence an1ms afterwards, as well as during shutdown.

Thermal Shutdown Protection

If the internal (die) temperature of SQ76004B goes higher than the thermal shutdown temperature threshold (typical 150℃), the device turns off both MOSFETs and enters thermal shutdown protection mode. The device resumes operation when the temperature decreases below 130℃.

Application Schematic (V_{OUT} = 1.8V)



BOM List

Designator	Description	Part Number	Manufacturer	Note
C_{IN1}	47µF/25V Electrolytic Cap			
C_{IN2}	10µF/16V/X7S ,0805	GRM21BC71C106KE11L	Murata	
C_{OUT1}, C_{OUT2}	22µF/6.3V/X7T,0805	GRM21BD70J226ME44L	Murata	
C_{FF}	NA			V_{OUT}≤0.8V, C_{FF}=120pF
R_H, R_{PG}	100kΩ,1%,0603			
R_L	50kΩ,1%,0603(V_{OUT}=1.8V)			
R_{EN}	1MΩ,1%,0603			

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

- C_{IN} must be close to the pins VIN and GND. The loop area formed by C_{IN} and GND must be minimized.
- C_{OUT} must be close to the pins VOUT and GND. The loop area formed by C_{OUT} and GND must be minimized.
- Place the FB components (R_H, R_L and C_{FF}) as close to the FB pin as possible. Avoid routing the FB trace near LX as it is noise sensitive.
- It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

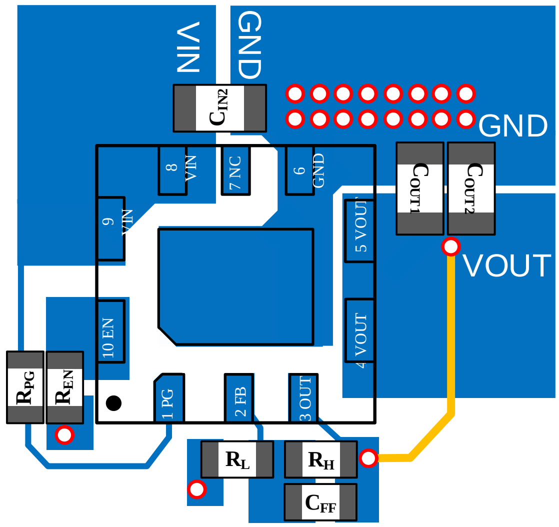
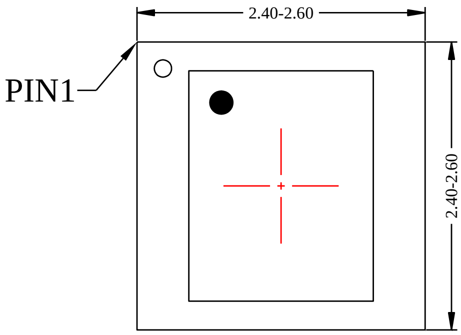
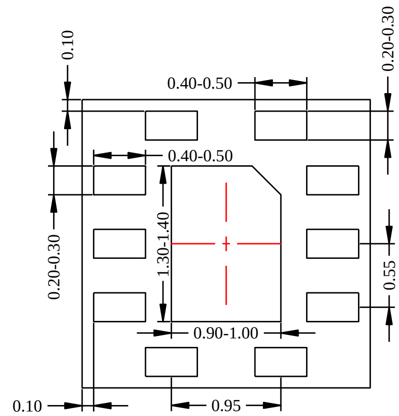


Figure 18. Suggested PCB Layout

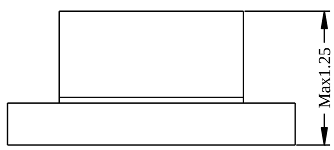
QFN2.5×2.5-10 Package Outline Drawing



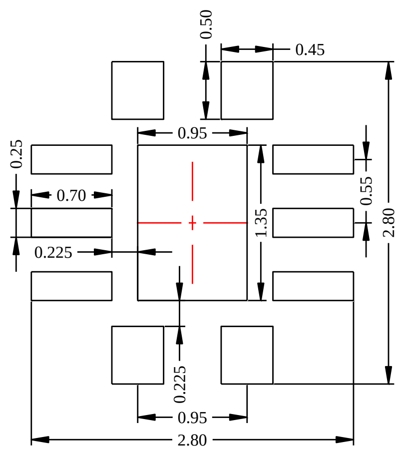
Top View



Bottom View



Side View



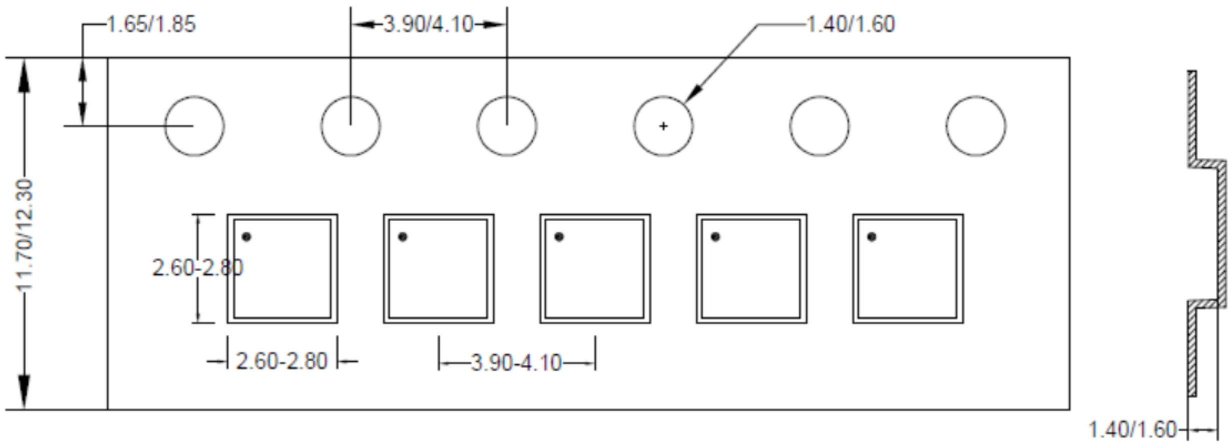
Recommended PCB layout
(Reference only)

Notes: 1.All dimension in millimeter and exclude mold flash & metal burr.

2.Center line on drawing refers to the chip body center.

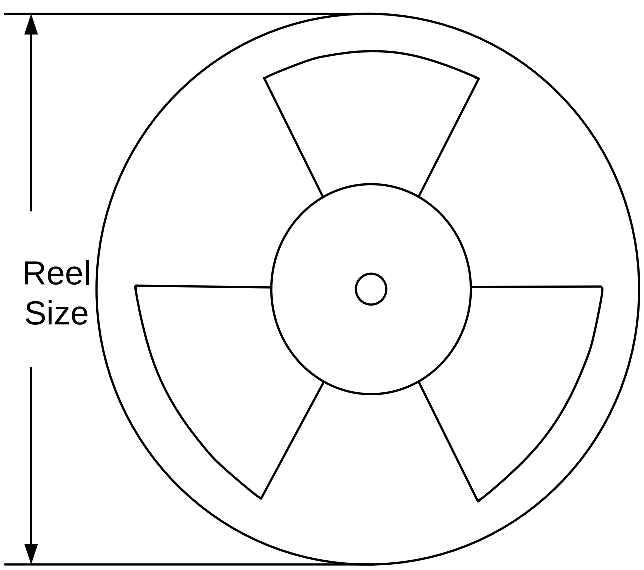
Taping and Reel Specification

QFN2.5×2.5 Package Orientation



Feeding Direction

Carrier tape and reel specification for packages



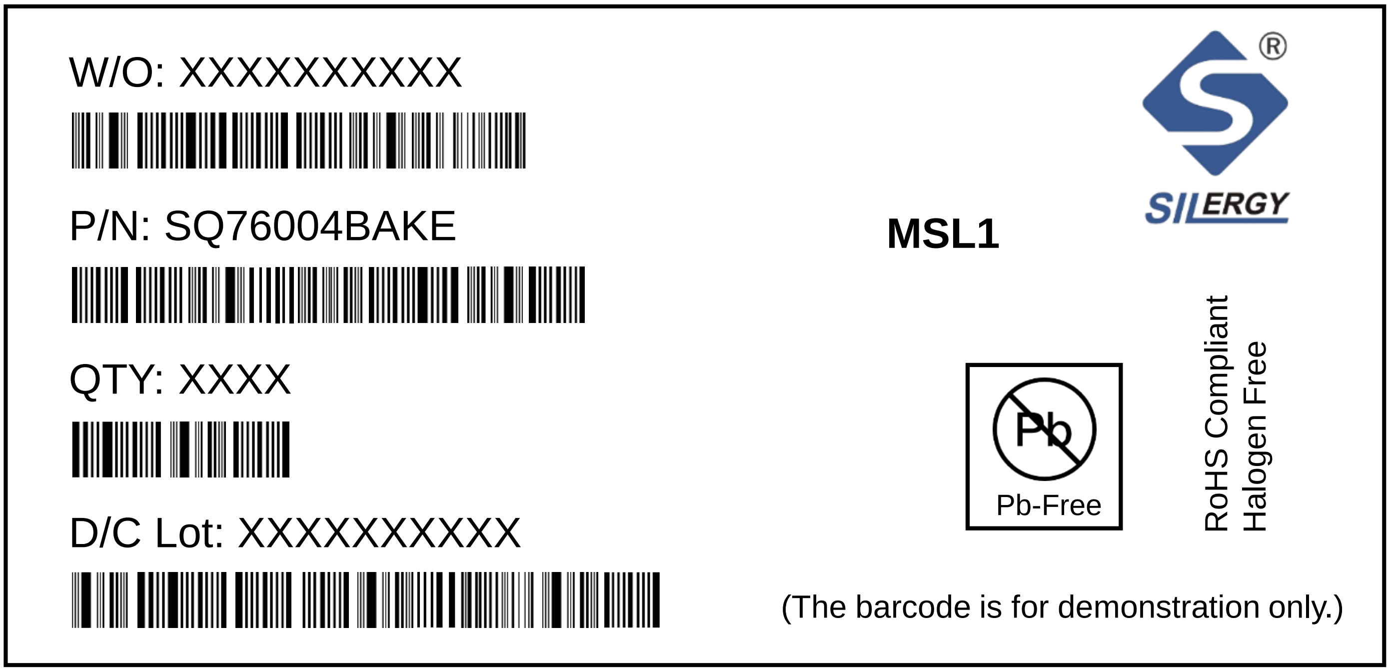
Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN2.5×2.5-10	12	4	7"	400	400	2500

Others: NA

Packaging Information

Device Code: HLJ

Label Information



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.20, 2024	Revision 0.0	Initial Release

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