SQ76825B/SQ76825D

High Efficiency 6A, 1.5MHz, I²C Programmable Synchronous Buck Power Module

General Description

The SQ76825B and SQ76825D belong to the same series of high efficiency 1.5MHz synchronous step-down DC/DC converter modules, which have the capability of delivering up to 6A output current. They can operate over a wide input voltage range from 2.7V to 5.5V and integrate main and synchronous MOSFETs with very low $R_{DS(ON)}$ to minimize conduction loss. The output voltage can be programmed from 0.6V to 1.5V through I²C interface.

The modules are available in a 3mm x 4mm package with a height of 1.68mm.

Applications

- Optical modules
- Smartphones
- Notebooks and Tablets

Features

- 2.7V to 5.5V Input Voltage Range
- Pseudo-Constant Frequency: 1.5MHz
- Internal Soft-Start Limits the Inrush Current
- Programmable Output Voltage: 0.6V to 1.5V in 10mV Steps
- Default Output Voltage:
  --SQ76825B: 1V
  --SQ76825D: 0V
- 6A Continuous Load Current Capability
- Remote Voltage Sense Function to Provide Improved Output Accuracy
- Hiccup Mode Protection for Hard Short Condition
- Power Good Indicator
- RoHS Compliant and Halogen Free
- Compact Package: MQFN3×4-16

Typical Application

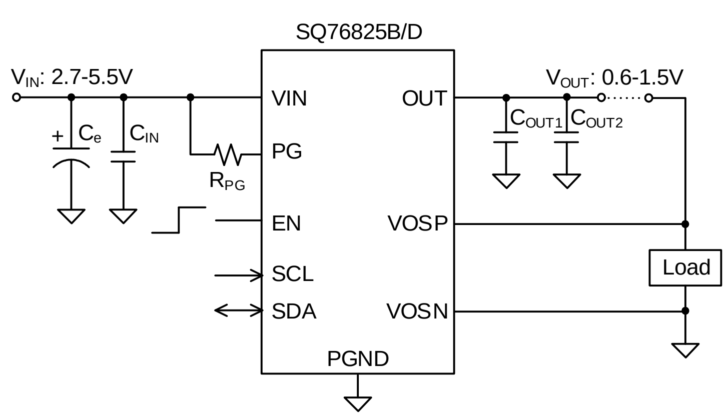


Figure 1. Application Circuit

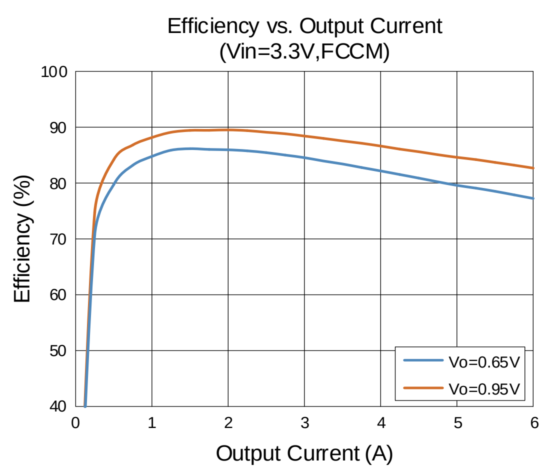
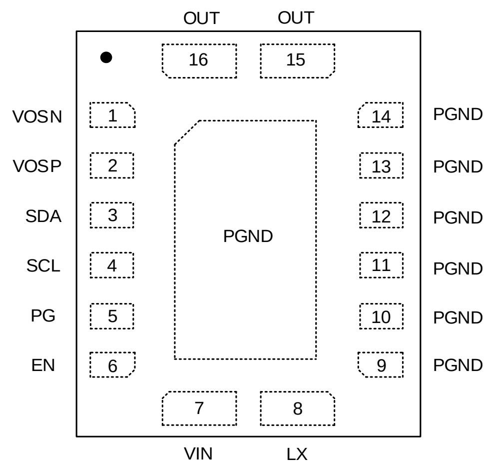


Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Default output voltage	Package Type
SQ76825BABE	1V	MQFN3×4 RoHS-Compliant and Halogen-Free
SQ76825DABE	0V	

Pinout (top view)



Pin Name	Pin Number	Pin Description
VOSN	1	Negative remote sense pin. Connect to GND at the load.
VOSP	2	Positive remote sense pin. Connect to OUT of the load.
SDA	3	I^2C interface bi-directional data line.
SCL	4	I^2C interface clock line.
PG	5	Power good indicator. When output voltage exceeds 90% of regulation point, it becomes high impedance. Driven low otherwise.
EN	6	Enable control pin. Pull high to turn on. Do not leave floating. When EN pin is low, the I^2C register settings will reset to default values.
VIN	7	Power input pins. Decouple this pin to PGND with at least one 22µF ceramic capacitor.
LX	8	Inductor pin. Leave floating.
PGND	9-14	Power ground pin. Connect to power ground.
OUT	15,16	Output pin. Decouple this pin to PGND with at least two 22µF ceramic capacitors.

Block Diagram

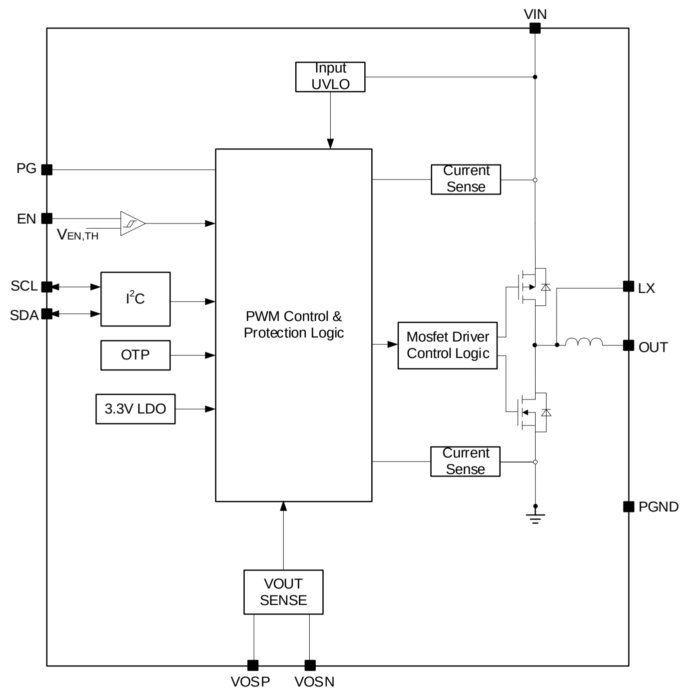


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	6	V
EN, PG, SCL, SDA, VOSP, VOSN	-0.3	VIN+0.6	
LX (DC)	-0.3	VIN+0.3	
LX (AC, less than 10ns)	-5	11	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering,10 sec.)		260	
Storage Temperature	-40	125	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	26.8	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	0.2	
Ψ_{JB} Junction-to-Board Thermal Resistance	12.3	
P_D Power Dissipation T_A = 25°C	3.7	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.7	5.5	V
Output Voltage	0.6	1.5	
Output Current (Note 6)	0	6	A

Electrical Characteristics

(VIN = 3.3V, V_{OUT}= 0.95V, C_{OUT} = 2x22µF, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply	Input Voltage	VIN		2.7	3.3	5.5	V
	UVLO, rising	V_{UVLOR}	VIN rising edge	2.3	2.55	2.7	V
	UVLO, hysteresis	V_{UVHYST}			150		mV
	Quiescent Current	I_Q	EN=3.3V, VOSP=110%×VREF, IOUT=0		95		µA
	Shutdown Current	$I_{SHDN\_H/W}$	EN=0V, T_J = 25°C		0.5	1	µA
		$I_{SHDN\_S/W}$	EN=VIN=3.3V, Buck_EN=0		40		µA
	Input OVP Threshold	V_{OVP}	Rising threshold	5.9	6.2	6.5	V
			Falling threshold	5.65	5.85	6.15	
	Input OVP Blanking Time (Note 5)	$T_{Blanking}$			10		µs
Output	Output Voltage Set-Point (Note 5)	V_{SET}	Forced PWM, VOUT=VSEL0, default value	-1		+1	%
	Soft start time	t_{SS}	10%-90% V_{OUT}		300		µs
	VOSN Compensation Range	V_{VOSN}		120			mV
Power Switch	Switching Frequency	f_{SW}		1.2	1.5	1.8	MHz
	Min On Time(Note5)	t_{ON_MIN}			65		ns
	Output Discharge Resistance	R_{DIS}			120		Ω
Thermal Protection	Thermal Shutdown Thershold (Note5)	T_{SD}	Die temperature		150		˚C
	Thermal Shutdown Hysteresis (Note5)	T_{WNHYS}			15		˚C
EN Control	EN Logic Low	$V_{EN, L}$				0.4	V
	EN Logic High	$V_{EN, H}$		1.1			V
SCL SDA	Low Level Input Voltage	$V_{I2C, L}$				0.4	V
	High Level Input Voltage	$V_{I2C, H}$		1.5			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA}, θ_{JC} and Ψ_{JB} are evaluated based on a four-layer 8cm×8cm Silergy Evaluation Board under natural convection conditions at T_A = 25°C. Board thickness: 1.6mm, copper thickness: 2 oz, copper coverage: 95%. Junction temperature (T_J) refers to the hottest device temperature which is the inductor temperature for this product. Case temperature (T_C), refers to the device package surface temperature which is the surface temperature of the Inductor. Ambient temperature (T_A) refers to the air temperature 0.5 inch above the module. Board temperature (T_B) refers to the PCB point to the hottest IC pin with a 1mm distance on the same PCB surface layer.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: The values are guaranteed by design, statistical correlation, not production tested.

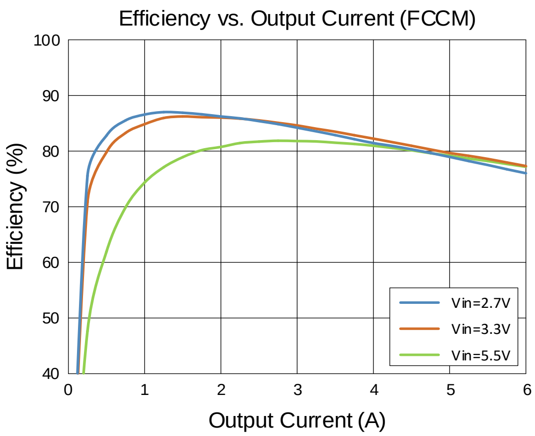
Note 6: Please refer to the Thermal Derating Curve to get the maximum output current under different ambient temperatures.

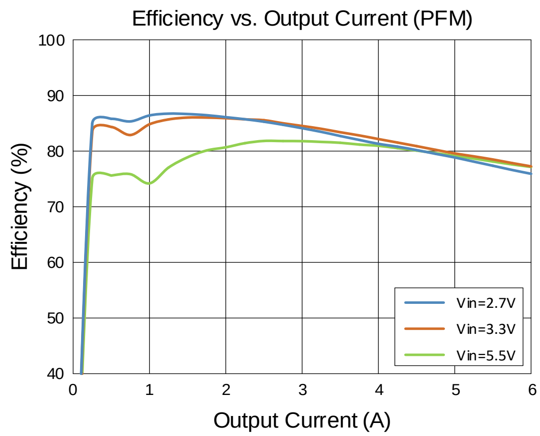
Typical Performance Characteristics

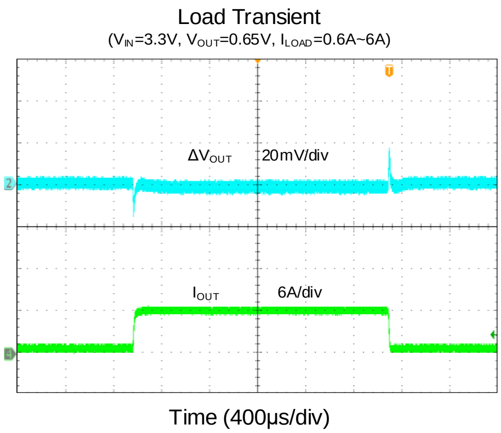
(V_{IN} = 3.3V, C_{OUT} = 2×22μF, T_A = 25°C, FCCM mode, resistor tolerance is ±1%, unless otherwise specified.)

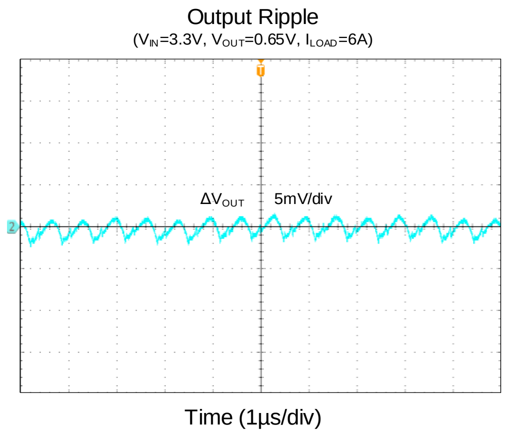
SQ76825B

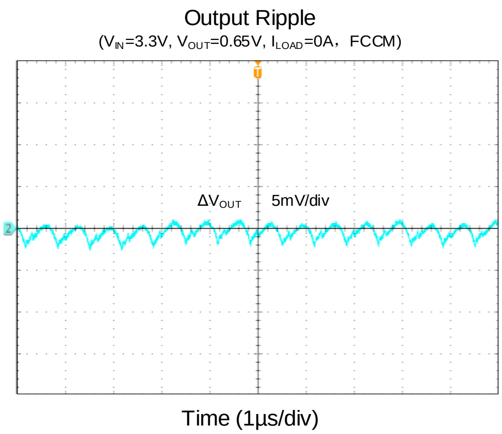
V_{OUT}=0.65V

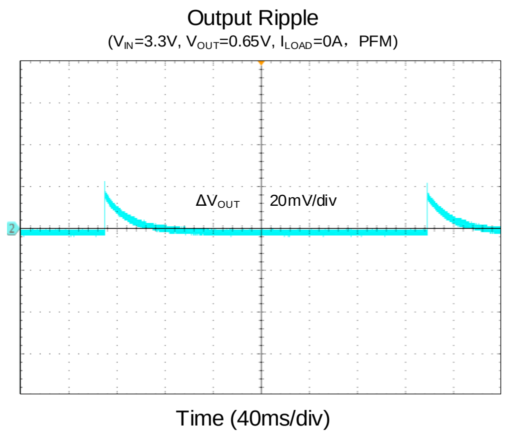




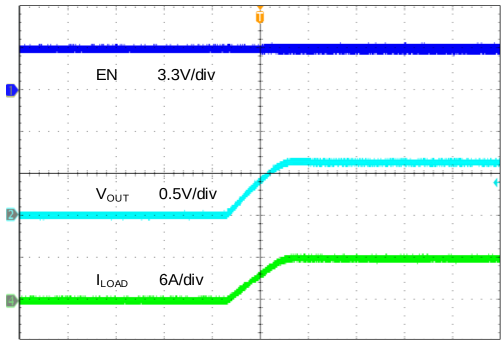






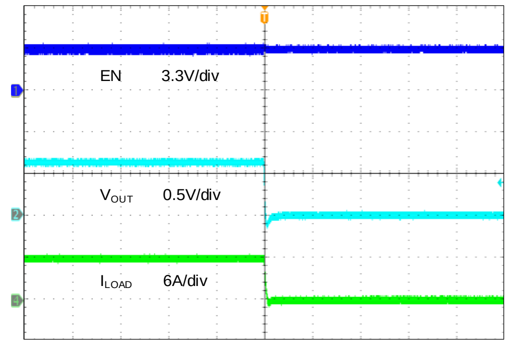


Startup from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A)



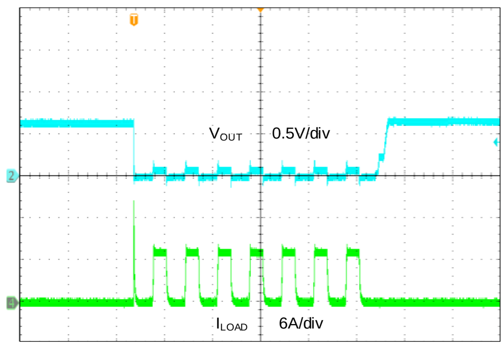
Time (200us/div)

Shutdown from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A)



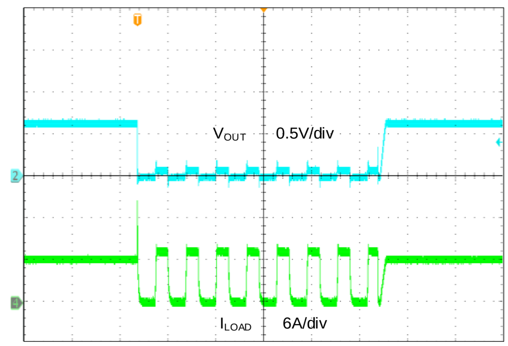
Time (200us/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=0A-Short)



Time (2ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A-Short)

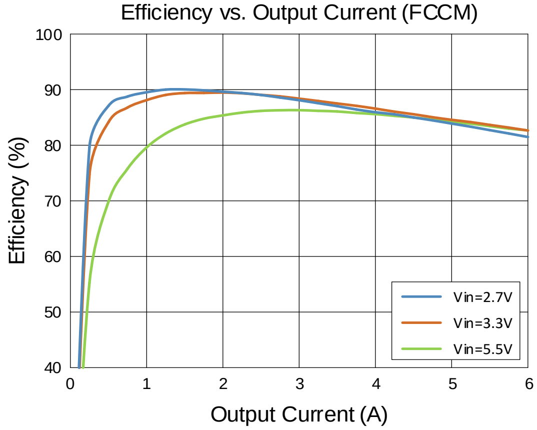


Time (2ms/div)

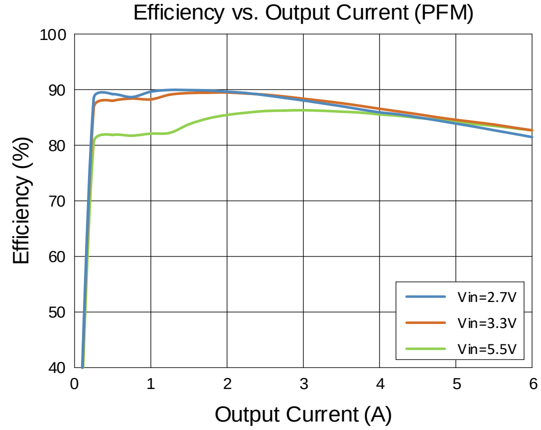
SQ76825B

V_{OUT}=0.95V

Efficiency vs. Output Current (FCCM)

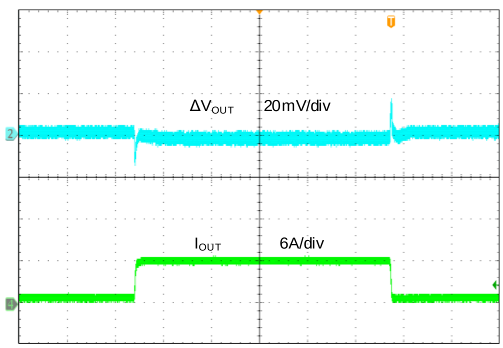


Efficiency vs. Output Current (PFM)



Load Transient

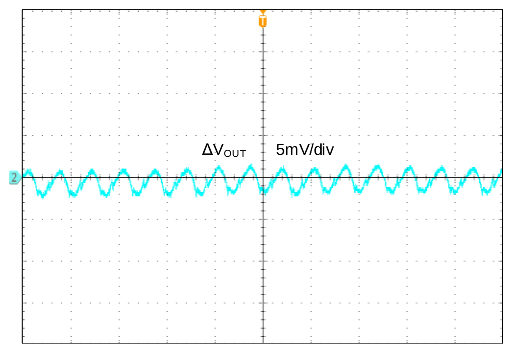
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0.6A~6A)



Time (400μs/div)

Output Ripple

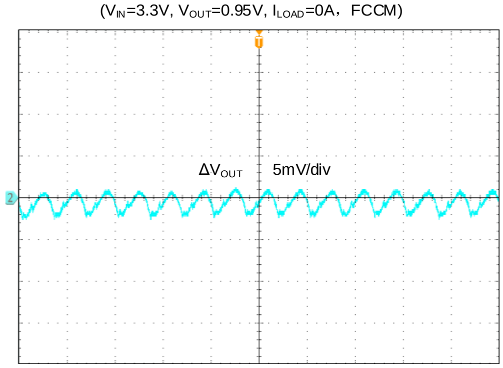
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A)



Time (1μs/div)

Output Ripple

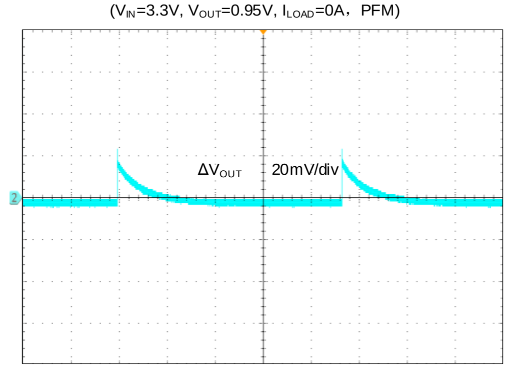
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0A, FCCM)



Time (1μs/div)

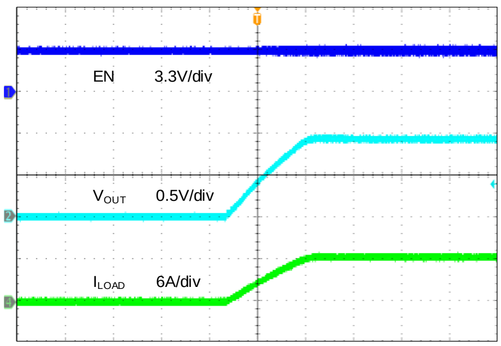
Output Ripple

(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0A, PFM)



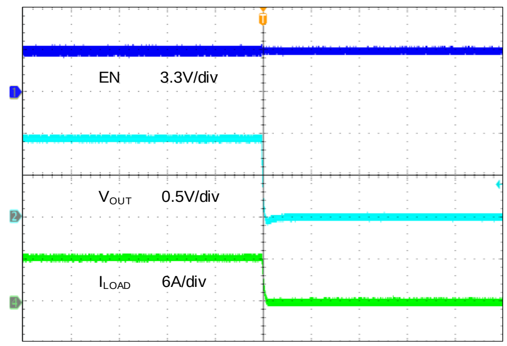
Time (40ms/div)

Startup from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A)



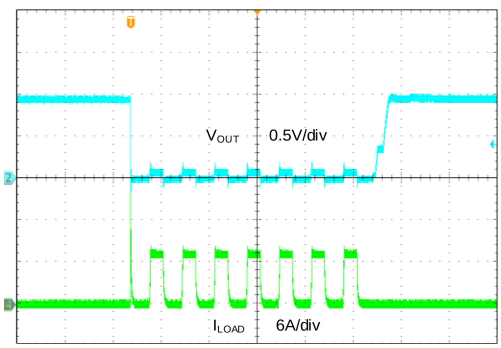
Time (200us/div)

Shutdown from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A)



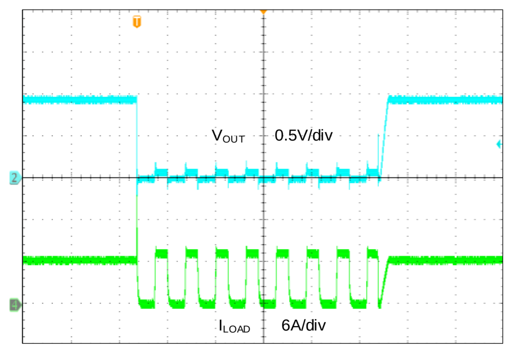
Time (200us/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0A-Short)



Time (2ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A-Short)

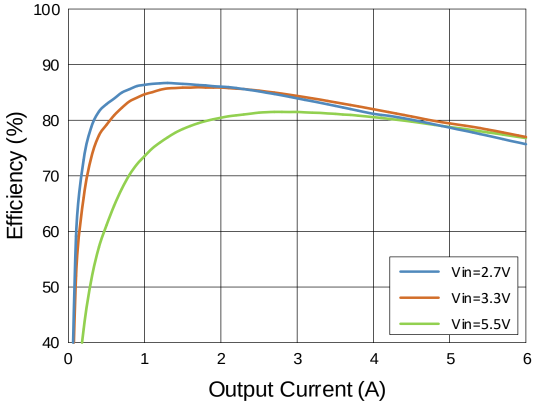


Time (2ms/div)

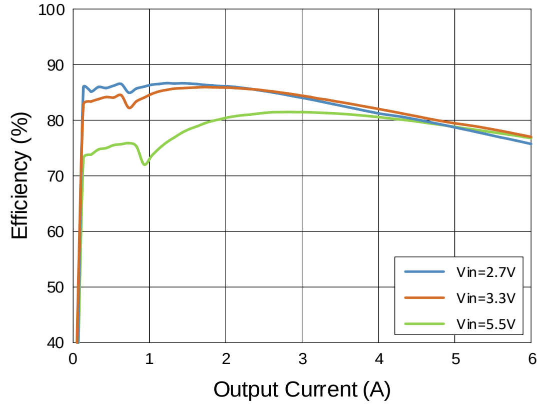
SQ76825D

V_{OUT}=0.65V

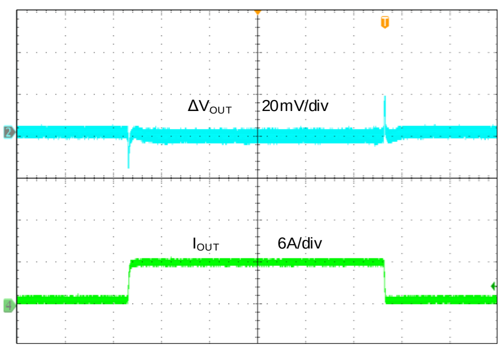
Efficiency vs. Output Current (FCCM)



Efficiency vs. Output Current (PFM)

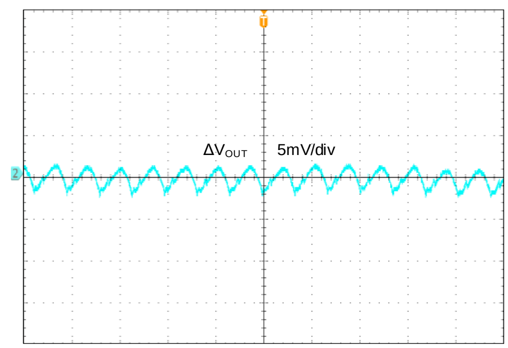


Load Transient
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=0.6A~6A)



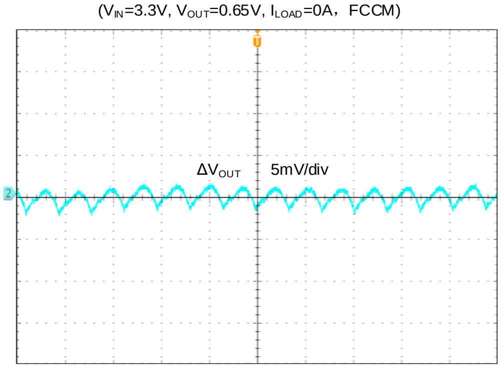
Time (400μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A)



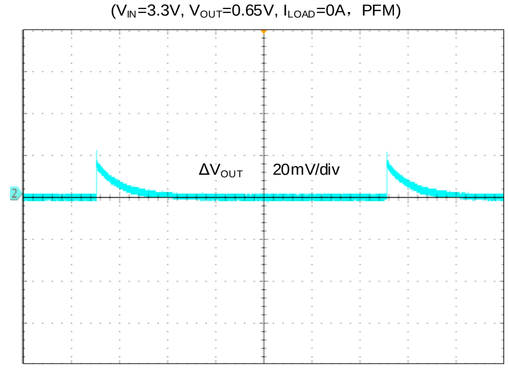
Time (1μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=0A，FCCM)



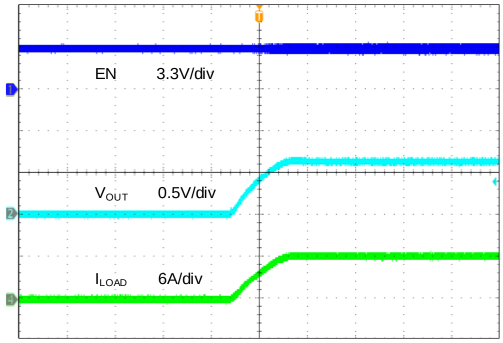
Time (1μs/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=0A，PFM)



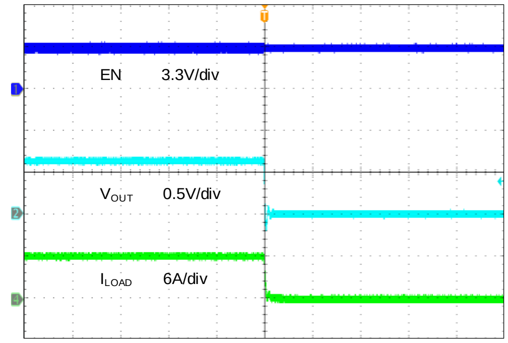
Time (40ms/div)

Startup from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A)



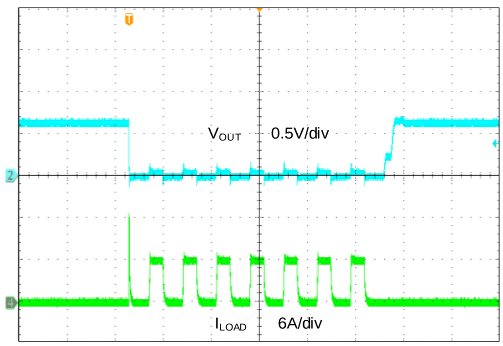
Time (200us/div)

Shutdown from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A)



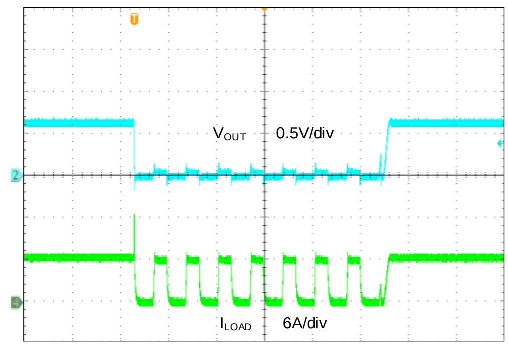
Time (200us/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=0A-Short)



Time (2ms/div)

Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.65V, I_{LOAD}=6A-Short)

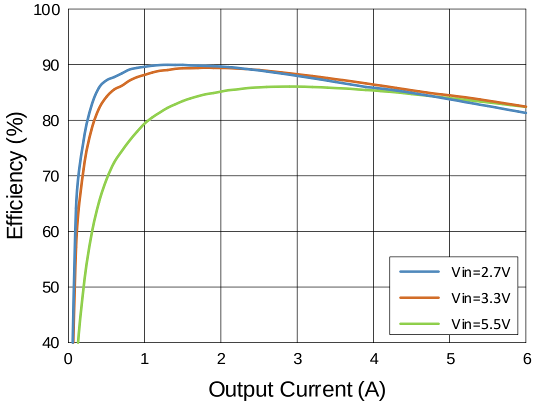


Time (2ms/div)

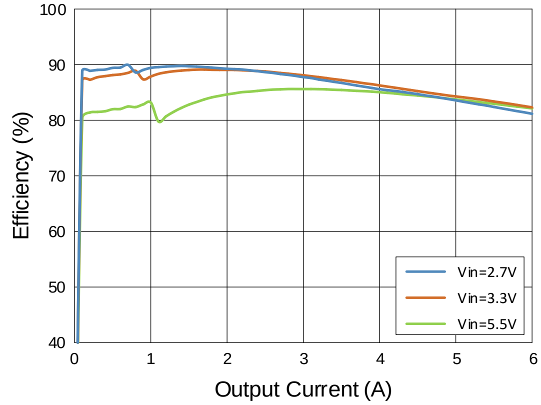
SQ76825D

V_{OUT}=0.95V

Efficiency vs. Output Current (FCCM)

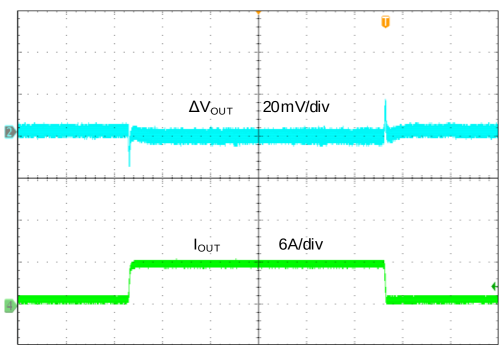


Efficiency vs. Output Current (PFM)



Load Transient

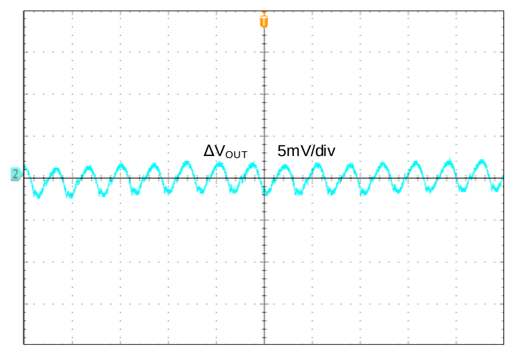
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0.6A~6A)



Time (400µs/div)

Output Ripple

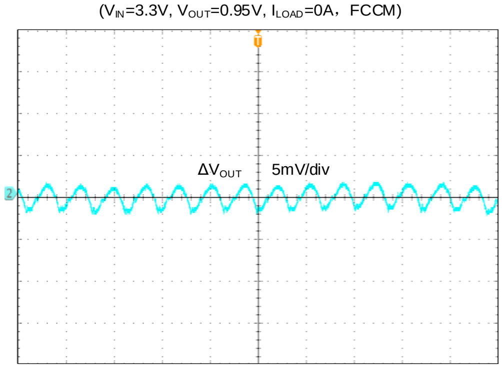
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A)



Time (1µs/div)

Output Ripple

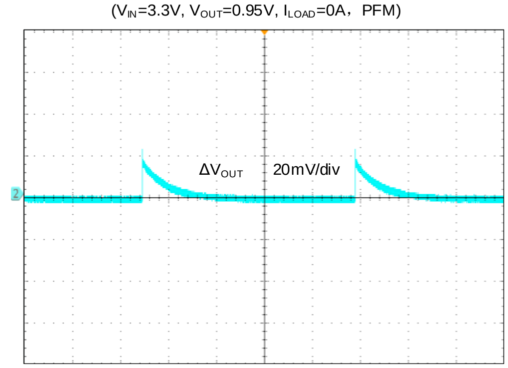
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0A， FCCM)



Time (1µs/div)

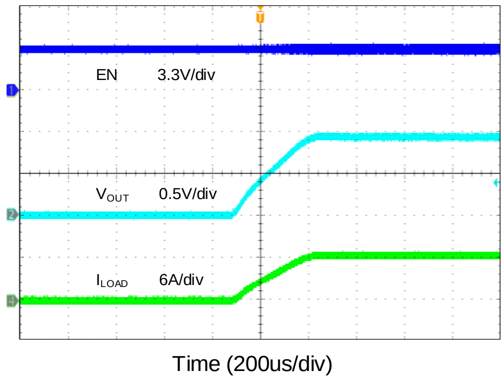
Output Ripple

(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0A， PFM)

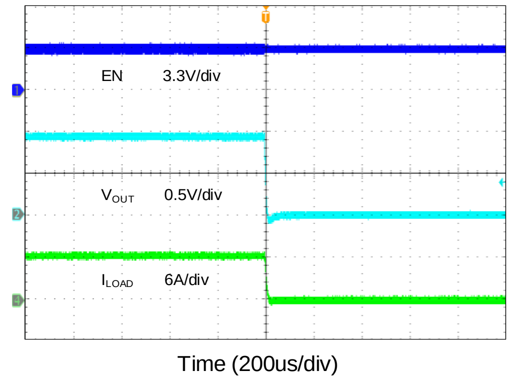


Time (40ms/div)

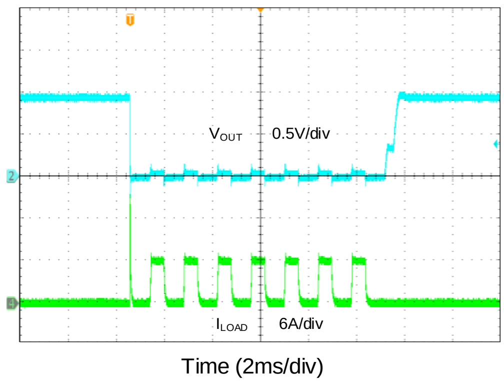
Startup from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A)



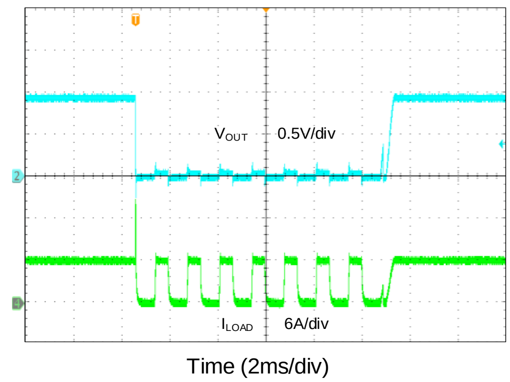
Shutdown from Buck_EN
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A)



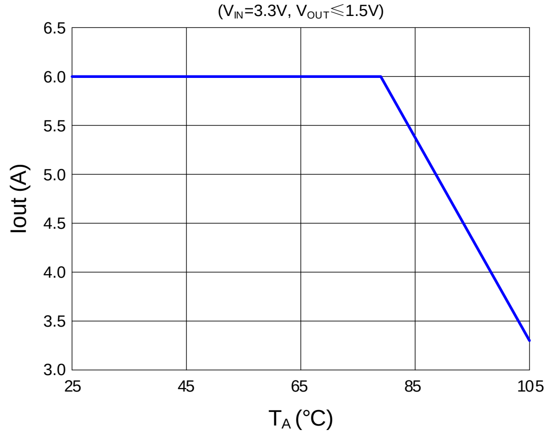
Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=0A-Short)



Short Circuit Protection
(V_{IN}=3.3V, V_{OUT}=0.95V, I_{LOAD}=6A-Short)



Thermal Derating
(V_{IN}=3.3V, $V_{OUT}\leqslant$1.5V)



1) T_A: Air temperature, 0.5 inch above IC.

2) Based on a four-layer Silergy Evaluation Board in natural convection.

3) The inductor is exposed, and the package case is the top surface of the inductor.

4) The module case temperature (the surface temperature of the inductor) should not e xceed 110°C.

Detailed Description

The SQ76825B and SQ76825D belong to the same series of high efficiency 1.5MHz synchronous step-down DC/DC converter modules, which have the capability of delivering up to 6A output current. Both devices use a constant on-time architecture, which is able to provide good transient performance.

The input and output capacitors, C_{IN} and C_{OUT} need to be selected for the targeted applications.

Input capacitor C_{IN}

A ceramic capacitor whose capacitance is greater than 22µF is recommended. The component should be placed as close as possible to the module, while also minimizing the loop area formed by C_{IN} and the VIN/PGND pins. When selecting an input capacitor ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X7R or X7S dielectric types are the most often selected due to their small size, low cost, surge current capability and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)},$$

where D represents the converter duty cycle (VOUT/VIN).

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, a single 22uF X7S capacitor is sufficient.

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For best performance, it is recommended to use two 22uF X7S or better grade ceramic capacitors with higher than 4V rating. Place the ceramic capacitors close to the OUT and PGND pins to minimize the loop area formed by C_{OUT}, and the OUT/PGND pins.

Table1. External Capacitor Recommendation

	Description	Vendor	PN
C_{IN}, C_{OUT}	22µF/16V/X7S, 1206	Murata	GRM31CC71C226ME11#

Output Voltage Setting

The output voltage can be programmed from 0.6V to 1.5V by writing an 8-bit register VSEL0(0x00) using the I^2C interface.

Enable Control

The EN pin controls the device start-up. An EN pin low to high transition starts the power-up sequence. If EN pin is LOW, the module will be turned off, and all I^2C registers will be reset to default values.

When EN pin is HIGH, the output can be controlled using the BUCK_EN bit ("Register 0x01" [7]). The logic table is shown below in Table 2.

Table 2. Hardware and software EN logic

EN pin	BUCK_EN bit	I^2C	Output
0	X	disabled	OFF
1	0	enabled	OFF
1	1	enabled	ON

Power Good Signal

The voltage of pin PG reflects the status of output voltage. The pin needs to be connected to VIN or an external voltage source using a 1MΩ pull-up resistor. If the output voltage is over ~90% and under ~120% target voltage, PG becomes high impedance, otherwise it's driven low.

Voltage Remote Sense Function

The module uses remote sense function to compensate for voltage drop, which is caused by long connections. The VOSP and VOSN pin should use a Kelvin-connection at the output capacitor close to the load and routed back to the device as a differential pair. The remote sensing traces must NOT be adjacent to the LX node on the PCB layout to minimize noise coupling.

PFM mode and FCCM mode

Under light load conditions, the converter can be configured using Control Register (0x01, bit[6]), to operate in FCCM (Forced Continuous Conduction Mode) or PFM (Pulse Frequency Modulation) mode.

In PFM mode, the module operates only when output voltage falls below the target value. It enters a sleep period where internal circuits will be turned off to reduce quiescent current. This control method is used to improve the light-load efficiency.

In FCCM mode, the device operates using fixed frequency, which allows filtering of the switching frequency and its spectral components in noise-sensitive applications.

Input Overvoltage Protection

When the VIN exceeds the over voltage protection threshold, the module stops switching to protect the circuitry. An internal 10µs blanking time filter helps prevent the circuit from shutting down due to noise.

Over Temperature Protection

The module includes over temperature protection to prevent overheating due to excessive power dissipation. The die temperature is continuously monitored, and when it exceeds 150°C, the module shuts down. When the junction temperature cools down by 15°C (typical), the module resumes normal operation with a complete soft start cycle.

Over Current Protection

The module uses a cycle-by-cycle “valley” current

limit. The inductor current value is obtained by measuring the current flowing in the synchronous MOSFET when it is on, as the inductor current ramps down. If the current exceeds the valley current limit (~7A), the low side MOSFET stays on until the current returns to safe levels.

This mechanism limits the inductor current, but the module does not latch off. Under an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall. When the output voltage falls below ~40% target output voltage, the module operates in hiccup mode. The hiccup frequency is ~700Hz, with a duty cycle of 50%. If the hard short is removed, the module will return to normal operation. The overtemperature protection may be triggered if the device overheats. In this case, the module will shut down to protect itself and any downstream devices.

The module also features a cycle-by-cycle “peak” current limit (~10A), current limit for the main MOSFET). During on-time t_{ON}, the high-side power switch current is monitored. If the monitored current exceeds the current limit, the high-side power switch is turned off, and the low-side synchronous rectifier is turned on, which inhibits t_{ON}. t_{ON} cannot be disabled once the low-side synchronous rectifier current is lower than the current limit value. The peak current limit protection uses a blanking time. During the initial on-time, the high-side power switch current sampling is disabled to reduce noise interference. The peak current limit protection priority is lower than the minimum on-time.

I²C Interface

The module features an I²C interface that allows the host processor to control the output voltage to achieve the DVS (Digital Voltage Scaling) function. The I²C uses standard I²C commands. The module always operates as a target device and is addressed using a 7-bit target address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C controller always generates the START and STOP conditions.

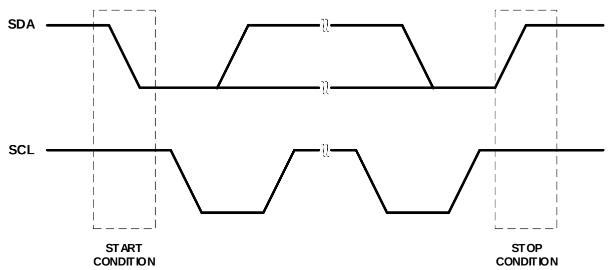


Figure 4. I²C START and STOP Conditions

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

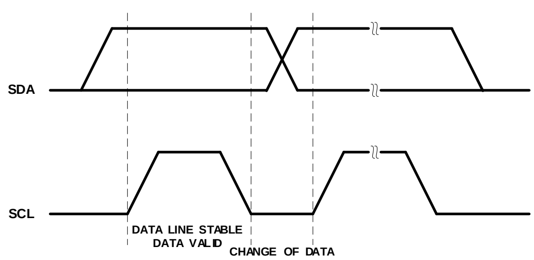


Figure 5. I²C Data Validity Condition

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the controller sends 7-peripheral address bits and an R/$\overline{\text{W}}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the controller and the peripheral to acknowledge receipt of register addresses and data.

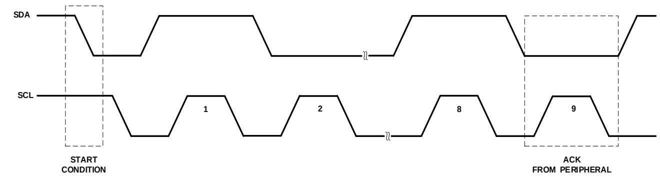


Figure 6. I²C Acknowledge Condition

Data Transactions

All transactions start with a control byte sent from the I²C controller device. The control byte begins with a START condition, followed by 7-bits of peripheral address (1100000x) for the device followed by the 8th bit, R/$\overline{\text{W}}$ bit. The R/$\overline{\text{W}}$ bit is 0 for write commands or 1 for read. If any peripheral devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no peripherals exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge (NACK) condition. Once the control byte is sent, and the device acknowledges it, the 2nd byte sent by the controller must be a register address byte. The register address byte tells the device which register the controller will write or read. Once the device receives a register address byte it responds with an acknowledge (ACK).

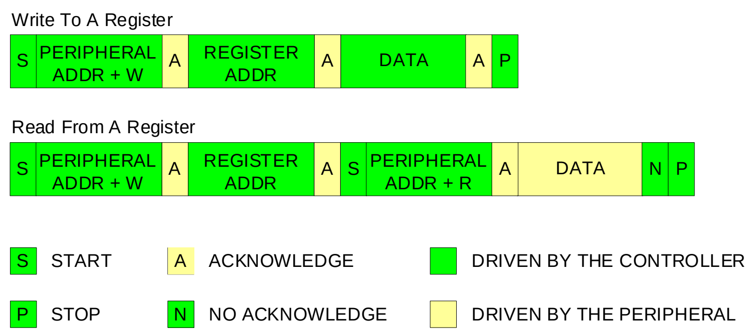


Figure 7. Data transfer format

Register Settings

1. VSEL0 (0x00)

Register Name	VSEL0			
Address	0x00			
Field	Bit	R/W	Default	Description
Reserved	7	R/W	0	Always reads back 0.
NSEL	6:0	R/W	0101000 (VOUT=1.00V)	Set output voltage from 0.60V to 1.50V as Table 3. Default value is 1.00V.

Table 3. Output Voltage Setting

NSEL[6:0]	VOUT(V)	NSEL[6:0]	VOUT(V)	NSEL[6:0]	VOUT(V)	NSEL[6:0]	VOUT(V)
000 0000	0.60	010 0000	0.92	100 0000	1.24	110 0000	1.50
000 0001	0.61	010 0001	0.93	100 0001	1.25	110 0001	1.50
000 0010	0.62	010 0010	0.94	100 0010	1.26	110 0010	1.50
000 0011	0.63	010 0011	0.95	100 0011	1.27	110 0011	1.50
000 0100	0.64	010 0100	0.96	100 0100	1.28	110 0100	1.50
000 0101	0.65	010 0101	0.97	100 0101	1.29	110 0101	1.50
000 0110	0.66	010 0110	0.98	100 0110	1.30	110 0110	1.50
000 0111	0.67	010 0111	0.99	100 0111	1.31	110 0111	1.50
000 1000	0.68	010 1000	1.00(default)	100 1000	1.32	110 1000	1.50
000 1001	0.69	010 1001	1.01	100 1001	1.33	110 1001	1.50
000 1010	0.70	010 1010	1.02	100 1010	1.34	110 1010	1.50
000 1011	0.71	010 1011	1.03	100 1011	1.35	110 1011	1.50
000 1100	0.72	010 1100	1.04	100 1100	1.36	110 1100	1.50
000 1101	0.73	010 1101	1.05	100 1101	1.37	110 1101	1.50
000 1110	0.74	010 1110	1.06	100 1110	1.38	110 1110	1.50
000 1111	0.75	010 1111	1.07	100 1111	1.39	110 1111	1.50
001 0000	0.76	011 0000	1.08	101 0000	1.40	111 0000	1.50
001 0001	0.77	011 0001	1.09	101 0001	1.41	111 0001	1.50
001 0010	0.78	011 0010	1.10	101 0010	1.42	111 0010	1.50
001 0011	0.79	011 0011	1.11	101 0011	1.43	111 0011	1.50
001 0100	0.80	011 0100	1.12	101 0100	1.44	111 0100	1.50
001 0101	0.81	011 0101	1.13	101 0101	1.45	111 0101	1.50

001 0110	0.82	011 0110	1.14	101 0110	1.46	111 0110	1.50
001 0111	0.83	011 0111	1.15	101 0111	1.47	111 0111	1.50
001 1000	0.84	011 1000	1.16	101 1000	1.48	111 1000	1.50
001 1001	0.85	011 1001	1.17	101 1001	1.49	111 1001	1.50
001 1010	0.86	011 1010	1.18	101 1010	1.50	111 1010	1.50
001 1011	0.87	011 1011	1.19	101 1011	1.50	111 1011	1.50
001 1100	0.88	011 1100	1.20	101 1100	1.50	111 1100	1.50
001 1101	0.89	011 1101	1.21	101 1101	1.50	111 1101	1.50
001 1110	0.90	011 1110	1.22	101 1110	1.50	111 1110	1.50
001 1111	0.91	011 1111	1.23	101 1111	1.50	111 1111	1.50

2. Control Register (0x01)

Register Name	Control Register			
Address	0x01			
Field	Bit	R/W	Default	Description
BUCK_EN	7	R/W	SQ76825D: 0 SQ76825B: 1	Software device enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent. BUCK_EN bit must be written as 1 to enable SQ76825D.
MODE0	6	R/W	0	0 = Allow auto-PFM mode during light load. 1 = FCCM mode.
Output Discharge	5	R/W	0	0 = Discharge resistor is disabled. 1 = Discharge resistor is enabled.
Slew Rate	4:2	R/W	000=10mV/0.15us	Set the slew rate for positive voltage transitions. 000 = 10mV/0.15µs 001 = 10mV/0.3µs 010 = 10mV/0.6µs 011 = 10mV/1.2µs 100 = 10mV/2.4µs 101 = 10mV/4.8µs 110 = 10mV/9.6µs 111 = 10mV/19.2µs
RESET	1	R/W	0	Setting to 1 resets all registers to default values.
Reserved	0	R/W	0	Always reads back 0.

3. Power Good Register (0x02)

Register Name	PGOOD Register			
Address	0x02			
Field	Bit	R/W	Default	Description
PGOOD	7	R	0	1: Buck is enabled and soft-start is completed.
Reserved	6:0	R	000 0000	Always reads back 0.

Application Schematic

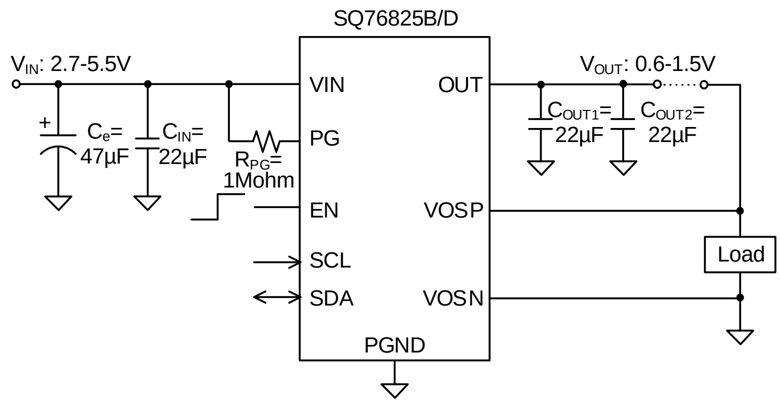


Figure 8. Application schematic

BOM List

Designator	Description	Part Number	Manufacturer
C_e	47μF/16V Electrolytic Capacitor		
C_{IN}	22μF/16V/X7S, 1206	GRM31CC71C226ME11#	Murata
C_{OUT1}, C_{OUT2}	22μF/16V/X7S, 1206	GRM31CC71C226ME11#	Murata
R_{PG}	1Mohm, 0603		

Layout Design

1) C_{IN} must be close to VIN and PGND pins. The loop area formed by C_{IN}, VIN and PGND must be minimized.
2) C_{OUT} must be close to OUT and PGND pins. The loop area formed by C_{OUT}, OUT and PGND must be minimized.
3) It is desirable to maximize the PCB copper area connecting to PGND pin to achieve optimal thermal and noise performance. A ground plane is highly desirable.
4) The VOSP/VOSN traces should be kept short and away from noise sources on the PCB.

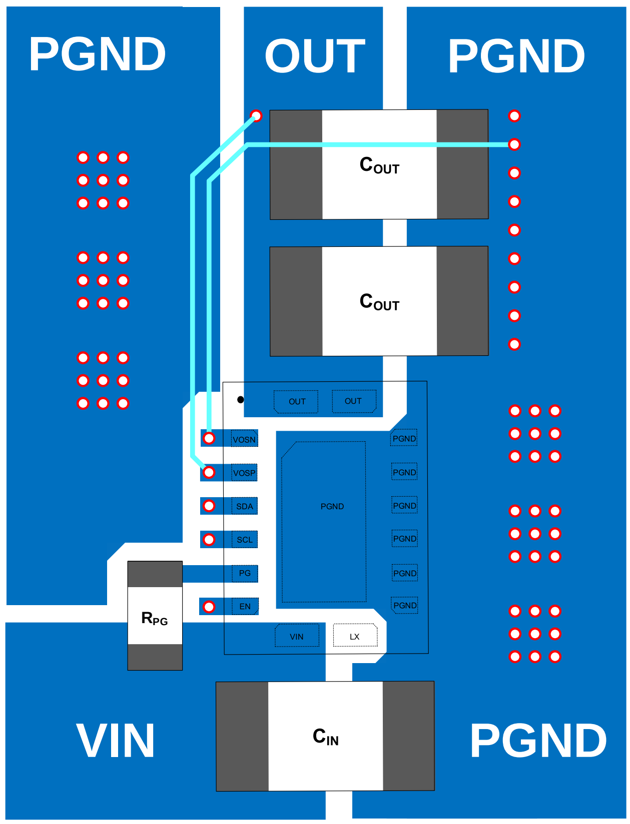
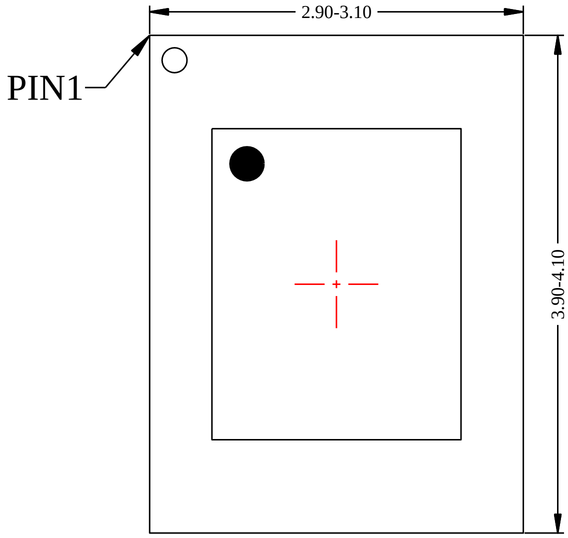
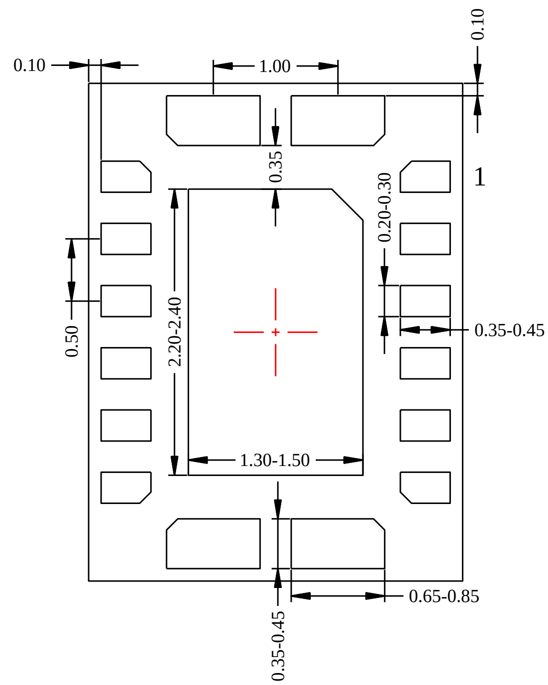


Figure 9. Suggested PCB Layout

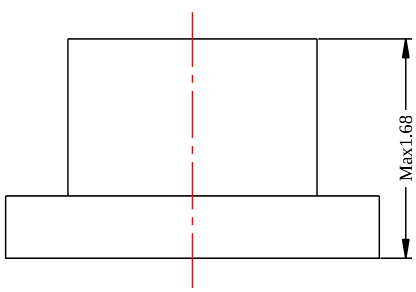
MQFN3X4-16 Package Outline Drawing



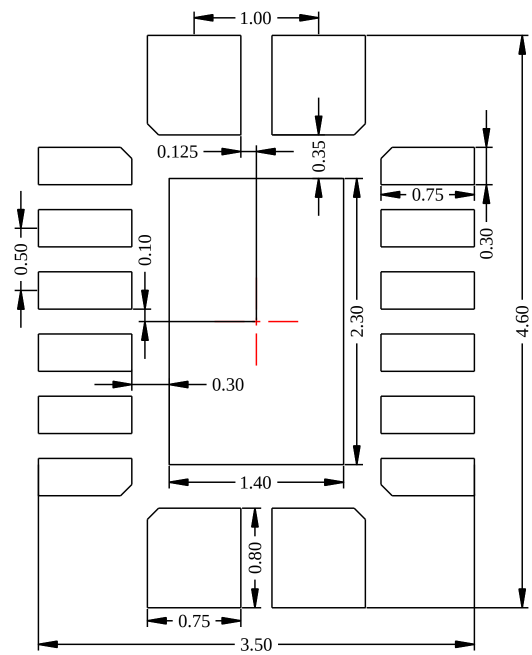
Top View



Bottom View



Front View

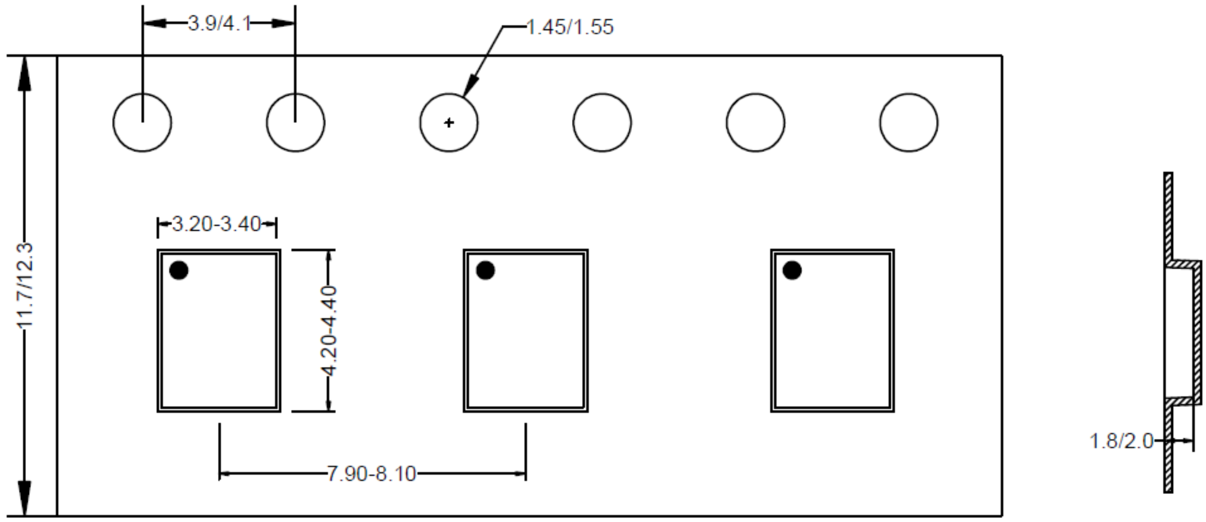


Recommended PCB layout
(Reference only)

Notes: 1. All dimensions are in millimeters and exclude mold flash & metal burr.
2. Center line on drawing refers to module body center.

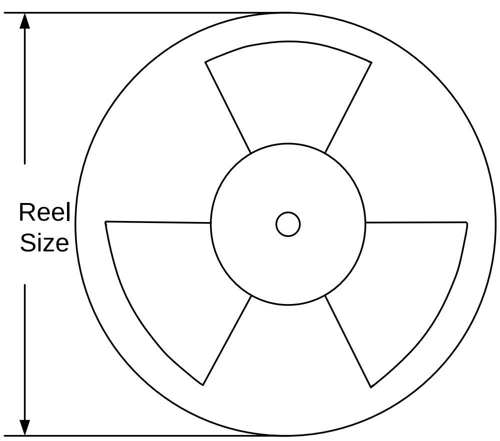
Tape and Reel Specification

QFN3×4 Package Orientation



Feeding Direction

Carrier tape and reel dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	3000

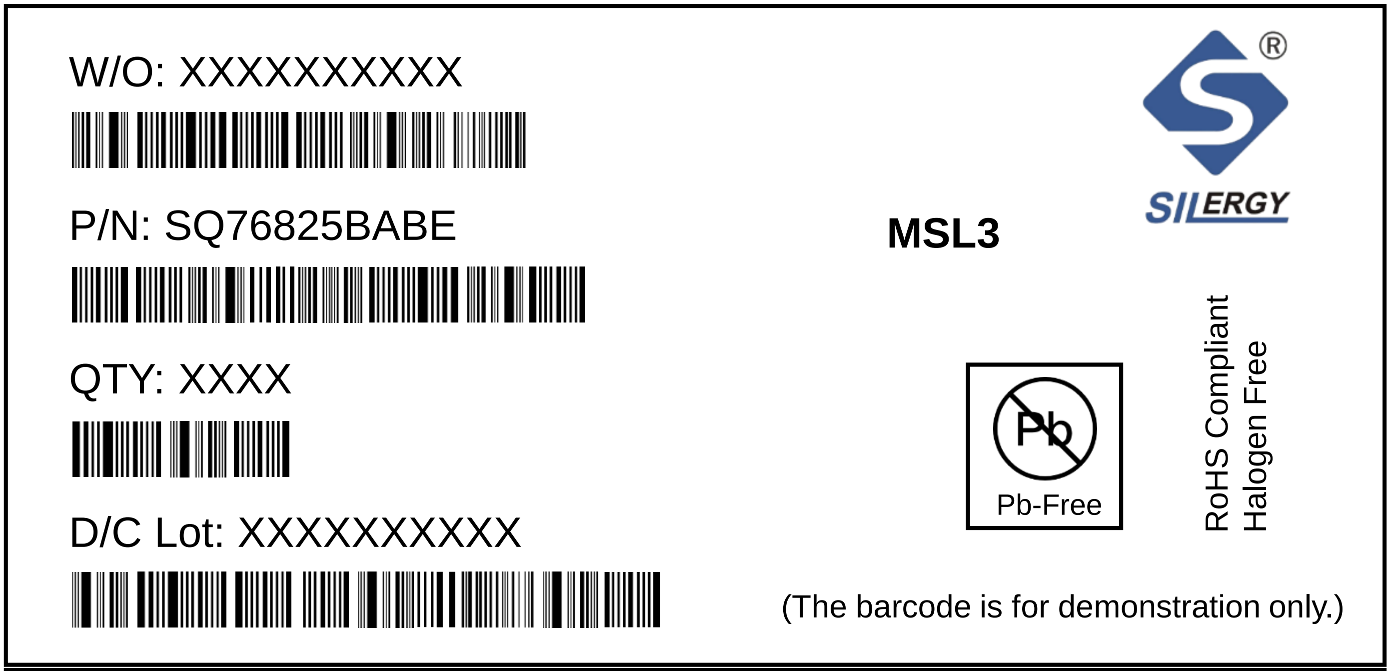
Packaging Information

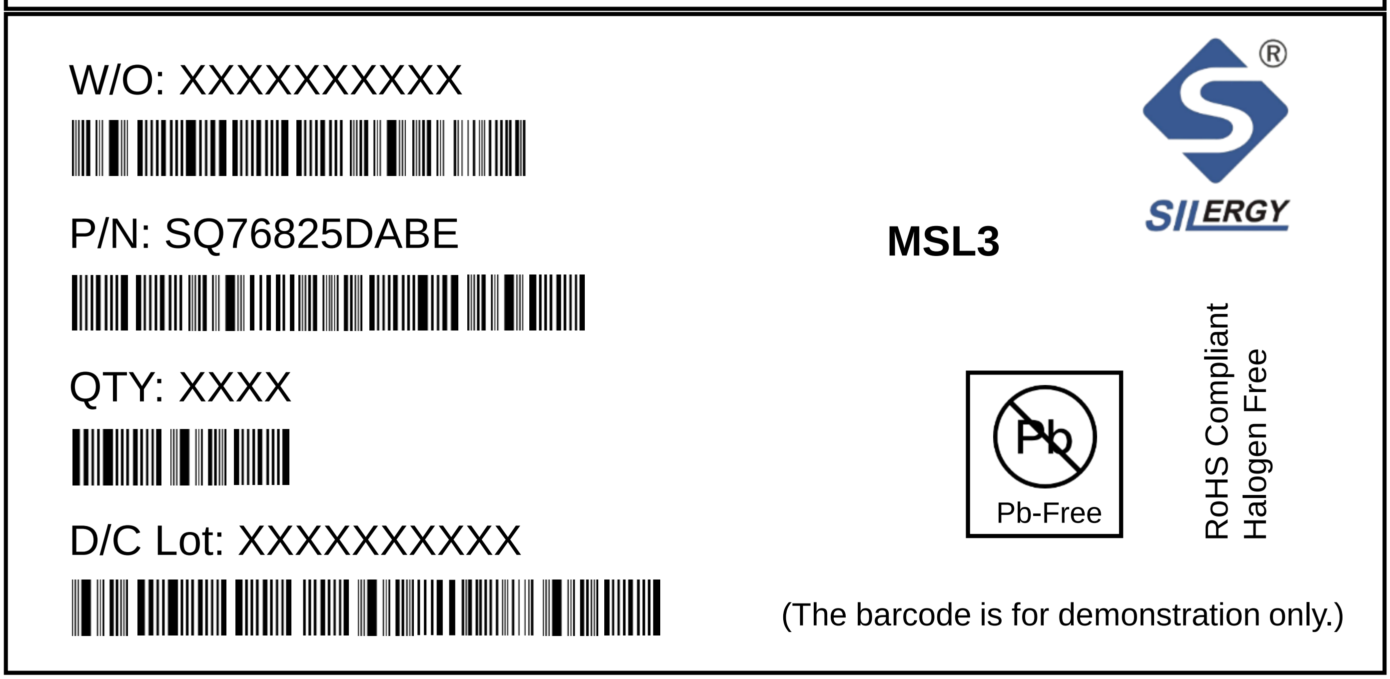
Device Code:

SQ76825BABE: HGK

SQ76825DABE: HAU

Label Information





Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
2023/9/12	0.0	Initial Release
2024/9/12	1.0	Production Release

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