

General Description

The SY205280DXD is an ultra-low capacitance bi-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces.

With a typical capacitance of 0.14pF, the SY205280DXD is designed to protect parasitic-sensitive systems against overvoltage and overcurrent transient events. It complies with IEC61000-4-2 (ESD), ($\pm 12\text{kV}$ air, $\pm 10\text{kV}$ contact discharge), and IEC61000-4-5 (Surge) (3A, 8/20 μs) standards.

The SY205280DXD is available in a DFN0.6x0.3-2 package. Each SY205280DXD device can protect one high-speed data line. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make the SY205280DXD ideal for high-speed data ports and high-frequency line (e.g., USB4 and thunderbolt 4.0) applications. The low clamping voltage of the SY205280DXD ensures minimum stress on the protected device.

Features

- Operating Voltage: 1V and Below
- Transient Protection for High-Speed Data Lines
 - IEC61000-4-2 (ESD) $\pm 12\text{kV}$ (Air) $\pm 10\text{kV}$ (Contact)
 - IEC61000-4-5 (Surge) 3A (8/20 μs)
- Low Capacitance: 0.14pF (Typical)
- Low Leakage Current: 0.01 μA at V_{RWM} (Typical)
- Low Clamping Voltage

Applications

- USB3.x and USB4
- Thunderbolt 4 and 5

Mechanical Characteristics

- DFN0.6x0.3-2 Package
- Marking: Device Code
- Packaging: Tape and Reel

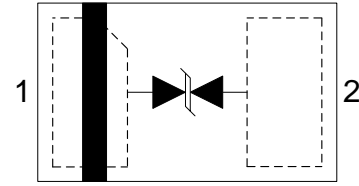
Circuit Diagram



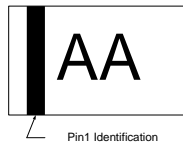
Ordering Information

Pinout (Top View)

Part Number	Package Type	Top Mark
SY205280DXD	DFN0.6x0.3-2	AA



Marking Codes



Note: "AA" is the device code, fixed.

Pin Descriptions

Device Pins	Name	Description
1	Input/Output	IO
2	Input/Output	IO

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Min	Max	Unit
Peak Pulse Current (8/20 μ s)	I_{PP}		3	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	-12	12	kV
ESD per IEC 61000-4-2 (Contact)		-10	10	
Junction Temperature	T_J	-40	+125	$^{\circ}$ C
Storage Temperature	T_{STG}	-55	+150	$^{\circ}$ C

Electrical Characteristics (IO Referenced to IO, $T_A = 25^{\circ}$ C, Note 4)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				1.0	V
Reverse Leakage Current at V_{RWM}	I_R	$V_{RWM} = 1V, T_A = 25^{\circ}$ C		0.01	0.5	μ A
Reverse Breakdown Voltage at I_T	V_{BR}	$I_T = 1mA$	1.4		2.3	V
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 4A, t_p = 10/100ns$		4.5		V
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 8A, t_p = 10/100ns$		6.0		V
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 3A, t_p = 8/20\mu s$		4.5	5.5	V
Dynamic Resistance (Note 2, 5)	R_{DYN}	$t_p = 10/100ns$		0.38		Ω
Insertion Loss (Note 5)	S_{21}	$f = 10GHz$		0.21		dB
Parasitic Capacitance (Note 5)	C_{ESD}	$V_R = 0V, f = 1MHz$		0.14	0.18	pF

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: R_{DYN} calculated based on $I_{PP}=8A$ to $I_{PP}=16A, t_p = 10/100ns$.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ\text{C}$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

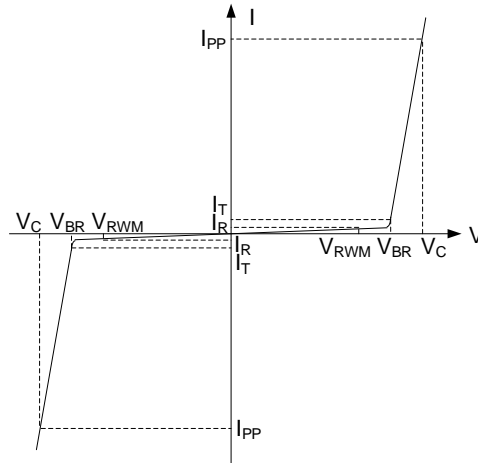
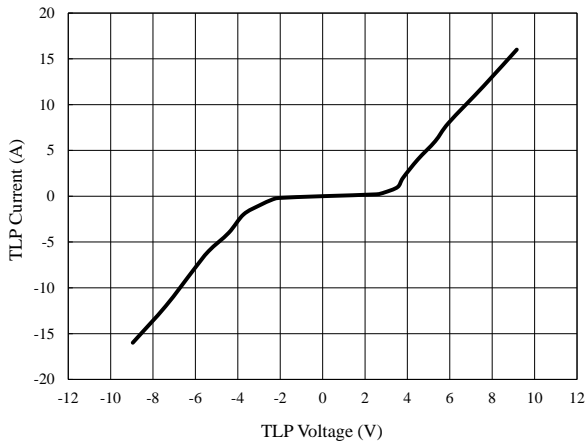


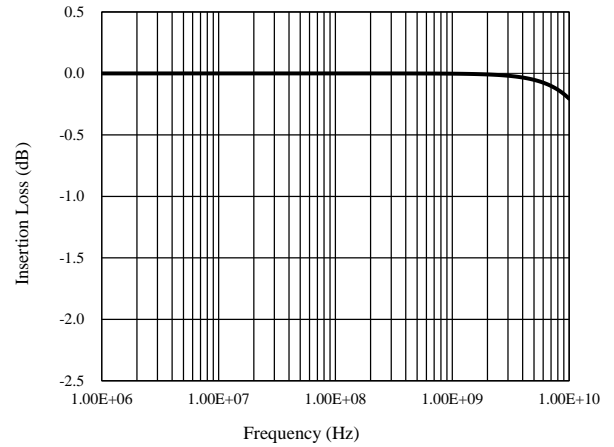
Figure 1. Bi-Directional TVS

Typical Performance Characteristics, Between IO1 and IO2

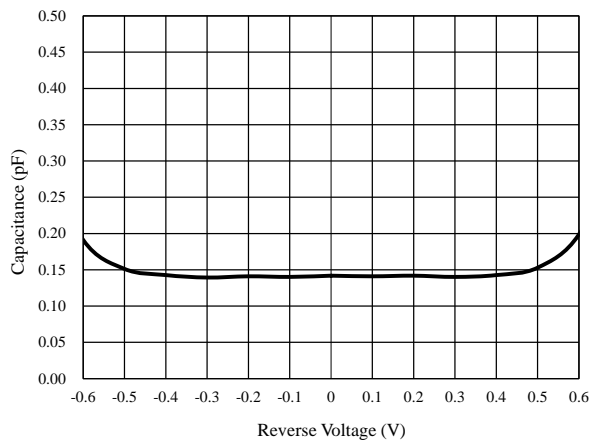
TLP Testing



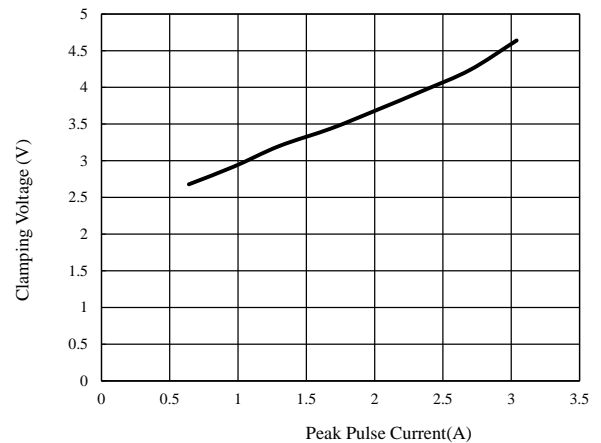
Insertion Loss



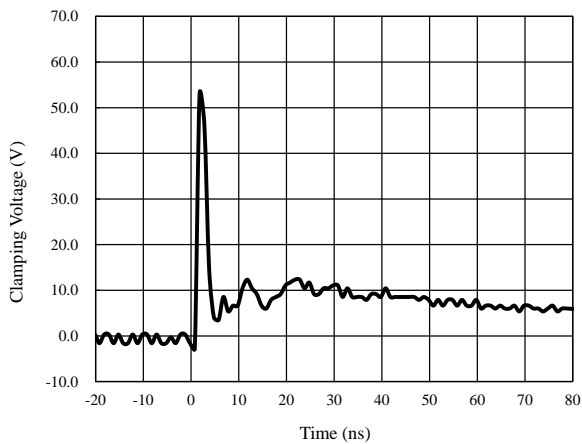
Capacitance vs. Voltage



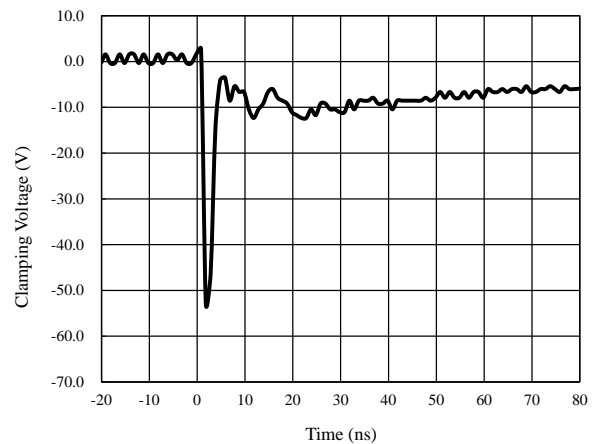
Clamping Voltage vs. Peak Pulse Current



ESD Clamping (+8kV Contact per IEC 61000-4-2)



ESD Clamping (-8kV Contact per IEC 61000-4-2)



Eye Diagram Measurement for Thunderbolt 4.0

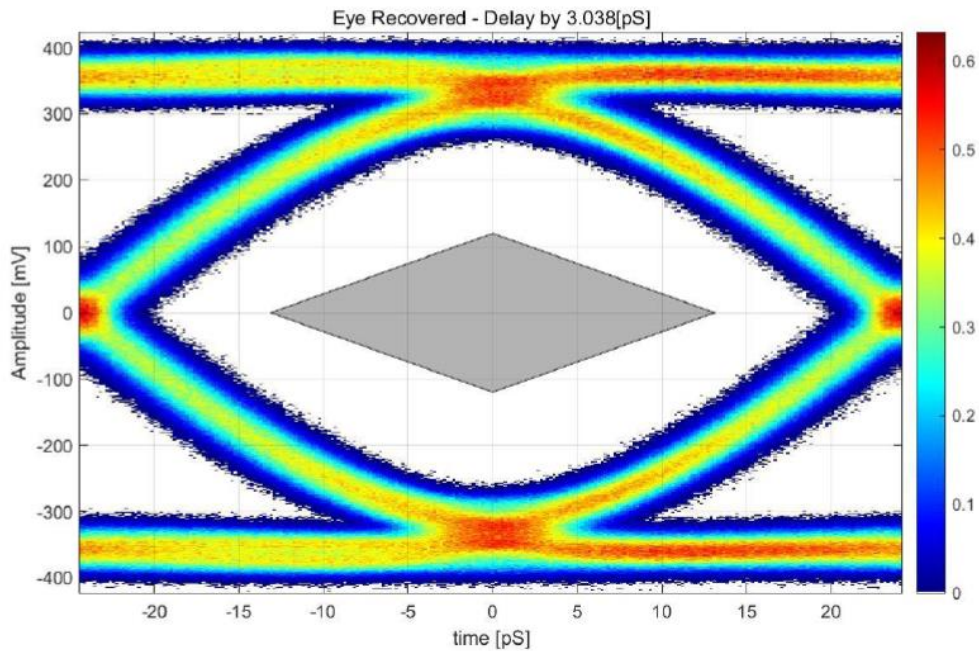


Figure 2. Thunderbolt 4.0 Eye Diagram without SY205280DXD 20.6Gb/s

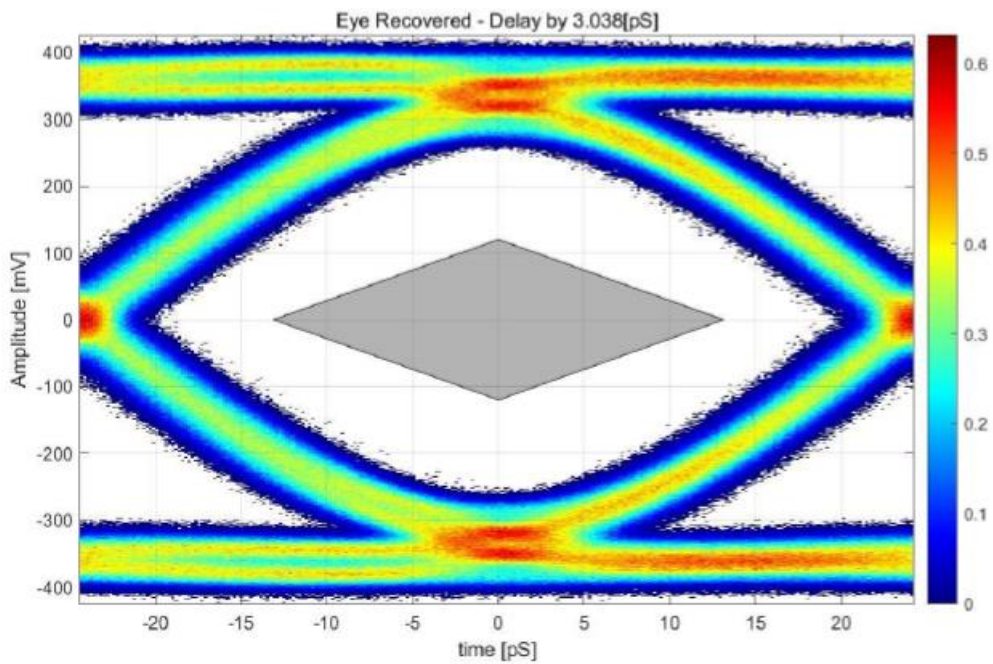


Figure 3. Thunderbolt 4.0 Eye Diagram with SY205280DXD 20.6Gb/s

Application Information

The SY205280DXD protects one bi-directional data line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The pin connections are shown in Figure 2. The protected line is connected at Pin1 while Pin2 is connected to GND, which should connect to a ground plane on the board. All path lengths connected to the pins of the SY205280DXD should be as short as possible to minimize parasitic inductance.

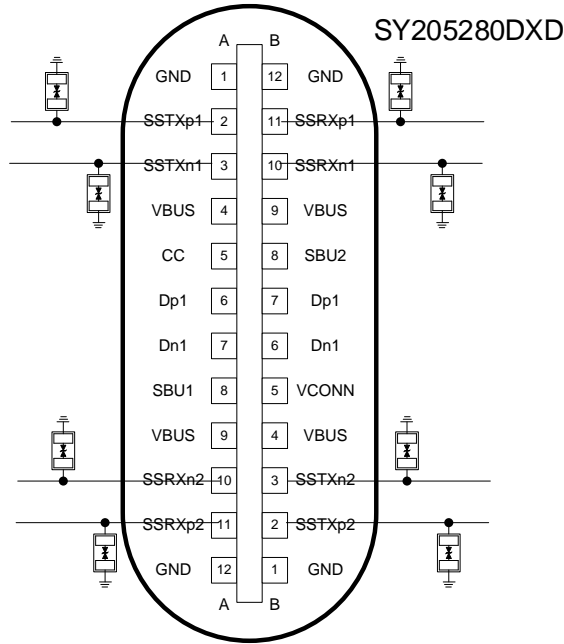


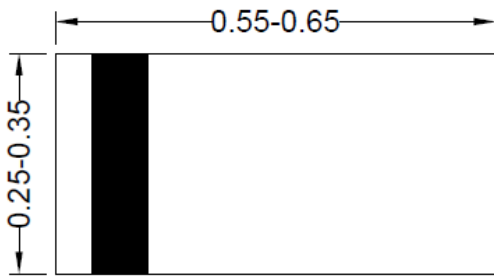
Figure 4. ESD/Surge Protection Circuit

PCB Layout Guidelines

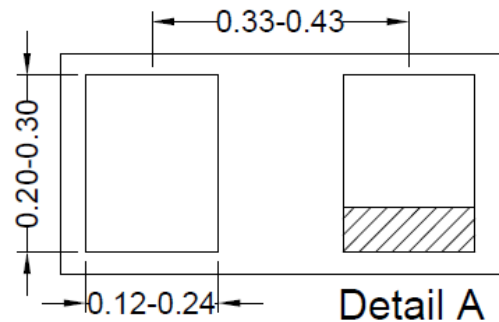
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place the SY205280DXD as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205280DXD pin to the ground.
- Avoid running signals near board edges.
- The SY205280DXD should be placed near the protected line.
- The distance between the SY205280DXD ground pin and the GND reference path should be as short as possible.

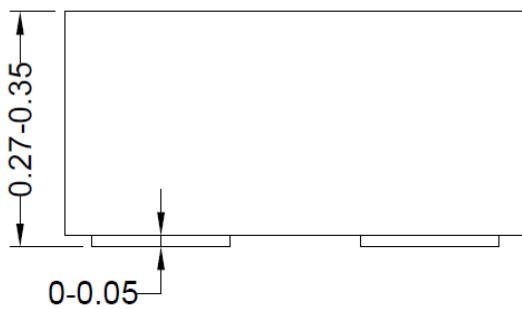
DFN0.6x0.3-2 Package Outline



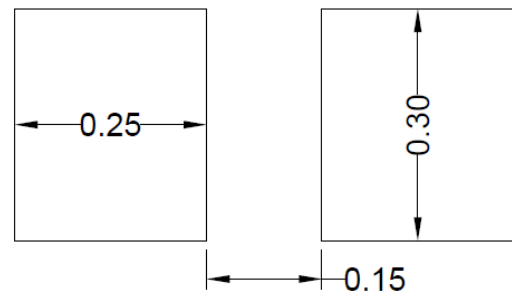
Top View



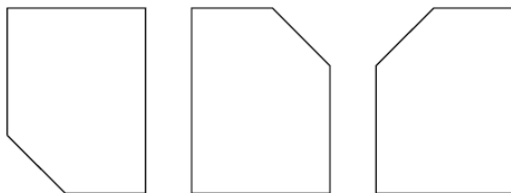
Bottom View



Front View



**Recommended PCB Layout
(Reference Only)**



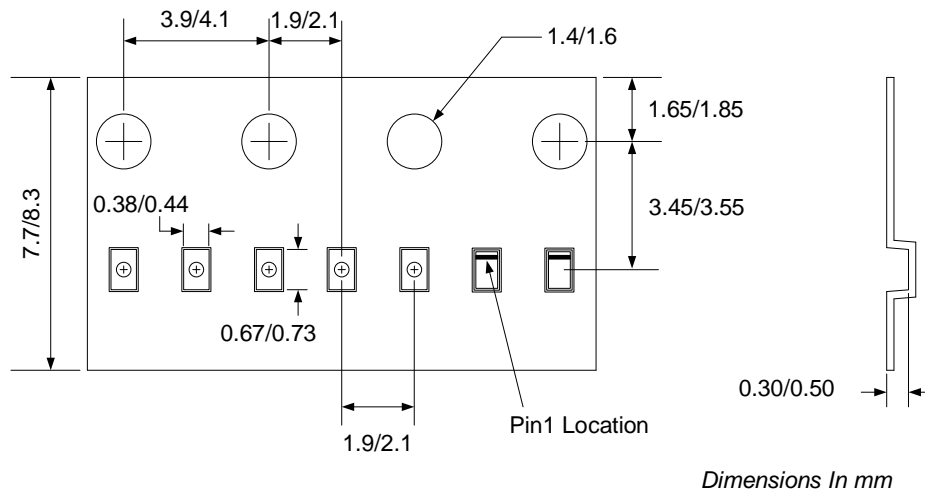
Detail A

Pin1 Identifier: Three Options

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

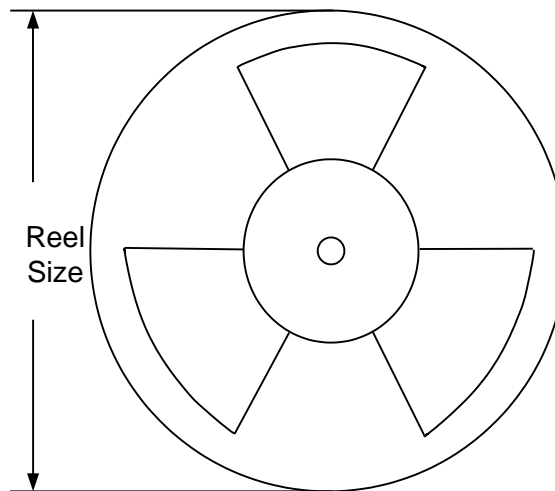
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Feeding direction →

Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN0.6x0.3-2	8	2	7"	10000



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Nov. 29, 2024	Initial Release	

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