SQ81137AS22-J00

Ambient Light Sensor for Industrial Application

General Description

The SQ81137AS22-J00 is an industrial-grade ambient light sensor. It features two photodiode arrays manufactured through different coating processes to sense ambient light. Both channels output ADC counts proportional to external irradiance intensity. The ALS channel, coated to sense visible light, is typically used to calculate the lux level. The CLEAR channel is used for lux calculation compensation, enhancing lux calculation accuracy in various ambient light environments.

The SQ81137AS22-J00 design features high performance, high data uniformity, low data noise, a user-friendly interface, and high reliability. These features make it suitable for industrial applications requiring ambient light sensing.

Features

- Electrical Operation Performance:
  - Power Supply Voltage: 2.5V~3.6V
  - Operation Current: 150μA
  - Shutdown Current: Less Than 10μA
  - Operation Temperature: -40°C to +85°C
- Ambient Light Sensing:
  - ALS Channel with Photopic Coating and CLEAR Channel Without Coating
  - Programmable Gain Settings from 256x to 1x
  - Programmable Integration Time Settings Ranging from 25ms to 800ms
- Programmable Sleep Time Between Two Sequential ADC Cycles for Power-Saving
- High Sensitivity 0.0002 Lux/Count at IT=800ms and Gain=256x
- Measurement Range: 0.0002~107k Lux for ALS Channel
- Hardware Interrupt Pin with Programmable Configuration
- BT Substrate with Transparent Molding Compound
- Package Size: 2.0×2.0×0.6mm^3

Application Schematic

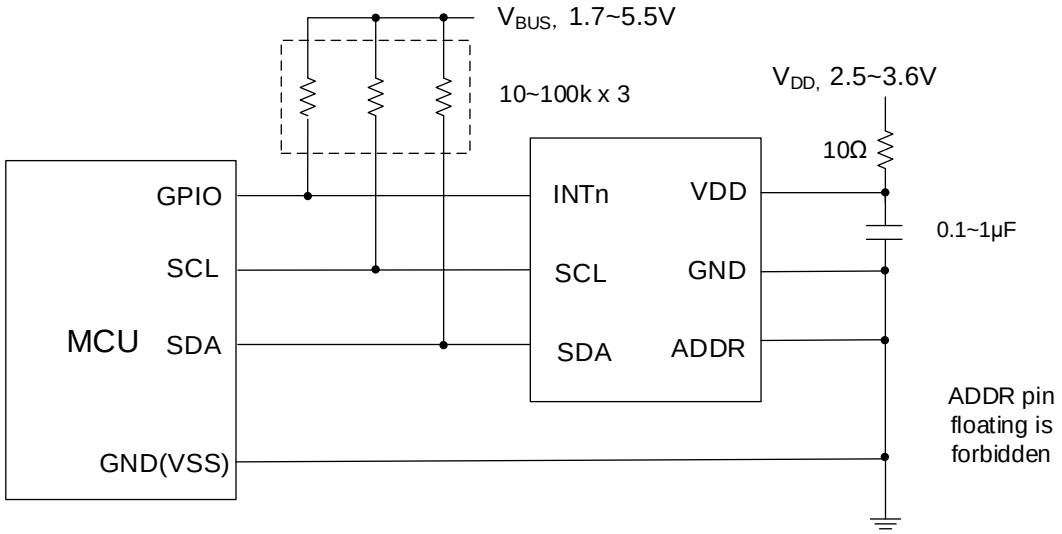
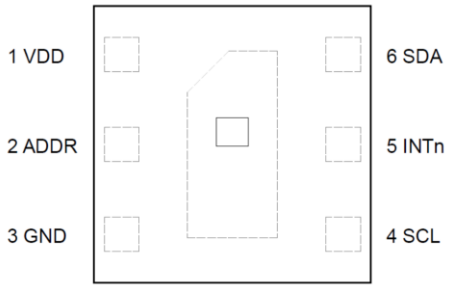


Figure 1. Typical Application Schematic

Ordering Information

Part Number	Package Type	Top Mark	MSL	Delivery Quantity
SQ81137AS22-J00	LGA2×2-6 RoHS-Compliant and Halogen-Free	N/A	3	3000 pcs/reel

Device Pinout (top view)



No.	Pin Name	Pin Description
1	VDD	Positive supply: 2.5V~3.6V.
2	ADDR	Address selection pin. Pulled high for I²C target address 0x45, pulled low for 0x44.
3	GND	Power supply ground. All voltages are referenced to GND.
4	SCL	I²C clock line. The I²C bus lines can be pulled high to a voltage range of 1.7V to 5.5V.
5	INTn	Interrupt output. Open-drain configuration, low-level active.
6	SDA	I²C data line. The I²C bus lines can be pulled high to a voltage range of 1.7V to 5.5V.

Block Diagram

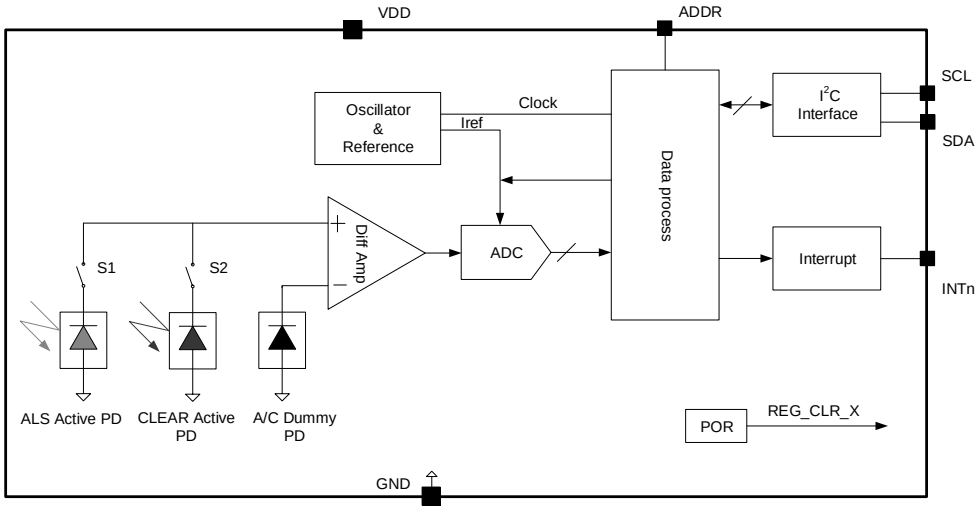


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter (Note 1)	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.3	4	V
I²C Bus Voltage	V_{I^2C}	-0.3	6	
Interrupt Pin Voltage	V_{INTn}	-0.3	6	
I²C Bus Current	I_{I^2C}		10	mA
HBM	ESD	±2000		V
CDM		±500		V
Latch up		±200		mA

Recommended Operating Conditions (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.5	3.6	V
I²C Bus Voltage	V_{I^2C}	1.7	5.5	V
Storage Temperature	T_{STG}	-40	+85	°C
Operating Temperature	T_{OPR}	-40	+85	°C

Electrical and Optical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified) (Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		2.5	3.0	3.6	V
Supply Current When Powered Down	I_{DD_SD}	ALS_EN=0, CLEAR_EN=0	-	-	10	μA
Supply Current When Working	I_{DD_OPE}	ALS_EN=1, CLEAR_EN=1	110	150	190	μA
Supply Voltage Range for I²C Interface	V_{I^2C}		1.7	-	5.5	V
Low Level Input Voltage of SCL and SDA	V_{IL}		-	-	0.55	V
High Level Input Voltage of SCL and SDA	V_{IH}		1.25	-	-	V
SDA Current Sinking Capability	I_{SDA}	V_{OL} = 0.4V	2.7	5	-	mA
Low-Level Output Voltage of SDA	V_{OL}	I_{OL}=4mA	-	-	0.4	V
Input Leakage for SDA, SCL	I_i		-10	-	10	μA
Full Scale of Two Channels	$DATA_{ALS\&CLEAR}$		-	-	65535	counts
Gain Ratio	ALS/CLEAR channel gain ratio	256x/128x	1.8	2.00	2.2	
		128x/64x	1.85	2.05	2.25	
		64x/32x	1.8	2.00	2.2	
ADC Integration Time	IT	ALS_IT1=0	23.5	25	26.5	ms
ALS Channel Output Count	$DATA_{ALS}$	IT=25ms, ALS_GAIN=CLEAR_GAIN= 256x, Ev=200lux, 2700K LED	28125	31250	34375	counts
Clear Channel Output Count	$DATA_{CLEAR}$		3915	4350	4785	
Dark Count of ALS Channel [1]		IT=200ms, ALS_GAIN=256x, Ev=0lux			5	

Note 1: Dark count of ALS channel maximum value is achieved after cancellation by algorithm.

I²C Timing Specifications

(V_{DD} = 3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Clock Frequency	f_{SCL}		-	-	1000	kHz
Capacitance for Each SDA and SCL Pin	C_i		-	-	10	pF
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.26	-	-	µs
Low Period of the SCL Clock	t_{LOW}		0.5	-	-	µs
High Period of the SCL Clock	t_{HIGH}		0.26	-	-	µs
Set-Up Time for a Repeated START Condition	$t_{SU:STA}$		0.26	-	-	µs
Data Hold Time	$t_{HD:DAT}$		0	-	-	ns
Data Set-Up Time	$t_{SU:DAT}$		50	-	-	ns
Set-Up Time for STOP Condition	$t_{SU:STO}$		0.26	-	-	µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		0.5	-	-	µs
Rise Time of Both SDA and SCL	t_R	$R_{pull-up}$ = 10kΩ, C_b = 10pF	-	-	120	ns
Fall Time of SDA and SCL	t_F	$R_{pull-up}$ = 10kΩ, C_b = 10pF	-	-	120	ns
Capacitive Load for Each Bus Line	C_b		-	-	0.55	nF

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c−bus.org/references/.

Note 3: The device is not guaranteed to function outside its recommended operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that T_A @ T_J = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

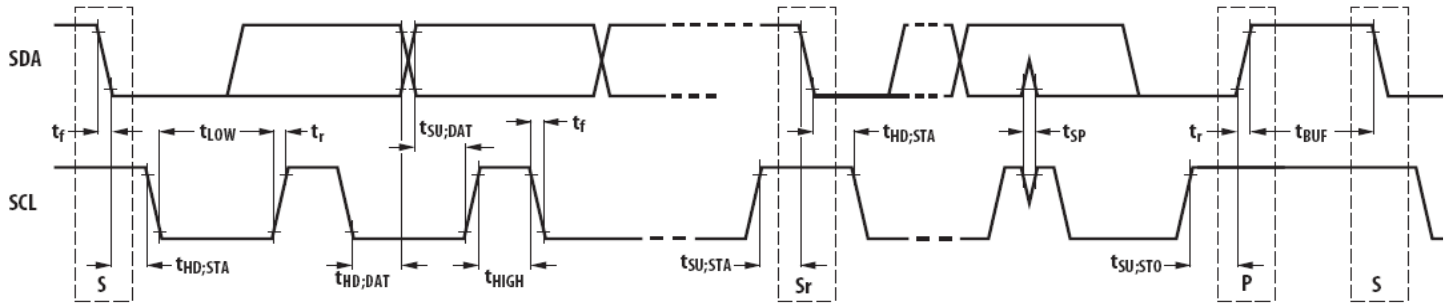
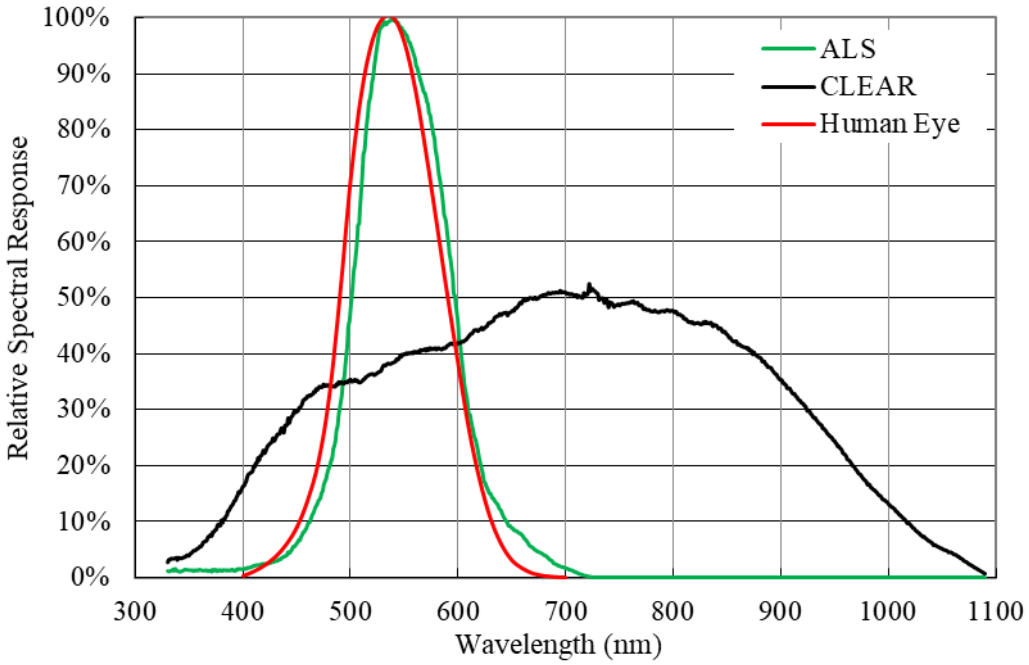


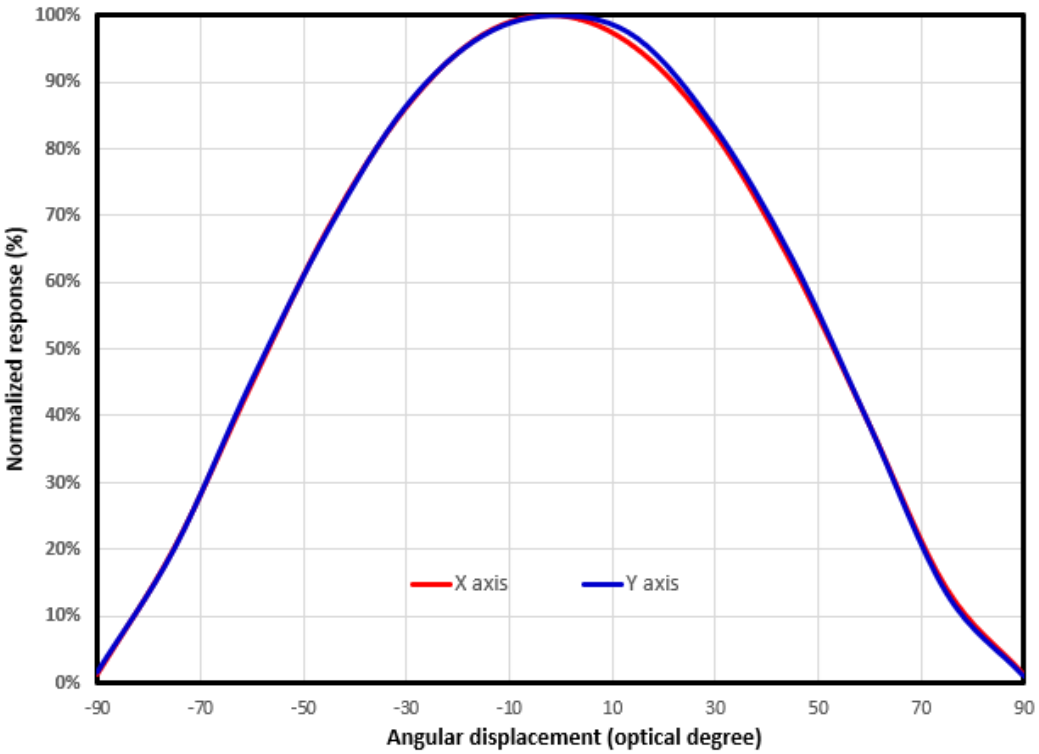
Figure 3. I²C Timing Diagram

Typical Characteristics

Relative Spectral Response



Normalized Output vs. Angular Displacement



Interrupt Function

The SQ81137AS22-J00 provides only a window-type interrupt. This interrupt is governed by the high and low thresholds in registers 0x04 to 0x07. The AINT_FLAG is set when the specific reading (ALS_DATA or CLEAR data, determined by the AINT_SOURCE configuration) exceeds the interrupt high threshold (INT_HTL & INT_HTH) or falls below the interrupt low threshold (INT_LTL & INT_LTH).

To further control when an interrupt occurs, the SQ81137AS22-J00 provides a persistence filter that allows the user to specify the number of consecutive out-of-range ALS readings before an interrupt is asserted. See Figure 4 for details where INT_PRST is set to 0b'000.

If only the above-high-threshold interrupt is required, set the low threshold value 0x0000. If only the below-low-threshold interrupt is required, set the high threshold value 0xFFFF. If no interrupt is required, set the high threshold value 0xFFFF, and the low threshold value 0x0000, which is the default setting.

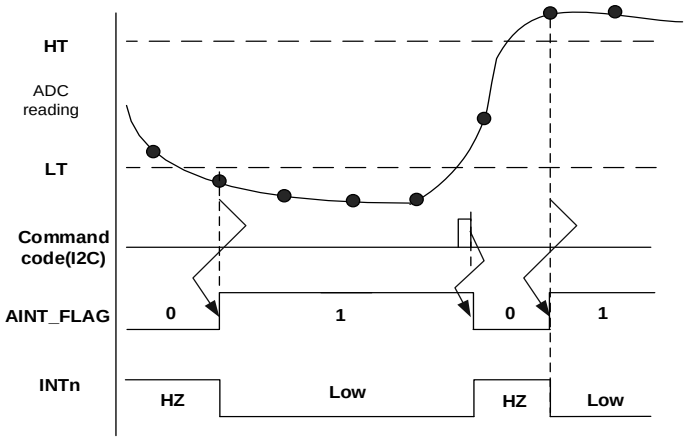


Figure 4. ALS Window Interrupt

Calculating the Ambient Illuminance

The ALS channel data is directly proportional to the illuminance at the surface of the IC. No extra data manipulation is required for normal application where lux accuracy is not strict. The illuminance (lux) can be obtained simply by multiplying ALS data (ALS_DATA) by its corresponding resolution if exposed to ambient light without other optical structure. Please refer to below Table 1 for its sensitivity at different configurations.

Table 1. ALS Sensitivity Table

Integration time(IT) / ms	Sensitivity at specific configuration / lux								
	Gain=256x	128x	64x	32x	16x	8x	4x	1x	Max Detection Range
25	6.4m	12.8m	25.6m	51.2m	102.4m	204.8m	409.6m	1.638	107.372k lux
50	3.2m	6.4m	12.8m	25.6m	51.2m	102.4m	204.8m	819.2m	53.686 klux
100	1.6m	3.2m	6.4m	12.8m	25.6m	51.2m	102.4m	409.6m	26.843 klux
200	0.8m	1.6m	3.2m	6.4m	12.8m	25.6m	51.2m	204.8m	13.421 klux
400	0.4m	0.8m	1.6m	3.2m	6.4m	12.8m	25.6m	102.4m	6710.8 lux
800	0.2m	0.4m	0.8m	1.6m	3.2m	6.4m	12.8m	51.2m	3355.3 lux
Max Detection range	419.4 lux	838.8 lux	1677.6 lux	3355.3 lux	6710.8 lux	13.421 klux	26.843 klux	107.372 klux	

Since SQ81137AS22-J00 is with 16-bit ADC output, its max detection range can be calculated according to below formula:

Range = Sensitivity * 65535 * Gain range * IT range

User can also refer to Table 1 for the calculated detection range based on combination of different gain and integration time settings. For example, the detection range is 53.686 klux if IT is fixed to 50ms and gain setting is flexible where range is calculated as

819.2mlux * 65535=53.686klux

However, in a typical application, the ambient light sensor is packaged or placed behind a window as shown in Figure 5. The transmittance of the sensor window ranges from 80% to 5% or less. To obtain the actual illuminance, the transmittance has to be taken into account for accurate estimation:

ALS_DATA = (Ambient Light in lux) * (Transmittance of Window)/Sensitivity

Example 1

The illuminance where the ambient light sensor is placed is 100 lux, the transmittance of sensor window is 20%, the sensitivity of the ambient light sensor is set at 6.4mlux/counts; the output count of the ambient light sensor is calculated as:

ALS_DATA = Illuminance * Transmittance/Sensitivity = 100 lux * 20%/(0.0064lux/counts) = 3125 counts.

This translates to an overall device sensitivity of 31.25 counts/lux.

Example 2

The illuminance where the ambient light sensor is placed is 100 lux, the transmittance of sensor window is 5% and the resolution of the ambient light sensor is set at 0.8mlux/counts. Under these conditions, the output count of the ambient light sensor is:

ALS_DATA = Illuminance * Transmittance/Sensitivity = 100 lux * 5%/(0.0008lux/counts) = 6250 counts.

This translates to an overall device sensitivity of 62.5 counts/lux.

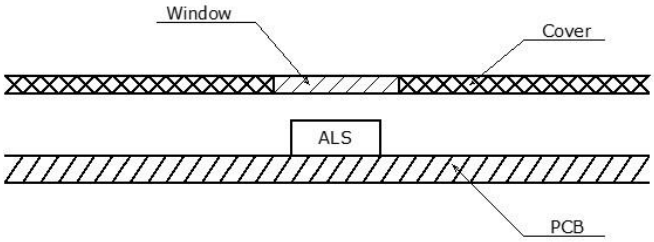


Figure 5. Ambient Light Sensor Mounted Inside an Apparatus

The light attenuation due to air gap between window bottom surface and top surface of sensor was neglected for the above calculations. In actual applications, light attenuation can be induced by window transmittance, air gap, device placement tolerances, etc. A thorough validation using real use case parameters is recommended to confirm the operation and evaluate the device performance and accuracy across all operating conditions.

Layout Considerations

The SQ81137AS22-J00 is designed to reduce the influences of the PCB layout. There are only a few considerations that will ensure best performance. Route the supply and I²C traces as far as possible from all sources of noise. A 0.1μF to 1μF decoupling capacitor needs to be placed as close as possible to the device.

I²C Read / Write Register Data

The SQ81137AS22-J00's I²C target address is 0x44 (7 bits, 0b' 1000100) when the ADDR pin is connected to GND, and 0x45 (7 bits, 0b'1000101) when the ADDR is connected to VDD. Figures 6 and 7 graphically depict the protocol for writing or reading the register data. The first 8-bit data following the write-operation can be either the register address or a special function command code; refer to Table 2 for details.

A : Acknowledge (0)
NA : Not Acknowledged (1)
P : Stop Condition

R : Read (1)
W : Write (0)
S : Start Condition
Sr : Repeat Start
... : Continuation of Protocol
□ : Controller to Target
□ : Target to Controller

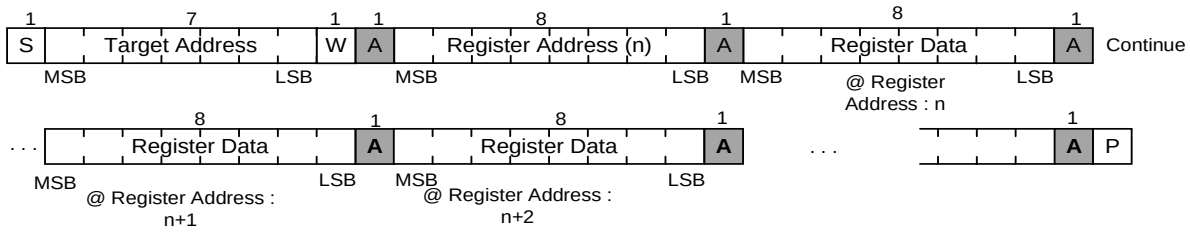


Figure 6. I²C Write-Register-Data Protocol

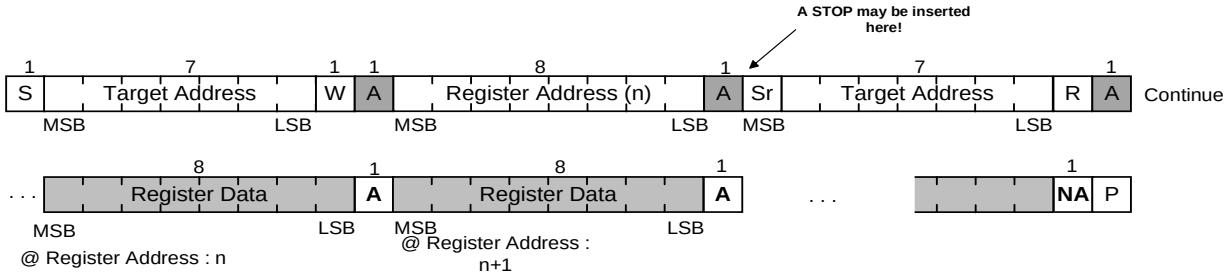


Figure 7. I²C Read-Register-Data Procotol

Register Map

The SQ81137AS22-J00's I²C target address is 0x44 when the ADDR pin is connected to GND and 0x45 when the ADDR pin is connected to VDD.

Table 2. Registers and Register Bits

REG Address	REG Name	Bit								
		7	6	5	4	3	2	1	0	Default
0x00	COM_TEST	Chip ID								0x33
0x01	CON1	ALS_EN	CLEAR_EN	ALS_GAIN[2:0]			CLEAR_GAIN[2:0]			0x00
0x02	CON2	Reserved		SLEEP_TIME[2:0]			IT_TIME[2:0]			0x00
0x03	CON3	Reserved		POWER_ON	AINT_EN	AINT_SOURCE	INT_PRST[2:0]			0x00
0x04	INT_LTL	INT_LT[7:0]								0x00
0x05	INT_LTH	INT_LT[15:8]								0x00
0x06	INT_HTL	INT_HT[7:0]								0xFF
0x07	INT_HTH	INT_HT[15:8]								0xFF
0x08	ALS_DATAL	ALS_DATA[7:0]								0x00
0x09	ALS_DATAH	ALS_DATA[15:8]								0x00
0x0A	CLR_DATAL	CLEAR_DATA[7:0]								0x00
0x0B	CLR_DATAH	CLEAR_DATA[15:8]								0x00
0x0C	FLAG	AINT_FLAG	ALS_DR	CLEAR_DR	Unused					0x00
0x1A	DARK_OFFSET	DARK_OFFSET[3:0]				Unused				0x00

Table 3. Command Code

Bit #	Access	Default	Name	Function / Operation
7:4				0111: special function-used in conjunction with bits 3:0 others: used for register addressing
3:0			Register Address / Special Function Register	Special function: 0100: clears AINT_FLAG flag 0110: clears ALS_DR, CLEAR_DR flags 1010: restart ADC process 1101: set all registers to default value others, these bits are used for register address

For example, the host can clear the AINT_FLAG by issuing the following command: 0x88 0x74 0x00.

Chip ID Register (0x00)

This read-only register contains a fixed data value of 0x33. Read this register through the I²C interface to identify that the device is present, or to verify the communication link.

Table 4. Register 0x01 (CON1) – Configuration 1

Bit #	Access	Default	Name	Function / Operation
7	RW	0x00	ALS_EN	When =0, ALS channel is disabled When =1, ALS channel is enabled
6	RW	0x00	CLEAR_EN	When =0, CLEAR channel is disabled When =1, CLEAR channel is enabled
5:3	RW	0x00	ALS_GAIN [3:0]	For bits 5:3= see the following: 000, gain setting for ALS channel is 256x 001, gain is 128x 010, gain is 64x 011, gain is 32x

				100, gain is 16x 101, gain is 8x, 110, gain is 4x, 111, gain is 1x
2:0	RW	0x00	CLEAR_GAIN [3:0]	For bits 2:0 = see the following: 000, gain setting for CLEAR channel is 256x 001, gain is 128x 010, gain is 64x 011, gain is 32x 100, gain is 16x 101, gain is 8x, 110, gain is 4x, 111, gain is 1x

Table 5. Register 0x02 (CON2) – Configuration 2

Bit #	Access	Default	Name	Function / Operation
7:6	RW	0x00	Reserved	Reserved
5:3	RW	0x00	SLEEP_TIME [2:0]	For bits 5:3 = see the following: 000, no sleep time between two adjacent ADC cycles 001, sleep time of two sequential ADC cycles is 100ms 010, sleep time of two sequential ADC cycles is 200ms 011, sleep time of two sequential ADC cycles is 400ms 100, sleep time of two sequential ADC cycles is 800ms 101, sleep time of two sequential ADC cycles is 1600ms others, reserved
2:0	RW	0x00	IT_TIME [2:0]	For bits 2:0 = see the following: 000, integration times is 25ms 001, integration times is 50ms 010, integration times is 100ms 011, integration times is 200ms 100, integration times is 400ms 101, integration times is 800ms others, reserved

Table 6. Register 0x03 (CON3) – Configuration 3

Bit #	Access	Default	Name	Function / Operation
7:6	RW	0x00	Reserved	Reserved
5	RW	0x00	POWER_ON	When =0, internal bandgap and OSC is disabled When =1, internal bandgap and OSC is enabled in advance
4	RW	0x00	AINT_EN	When =0, interrupt function is disabled When =1, interrupt function is enabled
3	RW	0x00	AINT_SOURCE	When =0, interrupt source is ALS channel data When =1, interrupt source is CLEAR channel data
2:0	RW	0x00	INT_PRST [2:0]	For bits 2:0 = see the following: 000, set interrupt flag if 1 reading trips the threshold value 001, set interrupt flag if 2 readings trip the threshold value 010, set interrupt flag if 4 readings trip the threshold value 011, set interrupt flag if 8 readings trip the threshold value 100, set interrupt flag if 16 readings trip the threshold value 101, every ADC cycle ending generates an interrupt others, reserved

Table 7. Register 0x04 to 0x07– Interrupt Threshold Registers

Addr #	Access	Default	Name	Function / Operation
0x04	RW	0x00	INT_LTL	Lower byte of interrupt low threshold
0x05	RW	0x00	INT_LTH	Upper byte of interrupt low threshold
0x06	RW	0xFF	INT_HTL	Lower byte of interrupt high threshold
0x07	RW	0xFF	INT_HTH	Upper byte of interrupt high threshold

Table 8. Register 0x08 to 0x0B – All Data Registers

Addr #	Access	Default	Name	Function / Operation
0x08	RO	0x00	ALS_DATAL	Lower byte of ALS channel readings
0x09	RO	0x00	ALS_DATAH	Upper byte of ALS channel readings
0x0A	RO	0x00	CLEAR_DATAL	Lower byte of CLEAR channel readings
0x0B	RO	0x00	CLEAR_DATAH	Upper byte of CLEAR channel readings

Table 9. Register 0x0C (INT_FLAG) – Interrupt Flag

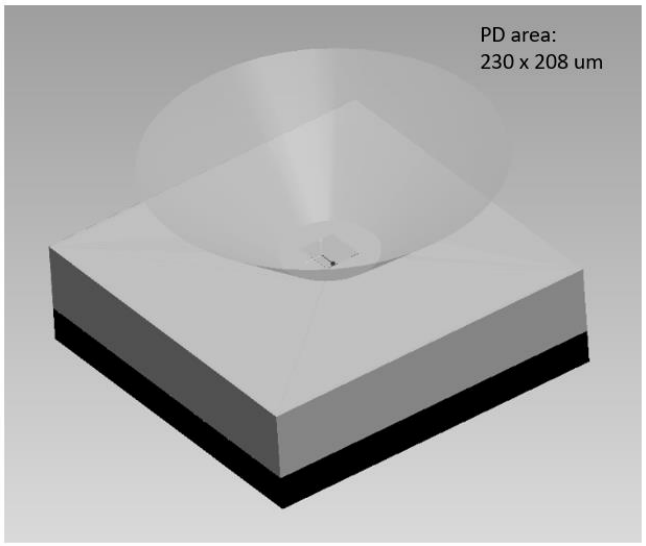
Bit #	Access	Default	Name	Function / Operation
7	RO	0x00	AINT_FLAG	When =0, no ambient light sensing interrupt has occurred since power-on or last “clear” When =1, an ambient light sensing interrupt event occurred. AINT_FLAG can be only cleared by command code. Refer to Table 2 for details.
6	RO	0x00	ALS_DR	When =0, ALS channel data is not updated after enabled or the last data reading When =1, new data is ready after enabled or the last data reading ALS_DR flag is set only when the ALS channel count is available in the corresponding register; when the ALS channel's high byte is read, the ALS_DR is automatically cleared. ALS_DR flag can also be cleared using a command code. Refer to Table 2 for details.
5	RO	0x00	CLEAR_DR	When =0, the CLEAR channel data is not updated after being enabled or after the last data reading When =1, new data is ready after being enabled or after the last data reading The CLEAR_DR flag is set only when the CLEAR channel count is available in the register. When the high byte of the CLEAR channel is read, both the ALS_DR and CLEAR_DR flags are cleared. The CLEAR_DR flag can also be cleared using a command code. Refer to Table 2 for details.
4:0	RO	0x00	Unused	Unused

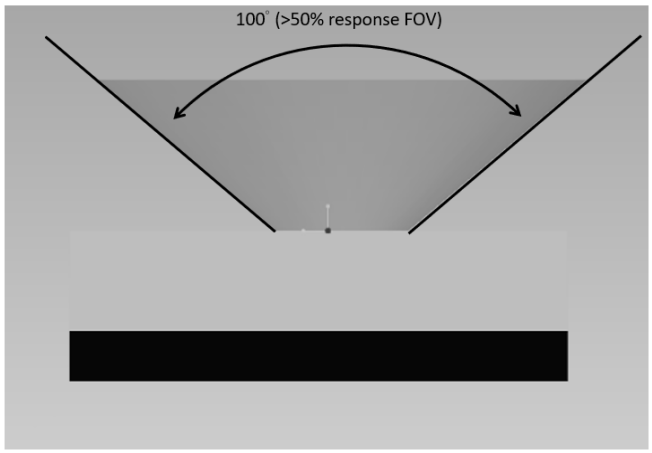
Table 10. Register 0x1A (DARK_OFFSET) – Dark count offset register

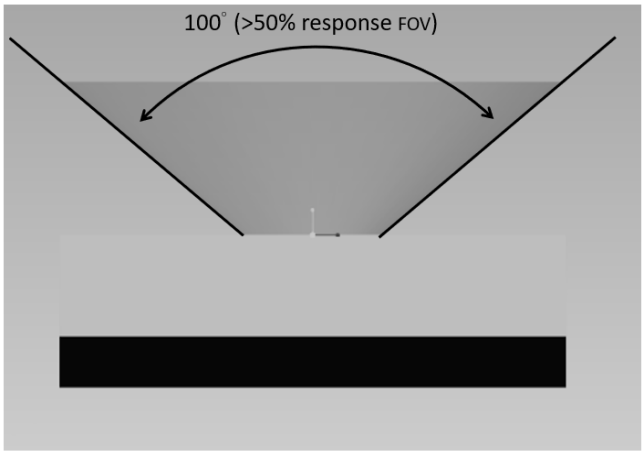
Bit #	Access	Default	Name	Function / Operation
7:4	RO	0x00	DARK_OFFSET[3:0]	Dark count offset value is used for dark count calibration. All ADC raw readings will subtract the offset before used for lux calculation. Dark_Offset = DARK_OFFSET * 3 * (IT_TIME/200) * (ALS_GAIN/256) ADC_data = ADC_raw_data – Dark_Offset where ADC_raw_data is data read through I2C communication, ADC_data is effective data used for lux calculation
3:0	RO	0x00	Unused	Unused

3D Product Drawing

Refer to the following 3D drawing of the SQ81137AS22-J00: ALS and Clear PD (photodiode) FOV (field of view):







Recommended Storage Method

Proper storage measures are recommended as soon as the bag is opened to prevent moisture absorption. The following conditions should be observed if bags are not available:

- Storage temperature: 10°C to 30°C
- Storage humidity: ≦60%RH max.
- Storage Time: ≦168hr max.

Moisture-Proof Package

To avoid moisture absorption by the resin, the product should be stored under the following conditions:

- Temperature: 23 ± 5°C
- Relative humidity: 60% (max)
- Baking is required if the devices have been stored unopened for more than 24 months and the HIC card is not discolored.

ESD Precaution

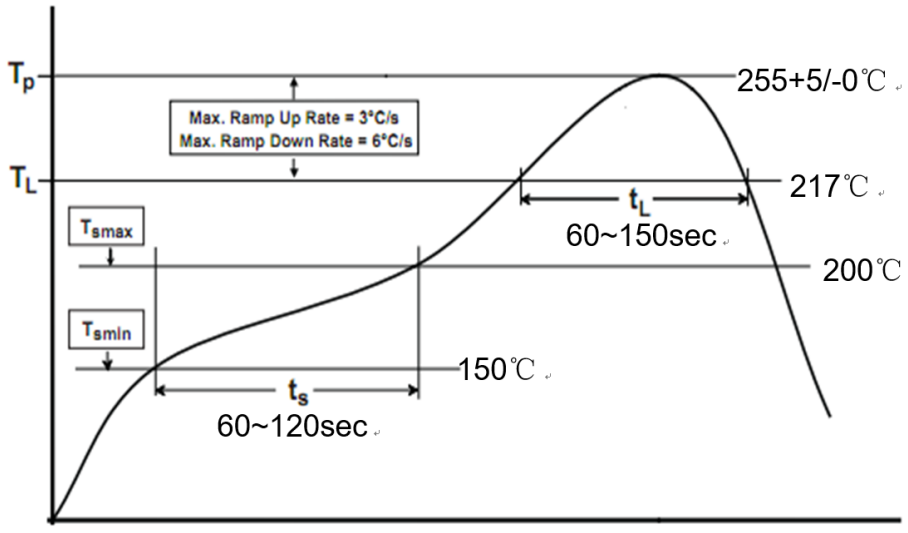
Proper storage and handling procedures should be followed to prevent ESD damage to the devices, especially when removed from the anti-static bag. Electro-Static Sensitive Devices warning labels are on the packing.

Manual Soldering Corrections

Make any necessary soldering corrections manually.

Temperature shall be no more than 350°C (25W for soldering iron) within 3 seconds. Do not do this more than once for any given pin.

Recommended Solder Profile

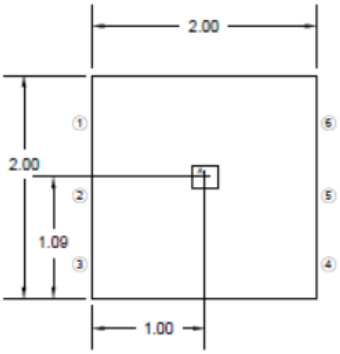


Note 1: Reflow soldering should not be done more than three times.

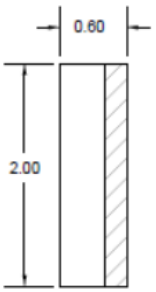
Note 2: Do not put stress on the devices during the heating stage while soldering.

Note 3: Do not warp the circuit board after soldering.

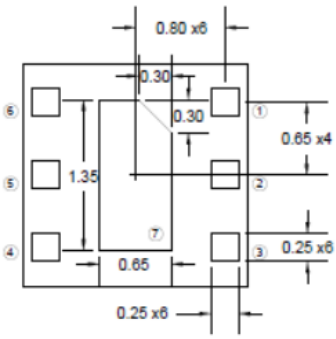
2.0×2.0×0.6mm³ Package Outline Drawings



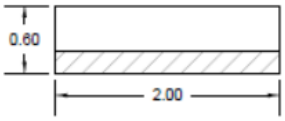
Top View



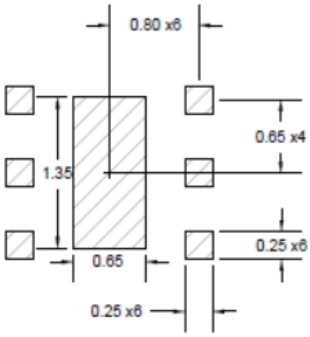
Edge View



Bottom View



Side View



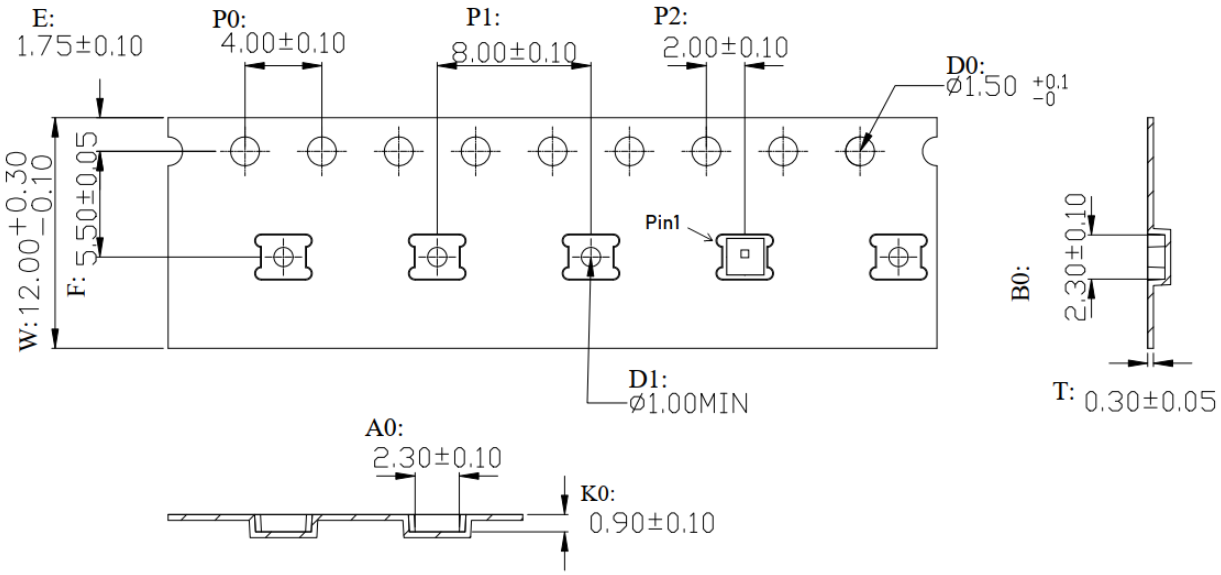
Recommended Land Pattern

Notes:

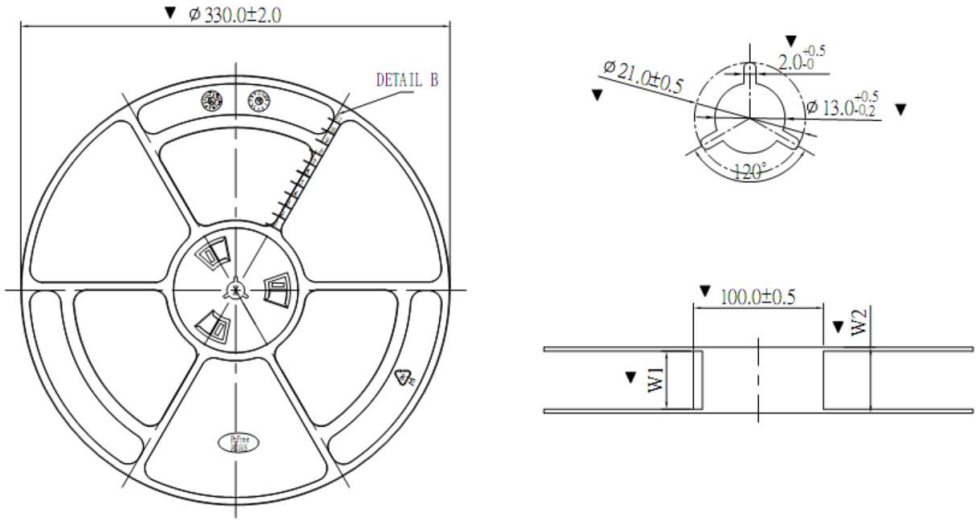
1. *Photodiode sensing area is 230μm x 208μm.*
2. *Photodiode sensing center is at A(x,y) = (1.00, 1.09).*
3. *All dimensions are in millimeters. All tolerances are ±0.1mm unless otherwise noted.*

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation (Units: mm)



Reel Dimensions (Units: mm)



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Dec.23, 2024	Initial Release	
1.0A	May.27, 2025	Revise the typo during Dark_Offset calculation formula at Table 10	11
1.0B	Aug.12, 2025	Based on process performance, update the I2C operating voltage upper value from 3.6V to 5.5V, update the I2C operating voltage maximum value from 4V to 6V.	1,2,3
1.0B1	Oct. 31, 2025	Updated maximum voltage of INTn pin to 6V (the same as that of I2C voltage)	3

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