SYVL927

High Efficiency, 40V Input Single Inductor Synchronous Step Up/Down Regulator

General Description

The SYVL927 is a high voltage synchronous buck-boost converter. The device operates over a wide input voltage range from 4V to 40V. The SYVL927 offers two operational modes, PSM and FCCM, under light load condition. The four-integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SYVL927 features external soft-start, enable control, open drain power good indicator and 1uA shutdown current. The SYVL927 also includes full protection features, such as output over current/short circuit protection, over voltage protection and thermal shutdown for reliable operating.

The device is available in compact QFN5×5-30 package.

Ordering Information

SYVL927 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SYVL927TVA	QFN5×5-30	

Features

- 4V to 40V Input Voltage Range
- 3V to 20V Output Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches: 35mΩ
- External Soft-start Limits the Inrush Current
- 1μA shutdown current
- 7A Internal Switch Peak Current Capability
- Programmable Frequency 200kHz~600kHz
- 1.0V±2% Reference over -40°C to 125°C
- Light Load Operating Mode Selection: PSM or FCCM
- Power Good Indicator
- Hiccup Mode for Output Over Current and Short-circuit
- Output Over Current Protection
- Thermal Shutdown with Auto Recovery
- -40 °C to +125°C Operation
- Compact Package: QFN5×5-30
- Automotive AEC- Q100 Grade 1 Qualified

Applications

- Automotive
- Infotainment
- High-Voltage DC-DC Converters

Typical Application

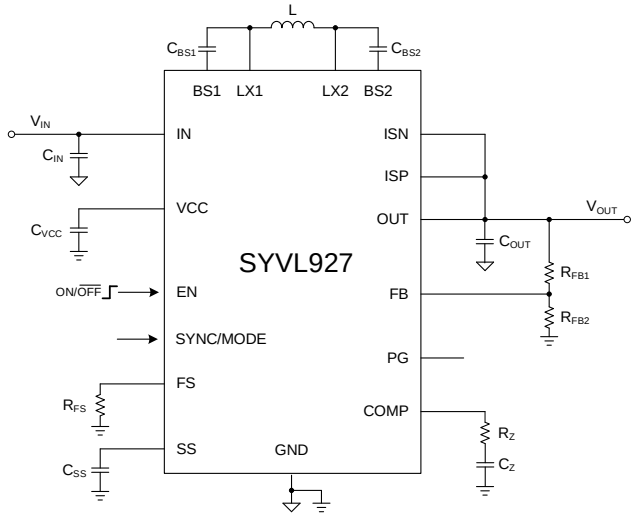


Fig.1a Typical Schematic Diagram (Average Output Current Limit is not used)

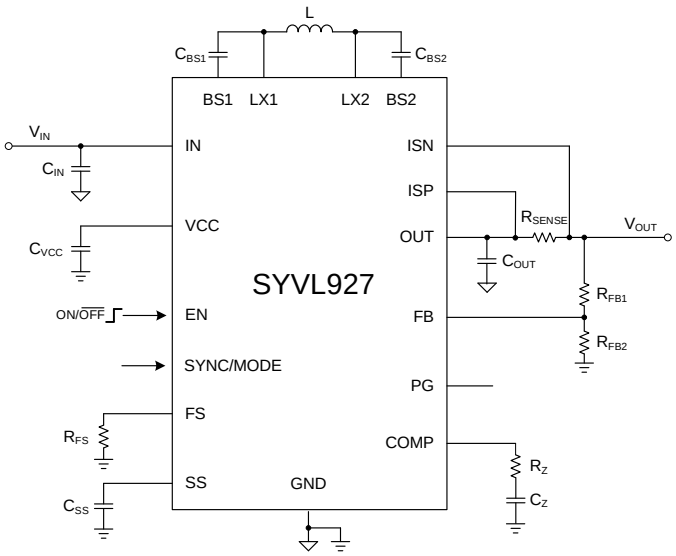
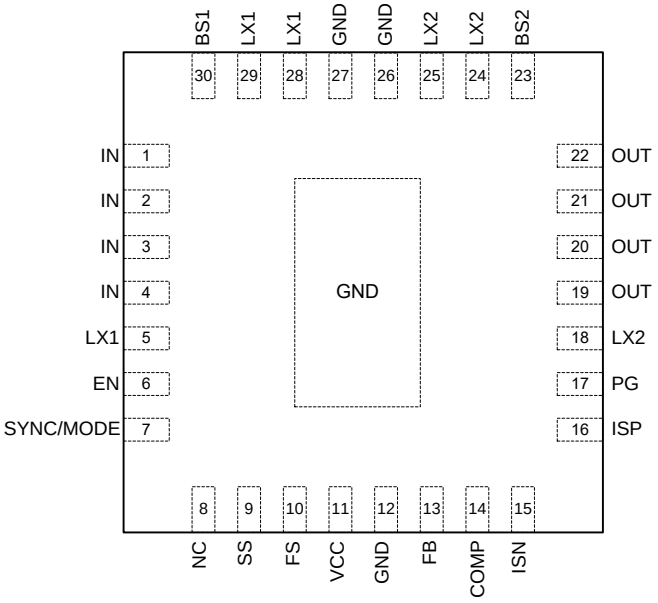


Fig.1b Typical Schematic Diagram (with Average Output Current Limit)

Pinout (Top View)



Top Mark: CBK*xyz* **(**Device code: CBK, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Description
IN	1,2,3,4	Power input pin, decouple this pin to GND with at least a 10μF ceramic capacitor.
LX1	5,28,29	Induction connection 1.
EN	6	Enable control. Pull high to enable the device, pull low to disable the device. Do not leave this pin floating.
SYNC /MODE	7	Sync input or operating mode selection under light load. If connected to GND or open, PSM (Power Saving Mode) operation is enabled. If connected to VCC or external clock, force-PWM operation is enabled. When connected to an external clock, the internal oscillator synchronizes to the external clock. This pin has an internal 1MΩ pull down resistor.
NC	8	No connection.
SS	9	Soft-start pin. Connector a capacitor from this pin to GND to program the soft-start time. Leave this pin open for default 2ms soft-start.
FS	10	Frequency setting pin. Connect a resistor from this pin to GND to program the switching frequency between 200kHz to 600kHz.
VCC	11	Internal 3.3V bias supply. Decouple this pin to GND with a minimum of 1μF ceramic capacitor.
GND	12, 26, 27	Ground pin.
FB	13	Output feedback pin. Connect this pin to the center point of the output resistor divider to adjust the V_{OUT} voltage: $V_{OUT}=V_{REF}\times(1+R_{FB1}/R_{FB2})$
COMP	14	Compensation pin. Connect RC network between this pin and ground.
ISN	15	Negative input of average current sense amplifier. Short to ISP and then connect to OUT if it is not used.
ISP	16	Positive input of average current sense amplifier. Short to ISN and then connect to OUT if it is not used.
PG	17	Power good indicator. Open drain output. Externally pulled high when the output voltage is above 93% of regulation voltage. Pulled low otherwise.
LX2	18,24,25	Induction connection 2.

OUT	19,20,21,22	Power output pin. Decouple this pin to GND with at least a 10μF ceramic capacitor.
BS2	23	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the LX2 pin.
BS1	30	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the LX1 pin.

Block Diagram

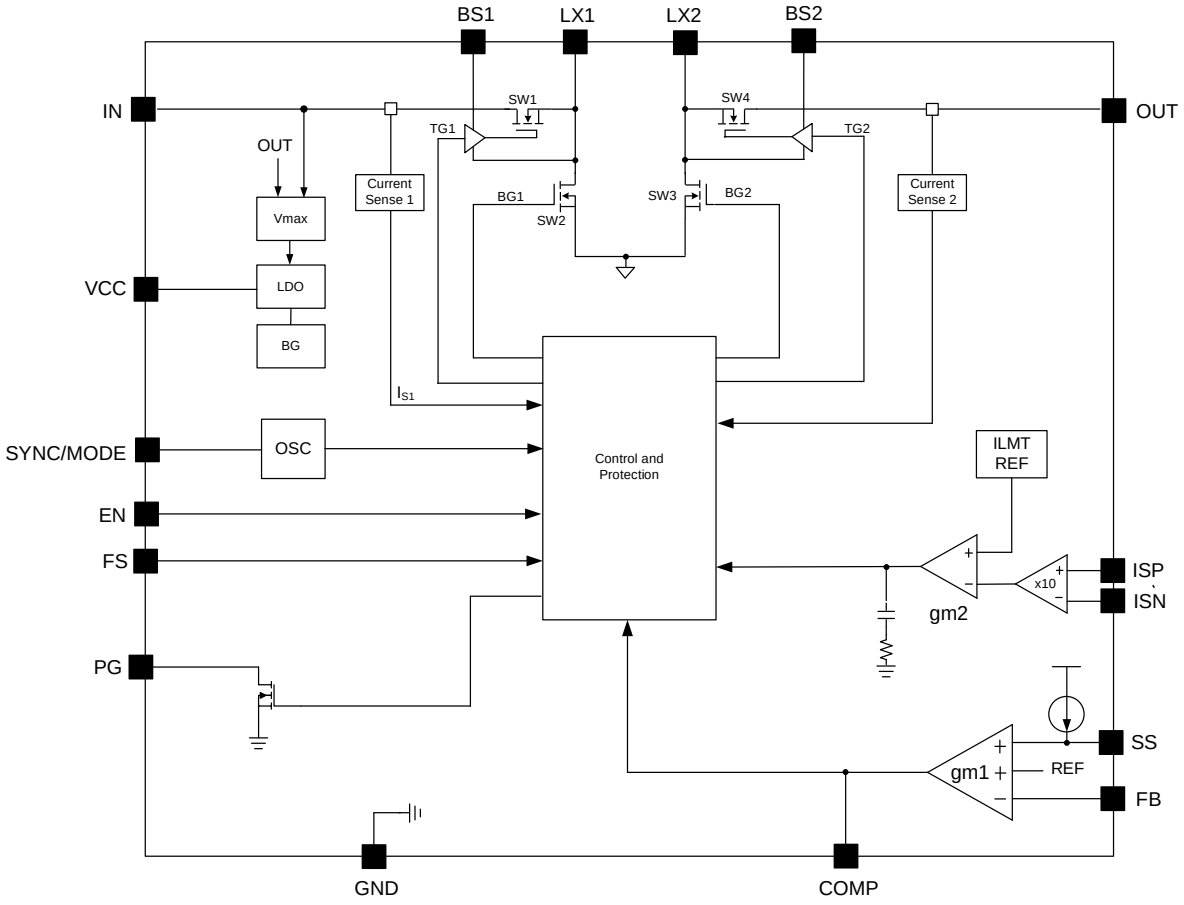


Fig.2 Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX1 ---------- -0.3V to 44V
OUT, LX2 ---------- -0.3V to 28V
ISP, ISN, EN, PG, SYNC/MODE ---------- -0.3V to 44V
COMP, VCC, SS, FB, FS ---------- -0.3V to 4V
BS-LX ---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C, QFN5×5-30 ---------- 3.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 28°C/W
θ_{JC} ---------- 2.8°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Input Voltage Range ---------- 4V to 40V
Output Voltage Range ---------- 3V to 20V
Ambient Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = -40°C~125°C, unless otherwise specified, the values are guaranteed by test design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		40	V
Input UVLO Threshold	V_{UVLO}		3.3		3.9	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
LDO Output Voltage	V_{LDO}	V_{IN}=12V, No Load	3.18	3.3	3.4	V
LDO Output Current Limit	$I_{LMT,LDO}$	CCM	30		110	mA
Quiescent Current	I_Q	No switching		200	260	μA
Shutdown Current	I_{SHDN}	EN=0, T_A = T_J = 25°C			1	μA
		EN=0, T_A = T_J = -40°C to 125°C			5	μA
Feedback Reference Voltage	V_{REF}	T_A = T_J = 25°C, internal reference	0.99	1	1.01	V
		T_A = T_J = -40°C to 125°C, internal reference	0.98	1	1.02	V
FB Input Current	I_{FB}	V_{FB}=1V	-50		50	nA
Internal FET R_{ON}	$R_{DS(ON)}$			35		mΩ
Peak Inductor Current Limitation	$I_{PK,LMT}$		6		8.5	A
Reverse Inductor Current Limitation	I_{NEG}	Force-PWM	-2		-5.5	A
Zero Current Detection Threshold	I_{ZERO}	PSM			500	mA
EN Rising Threshold	$V_{EN,R}$		1.1	1.2	1.3	V
EN Falling Threshold	$V_{EN,F}$		0.8	0.9	1	V
Internal Soft-start Time	t_{SS}	SS pin floating	0.7	1.6	3.2	ms
Soft-start Charging Current	I_{SS}		4	5	6	μA
Soft-start Done Threshold	V_{SS}			1		V
Switching Frequency Program Range	$f_{SW,RNG}$	R_{FS}=82.5k~300k	200		600	kHz
Switching Frequency Setting Accuracy	f_{SW}	R_{FS}=100kΩ, T_A = T_J = 25°C	450	500	550	kHz
		R_{FS}=100kΩ, T_A = T_J = -40°C to 125°C	425	500	575	kHz
Minimum ON Time	$t_{ON,MIN}$			70	100	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum OFF Time	$t_{OFF,MIN}$			70	100	ns
Clock Sync Input Voltage High	$V_{SYNC,H}$		1.5			V
Clock Sync Input Voltage Low	$V_{SYNC,L}$				0.8	V
Clock Sync Input Duty	D_{CLK}		20		80	%
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low	88	91	94	$\%V_{REF}$
		V_{FB} rising, PG from low to high	90	93	96	$\%V_{REF}$
Power Good Delay Time	$t_{PG,R}$	Low to high		200		μs
	$t_{PG,F}$	High to low		20		μs
Power Good Output Low	$V_{PG,L}$	I_{PG}=2mA			0.3	V
OUT Pin Over Voltage Protection Threshold	$V_{OUT,OVP1}$		22		28	V
Output Over Voltage Protection Threshold	$V_{OUT,OVP2}$	V_{FB} rising	115	120	125	$\%V_{REF}$
Output OVP Delay	$t_{OVP,DLY}$			15		μs
Output Under Voltage Protection Threshold	V_{UVP}	V_{FB} falling	40	50	60	$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			200		μs
Thermal Shutdown Temperature	T_{SD}		150	160	170	°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Average Current Regulation Range	$V_{ISP} - V_{ISN}$			50		mV

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

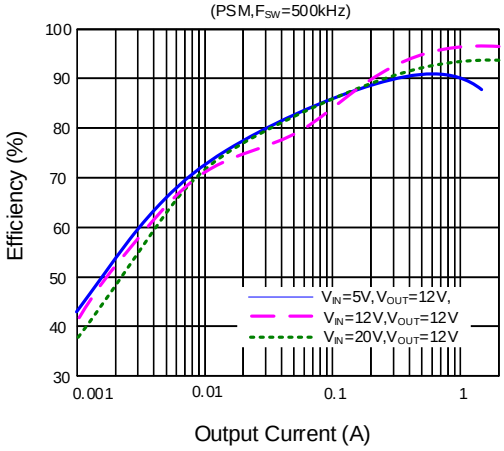
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

Efficiency vs. Output Current

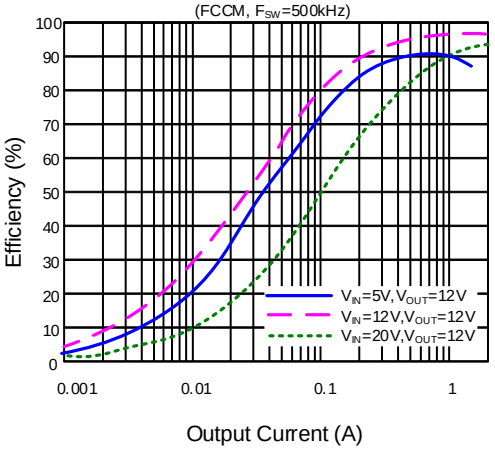
(PSM,F_{SW}=500kHz)



Output Current (A)

Efficiency vs. Output Current

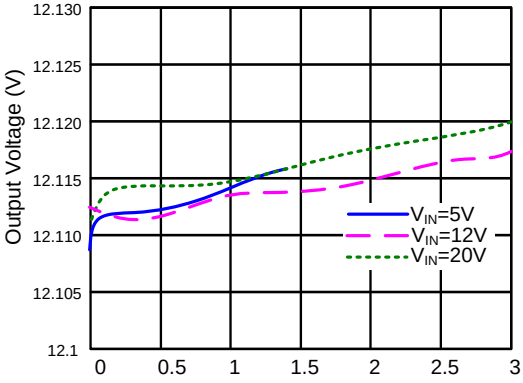
(FCCM, F_{SW}=500kHz)



Output Current (A)

Output Voltage vs Output Current

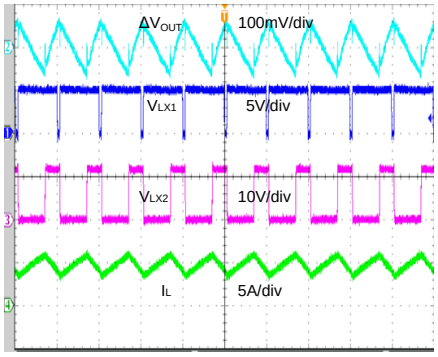
(F_{SW}=500kHz)



Output Current (A)

Output Ripple

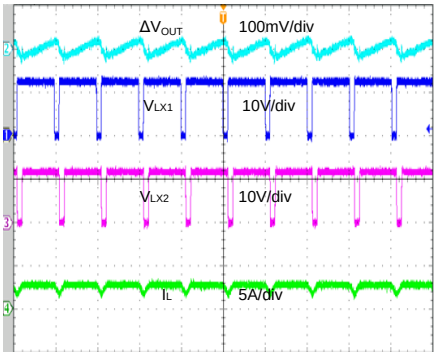
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}= 1.5A)



Time (2μs/div)

Output Ripple

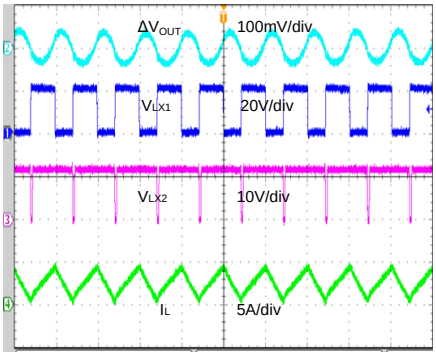
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 2A)



Time (2μs/div)

Output Ripple

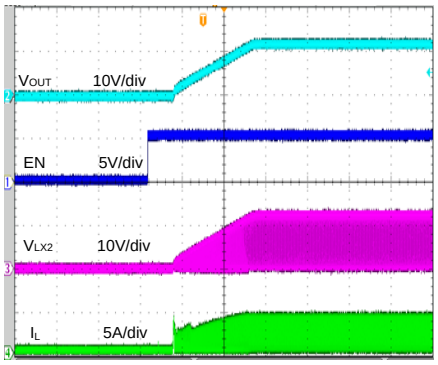
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 2A)



Time (2μs/div)

Startup from Enable

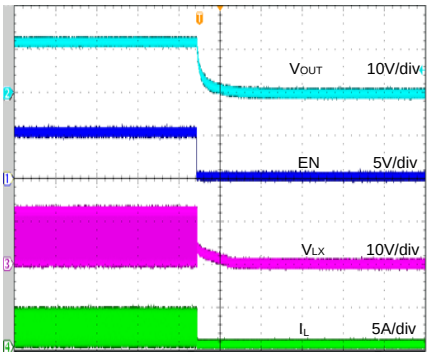
(V_{IN}=20V, V_{OUT}=12V, R_{Load}=6Ω)



Time (800us/div)

Shutdown from Enable

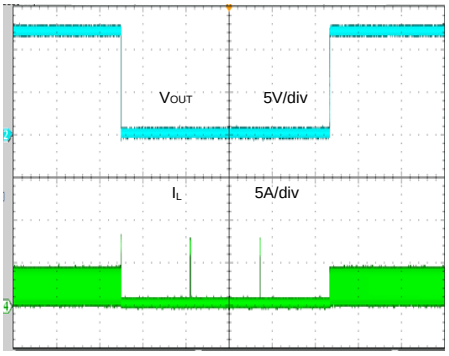
(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)



Time (800μs/div)

Short Circuit Protection

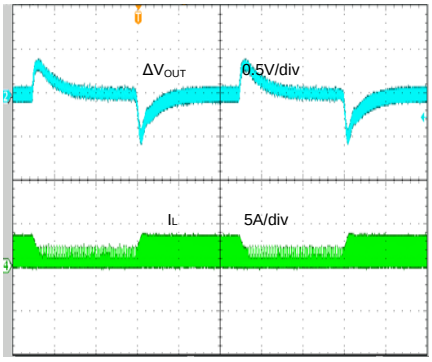
(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)



Time (2s/div)

Load Transient

(V_{IN}=20V, V_{OUT}=12V, I_{OUT}=0.1A ~ 1A)



Time (200μs/div)

Application Information

Input Under-voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches may be sufficiently enhanced, the IC incorporates input under-voltage lock-out (UVLO) protection. The device remains in a low current state and all switching is inhibited until V_{IN} exceeds V_{UVLO}, the input UVLO (rising) threshold. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} less the UVLO hysteresis, switching will be suppressed again.

Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1.3V normal device operation will be enabled. When driven < 0.8V the device will be shut down, reducing input current to < 1uA. In applications where EN is pulled high to the power input V_{IN}, a 10kΩ to 100kΩ resistor should be added between power input and EN.

Soft-start

The SYVL927 provides an external soft-start pin to smoothly ramp the output to the desired voltage whenever the device enabled. The soft-start time can be programmed by external capacitor connected between SS pin and GND, as given in equation (1).

$$t_{ss}(\text{ms}) = C_{SS}(nF) \times \frac{1V}{5uA} \quad (1)$$

Leave SS pin open for default 1.6ms soft-start.

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 100nF low ESR ceramic capacitor to be connected between BS1 and LX1, BS2 and LX2. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel power MOSFET switch.

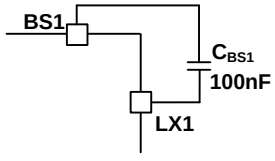


Fig. 3. External Bootstrap Capacitor Connection

VCC Linear Regulator

An internal linear regulator (VCC) produces a 3.3V supply from VIN that powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a minimum of 1μF low ESR ceramic capacitor from VCC to GND.

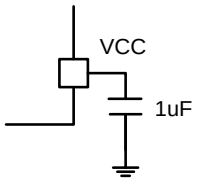


Fig. 4. VCC Regulator

Feedback resistor selection

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10kΩ and 100kΩ is highly recommended for both resistors. The output voltage VOUT is programmed by external voltage divider with the 1V internal voltage reference as given in equation (2).

$$V_{OUT} = 1V \times \frac{R_1 + R_2}{R_2} \quad (2)$$

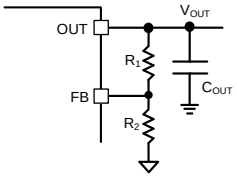


Fig. 5. V_{OUT} Programming

Light Load Operation Mode

PSM or force-PWM light load operation is selected by SYNC/MODE pin. Pull SYNC/MODE pin low or floating for PSM operation, and connect this pin to VCC or external clock for force-PWM operation.

Adjustable Switching Frequency and Synchronization

The FS pin can be used to set the switching frequency of the device by connecting a resistor R_{FS} between this pin and GND. The switching frequency is programmable from 200kHz to 600kHz, as given in equation (3). The switching frequency can also be synchronized to external clock by applying a clock signal to SYNC/MODE pin.

$$F_S(kHz) = \frac{50000}{R_{FS}(k\Omega)} \quad (3)$$

Fault Protection modes

Peak Inductor Current Limit

The device incorporates a cycle-by-cycle "peak" current limit. Inductor current is measured in SW1 when it is on. If the current exceeds the current limit, both SW1 and SW3 turn off, and SW2 and SW4 turn on.

The device incorporates reverse inductor current limit under force-PWM mode. Inductor current is measured in SW4 when it is on. If the reverse current exceeds the current limit, both SW2 and SW4 turn off, and SW1 and SW3 turn on.

Average Output Current Limit

The SYVL927 provides a function for output current limit by sensing the voltage drop between ISP pin and ISN pin (as shown in fig.1b). Once the differential voltage on R_{SENSE} exceeds the voltage threshold, the internal current control loop will regulate the output current by decreasing duty cycle until UVP or OTP is triggered. Short the ISP to ISN and then connect to OUT pin if this function is not used.

Short-circuit protection

If V_{OUT} < ~50% of the set point and the device is in current limit (peak inductor current) continuously for approximately 200μs, the short-circuit protection mode will be initiated, and the device will shut down for approximately 2.6s. The device will then restart with a complete soft-start cycle. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the UVP threshold is reached.

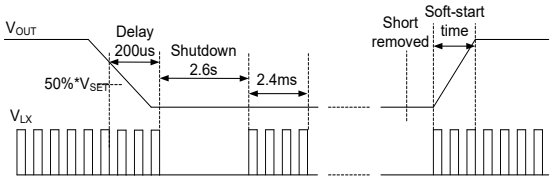


Fig. 6. Description of Short-circuit Protection

Output Over-voltage protection (OVP)

This device includes output over-voltage protection (OVP). If the output voltage rises above the feedback regulation level, SW1 and SW3 turn off and the synchronous rectifier turns on. If the output voltage remains high the SW2 and SW4 remain on until the inductor current reaches zero. If the output voltage continues to rise and exceeds the output over- voltage threshold for more the 10μs, the output over-voltage protection mode is triggered. The device resumes regulation once the overvoltage condition is removed.

Over-temperature Protection (OTP)

SYVL927 includes over-temperature protection (OTP) circuitry to prevent over heating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 15°C the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Layout Design

For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, C_{VCC} , C_{OUT}, C_{BS} , L, R_{TOP} and R_{BOT}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) The decoupling capacitor of VIN must be placed close enough to the IN pin and GND pin. The loop area formed by the input capacitors, IN pin and GND pins must be minimized.

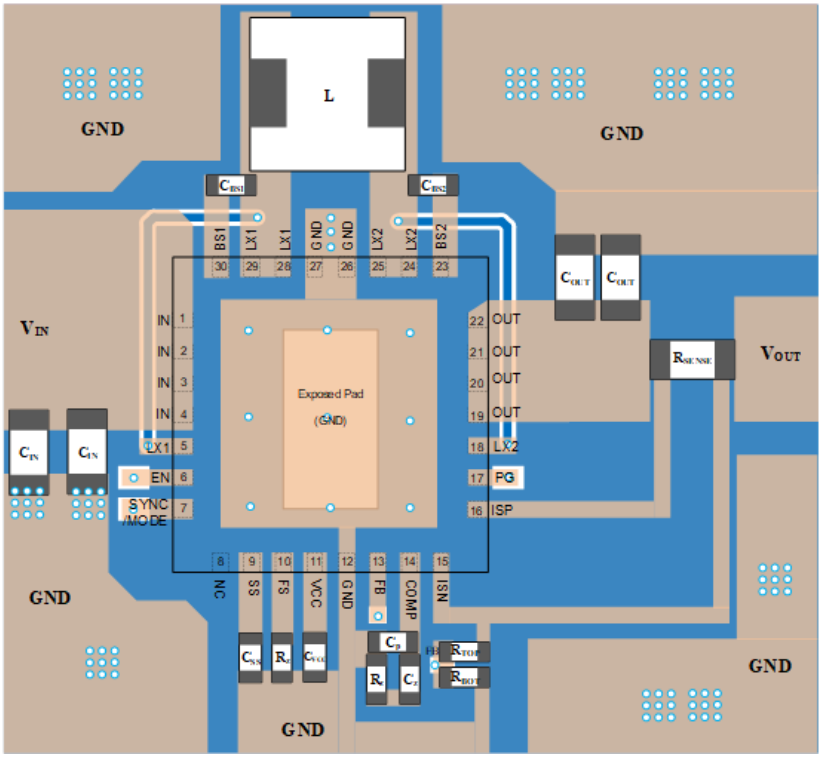
3) The decoupling capacitor of VOUT also must be placed close enough to the OUT pin and GND pin. The loop area formed by the output capacitors, OUT pin and GND pins also must be minimized.

4) BS pin is sensitive. Bootstrap cap must be placed between BS and LX as close as possible.

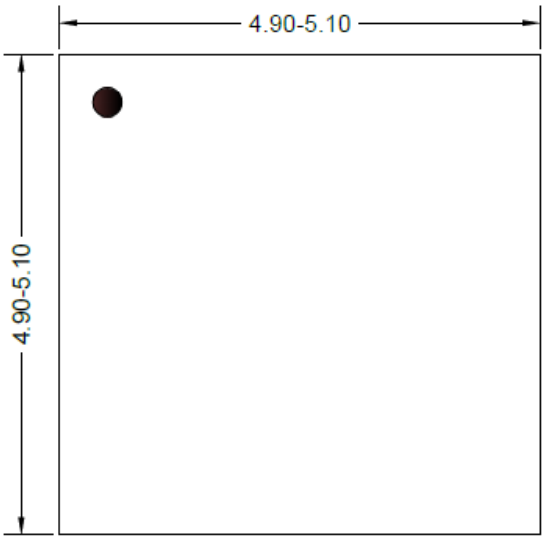
5) To prevent the circulating currents in the ground plane from disrupting operation of the regulator, all small-signal grounds should return to GND by a separation way. This main includes the ground connection for the FB pin resistor and the feedback network.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

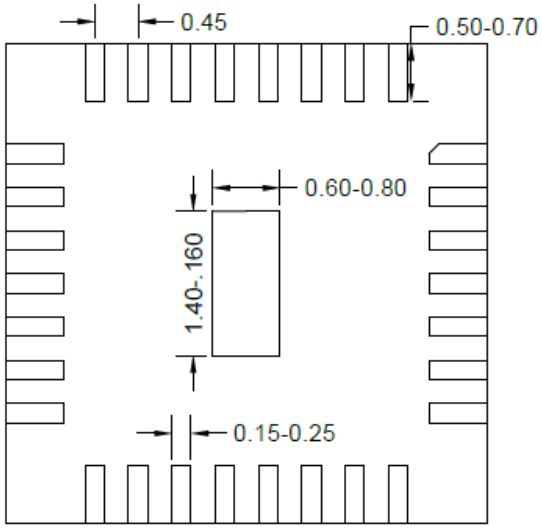
PCB layout Suggestion



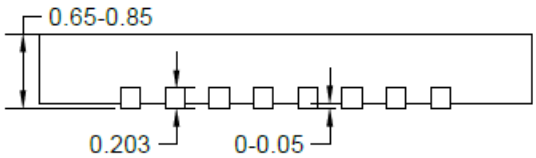
QFN5×5-30 Package Outline Drawing



Top View



Bottom View



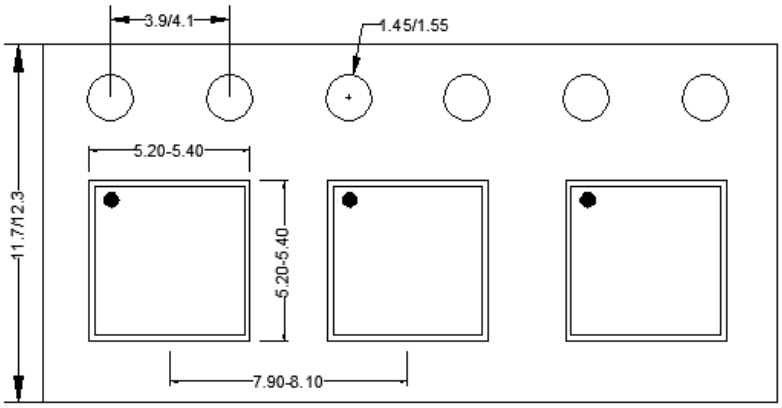
Side View

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

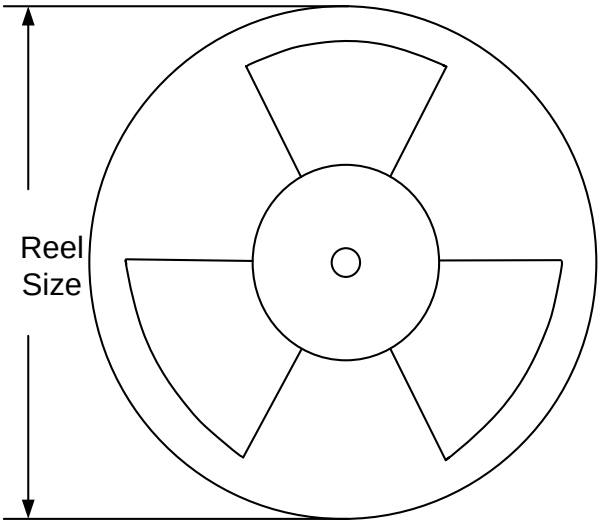
1. Taping orientation

QFN5x5



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5x5	12	8	13"	400	400	5000

3. Others: NA

Revision History

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Date	Revision	Change
Aug.01, 2022	Revision 0.9	Initial Release

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