SY21525x

5.5V, Multi-phase Buck Converter Family

General Description

The SY21525x integrates four synchronous buck converters, each converter is capable of delivering up to 5A continuous output current. These converters can be combined to form various multi-phase PMIC configurations, which are categorized as follows:

- SY21525E: 3-phase and 1-phase dual-output (3+1).
- SY21525F: 2-phase and two 1-phase three-output (2+1+1).
- SY21525J: 2-phase dual-output (2+2).

The SY21525x operates over a wide input voltage range from 2.5V to 5.5V and uses instant PWM control for rapid transient response stable operation. Additionally, during startup and voltage adjustments, the device manages the output slew rate to minimize inrush current and output voltage overshoot.

The SY21525x provides undervoltage lockout (UVLO), along with overvoltage (OVP), overcurrent (OCP), and over temperature protections (OTP). In addition to the standard interrupt, chip enable, the SY21525x also supports I²C communication protocol.

The SY21525x is available in a compact WLCSP2.66× 3.89-54 package.

Features

- 2.5V to 5.5V Wide Input Voltage Range
- Three Distinct Phase Configurations:
  - SY21525E (3+1)
  - SY21525F (2+1+1)
  - SY21525J (2+2)
- 5A per Phase Output Current Capability
- I²C Programmable Output Voltages from 0.3V to 1.85V or 0.45V to 2V
- COT Control Achieves Fast Transient Performance
- ±1.0% Accuracy with Remote Sensing
- Fixed-phase Configuration and Continuous Conduction Mode (FPCCM), OTP Programmable Light Load Mode(DCM/FPCCM)
- Supports Phase Shedding if Configured with DCM Mode by Factory OTP
- Supports Startup with Pre-Biased Output Voltage
- Status Feedback with Interrupt Pin
- Reliable OTP/SCP/UVP/OVP Protection
- Compact Package: WLCSP2.66×3.89-54

Applications

- Smartphones, Tablets
- FPGA and ASIC Power
- Industrial MPU Power
- Optical Module

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Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21525EVCS	WLCSP2.66×3.89-54 RoHS-Compliant and Halogen-Free	**HCJ*xyz***
SY21525FVCS		**HFF*xyz***
SY21525JVCS		**HFH*xyz***

x = year code, y = week code, z = lot number code

Ordering Part Number	Pitch	Output Phase Configuration	I^2C Address
SY21525EVCS	0.4mm	3+1	0x62(01100010)
SY21525FVCS		2+1+1	0x67(01100111)
SY21525JVCS		2+2	0x66(01100110)

Phase and Feedback Balls Configuration Map

Part Number	Phase and Feedback Balls	V_{OUT1} (Host Phase is CH1)	V_{OUT2} (Host Phase is CH2)	V_{OUT3}	V_{OUT4}
SY21525E (3+1)	CHx	Multi-phase: CH1/CH2/CH3	–	–	Single phase: CH4
	FBx/RTNx ball	E6/D6	–	–	E1/F1
SY21525F (2+1+1)	CHx	Multi-phase: CH1/CH4	Single phase: CH2	Single phase: CH3	–
	FBx/RTNx ball	E6/D6	E4/E5	E3/E2	–
SY21525J (2+2)	CHx	Multi-phase: CH1/CH4	Multi-phase: CH2/CH3	–	–
	FBx/RTNx ball	E1/F1	E6/D6	–	–

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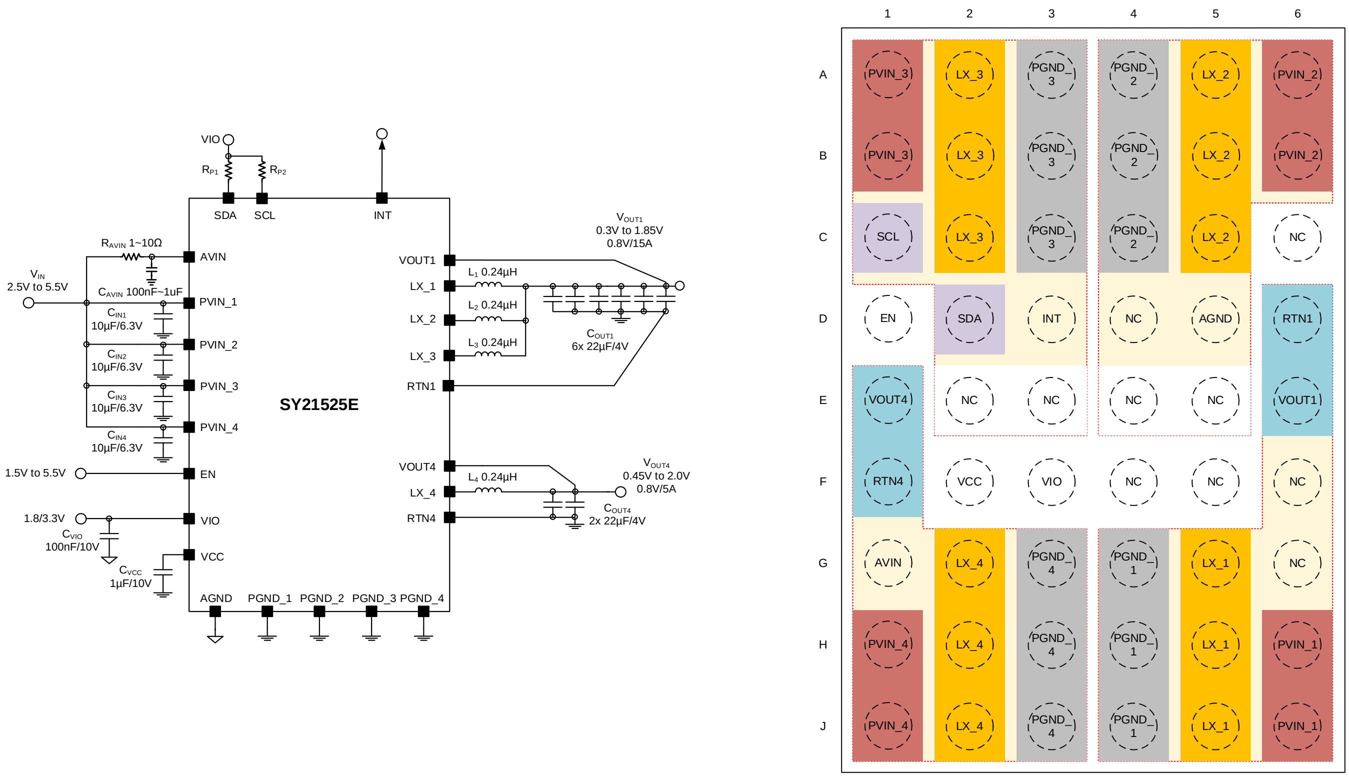
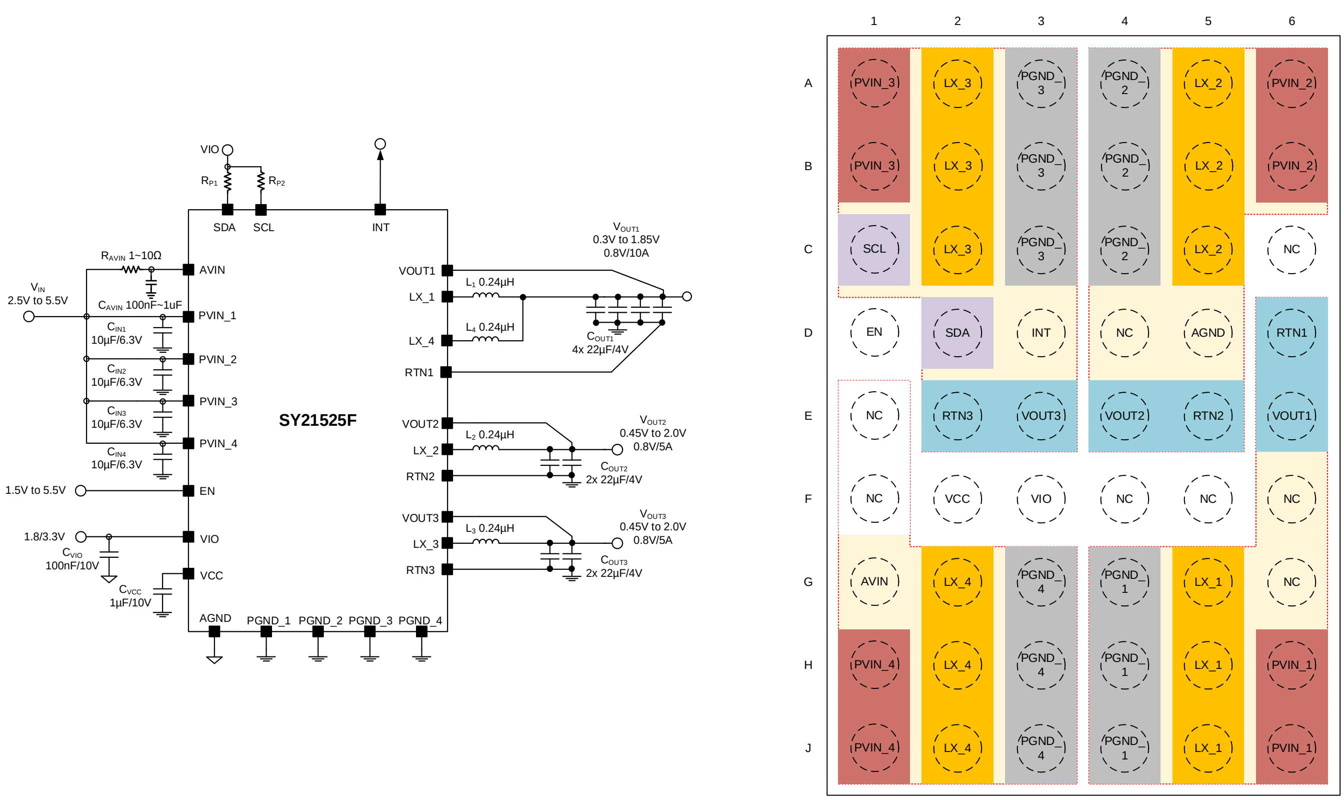
Typical Application and Pinout (top view)



a) SY21525E



b) SY21525F

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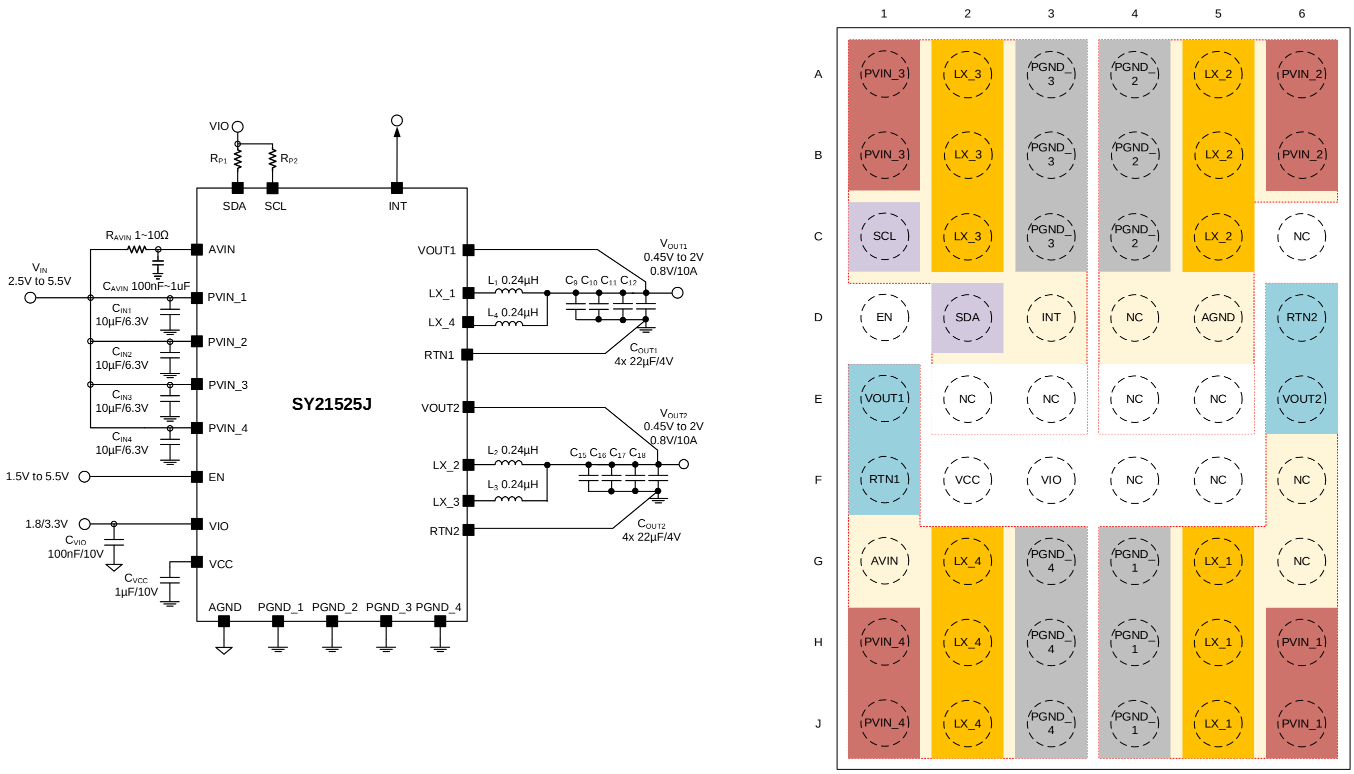

c) SY21525J

Pin Description

Pin Number	Pin Name	Type	Description
A1, B1	PVIN_3	PS	Power supply for Power Stage 3
A2, B2, C2	LX_3	A/O	Switching node for Power Stage 3
A3, B3, C3	PGND_3	G	Ground connection for Power Stage 3
A4, B4, C4	PGND_2	G	Ground connection for Power Stage 2
A5, B5, C5	LX_2	A/O	Switching node for Power Stage 2
A6, B6	PVIN_2	PS	Power supply for Power Stage 2
C1	SCL	D/I	I^2C clock
C6, D4, F4, F5, F6, G6	NC	–	Not connected (NC pins can connect to GND directly)
D1	EN	D/I	Host chip enable input, NMOS logic threshold
D2	SDA	D/I/O	I^2C data
D3	INT	D/O	Interrupt line
D5	GND	–	Analog chip ground. Ensure that pin D5 has a low impedance connection to the internal ground layer.
D6	RTN1 (RTN2)	A/I	Remote ground voltage sense for output 1 Named RTN2 in SY21525J
E1	VOUT4 (VOUT1,NC)	A/I	Remote output voltage sense for output 4 Named VOUT1 in SY21525J NC PIN in SY21525F
E2	RTN3 (NC)	A/I	Remote output voltage sense for output 3 NC PIN in SY21525E/J

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Pin Number	Pin Name	Type	Description
E3	VOUT3 (NC)	A/I	Remote output voltage sense for output 3 NC PIN in SY21525E/J
E4	VOUT2 (NC)	A/I	Remote output voltage sense for output 2 NC PIN in SY21525E, SY21525J
E5	RTN2 (NC)	A/I	Remote output voltage sense for output 2 NC PIN in SY21525E, SY21525J
E6	VOUT1 (VOUT2)	A/I	Remote output voltage sense for output 1 Named VOUT2 in SY21525J
F1	RTN4 (RTN1,NC)	A/I	Remote output voltage sense for output 4 Named RTN1 in SY21525J NC PIN in SY21525F
F2	VCC	A/O	Internal 2.7V LDO output, power supply for the internal analog and digital control circuits. Decouple this pin to the AGND pin with at least a 1μF ceramic capacitor.
F3	VIO	PS	IO supply voltage for digital communications. SDA/SCL should be pulled up to VIO voltage with a pull-up resistor. Normally connected to 1.8V/3.3V supply. Decouple this pin to AGND pin with at least 100nF ceramic capacitor, if VIO connect to PVIN, it is better to add RC filter (typical R_F = 10Ω, C_{FN} = 1μF) to decrease input ripple voltage.
G1	AVIN	PS	Analog supply voltage, 2.5V to 5.5V. Decouple this pin to AGND pin with at least 100nF ceramic capacitor, if AVIN connect to PVIN, it is better to add RC filter to decrease input ripple voltage.
G2, H2, J2	LX_4	A/O	Switching node for Power Stage 4
G3, H3, J3	PGND_4	G	Ground connection for Power Stage 4
G4, H4, J4	PGND_1	G	Ground connection for Power Stage 1
G5, H5, J5	LX_1	A/O	Switching node for Power Stage 1
H1, J1	PVIN_4	PS	Power supply connection for Power Stage 4
H6, J6	PVIN_1	PS	Power supply connection for Power Stage 1

Abbreviations: A: Analog Pin, D: Digital Pin, G: Ground Pin, PS: Power Supply Pin, I: Input Pin, O: Output Pin

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Block Diagram

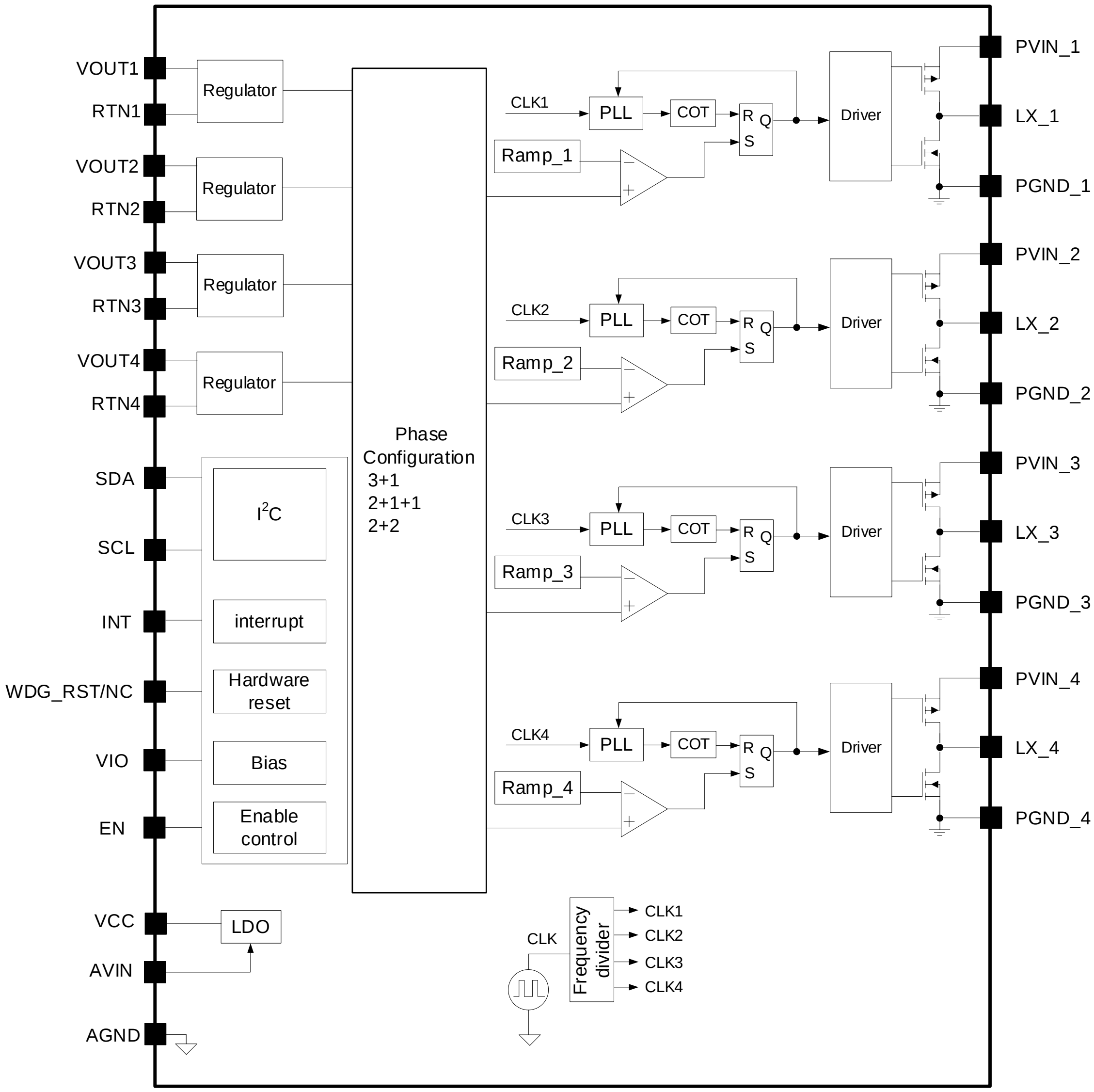

Figure 1. Block Diagram

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Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
PVIN, AVIN	-0.3	6	V
LX1-LX4	-0.3	PVIN + 0.3	
LX1-LX4, transient 10ns	-3.0	7.0	
VIO, EN, SCL, SDA	-0.3	AVIN + 0.3	
OUT	-0.3	3	
RTN, GND	-0.3	0.3	
Other pins	-0.3	6	
Junction Temperature		150	°C
Ambient Temperature	-40	105	
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)	2000		V
CDM (Charged Device Model)	750		
Latch-up	200		mA

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	21	°C/W
θ_{JC_TOP} Junction-to-Case Top Thermal Resistance	2	
P_D Power Dissipation T_A = 25°C	5	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
PVIN, AVIN	2.5	5.5	V
VIO	1.7	AVIN	
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	105	

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Electrical Characteristics

(T_A = -40°C–105°C, V_{AVIN}/V_{PVIN} = 3.7V, V_{OUT} = 1V, unless otherwise specified (**Note 4**))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply	Supply Voltage	V_{AVIN}		2.5		5.5	V
	Supply Voltage	V_{PVIN}		2.5		5.5	V
	AVIN Supply Current	I_Q	EN = 0		1	2	μA
	AVIN + PVIN Supply Current	I_Q	EN = 0		3	6	μA
	AVIN + PVIN Supply Current EN = 3.3V	I_Q	All buck off (EN bit = 0)		30		μA
			No switching, DCM mode		290		μA
	UVLO Rising Threshold	V_{UVLOR}	Rising	2.52	2.60	2.67	V
	UVLO Falling Threshold	V_{UVLOF}	Falling	2.28	2.34	2.40	V
	Input OVP Rising Threshold	V_{OVPR}	Rising	5.684	5.8	5.916	V
	Input OVP Falling Threshold	V_{OVPF}	Falling	5.567	5.68	5.794	V
Power Stage	V_{OUT} Voltage Range	V_{OUT}	SY21525E/F :V_{OUT1}	0.3		1.85	V
			SY21525J: V_{OUT1} SY21525F/J: V_{OUT2} SY21525F: V_{OUT3} SY21525E: V_{OUT4}	0.45		2	V
	V_{OUT} Step Size	V_{step}	V_{OUT} ≤1.3V; SY21525E/F:V_{OUT1}		5		mV
			V_{OUT} >1.3V; SY21525E/F:V_{OUT1}		10		mV
			V_{OUT} ≤1.45V; SY21525J: V_{OUT1}, SY21525F/J: V_{OUT2}, SY21525F: V_{OUT3}, SY21525E: V_{OUT4}		5		mV
			V_{OUT} >1.45V; SY21525J: V_{OUT1}, SY21525F/J: V_{OUT2}, SY21525F: V_{OUT3}, SY21525E: V_{OUT4}		10		mV
	V_{OUT} Accuracy	V_{ACC}	CCM, V_{OUT} > 0.6V T_A = +25°C	-0.5		0.5	%
			CCM, V_{OUT} > 0.6V T_A = -10°C to +85°C	-1		1	%
			CCM, V_{OUT} > 0.6V T_A= -40°C to +105°C	-1.5		1.5	%
			CCM,V_{OUT} < 0.6V T_A = +25°C	-4		+4	mV
			CCM,V_{OUT} < 0.6V T_A= -10°C to +85°C	-5.5		+5.5	mV
			CCM,V_{OUT} < 0.6V T_A = -40°C to +105°C	-8		+8	mV
	Current Sharing	I_{MATCH}	2/3-phase, I_{OUT} = 10A, 2.5A per phase.			0.5	A
			3 phase, I_{OUT} = 15A, 3.75A per phase.			0.5	A
	DVS Slew Rate Accuracy	V_{DVS}	Default DVS up = 16mV/μs Default DVS down = 4mV/μs	-15		15	%
	Soft-Start Slew Rate Accuracy	T_{SS}	Slew Rate = 10mV/μs	-15		15	%
	Switching Frequency	f_{SW}	T_A = 25°C; SY21525E/F/J	1.7	1.8	1.9	MHz
			T_A = -40°C to 125°C; SY21525E/F/J	1.55	1.8	2.04	MHz
	Maximum Output Current (Each Phase)	I_{OUT}		5			A
	Top FET R_{ON}	$R_{DS(ON)HS}$	PVIN = 3.7V		26		mΩ
	Bottom FET R_{ON}	$R_{DS(ON)LS}$	PVIN = 3.7V		9		mΩ

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	Output Discharge Resistance		R_{DIS}	Output disabled		125		Ω
	Minimum Off-Time (Note 5)		T_{MIN_OFF}			100		ns
	I²C Turn-On Command to Output Response Delay Time		T_{I2C_OUT}				100	μs
Protection Characteristics	High Side Switch Current Limit		I_{PLMT}	T_A = 25°C	7.7		9.3	A
				T_A = -40°C to +105°C	6.8		10.2	A
	Low Side Switch Current Limit		I_{VLMT}	T_A = 25°C	5.8		7	A
				T_A = -40°C to +105°C	4.8		8	A
	Low Side Switch Negative Current Limit		I_{NLMT}	T_A = 25°C	-4.8		-2.4	A
				T_A = -40°C to +105°C	-5.4		-1.8	A
	Thermal Warning Threshold		T_{WN}	Typical = +109°C	-10		10	%
	Thermal Warning Hysteresis		T_{WNHYS}	Typical = +15°C	-10		10	%
	Thermal Shutdown Temperature		T_{SD}	Typical = +155°C	-10		10	%
	Thermal Shutdown Hysteresis		T_{SDHYS}	Typical = +15°C	-10		10	%
	Output OVP Threshold		V_{TH_OVP}		116	126	136	% V_{SET}
	Output UVP Threshold		V_{TH_UVP}		30	40	50	% V_{SET}
	Output OCP Threshold		V_{TH_OCP}		70	80	90	% V_{SET}
IO Pins	EN	Low Level Input Voltage	V_{ENIL}				0.4	V
		High Level Input Voltage	V_{ENIH}		1.2			V
	VIO PIN	Power Supply Voltage			1.7	1.8	AVIN	V
		Supply Current					1	μA
	SCL, SDA	Low Level Input Voltage	V_{I2CIL}				0.3×VIO	V
		High Level Input Voltage	V_{I2CIH}		0.7×VIO			V
	Serial Interfaces	I²C Frequency Capability	f_{I2C}				3.4	MHz

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25°C on a Silergy test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

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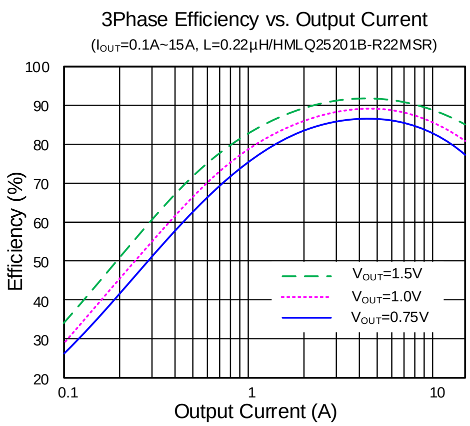
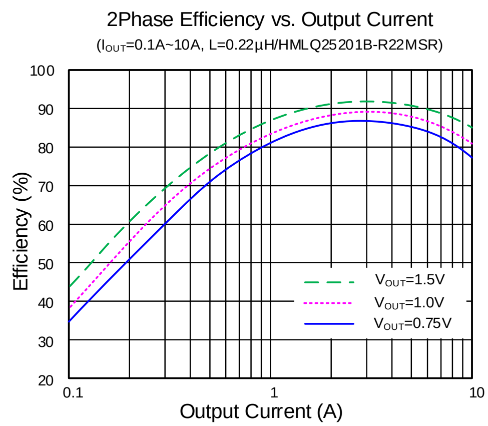
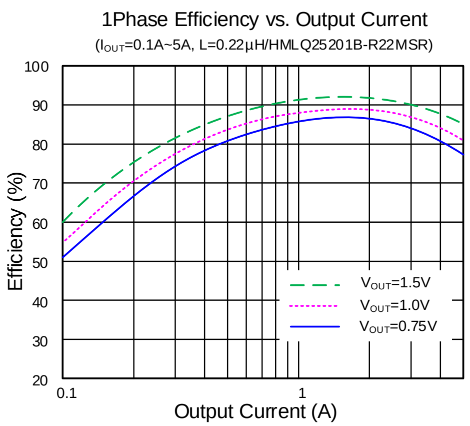
Typical Performance Characteristics

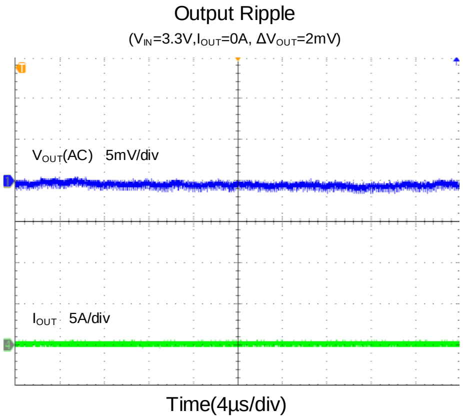
Fixed-Phase Configuration (Default)

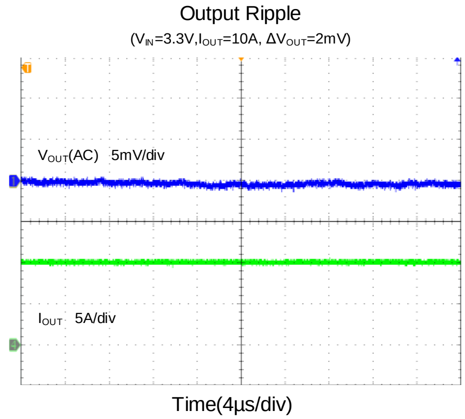
(V_{IN} = 3.7V, V_{OUT} = 1.0V, Fixed-Phase Configuration (3-Phase configuration for example), L = 0.22µH (HMLQ25201B-R22MSR), C_{OUT} = 22µF × 6, T_A = +25°C, unless otherwise noted)











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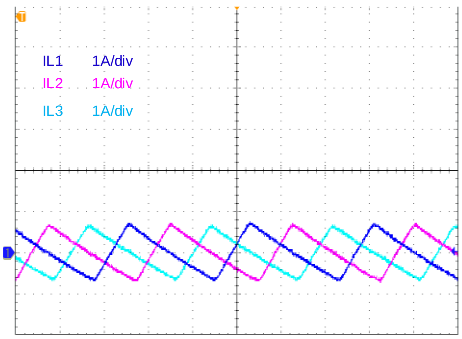
Current Balance and 3-phase Interleave

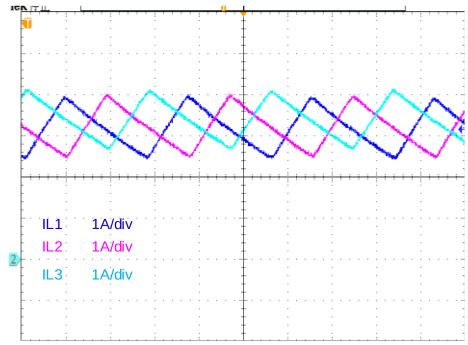
(V_{IN}=3.3V,I_{OUT}=0A)



Time(200ns/div)

Current Balance and 3-phase Interleave

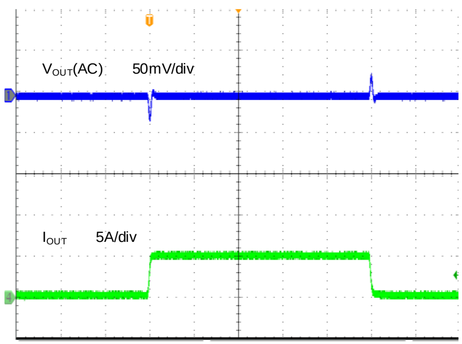
(V_{IN}=3.3V,I_{OUT}=10A)



Time(200ns/div)

Load Transient

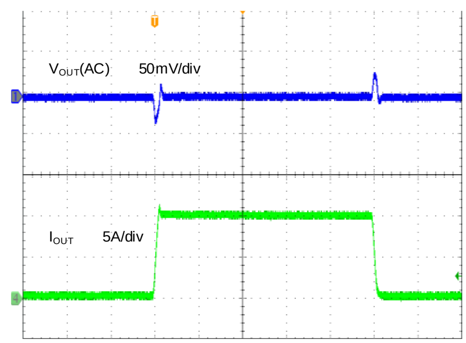
(V_{IN}=3.3V,I_{OUT}=0~5A,5A/10µs)



Time(200µs/div)

Load Transient

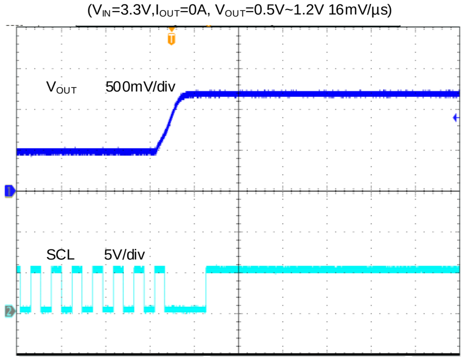
(V_{IN}=3.3V,I_{OUT}=0~10A,10A/20µs)



Time(200µs/div)

DVS Up

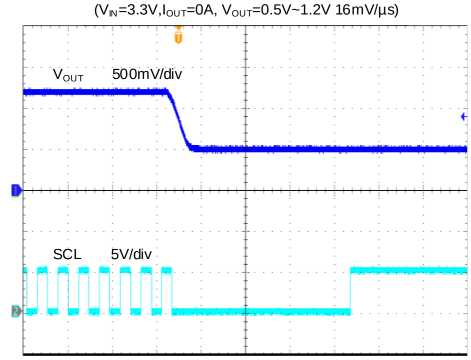
(V_{IN}=3.3V,I_{OUT}=0A, V_{OUT}=0.5V~1.2V 16mV/µs)



Time(100µs/div)

DVS Down

(V_{IN}=3.3V,I_{OUT}=0A, V_{OUT}=0.5V~1.2V 16mV/µs)



Time(100µs/div)

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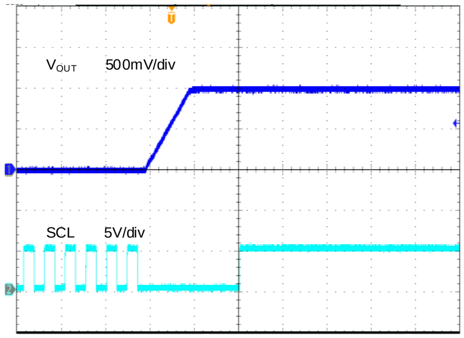
Startup from Software Enable

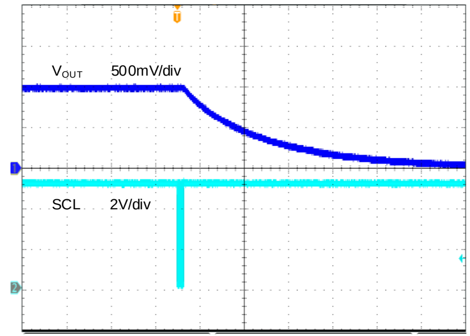
(V_{IN}=3.3V,I_{OUT}=0A, V_{OUT}=0~1.2V, 10mV/µs)



Time(100µs/div)

Shutdown from Software Enable

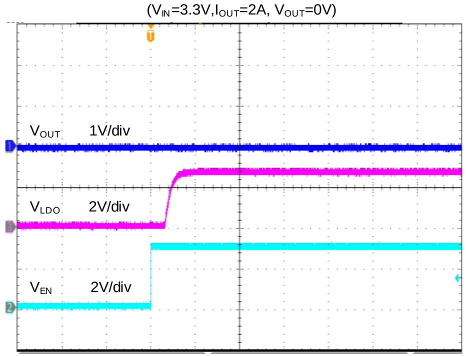
(V_{IN}=3.3V,I_{OUT}=0A, V_{OUT}=1.2V~0V)



Time(10ms/div)

Startup from Hardware Enable

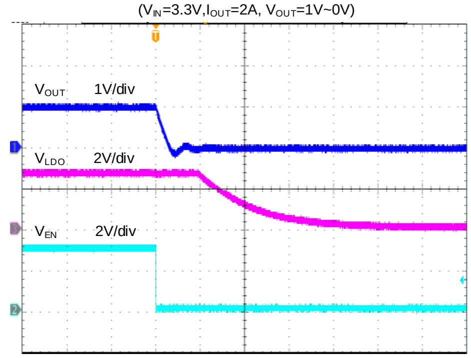
(V_{IN}=3.3V,I_{OUT}=2A, V_{OUT}=0V)



Time(100µs/div)

Shutdown from Hardware Enable

(V_{IN}=3.3V,I_{OUT}=2A, V_{OUT}=1V~0V)



Time(200µs/div)

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Functional Description

Output Voltage Setting and Dynamic Voltage Scaling (DVS)

Output Voltage Setting

The output voltage can be programmed by writing to the 8-bit register BUCKx_DVS0CFG1. Table 1 provides the registers for setting the output voltage of each channel of SY21525x, the corresponding reference table, and the default output voltage codes and their respective values. For more details on voltage settings, see Table 2 and Table 3.

Table 1. Default Output Voltage Configuration Table

Part Number	V_{OUT1} (Register: 0x48)	V_{OUT2} (Register: 0x7C)	V_{OUT3} (Register: 0x62)	V_{OUT4} (Register: 0x96)
SY21525E (3+1)	Table 2: 0x64/0.8V	-	-	Table 3: 0x46/0.8V
SY21525F (2+1+1)	Table 2: 0x64/0.8V	Table 3: 0x46/0.8V	Table 3: 0x46/0.8V	-
SY21525J (2+2)	Table 3: 0x46/0.8V	Table 3: 0x46/0.8V	-	-

Table 2. DAC Code vs. Setting V_{OUT}

DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0000 0000	0.300	0100 0001	0.625	1000 0010	0.950	1100 0011	1.275
0000 0001	0.305	0100 0010	0.630	1000 0011	0.955	1100 0100	1.280
0000 0010	0.310	0100 0011	0.635	1000 0100	0.960	1100 0101	1.285
0000 0011	0.315	0100 0100	0.640	1000 0101	0.965	1100 0110	1.290
0000 0100	0.320	0100 0101	0.645	1000 0110	0.970	1100 0111	1.295
0000 0101	0.325	0100 0110	0.650	1000 0111	0.975	1100 1000	1.300
0000 0110	0.330	0100 0111	0.655	1000 1000	0.980	1100 1001	1.310
0000 0111	0.335	0100 1000	0.660	1000 1001	0.985	1100 1010	1.320
0000 1000	0.340	0100 1001	0.665	1000 1010	0.990	1100 1011	1.330
0000 1001	0.345	0100 1010	0.670	1000 1011	0.995	1100 1100	1.340
0000 1010	0.350	0100 1011	0.675	1000 1100	1.000	1100 1101	1.350
0000 1011	0.355	0100 1100	0.680	1000 1101	1.005	1100 1110	1.360
0000 1100	0.360	0100 1101	0.685	1000 1110	1.010	1100 1111	1.370
0000 1101	0.365	0100 1110	0.690	1000 1111	1.015	1101 0000	1.380
0000 1110	0.370	0100 1111	0.695	1001 0000	1.020	1101 0001	1.390
0000 1111	0.375	0101 0000	0.700	1001 0001	1.025	1101 0010	1.400
0001 0000	0.380	0101 0001	0.705	1001 0010	1.030	1101 0011	1.410
0001 0001	0.385	0101 0010	0.710	1001 0011	1.035	1101 0100	1.420
0001 0010	0.390	0101 0011	0.715	1001 0100	1.040	1101 0101	1.430
0001 0011	0.395	0101 0100	0.720	1001 0101	1.045	1101 0110	1.440
0001 0100	0.400	0101 0101	0.725	1001 0110	1.050	1101 0111	1.450
0001 0101	0.405	0101 0110	0.730	1001 0111	1.055	1101 1000	1.460
0001 0110	0.410	0101 0111	0.735	1001 1000	1.060	1101 1001	1.470
0001 0111	0.415	0101 1000	0.740	1001 1001	1.065	1101 1010	1.480
0001 1000	0.420	0101 1001	0.745	1001 1010	1.070	1101 1011	1.490
0001 1001	0.425	0101 1010	0.750	1001 1011	1.075	1101 1100	1.500
0001 1010	0.430	0101 1011	0.755	1001 1100	1.080	1101 1101	1.510

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DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0001 1011	0.435	0101 1100	0.760	1001 1101	1.085	1101 1110	1.520
0001 1100	0.440	0101 1101	0.765	1001 1110	1.090	1101 1111	1.530
0001 1101	0.445	0101 1110	0.770	1001 1111	1.095	1110 0000	1.540
0001 1110	0.450	0101 1111	0.775	1010 0000	1.100	1110 0001	1.550
0001 1111	0.455	0110 0000	0.780	1010 0001	1.105	1110 0010	1.560
0010 0000	0.460	0110 0001	0.785	1010 0010	1.110	1110 0011	1.570
0010 0001	0.465	0110 0010	0.790	1010 0011	1.115	1110 0100	1.580
0010 0010	0.470	0110 0011	0.795	1010 0100	1.120	1110 0101	1.590
0010 0011	0.475	0110 0100	0.800	1010 0101	1.125	1110 0110	1.600
0010 0100	0.480	0110 0101	0.805	1010 0110	1.130	1110 0111	1.610
0010 0101	0.485	0110 0110	0.810	1010 0111	1.135	1110 1000	1.620
0010 0110	0.490	0110 0111	0.815	1010 1000	1.140	1110 1001	1.630
0010 0111	0.495	0110 1000	0.820	1010 1001	1.145	1110 1010	1.640
0010 1000	0.500	0110 1001	0.825	1010 1010	1.150	1110 1011	1.650
0010 1001	0.505	0110 1010	0.830	1010 1011	1.155	1110 1100	1.660
0010 1010	0.510	0110 1011	0.835	1010 1100	1.160	1110 1101	1.670
0010 1011	0.515	0110 1100	0.840	1010 1101	1.165	1110 1110	1.680
0010 1100	0.520	0110 1101	0.845	1010 1110	1.170	1110 1111	1.690
0010 1101	0.525	0110 1110	0.850	1010 1111	1.175	1111 0000	1.700
0010 1110	0.530	0110 1111	0.855	1011 0000	1.180	1111 0001	1.710
0010 1111	0.535	0111 0000	0.860	1011 0001	1.185	1111 0010	1.720
0011 0000	0.540	0111 0001	0.865	1011 0010	1.190	1111 0011	1.730
0011 0001	0.545	0111 0010	0.870	1011 0011	1.195	1111 0100	1.740
0011 0010	0.550	0111 0011	0.875	1011 0100	1.200	1111 0101	1.750
0011 0011	0.555	0111 0100	0.880	1011 0101	1.205	1111 0110	1.760
0011 0100	0.560	0111 0101	0.885	1011 0110	1.210	1111 0111	1.770
0011 0101	0.565	0111 0110	0.890	1011 0111	1.215	1111 1000	1.780
0011 0110	0.570	0111 0111	0.895	1011 1000	1.220	1111 1001	1.790
0011 0111	0.575	0111 1000	0.900	1011 1001	1.225	1111 1010	1.800
0011 1000	0.580	0111 1001	0.905	1011 1010	1.230	1111 1011	1.810
0011 1001	0.585	0111 1010	0.910	1011 1011	1.235	1111 1100	1.820
0011 1010	0.590	0111 1011	0.915	1011 1100	1.240	1111 1101	1.830
0011 1011	0.595	0111 1100	0.920	1011 1101	1.245	1111 1110	1.840
0011 1100	0.600	0111 1101	0.925	1011 1110	1.250	1111 1111	1.850
0011 1101	0.605	0111 1110	0.930	1011 1111	1.255		
0011 1110	0.610	0111 1111	0.935	1100 0000	1.260		
0011 1111	0.615	1000 0000	0.940	1100 0001	1.265		
0100 0000	0.620	1000 0001	0.945	1100 0010	1.270		

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Table 3. DAC Code vs. Setting V_{OUT}

DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0000 0000	0.45	0100 0001	0.775	1000 0010	1.1	1100 0011	1.425
0000 0001	0.455	0100 0010	0.78	1000 0011	1.105	1100 0100	1.43
0000 0010	0.46	0100 0011	0.785	1000 0100	1.11	1100 0101	1.435
0000 0011	0.465	0100 0100	0.79	1000 0101	1.115	1100 0110	1.44
0000 0100	0.47	0100 0101	0.795	1000 0110	1.12	1100 0111	1.445
0000 0101	0.475	0100 0110	0.8	1000 0111	1.125	1100 1000	1.45
0000 0110	0.48	0100 0111	0.805	1000 1000	1.13	1100 1001	1.46
0000 0111	0.485	0100 1000	0.81	1000 1001	1.135	1100 1010	1.47
0000 1000	0.49	0100 1001	0.815	1000 1010	1.14	1100 1011	1.48
0000 1001	0.495	0100 1010	0.82	1000 1011	1.145	1100 1100	1.49
0000 1010	0.5	0100 1011	0.825	1000 1100	1.15	1100 1101	1.5
0000 1011	0.505	0100 1100	0.83	1000 1101	1.155	1100 1110	1.51
0000 1100	0.51	0100 1101	0.835	1000 1110	1.16	1100 1111	1.52
0000 1101	0.515	0100 1110	0.84	1000 1111	1.165	1101 0000	1.53
0000 1110	0.52	0100 1111	0.845	1001 0000	1.17	1101 0001	1.54
0000 1111	0.525	0101 0000	0.85	1001 0001	1.175	1101 0010	1.55
0001 0000	0.53	0101 0001	0.855	1001 0010	1.18	1101 0011	1.56
0001 0001	0.535	0101 0010	0.86	1001 0011	1.185	1101 0100	1.57
0001 0010	0.54	0101 0011	0.865	1001 0100	1.19	1101 0101	1.58
0001 0011	0.545	0101 0100	0.87	1001 0101	1.195	1101 0110	1.59
0001 0100	0.55	0101 0101	0.875	1001 0110	1.2	1101 0111	1.6
0001 0101	0.555	0101 0110	0.88	1001 0111	1.205	1101 1000	1.61
0001 0110	0.56	0101 0111	0.885	1001 1000	1.21	1101 1001	1.62
0001 0111	0.565	0101 1000	0.89	1001 1001	1.215	1101 1010	1.63
0001 1000	0.57	0101 1001	0.895	1001 1010	1.22	1101 1011	1.64
0001 1001	0.575	0101 1010	0.9	1001 1011	1.225	1101 1100	1.65
0001 1010	0.58	0101 1011	0.905	1001 1100	1.23	1101 1101	1.66
0001 1011	0.585	0101 1100	0.91	1001 1101	1.235	1101 1110	1.67
0001 1100	0.59	0101 1101	0.915	1001 1110	1.24	1101 1111	1.68
0001 1101	0.595	0101 1110	0.92	1001 1111	1.245	1110 0000	1.69
0001 1110	0.6	0101 1111	0.925	1010 0000	1.25	1110 0001	1.7
0001 1111	0.605	0110 0000	0.93	1010 0001	1.255	1110 0010	1.71
0010 0000	0.61	0110 0001	0.935	1010 0010	1.26	1110 0011	1.72
0010 0001	0.615	0110 0010	0.94	1010 0011	1.265	1110 0100	1.73
0010 0010	0.62	0110 0011	0.945	1010 0100	1.27	1110 0101	1.74
0010 0011	0.625	0110 0100	0.95	1010 0101	1.275	1110 0110	1.75
0010 0100	0.63	0110 0101	0.955	1010 0110	1.28	1110 0111	1.76
0010 0101	0.635	0110 0110	0.96	1010 0111	1.285	1110 1000	1.77
0010 0110	0.64	0110 0111	0.965	1010 1000	1.29	1110 1001	1.78
0010 0111	0.645	0110 1000	0.97	1010 1001	1.295	1110 1010	1.79
0010 1000	0.65	0110 1001	0.975	1010 1010	1.3	1110 1011	1.8
0010 1001	0.655	0110 1010	0.98	1010 1011	1.305	1110 1100	1.81

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DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0010 1010	0.66	0110 1011	0.985	1010 1100	1.31	1110 1101	1.82
0010 1011	0.665	0110 1100	0.99	1010 1101	1.315	1110 1110	1.83
0010 1100	0.67	0110 1101	0.995	1010 1110	1.32	1110 1111	1.84
0010 1101	0.675	0110 1110	1	1010 1111	1.325	1111 0000	1.85
0010 1110	0.68	0110 1111	1.005	1011 0000	1.33	1111 0001	1.86
0010 1111	0.685	0111 0000	1.01	1011 0001	1.335	1111 0010	1.87
0011 0000	0.69	0111 0001	1.015	1011 0010	1.34	1111 0011	1.88
0011 0001	0.695	0111 0010	1.02	1011 0011	1.345	1111 0100	1.89
0011 0010	0.7	0111 0011	1.025	1011 0100	1.35	1111 0101	1.9
0011 0011	0.705	0111 0100	1.03	1011 0101	1.355	1111 0110	1.91
0011 0100	0.71	0111 0101	1.035	1011 0110	1.36	1111 0111	1.92
0011 0101	0.715	0111 0110	1.04	1011 0111	1.365	1111 1000	1.93
0011 0110	0.72	0111 0111	1.045	1011 1000	1.37	1111 1001	1.94
0011 0111	0.725	0111 1000	1.05	1011 1001	1.375	1111 1010	1.95
0011 1000	0.73	0111 1001	1.055	1011 1010	1.38	1111 1011	1.96
0011 1001	0.735	0111 1010	1.06	1011 1011	1.385	1111 1100	1.97
0011 1010	0.74	0111 1011	1.065	1011 1100	1.39	1111 1101	1.98
0011 1011	0.745	0111 1100	1.07	1011 1101	1.395	1111 1110	1.99
0011 1100	0.75	0111 1101	1.075	1011 1110	1.4	1111 1111	2
0011 1101	0.755	0111 1110	1.08	1011 1111	1.405		
0011 1110	0.76	0111 1111	1.085	1100 0000	1.41		
0011 1111	0.765	1000 0000	1.09	1100 0001	1.415		
0100 0000	0.77	1000 0001	1.095	1100 0010	1.42		

DVS

The ramp-up slew rate BUCKx_RSPUP[2:0] bits and the ramp-down slew rate BUCKx_RSPDN[2:0] bits in the BUCKx_RSPCFG1 register set the slew rates (DVS speed) for BUCKx during normal DVS transitions. For more details, see registers BUCKx_RSPCFG.

The SY21525E/F/J multi-phase channels are available in both fixed-phase and auto-phase modes for light loads, and can be configured by factory one-time-programmable (OTP) configuration registers.

The SY21525E/F/J multi-phase channels are configured for fixed-phase configuration, in which all phases are activated and each phase is staggered 120 degrees for 3-phase, and 180 degrees for 2-phase channels to reduce output ripple under light loads. During the DVS process, the SY21525E/F/J multi-phase channels always operate in fixed-phase configuration and the registers BUCK1_RAMP and BUCK2_RAMP are ignored.

For parts configured to use auto-phase mode under light load, registers BUCK1_RAMP or BUCK2_RAMP are valid for both DVS up and down. During the DVS process, the device also has the option to choose fixed-phase configuration and auto-phase mode. When fixed-phase configuration is selected, all phases are enabled during DVS transition. When auto-phase mode is selected, the converter follows auto-phase adjustment logic. Figure 2 and Figure 3 show examples of DVS operation.

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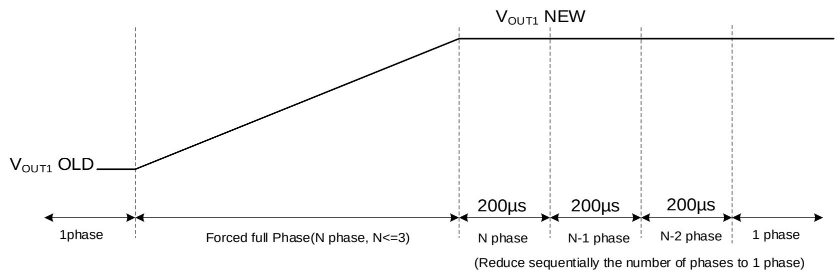

Figure 2. DVS Fixed-phase configuration (Channel 1 Example)

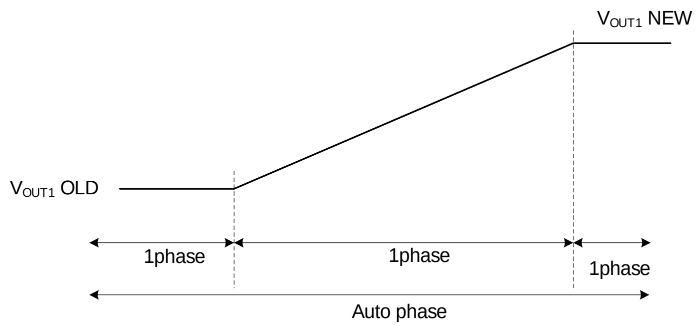

Figure 3. DVS Auto-Phase Mode (Channel 1 Example)

Power Sequencing

Enable Logic

The SY21525x features two levels of enable logic, as follows:

- Global EN pin
- Software EN bit BUCKx_EN_DVS0 in register BUCKx_DVS0CFG0

Figure 4 shows the enable logic when PVIN exceeds UVLO.

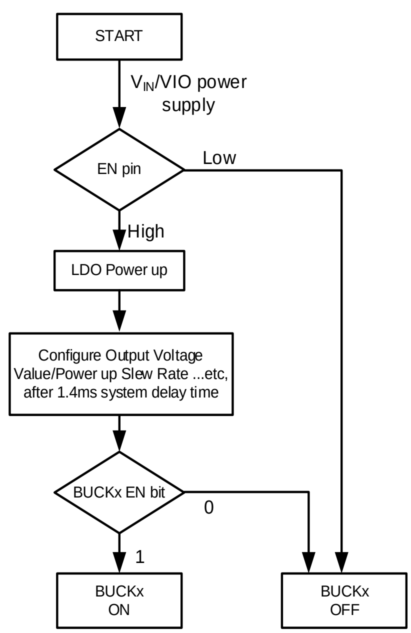

Figure 4. Enable Logic

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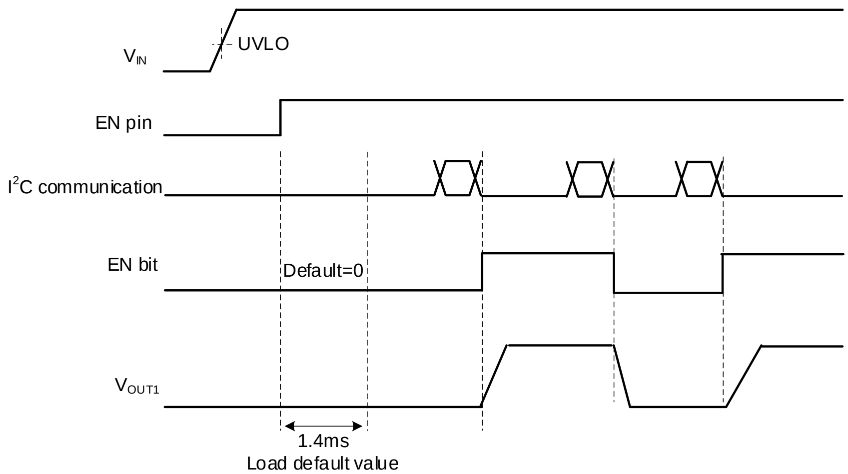

Figure 5. Power-Up Sequencing (Channel1 Example)

Power-Up Operation

When the global chip enable (EN) pin is pulled high, the SY21525x powers up its key biasing circuits and loads the (OTP) configuration registers. When the turn-on signal is detected, the buck converter enters forced CCM mode, all phases are activated, and a power-up sequence begins at the configured slew rate. When the output voltage reaches 0.25V, the phase-lock-loop (PLL) begins operating.

When the output voltage reaches the default value (see Table 1), the SY21525x always operates in fixed-phase configuration. For parts configured to use auto-phase mode (by factory OTP), the auto-phase adjustment logic is activated and the device operates in the specific phase mode determined by the output current level.

The slew rate of each buck during soft-start can be configured using register BUCKx_SLEWCTRL.

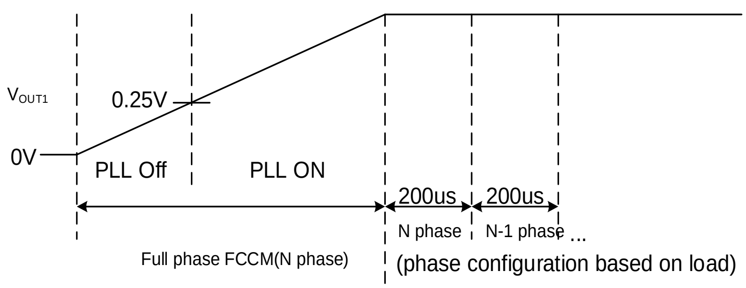

Figure 6. Power-up Operation (Channel 1 Example)

Shutdown Operation

When the turn-off signal is detected, the buck turns the high side switch off and the low side switch on until the inductor current reaches zero. The output can be pulled down by a discharge resistor or disabled using the VOUT_DISCHARGE_EN bit in register BUCKx_CFG0.

PFM/PWM Operation

The converter can be configured using register BUCKx_DVS0CFG0 to operate in either forced PWM mode or automatic PFM/PWM mode.

When fixed-phase configuration is used, the SY21525x always operates in forced PWM mode for Multi-phase Channels, and BUCKx_DVS0CFG0 registers are ignored except Single-phase channels.

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For parts configured to use auto-phase mode (by factory OTP), BUCKx_DVS0CFG0 configuration data is used. When forced PWM mode is used, the converter always operates in forced continuous conduction mode, even at light loads. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications, at the expense of a lower efficiency at light loads. In automatic PFM/PWM mode, the converter operates in regulated frequency PWM mode at moderate to heavy loads and in PFM mode during light loads. This maintains high efficiency over a wide load current range.

In order to prevent loss of interleaving control due to the minimum on-time, the SY21525x utilizes frequency foldback, which is a decrease in frequency from 2MHz to 1MHz when V_{OUT1} < 0.455V and V_{IN} > 4.2V. Note that the default frequency can be changed by factory OTP. When the default frequency is 1MHz, the frequency foldback function is disabled, and the folding function is the same for both fixed-phase configuration and automatic phase mode. See Figure 7.

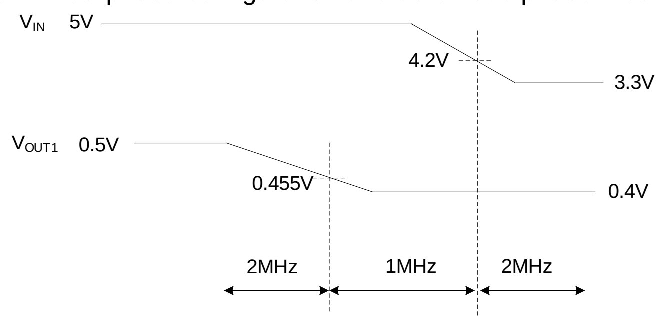

Figure 7. Foldback Logic (Channel 1 Example)

Protection Features

The SY21525x has integrated overcurrent (OC), overvoltage (OV), undervoltage (UV), and over-temperature (OT) protection features. See Table 4.

Table 4. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 155°C Falling: 140°C	-	Controlled by OT_CTRL Shut down when temperature > 155°C Restart when temperature < 140°C
Thermal Warning	Rising: 109°C Falling: 94°C	-	Thermal warning bit is set
OC	80% V_{SET}	200µs	Hiccup mode
Output OVP	126% V_{SET}	10µs	Stops switching when V_{OUT} > 126%V_{SET} Resumes switching when V_{OUT} < 126%V_{SET}
Output UVP	40% V_{SET}	20µs	Selected by BUCKx_CTRL Latch off or hiccup (default hiccup mode) For multi-phase channels, peripheral channels' BUCKx_CTRL must be configured identically
Input OVP	5.8V	4µs	Stops switching when V_{IN} > 5.8V, restarts when V_{IN} < 5.68V

Overtemperature Protection

The SY21525x provides thermal warning and thermal shutdown protection. If the junction temperature exceeds 109°C, the thermal warning bit TEMP_DIE is set to 1. Once the temperature drops below 94°C, the bit resets to 0 after an I^2C read. The thermal warning function is activated once the global EN pin is pulled high.

If the junction temperature continues to rise and exceeds 155°C (typ.), the SY21525x enters thermal shutdown. In this mode, the high side and low side switches are turned off. When the junction temperature falls below 140°C (typ.), the PMIC is re-enabled automatically.

Thermal fault detection is activated once the global EN pin is pulled high. Overtemperature protection can be disabled using register OT_CTRL.

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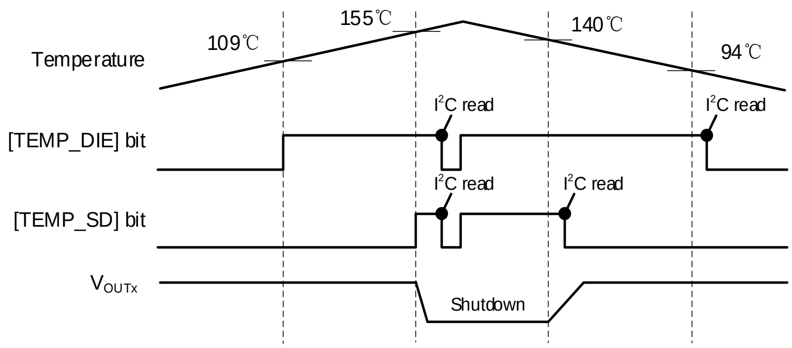

Figure 8. Thermal Warning and Thermal Shutdown

Overcurrent Protection

The SY21525x implements cycle-by-cycle current limit to protect the device against overcurrent. When the current in the high side MOSFET reaches its current limit, the high side MOSFET is turned off and the low side MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis. As the load current increases, the output voltage drops. As soon as the output voltage drops below 80% V_{SET} for a duration of 200us, the converter is turned off for a period of soft-start time × 7, then restarted. This restart will repeat until the overload condition is removed. Overcurrent fault detection is disabled during the normal power-up, shutdown, and DVS transitions.

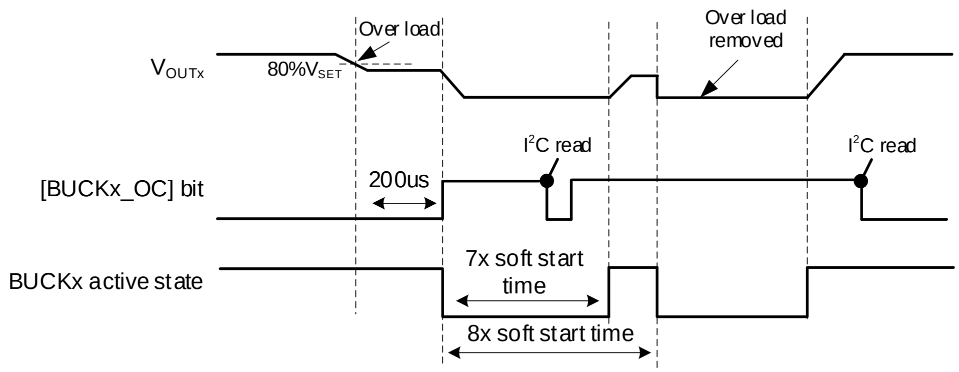

Figure 9. Overcurrent Protection

Output Overvoltage/ Undervoltage Protection

The SY21525x protects against output overvoltage (OV) and undervoltage (UV) fault conditions. When the output voltage reaches 126% of V_{SET} for a duration of 10μs, the buck converter enters no-switching mode. Both high side and low side switches are turned off until the output voltage drops below 126% of V_{SET}. OV fault detection is disabled during the normal power-up, shutdown, and DVS transitions.

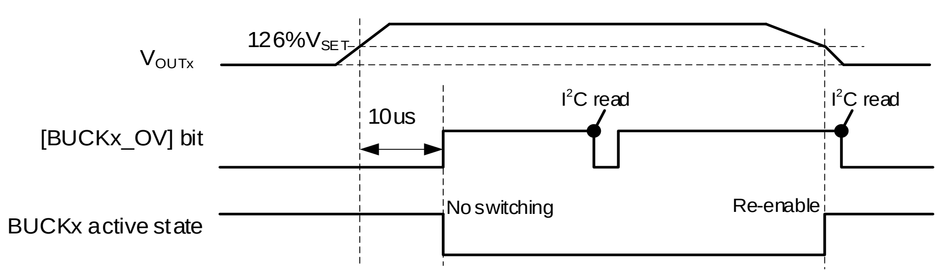

Figure 10. Output OV Protection

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When the output voltage drops below 40% V_{SET} for 20μs, the buck converter will be turned off. The SY21525x provides hiccup and latch-off protection modes, selected using BUCKx_CTRL registers. If latch-off mode is selected, the buck converter will not restart after an UV event. This state can only be cleared by recycling the PVIN_x/AVIN pins or by toggling the EN pin. When UV hiccup mode is selected, the buck will restart after a period of soft-start time × 7. UV fault detection is disabled during the normal power-up, shutdown, and DVS transitions. For multi-phase channels, channel registers BUCKx_CTRL must be configured with the same values.

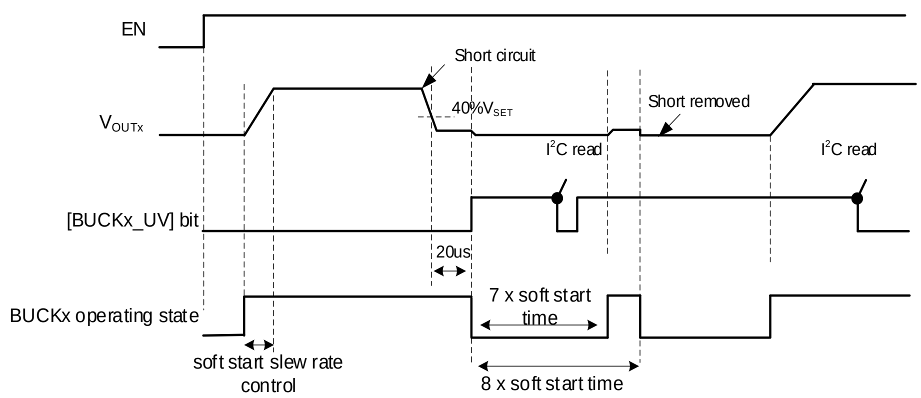

Figure 11. UV Protection, Hiccup Mode

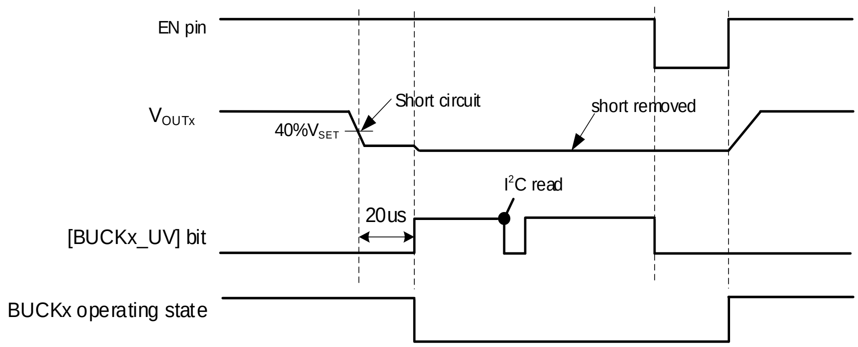

Figure 12. UV Protection, Latch-Off

Input Overvoltage Protection

The SY21525x provides overvoltage (OV) fault detection to protect the system. When V_{AVIN} exceeds 5.8V, the buck is turned off. When V_{AVIN} decreases to 5.68V, the buck restarts. Input OV fault detection is activated once the global EN pin is pulled high.

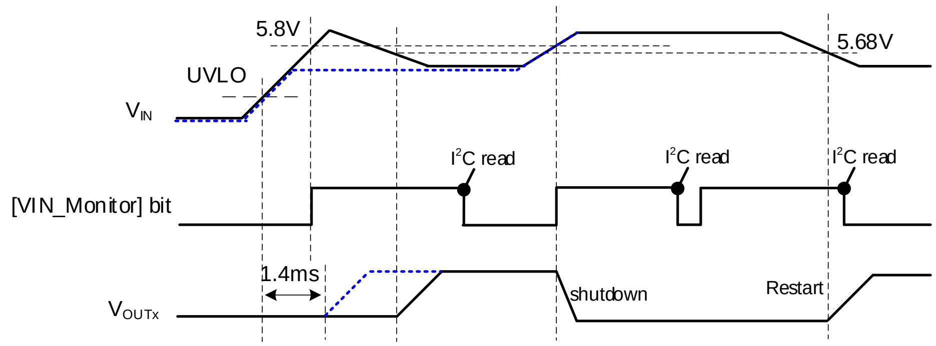

Figure 13. Input OV Protection

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Interrupt

The SY21525x can alert the host when a fault has occurred through a configurable interrupt (INT) pin, which reflects an interrupt request signal (IRQ) with configurable masking options. The interrupt pin is set internally as an active-low, open-drain output.

When a fault occurs, the corresponding fault record bit is set to 1 until the fault is cleared. The fault can be cleared using an I^2C read at the flag register address.

When a fault occurs and the corresponding fault bit is not masked, the INT pin is pulled low. Once all fault bits are cleared, the INT pin is released to a high impedance state. Figure 14 shows the interrupt logic structure.

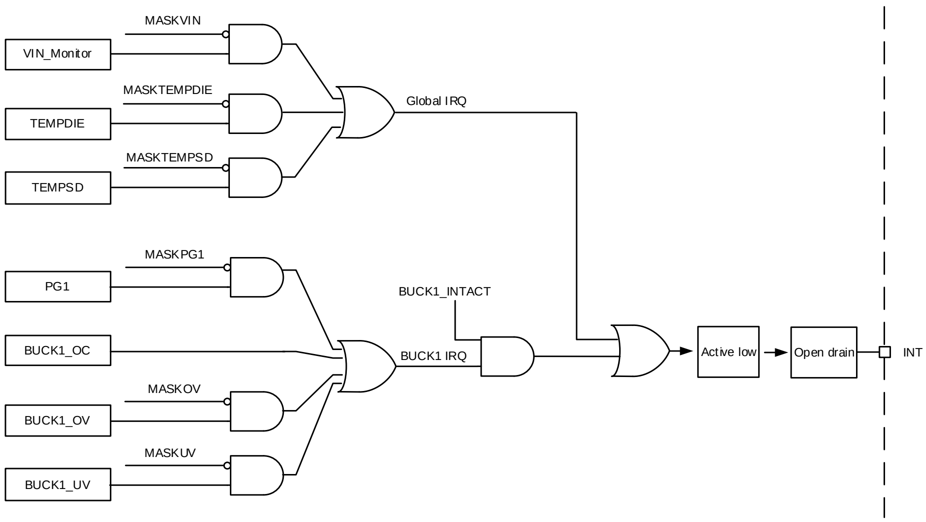

Figure 14. Interrupt Tree (Channel 1 Example)

Input OV Protection Interrupt

The SY21525x provides a VIN monitor bit in register RECORDTEMP to indicate an input overvoltage (OV) fault. If the input voltage is higher than the OV protection threshold, the bit is set to 1 and the INT pin is pulled low. The bit can be reset to 0 after it is read if the OV protection state is cleared. This interrupt can be masked by bit MASKVIN in register MASKTEMP.

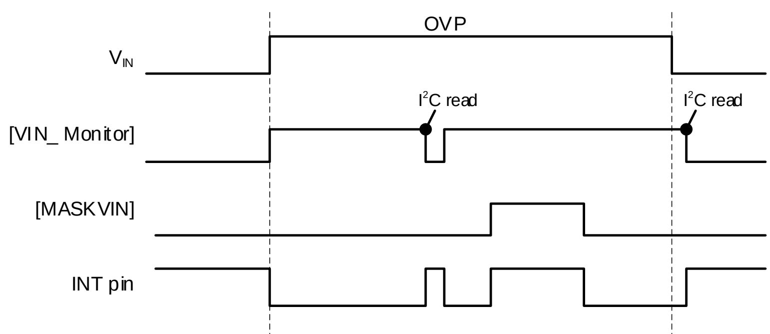

Figure 15. Input OV Protection Interrupt

Temperature Interrupt

The SY21525x provides a thermal warning record bit TEMP_DIE bit in register RECORDTEMP. If the temperature of the device is higher than 109°C, the bit is set to 1 and the INT pin is pulled low. The bit can be reset to 0 after it is read if the temperature drops below 94°C. This interrupt can be masked by bit MASKTEMP_DIE in register MASKTEMP.

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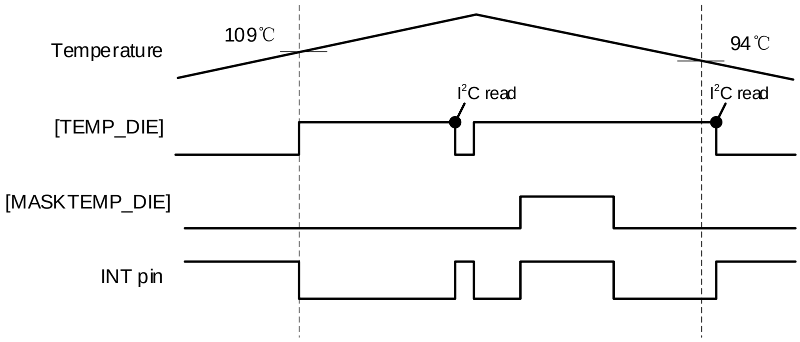

Figure 16. Thermal Warning Interrupt

The SY21525x also provides a thermal shutdown record bit TEMP_SD in register RECORDTEMP. If the junction temperature is higher than 155°C, the bit is set to 1 and the INT pin is pulled low. The bit can be reset to 0 after it is read if the temperature drops below 140°C. This interrupt can be masked by bit MASKTEMP_SD in register MASKTEMP.

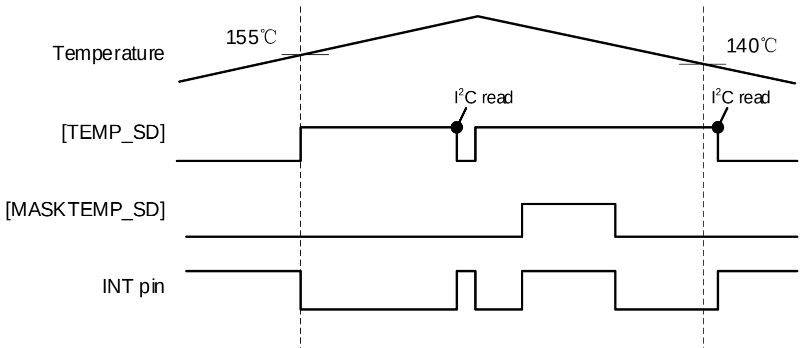

Figure 17. Thermal Shutdown Interrupt

Fault Power Good Interrupt

The SY21525x provides a PGx monitor bit in register RECORDBUCKx to indicate power good state for each buck. If the output voltage is between 90% V_{SET} and 110%V_{SET}, the bit is set to 0, and if the output voltage is out of range, the bit is set to 1. The bit can be reset to 0 after it is read, and if the fault state was cleared. This interrupt can be masked using the MASKPGx bit in register MASKBUCKx.

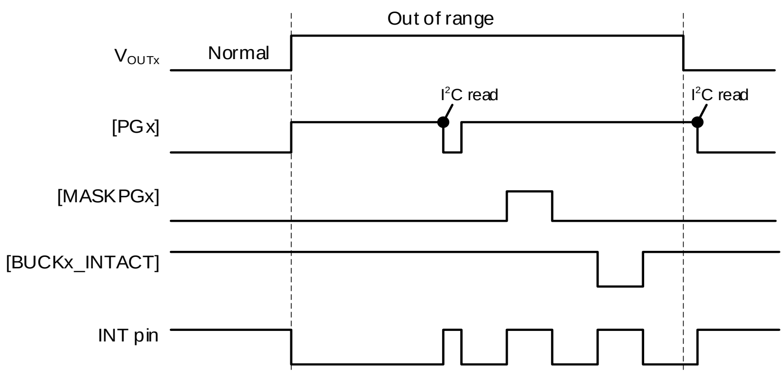

Figure 18. Power Good Interrupt

Overcurrent Interrupt

The SY21525x provides a BUCKx_OC bit in register RECORDBUCKx to indicate an overcurrent state. If an overcurrent state is detected, the bit is set to 1. The bit can be reset to 0 after it is read, and if the fault state was cleared. This interrupt can only be masked by bit BUCKx_INTACT in register MASKBUCKx.

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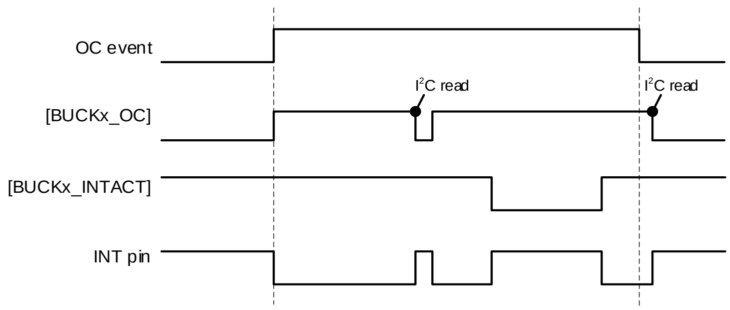

Figure 19. Overcurrent Interrupt

Overvoltage Interrupt

The SY21525x provides a BUCKx_OV bit in register RECORDBUCKx to indicate an overvoltage state. If an overvoltage state is detected, the bit is set to 1. The bit can be reset to 0 after it is read, and if the fault state was cleared. This interrupt can be masked by bits BUCKx_MASKOV and BUCKx_INTACT in register MASKBUCKx.

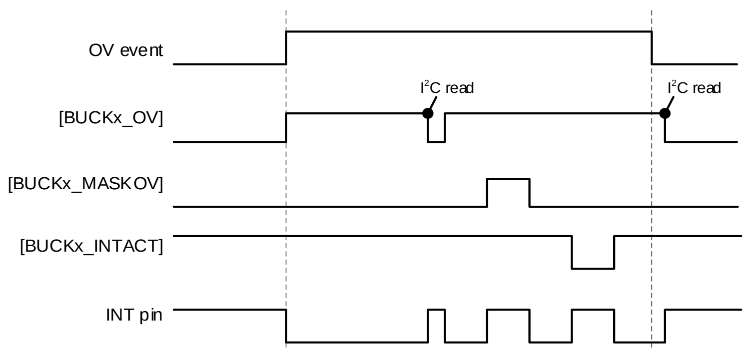

Figure 20. Input Overvoltage Interrupt

Undervoltage Interrupt

The SY21525x provides a BUCKx_UV bit in register RECORDBUCKx to indicate an undervoltage state. If an undervoltage state is detected, the bit is set to 1. The bit can be reset to 0 after it is read, and if the fault state was cleared. This interrupt can be masked by bits BUCKx_MASKUV and BUCKx_INTACT in register MASKBUCKx.

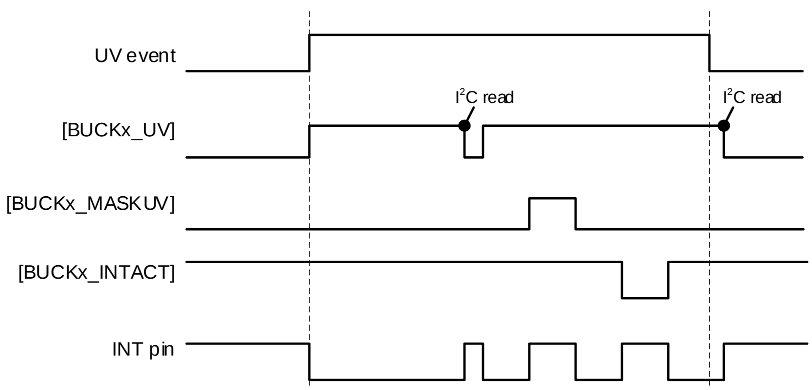

Figure 21. Input Undervoltage Interrupt

Interrupt Condition During Power Sequencing

The global fault detection (input OV protection, thermal warning, and thermal shutdown) is activated once the global EN pin is pulled high. The buck fault (PG, OC, OV, UV) detection is blocked during the normal power-up, shutdown, and DVS periods.

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When the buck is turned off by toggling the global EN pin, the fault record registers RECORDTEMP and RECORDBUCKx will be reset to default values.

When the buck is turned off by software, changing the EN bit will not affect the fault record registers RECORDTEMP and RECORDBUCKx.

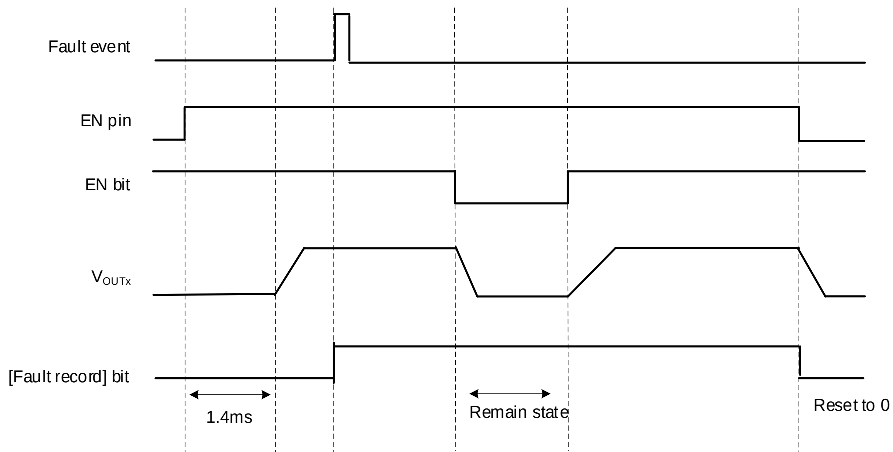

Figure 22. Interrupt Function during Power-Up Sequencing

Component Selection Guide

The following section provides guidance for selecting components, assuming that the buck operates in CCM, and ignoring capacitors' ESL.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (Δi_L) approximately 20%–50% of the desired full output load current of each phase. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_S), the maximum output current (I_{OMAX}) and estimating Δi_L as some percentage of that current.

$$\Delta_{iL} = \frac{V_O}{f_S \cdot L} \cdot (1 - D) = \frac{V_{IN}}{f_s \cdot L} \cdot D \cdot (1 - D)$$

$$iL_{PEAK} = Io + 0.5\Delta_{iL}$$

where $D = \frac{V_O}{V_{IN}}$.

The worst-case condition is $V_{OUT} = 0.5V_{IN}$, and $\Delta_{iL} = \frac{V_{IN}}{4f_S \cdot L}$, $iL_{PEAK} = I_{OMAX} + \frac{V_{IN}}{8f_S \cdot L}$.

Select an inductor with a saturation current and thermal rating in excess of iL_{PEAK}.

If FCCM light load operation is selected, make sure the inductor value is high enough to prevent the reverse current limit from being triggered under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low loss ferrite materials should be considered.

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Inductor Design Example

Consider a typical design for a device providing 1.65V_O at 20A output current and 5A per phase from 3.3V_{IN}, operating at 2MHz and using target inductor ripple current (ΔI_L) of 40% or 2A.

$$\Delta_{iL} = \frac{1.65V}{2MHz \cdot L} \cdot \left(1 - \frac{1.65V}{3.3V}\right) < 2A$$

Conclude from the preceding equation that L > 0.206μH.

For the inductor, a 0.24μH low ESR inductor is suggested for each phase.

$$\Delta_{iL} = \frac{1.65V}{2MHz \cdot 0.24\mu H} \cdot \left(1 - \frac{1.65V}{3.3V}\right) = 1.72A$$

$$iL_{PEAK} = 5A + 0.5 \times 1.72A = 5.29A$$

The resulting 1.72A ripple current is approximately 34.4% (1.72A/5A), well within the 20%–50% target.

Finally, select an available inductor with a saturation current higher than the resulting iL_{PEAK} of 5.29A.

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply, and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability, and high RMS current ratings over a wide temperature and voltage range. Systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{RMS} \approx I_O \cdot \sqrt{D \cdot (1 - D)}$$

$$\Delta_{Vin} = \frac{I_O}{f_S \cdot C_{IN}} \cdot D \cdot (1 - D) + iL_{MAX} \cdot ESR$$

where $I_O = I_{LOAD}/4$.

The worst-case condition is $V_{OUT} = 0.5V_{IN}$, and $\Delta_{VIN} = \frac{0.25 I_O}{f_S \cdot C_{IN}}$, $I_{RMS} = 0.5 I_O$.

The capacitance value is less important than the RMS current rating. Locate the ceramic input capacitor as close to the device IN and GND pins as possible.

For the input capacitor, one 10μF low ESR ceramic capacitor is suggested.

AVIN RC Filter Parameter Selection

The V_{IN} capacitor current for the buck is not continuous, which will generate a large ripple voltage. The heavier the load, the larger the ripple voltage. It is therefore necessary to add an RC filter to decrease AVIN ripple voltage if AVIN connects to PVIN, especially when the converter operates under heavy load. A low pass RC filter is recommended for most applications. The R, C values should satisfy the following equation:

$$f_{CUTOFF} = \frac{1}{2\pi RC} < f_S$$

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Generally, a resistor of 1Ω –5Ω and an MLCC capacitor of 0.1µF-1µF are suggested. Larger RC values are recommended for larger maximum loads.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

$$\Delta_{Vo} = \Delta_{iL}(ESR + \frac{1}{8f_S \cdot C_O})$$

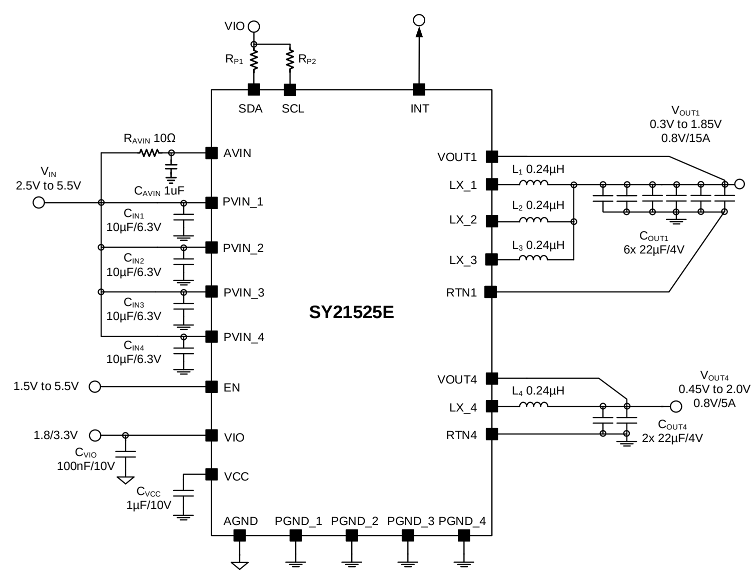
For the output capacitor, two 22µF low ESR ceramic capacitors are suggested for each phase, for a total of 8 pcs in the case of 4 phase operation.

Consider a typical application with ΔiL = 1.72A using eight 22µF ceramic capacitors, each with an ESR of 6mΩ for parallel total of 176µF and 0.75mΩ ESR. A capacitor DC derating 29% at 1.65V was used for the calculation.

$$\Delta_{Vo} = 1.72A \times \left(0.75m\Omega + \frac{1}{8 \times 2MHz \times 176uF \times 71\%}\right) = 2.15mV$$

Application Schematic

(SY21525E example)



BOM List

Designator	Description	Part Number	Manufacturer
U_1	PMIC	SY21525EVCS	Silergy
C_{IN1}, C_{IN2}, C_{IN3}, C_{IN4}	10µF/6.3V,0603,X5R	GRM188D70J106MA73	Murata
C_{AVIN}, C_{VCC}	1µF/10V, 0402, X5R	GRM155C81A105KA12	Murata
C_{VIO}	0.1µF/10V, 0603, X5R	GRM155R71A104MA01	Murata
C_{OUT1}	22µF/4V, 0603, X5R	GRM188C80G226ME15	Murata
L_1, L_2, L_3, L_4	0.24µH, 16mΩ, 2016, 6.8A	DFE201610E-R24M	Murata
R_{P1}, R_{P2}	NC		
R_{AVIN}	10Ω, 0603		

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Layout Design

(SY21525E example)

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitor(s) as close as possible to the PVIN_x and PGND_x pins, minimizing the loop formed by these connections. Connect the input capacitor(s) to the PVIN(s) and PGND(s) pins using a wide copper traces.
- **Inductors and Output Capacitors:**
  - Place the inductor as close as possible to the device while keeping the switch node small. For the best EMI performance, the LX trace must be thick and short enough to minimize the PCB DCR loss.
  - Ensure that the C_{OUT} positive sides are connected to inductors and negative sides are connected to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.
- **Feedback Network and Output Lines:** Avoid routing the feedback lines (VOUT1 and RTN1) near LX_x or other high-frequency signals (SCL/SDA), as they are noise-sensitive. The feedback traces should be routed as a differential pair to the output capacitor using a quiet layer and near the load terminals to achieve better accuracy and load transient response.
- **Analog Power Supply Loop:**
  - Place the AVIN filter capacitor as close as possible to the AVIN and AGND pins, and place the VCC output capacitor between the VCC and AGND pins.
  - Connect the AGND wire to a quiet ground point where no IR drop occurs.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. Maximize the copper area connected to the GND net on the top and bottom layers.

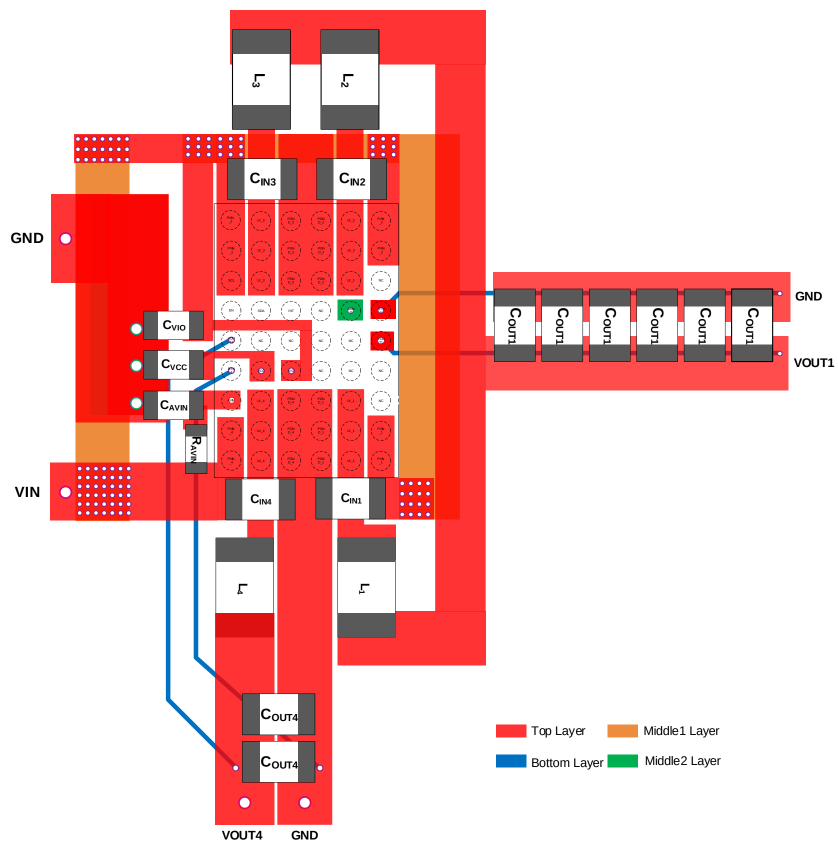

Figure 23. Suggested PCB

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I^2C Communication Interface

The I^2C interface is a bidirectional 2-wire bus protocol, consisting of the Serial Clock Control (SCL) and the Serial Data Signal (SDA). The SY21525x hosts a peripheral I^2C interface that supports data speeds up to 3.4Mbps. SCL is an input to the SY21525x and is supplied by the controller, whereas SDA is bidirectional. The SY21525x uses an open-drain output to transmit data on SDA. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission. The default addresses of the SY21525x are configured by factory one-time-programmable (OTP) configuration registers. The addresses are shown in Table 5 and the I^2C timing spec is show in Table 6.

Table 5. I^2C Timing Spec

Ordering Number	Output Configuration	I^2C Address
SY21525EVCS	3+1 Phase	0x62(01100010)
SY21525FVCS	2+1+1 Phase	0x67(01100111)
SY21525JVCS	2+2 Phase	0x66(01100110)

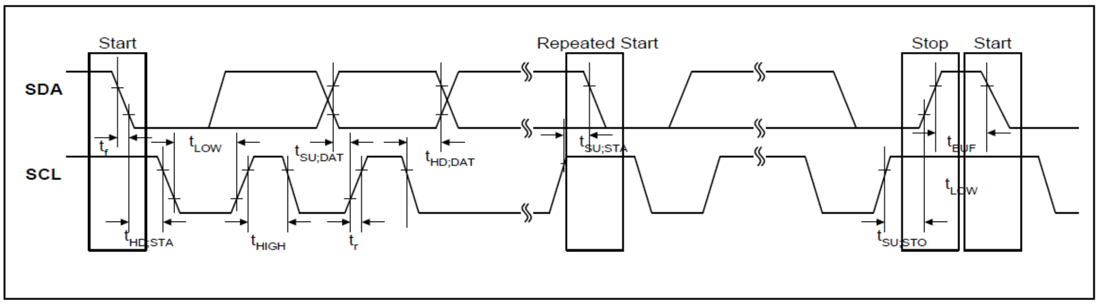

Figure 24. I^2C Timing

Table 6. I^2C Timing Spec

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
Pullup Voltage	VPU	V	1.7V to V_{IO}					
SCL Clock Frequency	f_{SCL}	kHz	0 to 100kHz		0 to 400kHz		0 to 3.4MHz	
Hold Time for a Repeated START Condition	$t_{HD;STA}$	μs	4		0.6		0.16	
Low Period of the SCL Clock	t_{LOW}	μs	4.7		1.3		0.16	
High Period of the SCL Clock	t_{HIGH}	μs	4		0.6		0.06	
Setup Time for a Repeated START Condition	$t_{SU;STA}$	μs	4.7		0.6		0.16	
DATA Hold Time	$t_{HD;DAT}$	ns	0	900	0	900	0	70
Data Setup Time	$t_{SU;DAT}$	ns	250		100		10	
Rise Time of both SDA and SCL Signals	t_R	ns		1000	5	300	5	40
Fall Time of both SDA and SCL Signals	t_F	ns		300	5	300	5	40
Setup Time for STOP Condition	$t_{SU;STO}$	μs	4		0.6		0.16	
Bus Free Time between STOP and START Conditions	t_{BUF}	μs	4.7		1.3			
Capacitive Load for Each Bus Line	C_B	pF		400		400		100

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START and STOP Conditions

The device is controlled via an I²C compatible interface. The START condition is a high-to-low transition of the SDA line while SCL is high. The STOP condition is a low-to-high transition on the SDA line while SCL is high. A STOP condition must be sent before each START condition. The I²C host always generates the START and STOP conditions. See Figure 25.

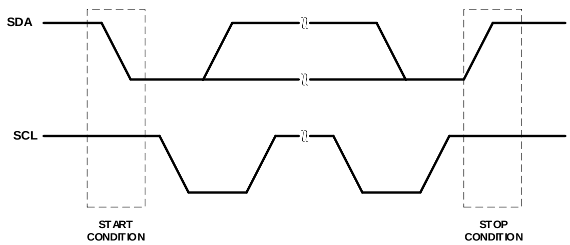

Figure 25. START and STOP

Data Validity

The data on the SDA line must be stable during the high period of the SCL, unless generating a START or STOP condition. The high or low state of the data line can only change when the clock signal on the SCL line is low. See Figure 26.

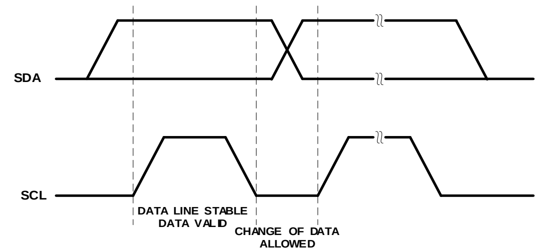

Figure 26. Data Validity

Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the START condition, the host sends seven peripheral address bits and an R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the host and the peripheral to acknowledge receipt of register addresses and data. See Figure 27.

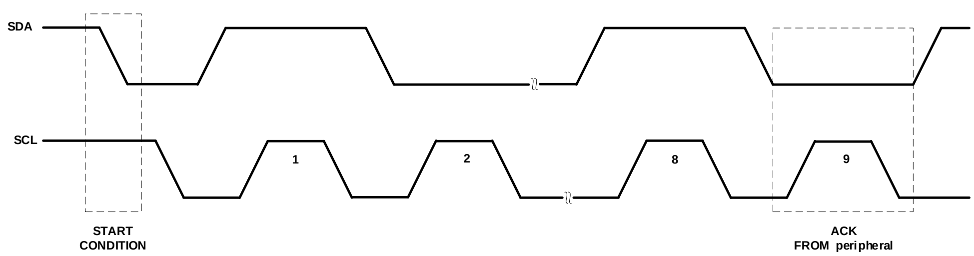

Figure 27. Acknowledge

Data Transactions

All transactions start with a control byte sent from the I²C host device. The control byte begins with a START condition, followed by seven bits of peripheral address (0011101x) for the device (this address can be changed if necessary), followed by the eighth bit, a R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any peripheral devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no peripherals exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the device acknowledges it, the second byte sent by the host must be a register address byte. The register address byte tells the device which registers the host will write or read. Once the device receives a register address byte, it responds with an acknowledge. See Figure 28.

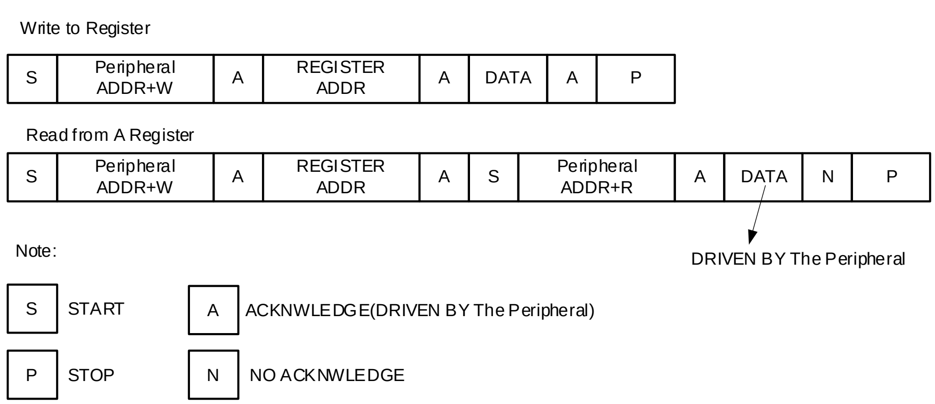

Figure 28. I²C Timing

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Register Map

Register Address Map

No.	Address	Register	No.	Address	Register
1	0x01	IO_CHIPNAME	23	0x49	BUCK1_DVS0CFG0
2	0x02	IO_CHIPVERSION	24	0X54	BUCK1_RSPCFG
3	0x0F	IO_SOFTRESET	25	0X55	BUCK1_SLEWCTRL
4	0x13	RECORDTEMP	26	0x5B	BUCK3_RAMP
5	0x14	RECORDBUCK1	27	0x5F	BUCK3_CFG0
6	0x15	RECORDBUCK3	28	0x62	BUCK3_DVS0CFG1
7	0x16	RECORDBUCK2	29	0x63	BUCK3_DVS0CFG0
8	0x17	RECORDBUCK4	30	0x6E	BUCK3_RSPCFG
9	0x22	IO_I2CCFG	31	0x6F	BUCK3_SLEWCTRL
10	0x30	OT_CTRL	32	0x75	BUCK2_RAMP
11	0x32	MASKTEMP	33	0x79	BUCK2_CFG0
12	0x33	MASKBUCK1	34	0x7C	BUCK2_DVS0CFG1
13	0x34	MASKBUCK3	35	0x7D	BUCK2_DVS0CFG0
14	0x35	MASKBUCK2	36	0x88	BUCK2_RSPCFG
15	0x36	MASKBUCK4	37	0x89	BUCK2_SLEWCTRL
16	0x37	BUCK1_CTRL	38	0x8F	BUCK4_RAMP
17	0x38	BUCK3_CTRL	39	0x93	BUCK4_CFG0
18	0x39	BUCK2_CTRL	40	0x96	BUCK4_DVS0CFG1
19	0x3A	BUCK4_CTRL	41	0x97	BUCK4_DVS0CFG0
20	0x3E	BUCK1_RAMP	42	0xA2	BUCK4_RSPCFG
21	0x42	BUCK1_CFG0	43	0xA3	BUCK4_SLEWCTRL
22	0x48	BUCK1_DVS0CFG1			

Register Description

IO_CHIPNAME				
Register Address:		0x01		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	11111111	CHIPNAME	R	Manufacturer Identification

IO_CHIPVERSION				
Register Address:		0x02		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	00000000	CHIPVERSION	R	Version Number Identification

IO_SOFTRESET				
Register Address:		0x0F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	0	SOFTRESET	R/W	Reset All Registers and Reload from OTP: 0: Do nothing 1: Reset and bit cleared

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RECORDTEMP				
Register Address:		0x13		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	VIN_Monitor	R/W	VIN OVP Occurred Record (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
6:3	0000	-	-	-
2	0	TEMP_DIE	R/W	Over temperature Record For Die (109℃) (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
1	0	TEMP_SD	R/W	Over temperature Shutdown Record (150℃) (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
0	0	-	-	-

RECORDBUCK1				
Register Address:		0x14		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	PG1	R/W	Output Power Good for Buck 1 0: 110% V_{SET} > VOUT1 > 90% V_{SET}. 1: VOUT1 is out of range, send interrupt request
6	0	BUCK1_OC	R/W	Overcurrent for Buck 1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
5	0	BUCK1_OV	R/W	Overvoltage for Buck 1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
4	0	BUCK1_UV	R/W	Undervoltage for Buck 1 (cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
3-0	0000	-	-	-

RECORDBUCK3				
Register Address:		0x15		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	PG3	R/W	Refer to RECORDBUCK1
6	0	BUCK3_OC	R/W	
5	0	BUCK3_OV	R/W	
4	0	BUCK3_UV	R/W	
3-0	0000	-	-	

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RECORDBUCK2				
Register Address:		0x16		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	PG2	R/W	Refer to RECORDBUCK1
6	0	BUCK2_OC	R/W	
5	0	BUCK2_OV	R/W	
4	0	BUCK2_UV	R/W	
3-0	0000	-	-	

RECORDBUCK4				
Register Address:		0x17		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	PG4	R/W	Refer to RECORDBUCK1
6	0	BUCK4_OC	R/W	
5	0	BUCK4_OV	R/W	
4	0	BUCK4_UV	R/W	
3-0	0000	-	-	

IO_I2CCFG				
Register Address:		0x22		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	Reserved	R/W	
6:0	refer to Table #x	I2C_ADDRESS	R	I²C device address setting, programmed by factory

OT_CTRL				
Register Address:		0x30		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	0	OT_CTRL	R/W	Over temperature Shutdown Mode 0: Shutdown and auto recover 1: Do nothing
2:0	000	-	-	-

MASKTEMP				
Register Address:		0x32		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	MASKVIN	R/W	Mask IRQ for VIN OVP 0: Pass IRQ to INT pin. 1: Mask IRQ.
6:3	0000	-	-	-
2	0	MASKTEMP_DIE	R/W	Mask IRQ for Hot Die 0: Pass IRQ to INT pin. 1: Mask IRQ
1	0	MASKTEMP_SD	R/W	Mask IRQ for Thermal Shutdown 0: Pass IRQ to INT pin. 1: Mask IRQ.

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0	0	-	-	-

MASKBUCK1				
Register Address:		0x33		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	BUCK1 _MASKPG	R/W	Mask IRQ for PG1 0: Pass IRQ to INT pin 1: Mask IRQ
6	0	BUCK1_INTACT	R/W	Enable or Disable Buck1 INT Function 0: Disable 1: Enable Metal change available for the default value
5	0	BUCK1 _MASKOV	R/W	Mask IRQ for BUCK1_OV 0: Pass IRQ to INT pin. 1: Mask IRQ
4	0	BUCK1 _MASKUV	R/W	Mask IRQ for BUCK1_UV 0: Pass IRQ to INT pin 1: Mask IRQ
3:0	0000	-	-	-

MASKBUCK3				
Register Address:		0x34		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	BUCK3 _MASKPG	R/W	Refer to MASKBUCK1
6	0	BUCK3_INTACT	R/W	
5	0	BUCK3 _MASKOV	R/W	
4	0	BUCK3 _MASKUV	R/W	
3:0	0000	-	-	

MASKBUCK2				
Register Address:		0x35		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	BUCK2 _MASKPG	R/W	Refer to MASKBUCK1
6	0	BUCK2_INTACT	R/W	
5	0	BUCK2 _MASKOV	R/W	
4	0	BUCK2 _MASKUV	R/W	
3:0	0000	-	-	

MASKBUCK4				
Register Address:		0x36		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	BUCK4_MASKPG	R/W	Refer to MASKBUCK1
6	0	BUCK4_INTACT	R/W	
5	0	BUCK4_MASKOV	R/W	
4	0	BUCK4_MASKUV	R/W	

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3:0	0000	-	-	

BUCK1_CTRL				
Register Address:		0x37		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	1	BUCK1_CTRL	R/W	Protection Mode For UV 0: UV Shutdown and latch off 1: UV Hiccup
2:0	000	-	-	-

BUCK3_CTRL				
Register Address:		0x38		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Similar to BUCK1_CTRL
3	1	BUCK3_CTRL	R/W	
2:0	000	-	-	

BUCK2_CTRL				
Register Address:		0x39		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Similar to BUCK1_CTRL
3	1	BUCK2_CTRL	R/W	
2:0	000	-	-	

BUCK4_CTRL				
Register Address:		0x3A		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Similar to BUCK1_CTRL
3	1	BUCK4_CTRL	R/W	
2:0	000	-	-	

BUCK1_RAMP				
Register Address:		0x3E		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Operating Mode during DVS low to high transitions 0: Controlled by OP_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Operating Mode during DVS high to low transitions 0: Controlled by OP_MODE bit 1: Forced PWM
1:0	00	-	-	-

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BUCK1_CFG0				
Register Address:		0x42		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0:.Disable 1: Enable

BUCK1_DVS0CFG1				
Register Address:		0x48		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	Refer to Table 1	BUCK1_DVS0	R/W	8-bit DAC[7:0] Value to Generate VOUT for DVS Configuration 0 Refer to Table 2 and Table 3.

BUCK1_DVS0CFG0				
Register Address:		0x49		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	OP_MODE	R/W	Buck 1 Operating Mode 0: Automatic PFM/PWM 1:Forced PWM
4:1	0000	-	-	-
0	0	BUCK1_EN_DVS	R/W	Enable Buck 1 0: Disable, VOUT1=0 1: Enable

<table>
<tr><th colspan="5">BUCK1_RSPCFG</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x54</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>6:4</td><td>001</td><td>BUCK1_RSPUP</td><td>R/W</td><td><table>
<tr><td></td><td>Ramp-Up Speed mV/μs</td></tr>
<tr><td>001</td><td>16</td></tr>
<tr><td>011</td><td>8</td></tr>
<tr><td>100</td><td>4</td></tr>
<tr><td>101</td><td>2</td></tr>
<tr><td>110</td><td>1</td></tr>
<tr><td>111</td><td>0.5</td></tr>
</table></td></tr>
<tr><td>3</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2:0</td><td>100</td><td>BUCK1_RSPDN</td><td>R/W</td><td><table>
<tr><td></td><td>Ramp-Down Speed mV/μs</td></tr>
<tr><td>001</td><td>16</td></tr>
<tr><td>011</td><td>8</td></tr>
<tr><td>100</td><td>4</td></tr>
<tr><td>101</td><td>2</td></tr>
<tr><td>110</td><td>1</td></tr>
<tr><td>111</td><td>0.5</td></tr>
</table></td></tr>
</table>

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BUCK1_SLEWCTRL				
Register Address:		0x55		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK1_POWERUP	R/W	<table><tr><td></td><td>Power-Up Speed mV/µs</td></tr><tr><td>00</td><td>10</td></tr><tr><td>01</td><td>5</td></tr><tr><td>10</td><td>2.5</td></tr><tr><td>11</td><td>1.25</td></tr></table>
3:0	0000	-	-	-

BUCK3_RAMP				
Register Address:		0x5B		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Operating Mode for DVS low to high transtions 0: Controlled by OP_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Operating Mode for DVS high to low transitions 0: Controlled by OP_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK3_CFG0				
Register Address:		0x5F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0:.Disable 1: Enable

BUCK3_DVS0CFG1				
Register Address:		0x62		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	Refer to Table 1	BUCK3_DVS0	R/W	8-bit DAC[7:0] Value to Generate VOUT for DVS Configuration 0 Refer to Table 2 and Table 3.

BUCK3_DVS0CFG0				
Register Address:		0x63		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	OP_MODE	R/W	Buck 3 Operating Mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK3_EN_DVS	R/W	Enable Buck 3 0: Disable 1: Enable

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BUCK3_RSPCFG				
Register Address:		0x6E		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK3_RSPUP	R/W	Ramp-Up Speed mV/µs 001: 16 011: 8 100: 4 101: 2 110: 1 111: 0.5
3	0	-	-	-
2:0	100	BUCK3_RSPDN	R/W	Ramp-Down Speed mV/µs 001: 16 011: 8 100: 4 101: 2 110: 1 111: 0.5

BUCK3_SLEWCTRL				
Register Address:		0x6F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK3_POWERUP	R/W	Power-Up Speed mV/µs 00: 10 01: 5 10: 2.5 11: 1.25
3:0	0000	-	-	-

BUCK2_RAMP				
Register Address:		0x75		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Operating Mode for DVS low to high transitions 0: Controlled by OP_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Operating Mode for DVS high to low trasitions 0: Controlled by OP_MODE bit 1: Forced PWM
1:0	00	-	-	-

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BUCK2_CFG0				
Register Address:		0x79		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0:.Disable 1: Enable

BUCK2_DVS0CFG1				
Register Address:		0x7C		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	Refer to Table 1	BUCK2_DVS0	R/W	8-bit DAC[7:0] Value to Generate VOUT for DVS Configuration 0 Refer to Table 2 and Table 3.

BUCK2_DVS0CFG0				
Register Address:		0x7D		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	OP_MODE	R/W	Buck 2 Operating Mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK2_EN_DVS	R/W	Enable Buck 2 0: Disable 1: Enable

<table>
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<tr><td colspan="2">Register Address:</td><td>0x88</td><td></td><td></td></tr>
<tr><td>Bits</td><td>Default</td><td>Signal Name</td><td>R/W</td><td>Description</td></tr>
<tr><td>7</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>6:4</td><td>001</td><td>BUCK2_RSPUP</td><td>R/W</td><td><table><tr><td></td><td>Ramp-Up Speed mV/μs</td></tr><tr><td>001</td><td>16</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>4</td></tr><tr><td>101</td><td>2</td></tr><tr><td>110</td><td>1</td></tr><tr><td>111</td><td>0.5</td></tr></table></td></tr>
<tr><td>3</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2:0</td><td>100</td><td>BUCK2_RSPDN</td><td>R/W</td><td><table><tr><td></td><td>Ramp-Down Speed mV/μs</td></tr><tr><td>001</td><td>16</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>4</td></tr><tr><td>101</td><td>2</td></tr><tr><td>110</td><td>1</td></tr><tr><td>111</td><td>0.5</td></tr></table></td></tr>
</table>

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BUCK2_SLEWCTRL				
Register Address:		0x89		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	00	BUCK2_POWERUP	R/W	<table><tr><td></td><td>Power-Up Speed mV/µs</td></tr><tr><td>00</td><td>10</td></tr><tr><td>01</td><td>5</td></tr><tr><td>10</td><td>2.5</td></tr><tr><td>11</td><td>1.25</td></tr></table>
3:0	0000	-	-	-

BUCK4_RAMP				
Register Address:		0x8F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Operating Mode during DVS low to high transitions 0: Controlled by OP_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Operating Mode during DVS high to low transitions 0: Controlled by OP_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK4_CFG0				
Register Address:		0x93		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0: Disable 1: Enable

BUCK4_DVS0CFG1				
Register Address:		0x96		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	Refer to table 1	BUCK4_DVS0	R/W	8-bit DAC[7:0] Value to Generate VOUT for DVS Configuration 0 Refer to Table 2 and Table 3.

BUCK4_DVS0CFG0				
Register Address:		0x97		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	1	OP_MODE	R/W	Buck 4 Operating Mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	0	BUCK4_EN_DVS	R/W	Enable Buck 4 0: Disable 1: Enable

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<table>
<tr><th colspan="5">BUCK4_RSPCFG</th></tr>
<tr><td colspan="2">Register Address:</td><td>0xA2</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>6:4</td><td>001</td><td>BUCK4_RSPUP</td><td>R/W</td><td><table><tr><td></td><td>DVS Up Speed mV/μs</td></tr><tr><td>001</td><td>16</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>4</td></tr><tr><td>101</td><td>2</td></tr><tr><td>110</td><td>1</td></tr><tr><td>111</td><td>0.5</td></tr></table></td></tr>
<tr><td>3</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2:0</td><td>100</td><td>BUCK4_RSPDN</td><td>R/W</td><td><table><tr><td></td><td>DVS Down Speed mV/μs</td></tr><tr><td>001</td><td>16</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>4</td></tr><tr><td>101</td><td>2</td></tr><tr><td>110</td><td>1</td></tr><tr><td>111</td><td>0.5</td></tr></table></td></tr>
</table>

<table>
<tr><th colspan="5">BUCK4_SLEWCTRL</th></tr>
<tr><td colspan="2">Register Address:</td><td>0xA3</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>00</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>00</td><td>BUCK4_POWERUP</td><td>R/W</td><td><table><tr><td></td><td>Power-Up Slew Rate</td></tr><tr><td>00</td><td>10 mV/μs</td></tr><tr><td>01</td><td>5 mV/μs</td></tr><tr><td>10</td><td>2.5 mV/μs</td></tr><tr><td>11</td><td>1.25 mV/μs</td></tr></table></td></tr>
<tr><td>3:0</td><td>0000</td><td>-</td><td>-</td><td>-</td></tr>
</table>

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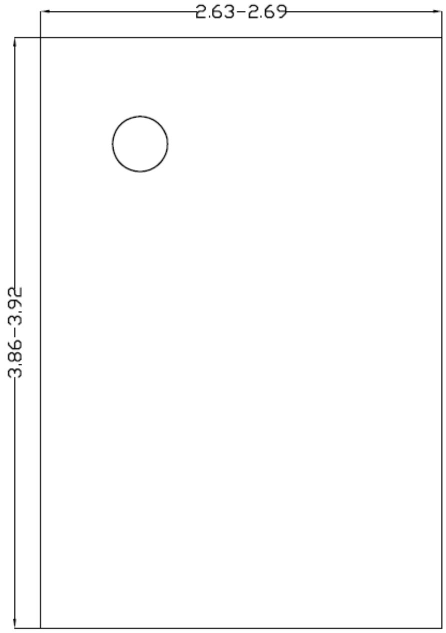
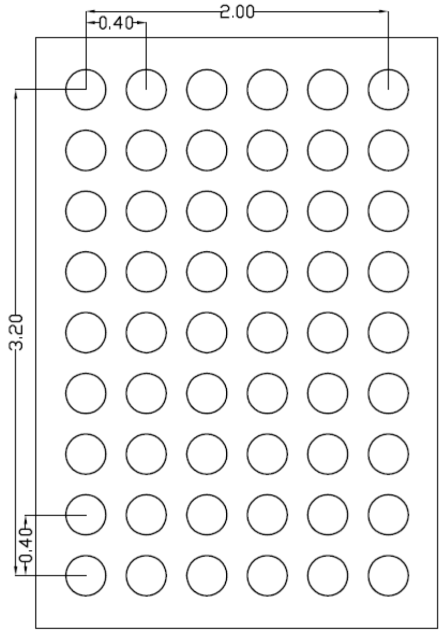
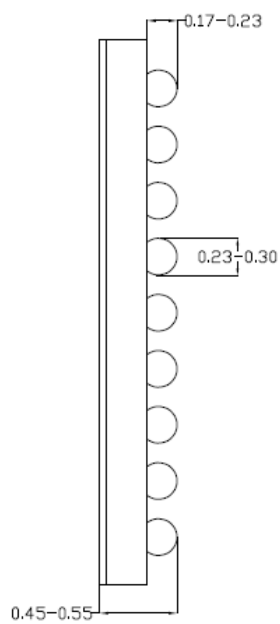
CSP2.66×3.89-54 Package Outline Drawing



Top View



Side View



Bottom View

Notes: *All dimensions are in millimeter and exclude mold flash and metal burr.*

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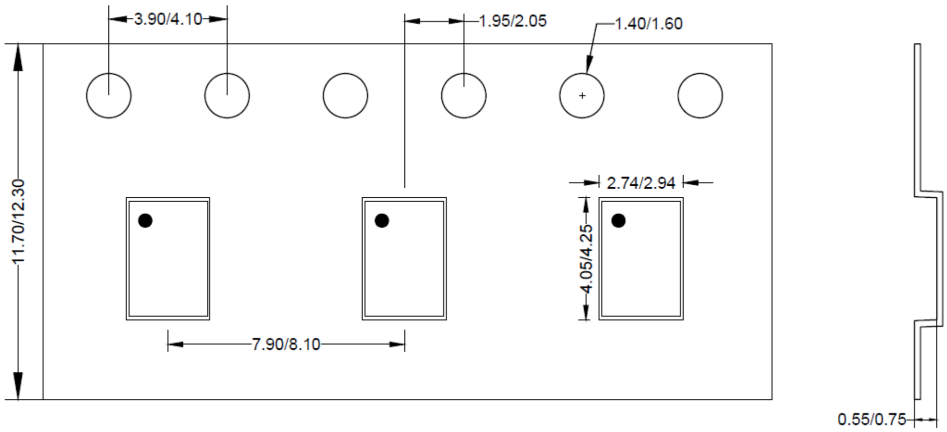
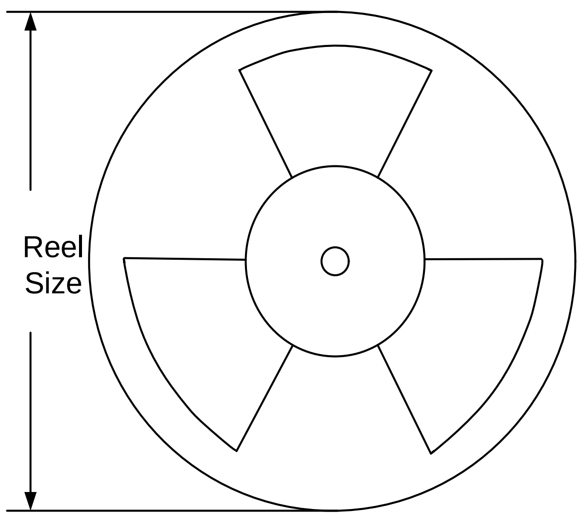
Tape and Reel Specification

CSP2.66×3.89-54 Taping Orientation



Direction of feed

Carrier Tape and Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
CSP2.66×3.89-54	12	8	13"	400	400	5000

All Dimension are nominal

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Nov. 07, 2024	Revision 1.0	SY21525J initial release.
Feb. 21, 2025	Revision 1.0	SY21525E/SY21525F initial release.

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