SY33519

Mixed-Signal Programmable Logic Device

1 General Description

The SY33519 is a programmable logic device with mixed-signal functions. It provides configurable logic, flexible control, and mixed-signal generation functions. It serves as an ideal replacement for discrete logic circuits, acting as a companion device for complex systems. It helps reduce PCB size, lower BOM costs, and provide a fast and cost-effective solution for specific applications.

2 Applications

- Computers and Servers
- PC Peripherals
- Smart Phone
- Handheld Terminals
- Consumer Electronics

3 Features

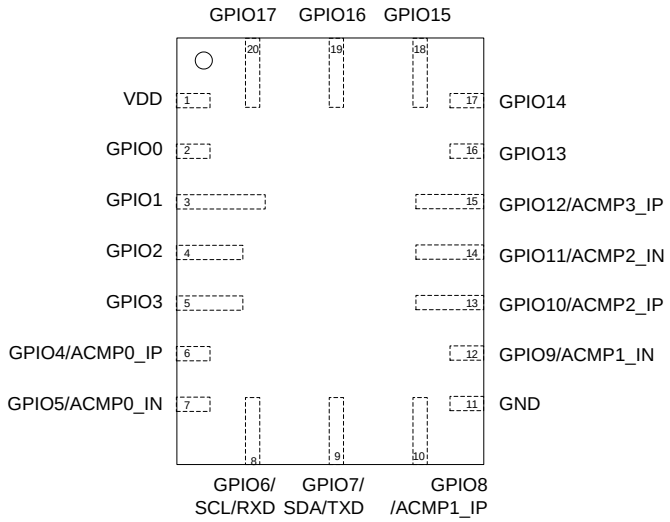
- 18 General-Purpose I/O (GPIO) Pins
- Nine 2-bit LUTs
- Nine 3-bit LUTs
- One 4-bit LUT
- Four DFF/Latches
- Nine CNT/Delays: Two for 16-bit CNT/Delays, Seven for 8-bit CNT/Delays
- Two Analog Glitch Filters
- One Asynchronous State Machine (ASM)
- Four Analog Comparators (ACMP)
- Embedded Crossbar for Application Flexibility
- On-Chip Voltage References (Vref)
- On-Chip RC Oscillators: 25kHz, 2MHz, 25MHz
- Serial Communication Interface by I^2C or UART
- 20-Pin QFN (2×3×0.55mm) Package
- MSL Rating: MSL1

4 Ordering Information

Ordering Part Number	Package Type	Top Mark
SY33519VYQ	QFN2×3-20	**HQH**xyz

Note： ***x=year code, y=week code, z=lot number code.***

5 Pinout (Top View)



(QFN2×3-20)

6 Pin Description

Pin Number	Pin Name	Pin Description
1	VDD	Power pin.
2	GPIO0	General Purpose input pin.
3	GPIO1	General Purpose I/O pin.
4	GPIO2	General Purpose I/O pin.
5	GPIO3	General Purpose I/O pin.
6	GPIO4	General Purpose I/O pin or ACMP0 IN+.
7	GPIO5	General Purpose I/O pin or ACMP0 IN-.
8	GPIO6/SCL/RXD	General Purpose I/O pin or I^2C SCL or UART RXD.
9	GPIO7/SDA/TXD	General Purpose I/O pin or I^2C SDA or UART TXD.
10	GPIO8	General Purpose I/O pin or ACMP1 IN+.
11	GND	Ground pin.
12	GPIO9	General Purpose I/O pin or ACMP1 IN-.
13	GPIO10	General Purpose I/O pin or ACMP2 IN+.
14	GPIO11	General Purpose I/O pin or ACMP2 IN-.
15	GPIO12	General Purpose I/O pin or ACMP3 IN+.
16	GPIO13	General Purpose I/O pin.
17	GPIO14	General Purpose I/O pin.
18	GPIO15	General Purpose I/O pin.
19	GPIO16	General Purpose I/O pin.
20	GPIO17	General Purpose I/O pin or External Clock Input.

7 Functional Block Diagram and Application Circuit

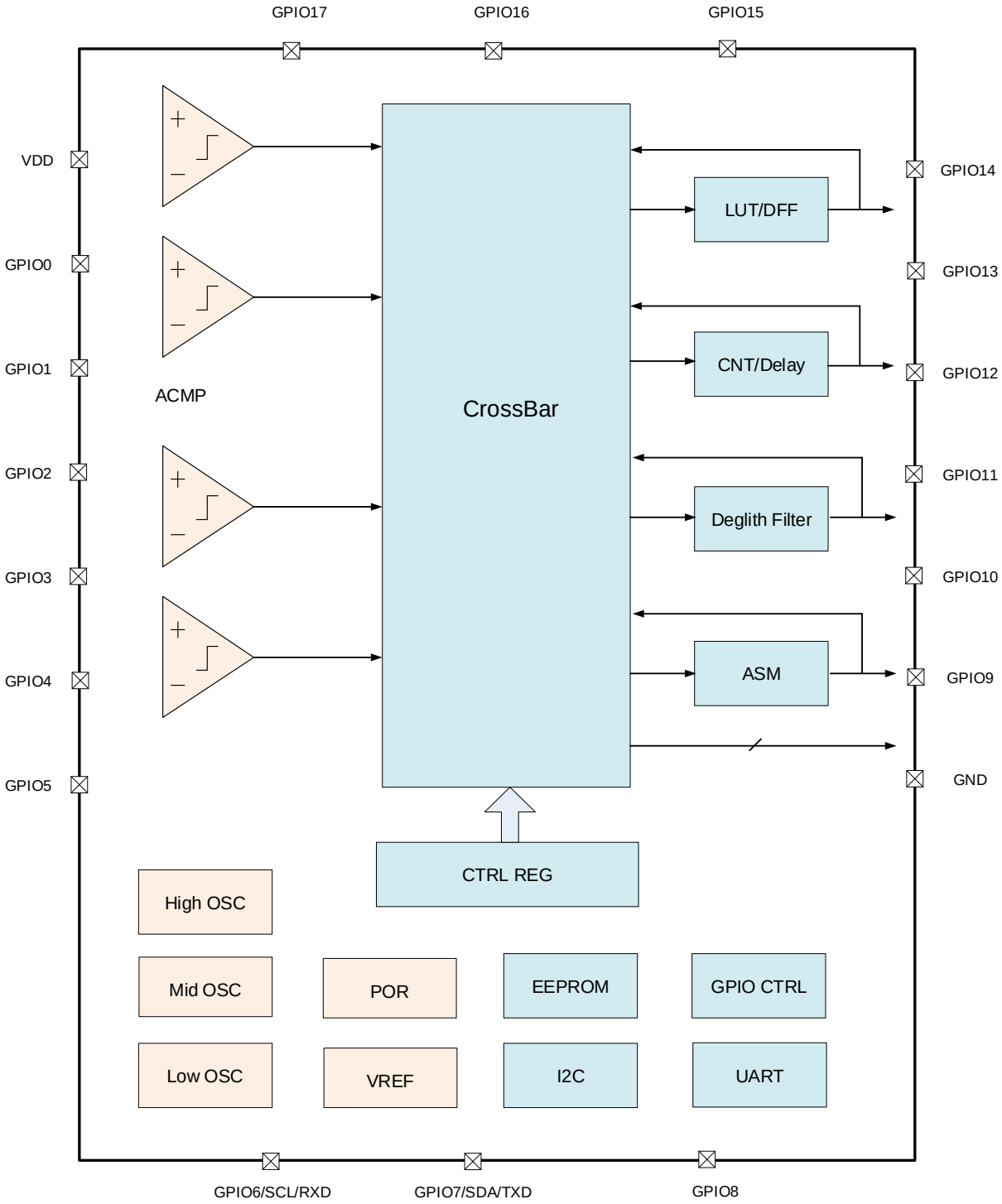


Figure 7-1. Simplified Block Diagram and Application Circuit

8 Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VDD	-0.3	6	V
DC Input Voltage	GND-0.3	V_{VDD} +0.3	
Junction Temperature		150	°C
Storage Temperature Range	-65	150	
ESD: HBM (Human Body Model)	2000		V
ESD: CDM (Charged Device Model)	1000		V

9 Thermal Information

Parameter (Note 2)	Value	Unit
Power Dissipation, PD at T_A = 25°C	0.497	W
θ_{JA} Junction-to-Ambient Thermal Resistance	161	°C/W
θ_{JC} Junction-to-Case (Top) Thermal Resistance	20	

10 Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VDD Supply Voltage (VDD range 2)	3.0	3.6	V
VDD Supply Voltage (VDD range 3)	4.5	5.5	V
GPIOx and Digital Input	0	V_{VDD}	V
ACMPx and Analog Input	0	V_{VDD}	V
Junction Temperature Range	-40	105	°C
Ambient Temperature Range	-40	85	°C

11 Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

11.1 General Specs with V_{VDD} =3.3V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power and Operation Conditions						
Supply Power Voltage	V_{VDD}		3	3.3	3.6	V
Supply Power Voltage POR Threshold	V_{POR}		1.41	1.54	1.66	V
Supply Power Voltage UVLO Threshold	V_{DD_UVLO}		1	1.34	1.57	V
Default Operation Current	I_{NOR}	Average DC current on V_{VDD} (Unprogrammed chip)			130	μA
Input / Output						
Input High Voltage	V_{IH}	Normal input	1.81		V_{VDD}	V
		Schmitt trigger input	2.14		V_{VDD}	V
		Low voltage input	1.06		V_{VDD}	V
Input Low Voltage	V_{IL}	Normal input	0		1.31	V
		Schmitt trigger input	0		0.97	V
		Low voltage input	0		0.67	V
Output High Voltage	V_{OH}	Push-pull, I_{OH}=3mA, normal drive	2.61	3.1		V
		Push-pull, I_{OH}=3mA, high drive	2.8	3.2		V
Output Low Voltage	V_{OL}	Push-pull, I_{OL}=3mA, normal drive		0.13	0.23	V
		Push-pull, I_{OL}=3mA, high drive		0.06	0.11	V
		Open-drain, I_{OL}=3mA, normal drive		0.08	0.15	V
		Open-drain, I_{OL}=3mA, high drive		0.04	0.08	V
Pull Up Resistance	R_{PU}	1M pull up		1		MΩ
		100kΩ pull up		100		kΩ
		10kΩ pull up		10		kΩ
Pull Down Resistance	R_{PD}	1MΩ pull down		1		MΩ
		100kΩ pull down		100		kΩ
		10kΩ pull down		10		kΩ

11.2 General Specs with V_{VDD} =5.0V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power and Operation Conditions						
Supply Power Voltage	V_{VDD}		4.5	5	5.5	V
Supply Power Voltage POR Threshold	V_{POR}		1.41	1.54	1.66	V
Supply Power Voltage UVLO Threshold	V_{DD_UVLO}		1	1.34	1.57	V
Default Operation Current	I_{NOR}	Average DC Current on V_{VDD} (unprogrammed chip)			150	μA
Input/Output						
Input High Voltage	V_{IH}	Normal input	2.68		V_{VDD}	V
		Schmitt trigger input	3.34		V_{VDD}	V
		Low voltage input	1.15		V_{VDD}	V
Input Low Voltage	V_{IL}	Normal input	0		1.96	V
		Schmitt trigger input	0		1.41	V
		Low voltage input	0		0.77	V
Output High Voltage	V_{OH}	Push-pull, I_{OH}=5mA, normal drive	4.14	4.76		V
		Push-pull, I_{OH}=5mA, high drive	4.32	4.89		V
Output Low Voltage	V_{OL}	Push-pull, I_{OL}=5mA, normal drive		0.19	0.24	V
		Push-pull, I_{OL}=5mA, high drive		0.09	0.12	V
		Open-drain, I_{OL}=5mA, normal drive		0.12	0.16	V
		Open-drain, I_{OL}=5mA, high drive		0.07	0.08	V
Pull Up Resistance	R_{PU}	1MΩ pull up		0.8		MΩ
		100kΩ pull up		100		kΩ
		10kΩ pull up		10		kΩ
Pull Down Resistance	R_{PD}	1MΩ pull down		0.8		MΩ
		100kΩ pull down		100		kΩ
		10kΩ pull down		10		kΩ

11.3 ACMP Specs

Parameter	Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Analog Comparator (ACMP)							
ACMP Input Voltage Range	V_{ACMP_P}	Positive Input		0		V_{VDD}	V
	V_{ACMP_N}	Negative Input		0		$V_{VDD}/2$	V
ACMP Input Offset Voltage	V_{OFFSET}	Low Bandwidth - Enable, V_{HYS} = 0 mV, Gain = 1, V_{REF} = 50~1200mV	T_A= 25°C	-10		10	mV
			T_A= -40°C to +85°C	-11.9		11.7	
		Low Bandwidth - Disable, V_{HYS} = 0 mV, Gain = 1, V_{REF} = 50~1200 mV	T_A= 25°C	-10		10	mV
			T_A= -40°C to +85°C	-11.9		11.7	
Built-In Hysteresis	V_{HYS}	V_{HYS} = 25 mV V_{IL} = V_{REF} - V_{HYS} /2 V_{IH} = V_{REF} + V_{HYS} /2	T_A = 25°C, Low Bandwidth Enable	7.32		35.5	mV
			T_A = 25°C, Low Bandwidth Disable	10		38.5	
		V_{HYS} = 50mV V_{IL} = V_{REF} - V_{HYS} V_{IH} = V_{REF}	T_A = 25°C, Low Bandwidth Enable	42.9		58.7	mV
			T_A = 25°C, Low Bandwidth Disable	44.2		54.3	
		V_{HYS} = 200 mV V_{IL} = V_{REF} - V_{HYS} V_{IH} = V_{REF}	T_A = 25°C, Low Bandwidth Enable	169		241	mV
			T_A = 25°C, Low Bandwidth Disable	170		240	
		V_{HYS} = 25 mV V_{IL} = V_{REF} - V_{HYS} /2 V_{IH} = V_{REF} + V_{HYS} /2	T_A = -40°C to +85°C, Low Bandwidth Enable	0		58	mV
			T_A = -40°C to +85°C, Low Bandwidth Disable	0		52.9	
		V_{HYS} = 50mV V_{IL} = V_{REF} - V_{HYS} V_{IH} = V_{REF}	T_A = -40°C to +85°C, Low Bandwidth Enable	22.5		86.9	mV
			T_A = -40°C to +85°C, Low Bandwidth Disable	29.2		76.5	
		V_{HYS} = 200 mV V_{IL} = V_{REF} - V_{HYS} V_{IH} = V_{REF}	T_A = -40°C to +85°C, Low Bandwidth Enable	157.1		251.6	mV
			T_A = -40°C to +85°C, Low Bandwidth Disable	160.2		245.3	
Series Input Resistance	R_{SIN}	Gain = 1x			130		MΩ
		Gain = 0.5x			0.6		MΩ
		Gain = 0.33x			0.6		MΩ
		Gain = 0.25x			0.6		MΩ
Gain Error (Including Threshold and Internal V_{REF} Error)	Gain	Gain = 1, V_{VDD} = 3.3 V	T_A= -40°C to +85°C V_{REF} = 50~1200 mV		1		-
		Gain = 1, V_{VDD} = 5 V			1		
		Gain = 0.5, V_{VDD} = 3.3 V		-0.96%		0.82%	
		Gain = 0.5, V_{VDD} = 5 V		-1.04%		0.90%	
		Gain = 0.33, V_{VDD} = 3.3 V		-1.95%		1.69%	
		Gain = 0.33, V_{VDD} = 5 V		-2.03%		1.77%	
		Gain = 0.25, V_{VDD} = 3.3 V		-1.98%		1.80%	
		Gain = 0.25, V_{VDD} = 5 V		-2.12%		1.90%	
Propagation Delay, Response Time	PROP	Low Bandwidth - Disable, Gain = 1, V_{VDD} =3.3~5.5V, Overdrive=5 mV	Low to High, T_A= -40°C to +85°C		5	32.62	µs
			High to Low, T_A= -40°C to +85°C		5.24	33.88	µs
		Low Bandwidth - Enable, Gain = 1, V_{VDD} =3.3~5.5V, Overdrive=5 mV	Low to High, T_A= -40°C to +85°C		30.62	167.56	µs
			High to Low, T_A= -40°C to +85°C		33.54	181.4	µs

ACMP Power Consumption (Note 5)	I_{CMP}		Low Bandwidth Disable, Hysteresis: 25mv, Gain = 1, Output Latch Disable, V_{VDD} =5V	-	230	-	μA
			Low Bandwidth Enable, Hysteresis: 25mv, Gain = 1, Output Latch Disable, V_{VDD} =5V	-	210	-	μA
Internal V_{REF} Error	V_{REF}	V_{VDD} = 3.3 V ± 10 % V_{REF} = 1200 mV	T_A = 25°C	-0.59		0.58	%
			T_A= -40°C to +85°C	-2.30		2.20	
		V_{VDD} = 5 V ± 10 % V_{REF} = 1200 mV	T_A = 25°C	-0.64		0.60	
			T_A= -40°C to +85°C	-2.20		2.30	
		V_{VDD} = 3.3 V ± 10 % V_{REF} = 1000 mV	T_A = 25°C	-0.59		0.58	
			T_A= -40°C to +85°C	-2.30		2.30	
		V_{VDD} = 5 V ± 10 % V_{REF} = 1000 mV	T_A = 25°C	-0.67		0.64	
			T_A= -40°C to +85°C	-2.20		2.40	
		V_{VDD} = 3.3 V ± 10 % V_{REF} = 500 mV	T_A = 25°C	-0.63		0.63	
			T_A= -40°C to +85°C	-2.50		2.40	
		V_{VDD} = 5 V ± 10 % V_{REF} = 500 mV	T_A = 25°C	-0.72		0.70	
			T_A= -40°C to +85°C	-2.38		2.40	
Internal V_{REF} Drift with Temperature			T_A= -40°C to +85°C	-4.5		4.5	%
ACMP1 Current Source	Iacmp1_ source		With IN+ 10kΩ R_{load}, V_{VDD} =5V	80		130	μA

11.4 Oscillators Specs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Frequency RC Oscillator (HOSC)						
HOSC Frequency	f_H	T_A = 25°C	24	25	26	MHz
HOSC Frequency Drift		T_A = -40°C to +85°C	-4		4	%
HOSC Power Consumption (Note 5)		Full voltage range		100		μA
Mid Frequency RC Oscillator (MOSC)						
MOSC Frequency	f_M	T_A = 25°C	1.95	2	2.05	MHz
MOSC Frequency Drift		T_A =-40°C to +85°C	-3	-	3	%
MOSC Power Consumption (Note 5)		Full voltage range		30		μA
Low Frequency RC Oscillator (LOSC)						
LOSC Frequency	f_L	T_A = 25°C	24	25	26	kHz
LOSC Frequency Drift		T_A =-40°C to +85°C	-4	-	4	%
LOSC Power Consumption (Note 5)		Full voltage range		10		μA

11.5 Deglitch Filter Specs

Parameter	Symbol	Test Conditions	V_{VDD}=3.3V	V_{VDD}=5V	Unit
Filtered Pulse Width for Deglitch Filter0	t_{pulse0}	T_A = 25°C	<180	<180	ns
Filtered Pulse Width for Deglitch Filter1	t_{pulse1}	T_A = 25°C	<110	<110	ns

11.6 ASM Specs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ASM Output Delay Time	$t_{st\_out\_delay}$	V_{VDD} = 3.3 V ± 10%	--	25	--	ns
		V_{VDD} = 5.0 V ± 10%	--	20	--	ns
ASM Input Pulse Acceptance Time	t_{st_pulse}	V_{VDD} = 3.3 V ± 10%	10	--	--	ns
		V_{VDD} = 5.0 V ± 10%	10	--	--	ns
ASM Input Complete Time	t_{st_comp}	V_{VDD} = 3.3 V ± 10%	--	--	15	ns
		V_{VDD} = 5.0 V ± 10%	--	--	15	ns

11.7 I²C Specs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Interface-100kHz						
Clock Operation Frequency	f_{SCL}	SCL Duty=50%			100	kHz
START Condition Hold Time	$t_{HD:STA}$		4			μs
			4.7			μs
			4			μs
			4.7			μs
DATA Hold Time (SDA Input)	$t_{HD:DAT}$		0			ns
DATA Setup Time (SDA Input)	$t_{SU:DAT}$		250			ns
Clock Rise Time	t_r	10%-90%			1000	ns
Clock Fall Time	t_f	90%-10%			300	ns
Setup Time STOP Condition	$t_{SU:STO}$		4			μs
BUS Free Time Stop to Start	t_{BUF}		4.7			μs
I²C Interface-400kHz						
Clock Operation Frequency	f_{SCL}	SCL Duty=50%			400	kHz
START Condition Hold Time	$t_{HD:STA}$		0.6			μs
Low Period of the SCL Clock	t_{LOW}		1.3			μs
High Period of the SCL Clock	t_{HIGH}		600			ns
SETUP Condition Hold Time	$t_{SU:STA}$		600			ns
DATA Hold Time (SDA Input)	$t_{HD:DAT}$		0			ns
DATA Setup Time (SDA Input)	$t_{SU:DAT}$		100			ns
Clock Rise Time	t_r	10%-90%			300	ns
Clock Fall Time	t_f	90%-10%			300	ns
Setup Time STOP Condition	$t_{SU:STO}$		0.6			μs
BUS Free Time Stop to Start	t_{BUF}		1.3			μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is mounted on low effective single layer PCB and tested under still air.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

12 Function Description

12.1 I/O Pins

There are a total of 18 multi-function I/O pins. The GPIO0 (PIN2) can only serve as a digital input pin while the others can serve as both digital input and digital output.

12.1.1 GPIO0

GPIO0 Register Definition (GPIO0 has no pull up option)

Function	Register bit	Register Description
Pull Down Resistor Value Selection	2	00: Floating
		01: Pull Down 10kΩ
		10: Pull Down 100kΩ
		11: Pull Down 1MΩ
Input Mode Control	2	00: Digital Input without Schmitt Trigger
		01: Digital Input with Schmitt Trigger
		10: Low Voltage Digital Input
		11: Reserved

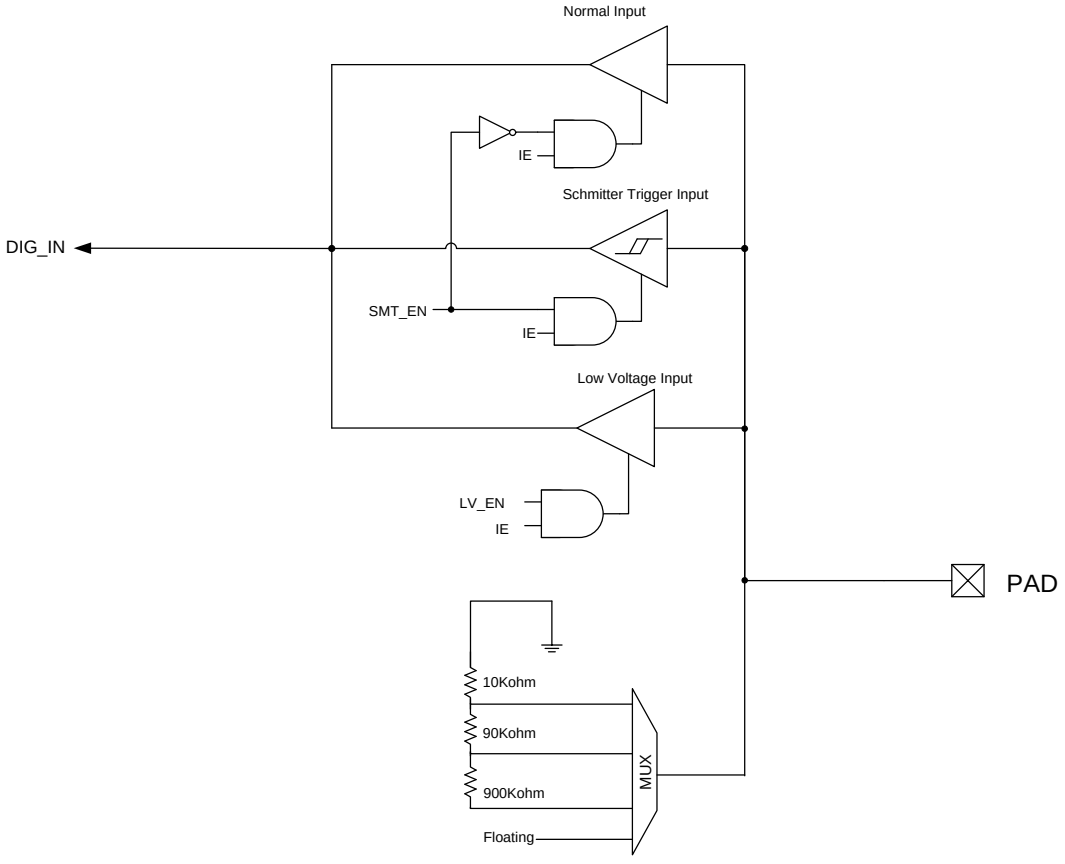


Figure 12-1. GPIO0 Block Diagram

12.1.2 GPIO1~17

GPIO1~17 Register Definition

Function	Register Bit	Register Description
Pull Up/Down	1	0: Pull Down
		1: Pull Up
Pull Resistor Value Selection	2	00: Floating
		01: 10kΩ
		10: 100kΩ
		11: 1MΩ
Input Mode Control	2	00: Digital Input without Schmitt Trigger
		01: Digital Input with Schmitt Trigger
		10: Low Voltage Digital Input
		11: Analog input/output (digital output disable, digital input disable, and pull disable)（Note 6）
Output Mode Control	2	00: Push Pull Normal Drive
		01: Push Pull High Drive
		10: Open Drain Normal Drive
		11: Open Drain High Drive

Note 6: The analog function is only available when GPIO4/5/8/9/10/11/12 are used as ACMP inputs. If any other GPIOs are used, the analog function cannot be utilized.

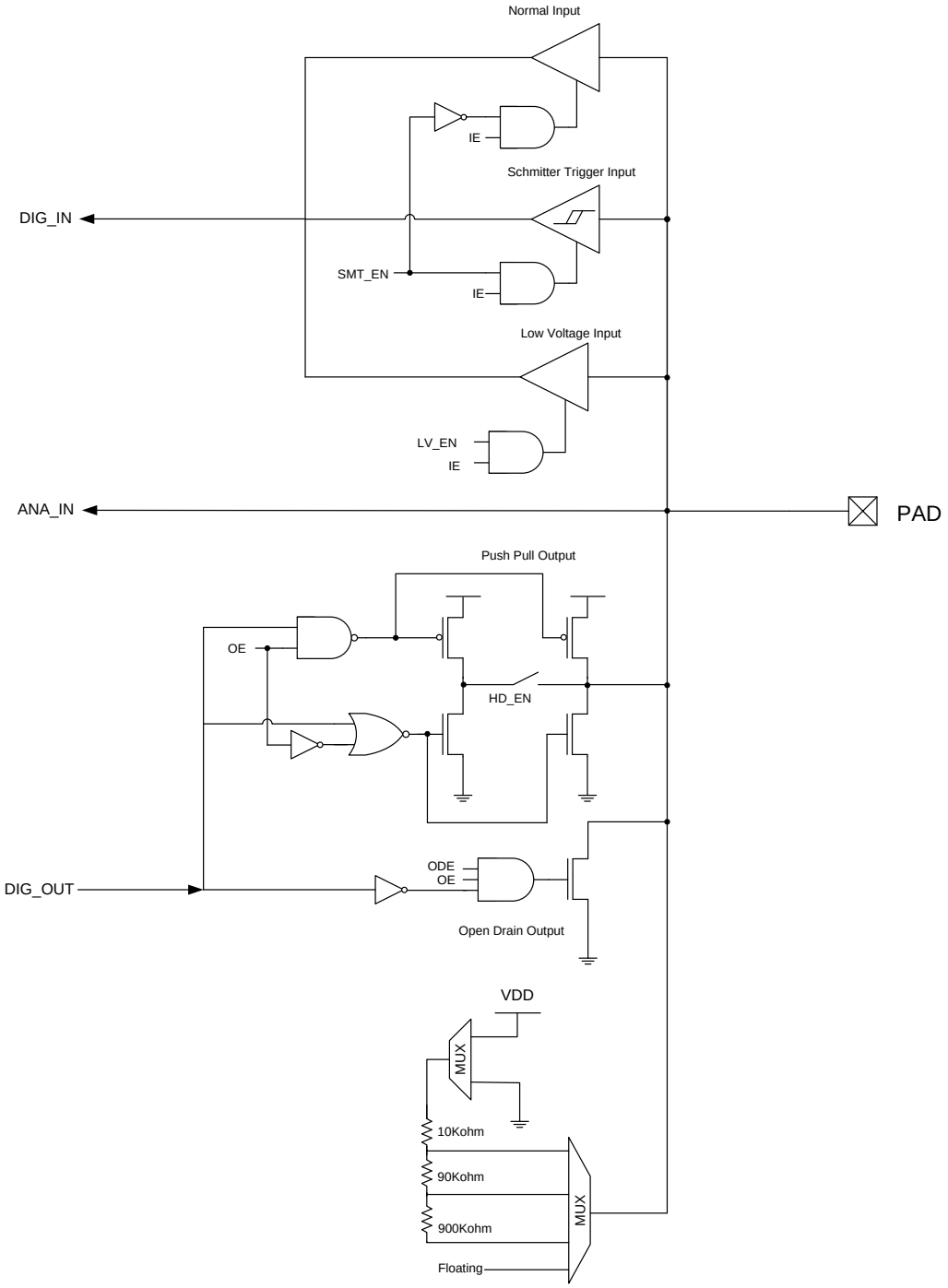


Figure 12-2. GPIO1~17 Block Diagram

12.2 Analog Comparators (ACMP)

There are four Analog Comparator (ACMP) blocks in the device. The power up signals (ACMPx_pdb) must be active before the ACMP starts operation.

The IN- voltage range for all ACMPs is limited to: 0 to V_{VDD} /2 with a recommended input range of 0 to 1.2V.

Each ACMP cell includes a hysteresis selection, with options of 0mV, 25mV, 50mV, or 200mV. All hysteresis options are one-way hysteresis, which means that the actual thresholds will be V_{REF} (high threshold) and V_{REF} - hysteresis (low threshold). If the input voltage falls within the threshold window (between V_{REF} and V_{REF} - hysteresis), the ACMP output retains its previous value.

The ACMP1 IN+ path includes an additional option that supports a 100μA current source. The source loading should be less than 16kΩ.

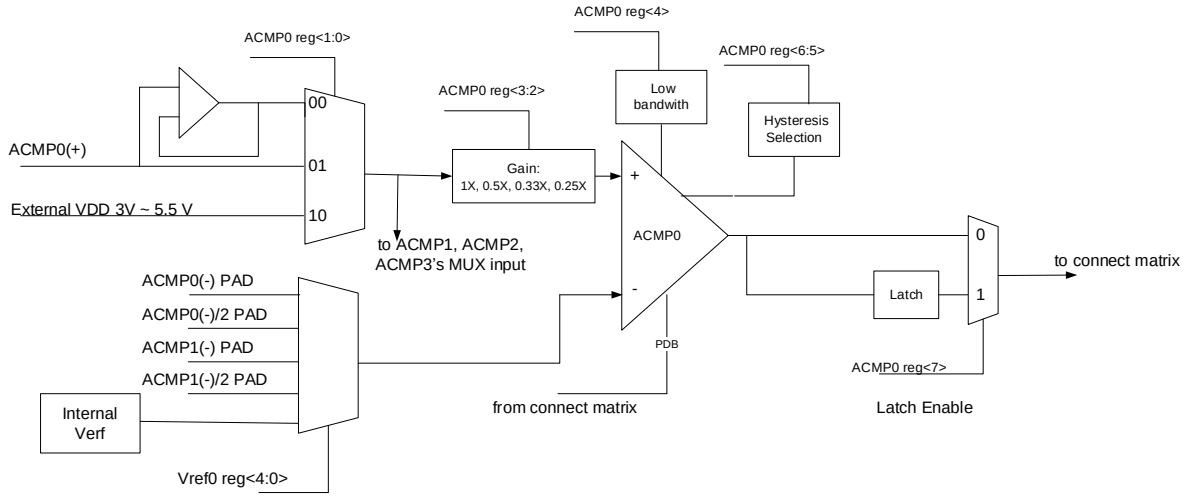


Figure 12-3. ACMP0 Block Diagram

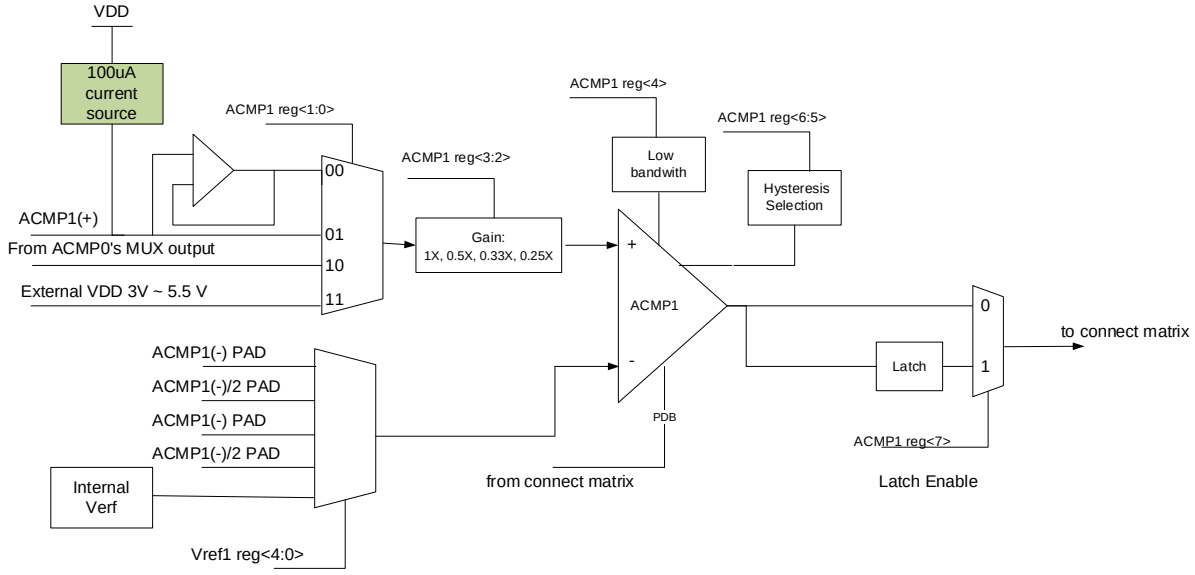


Figure 12-4. ACMP1 Block Diagram

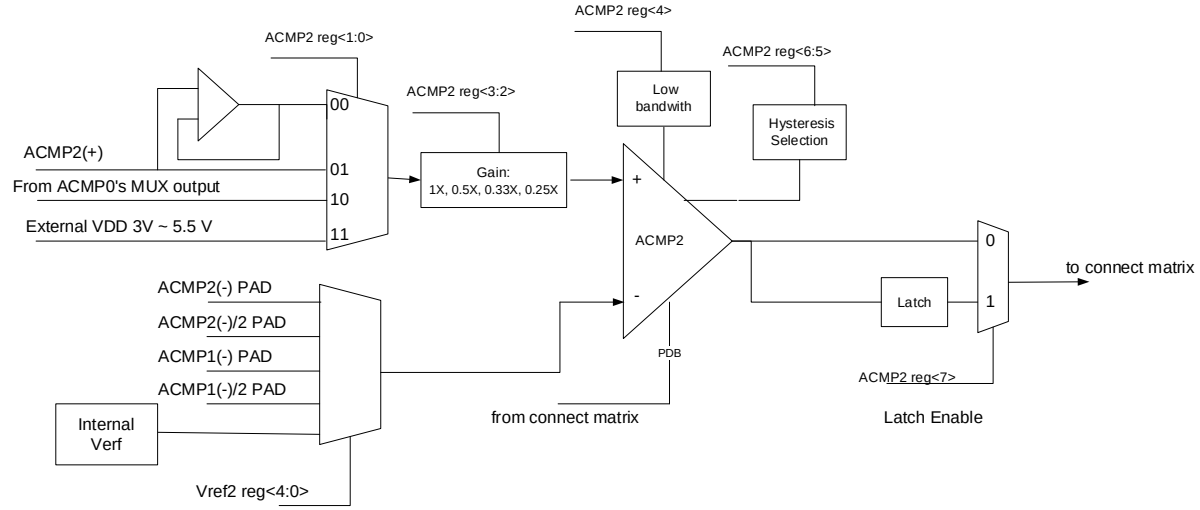


Figure 12-5. ACMP2 Block Diagram

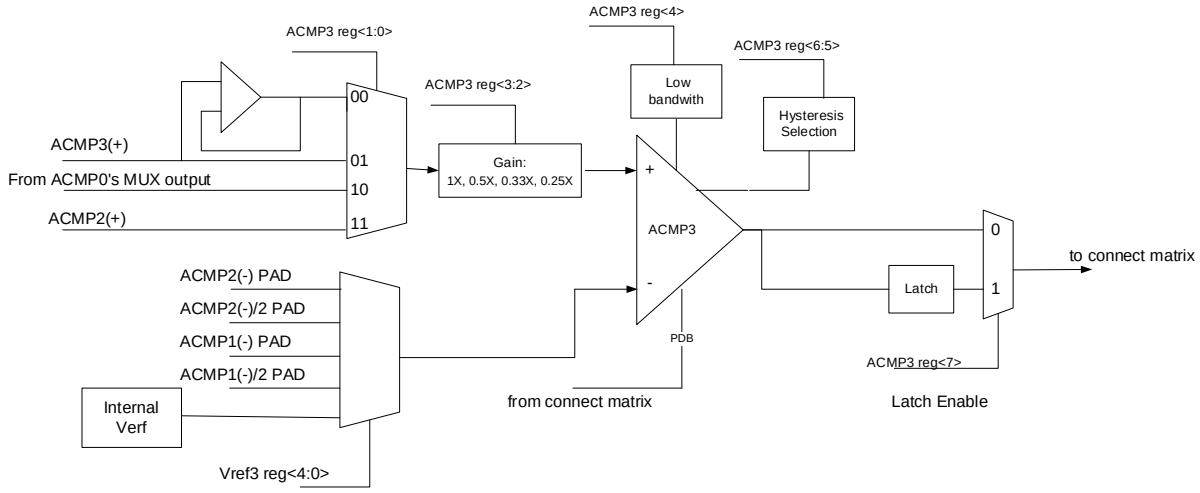


Figure 12-6. ACMP3 Block Diagram

12.3 RC Oscillator

- The device includes three RC oscillators (OSC) for different applications: 25kHz OSC, 2MHz OSC, and 25MHz OSC.
- Only one of three OSC modules can be active during operation.
- By default, the 2MHz OSC functions as the primary clock source after power-on.
- The oscillator can be bypassed using an external clock sourced from PIN20.
- The OSC clock output features a pre-divider (1/2/4/8) for subsequent functions, while each sub-function has a post-divider (1/2/4/8/16/32/64/128) for further adjustments.
- All clock oscillators outputs are stable after the start-up time. The typical start-up times are: 1.5µs for 25MHz, 2.5µs for 2MHz, and 30µs for 25kHz. This delay must be considered after Power-On Reset (POR) or when waking up from OSC power-down mode.

The diagram of the OSC is shown below:

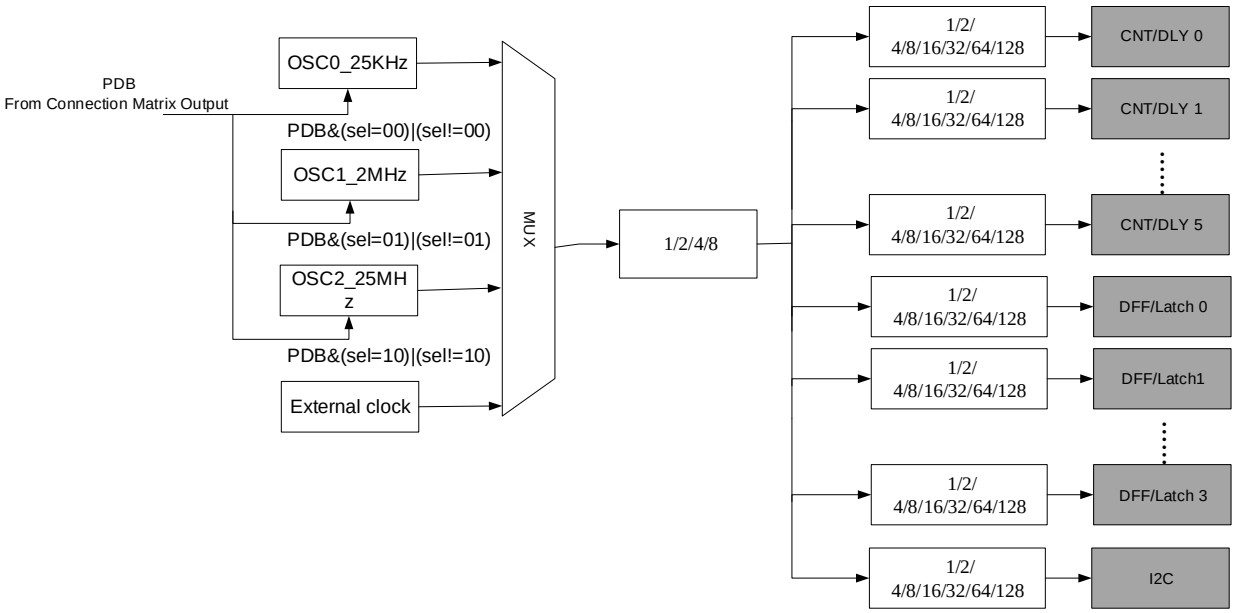


Figure 12-7. RC Oscillator Block Diagram

12.4 Deglitch Filter

The device has two deglitch filters with edge detector functions. A simplified block diagram is shown below:

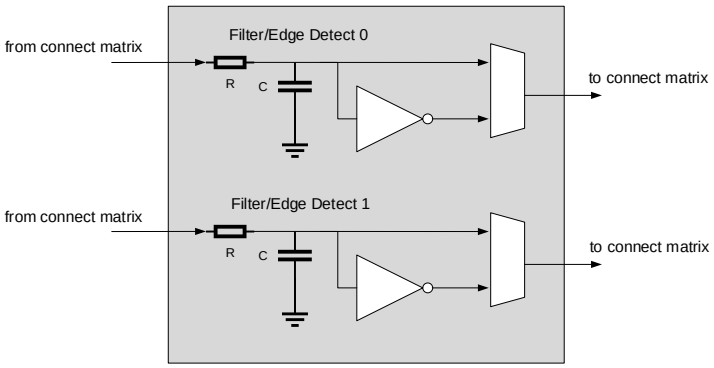


Figure 12-8. Deglitch Filter Block Diagram

12.5 2-Bit LUT

The device includes nine 2-bit LUTs. Each 2-bit LUT receives two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. The output of each LUT can be configured to perform one of the following logic operations: AND, NAND, OR, NOR, XOR, XNOR, or Inverter.

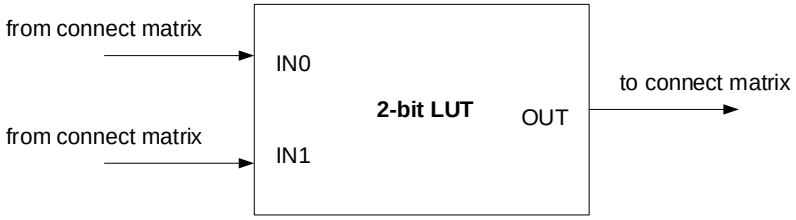


Figure 12-9. 2-Bit LUT Block Diagram

2-Bit LUT Truth Table:

IN1	IN0	OUT
0	0	LUT register bit 0
0	1	LUT register bit 1
1	0	LUT register bit 2
1	1	LUT register bit 3

2-Bit LUT Register Bit Settings for AND, NAND, OR, NOR, XOR, XNOR:

INPUT		LUT Register Bits						
IN1	IN0	OUT=AND	OUT=NAND	OUT=OR	OUT=NOR	OUT=XOR	OUT=XNOR	Note
0	0	0	1	0	1	0	1	LSB bit
0	1	0	1	1	0	1	0	
1	0	0	1	1	0	1	0	
1	1	1	0	1	0	0	1	MSB bit

12.6 3-Bit LUT

The device includes nine 3-bit LUTs. Each 3-bit LUT receives three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. The output of each LUT can be configured to perform one of the following logic operations: AND, NAND, OR, NOR, XOR, or XNOR.

Figure 12-10. 3-Bit LUT Block Diagram

3-Bit LUT Truth Table:

IN2	IN1	IN0	OUT
0	0	0	LUT register bit 0
0	0	1	LUT register bit 1
0	1	0	LUT register bit 2
0	1	1	LUT register bit 3
1	0	0	LUT register bit 4
1	0	1	LUT register bit 5
1	1	0	LUT register bit 6
1	1	1	LUT register bit 7

3-Bit LUT Register Bit Settings for AND, NAND, OR, NOR, XOR, XNOR:

INPUT			LUT Register Bits						
IN2	IN1	IN0	OUT=AND	OUT=NAND	OUT=OR	OUT=NOR	OUT=XOR	OUT=XNOR	Note
0	0	0	0	1	0	1	0	1	LSB bit
0	0	1	0	1	1	0	1	0	
0	1	0	0	1	1	0	1	0	
0	1	1	0	1	1	0	0	1	
1	0	0	0	1	1	0	1	0	
1	0	1	0	1	1	0	0	1	
1	1	0	0	1	1	0	0	1	
1	1	1	1	0	1	0	1	0	MSB bit

12.7 DFF or Latch

There are four DFF (D flip-flop)/Latch blocks in the device. Each DFF/Latch receives three input signals from either a pad or the connection matrix and produces a single output, which goes back into the connection matrix. The DFF/Latch blocks can also be cascaded for implementing more complex logic.

- DFF (D Flip Flop): CLK is rising edge triggered, then Q = D; otherwise Q will not change. The output of DFF will remain low before POR is ready.
- Latch: When CLK is low, then Q = D; otherwise Q retains its previous value (input D does not affect the output when CLK is high).

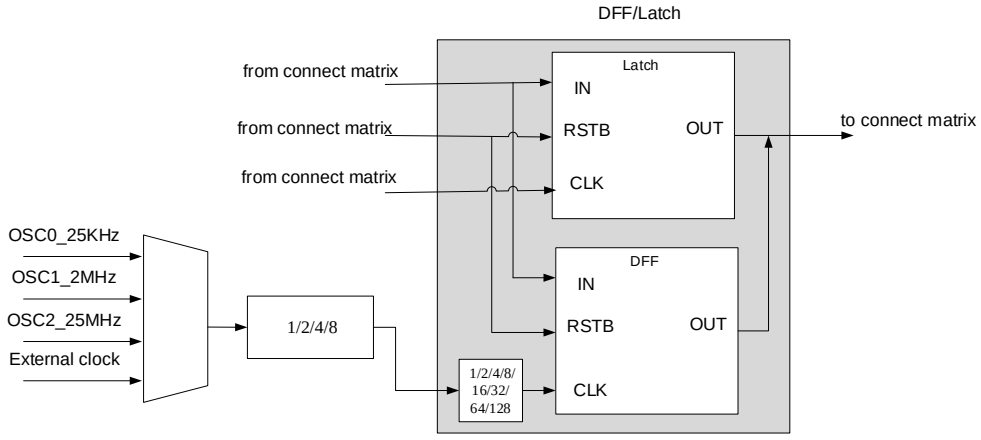


Figure 12-11. DFF/Latch Block Diagram

For the timing behavior of the DFF in different operating conditions, please refer to the following figure:

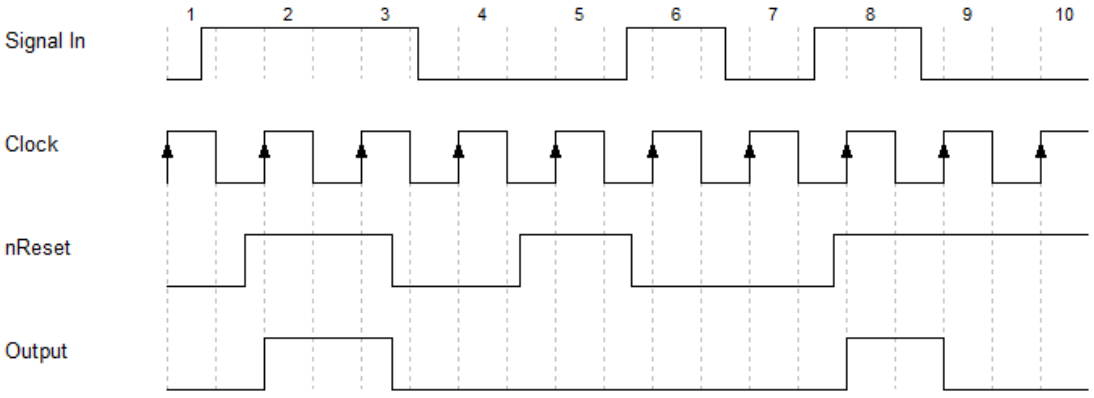


Figure 12-12. DFF Mode Reset Value=0

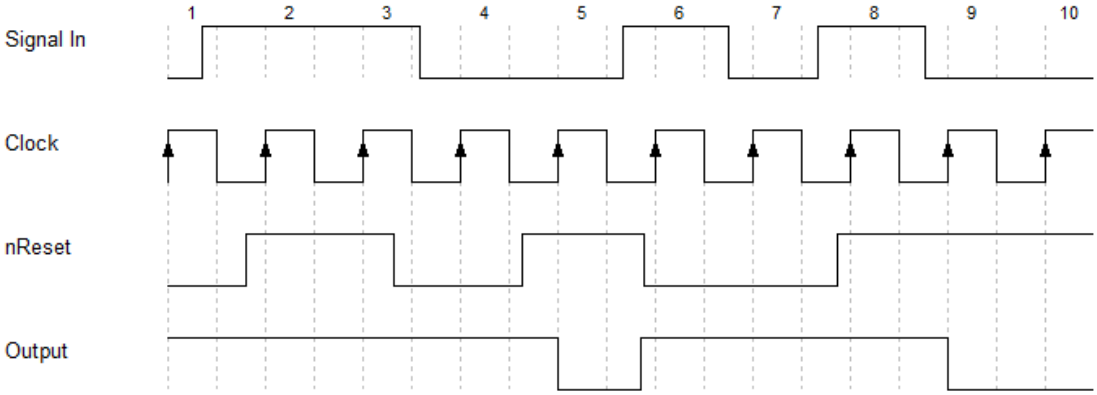


Figure 12-13. DFF Mode Reset Value=1

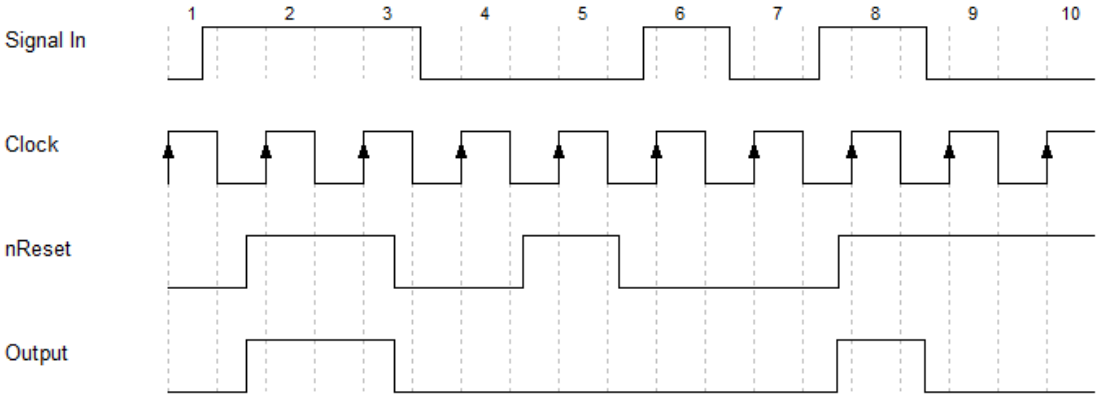


Figure 12-14. Latch Mode Reset Value=0

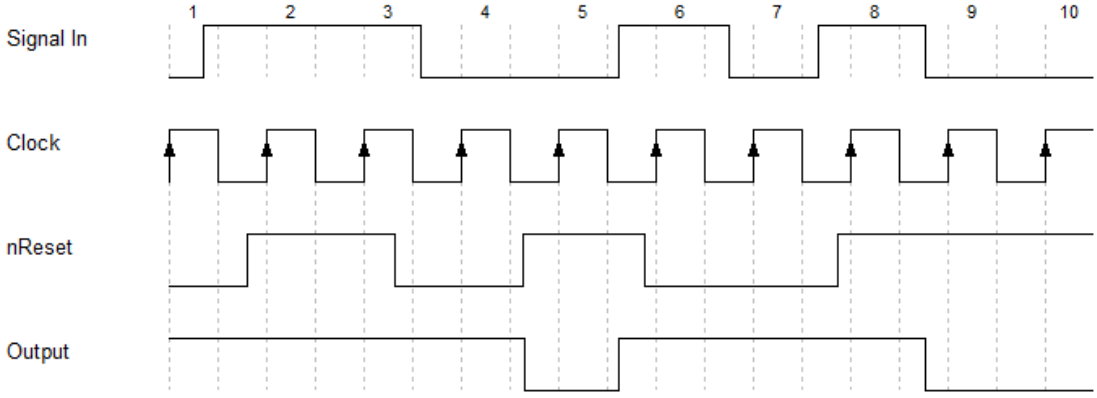


Figure 12-15. Latch Mode Reset Value=1

12.8 CNT/Delay

The device includes a total of nine Counter/Delay blocks consisting of seven 8-bit CNT/DLY and two 16-bit CNT/DLY modules. Each CNT/DLY receives two input signals and generates a single output, which goes back into the connection matrix.

The two 16-bit CNT/DLY modules feature an additional pause function: the pause control input of 16-bit CNT/DLY0 is shared with DFF/Latch2, the pause control input of 16-bit CNT/DLY1 is shared with DFF/Latch3.

The CNT/DLY clock source can be selected from one of the options below:

- Three internal OSCs (25kHz, 2MHz, 25MHz)
- An external clock

The CNT/DLYs also include a native frequency divider, which can be configured with division factors of 1/2/4/8/16/32/64/128.

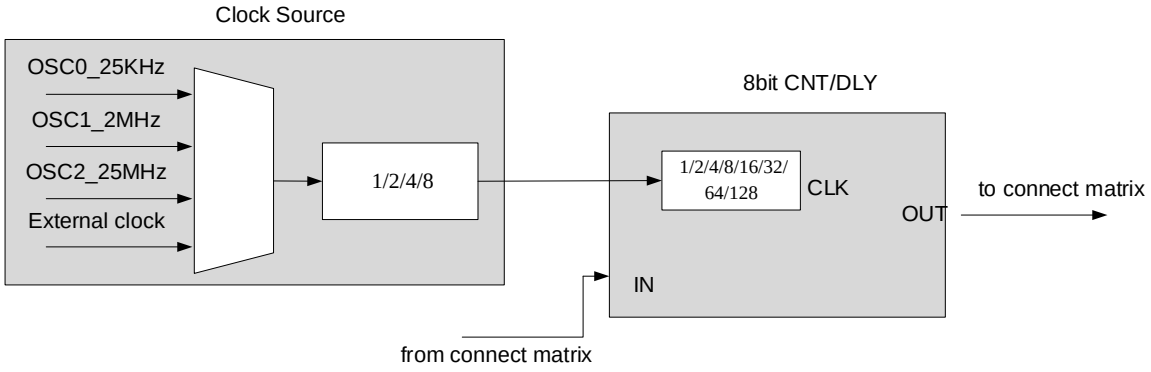


Figure 12-16. 8-Bit CNT/DLY Block Diagram

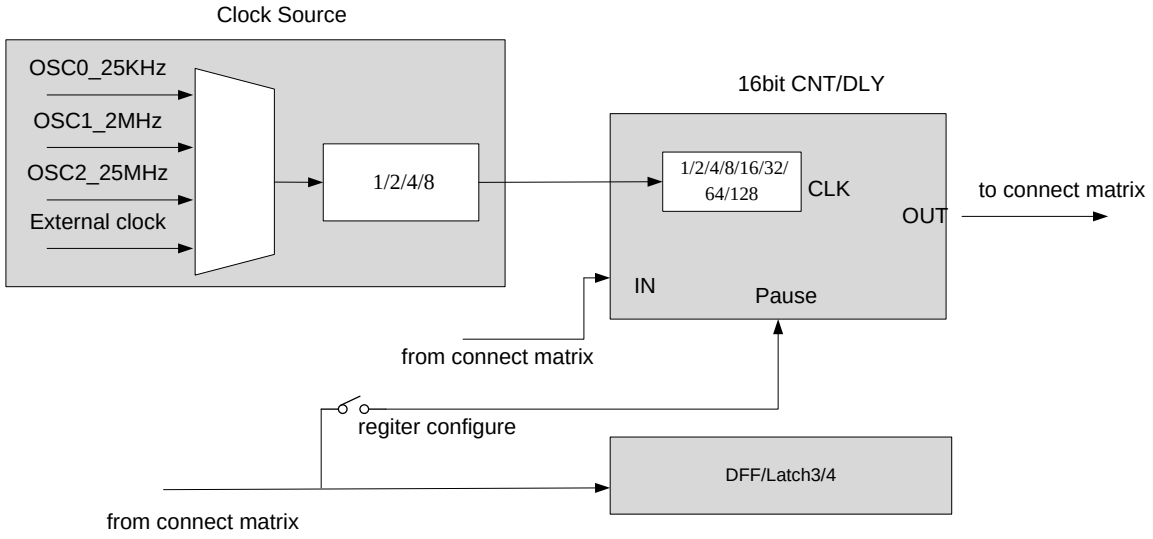


Figure 12-17. 16-Bit CNT/DLY Block Diagram

Each CNT/DLY can be configured in the following modes:

Detect Mode	Control Mode
00: on both falling and rising edges (for delay and counter reset)	000: Delay mode
01: on falling edge only (for delay and counter reset)	001: One shot
10: on rising edge only (for delay and counter reset)	010: Frequency detection mode
11: no delay on either falling or rising edges / high level reset	011: Counter mode
	100: Edge detector output mode

The timing behavior for different operating modes is illustrated in the following figures:

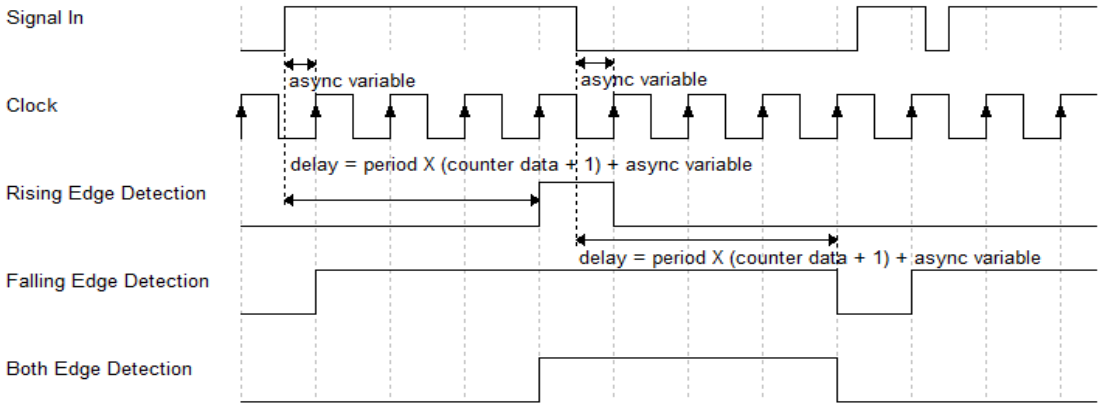


Figure 12-18. Delay Mode Counter Data = 2

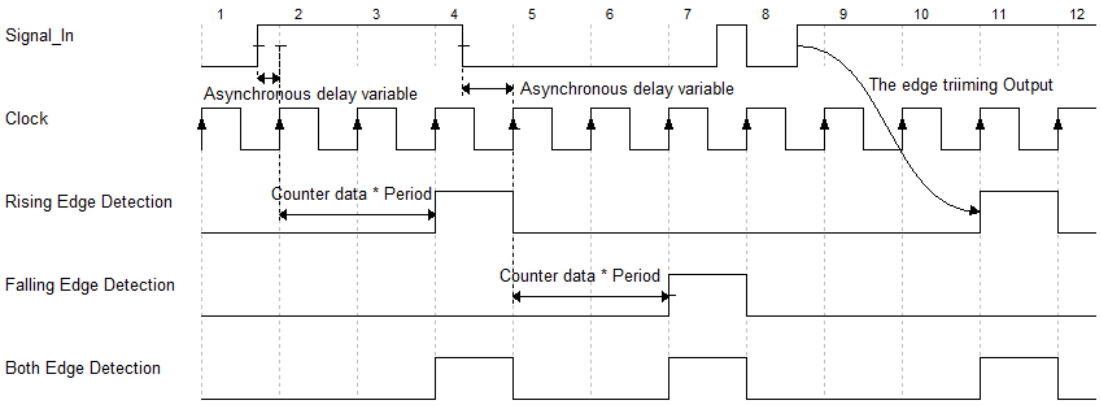


Figure 12-19. Counter Mode Counter Data = 2

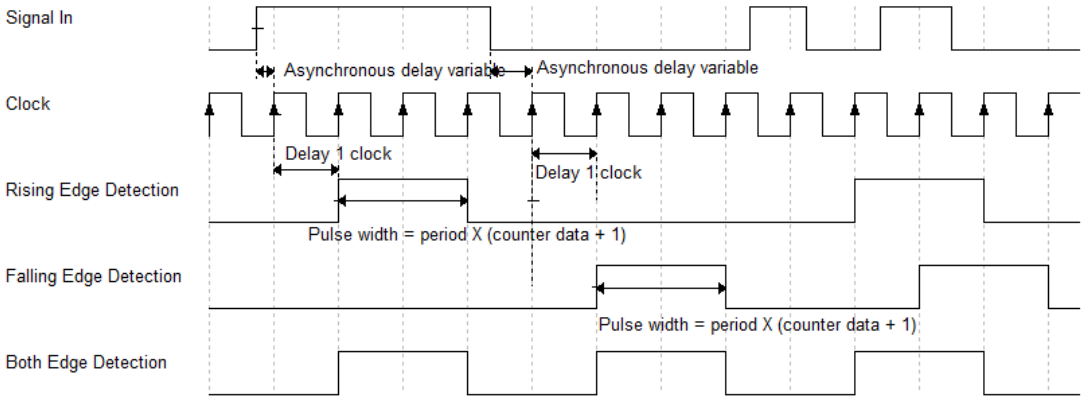


Figure 12-20. One-Shot Mode Counter Data = 1

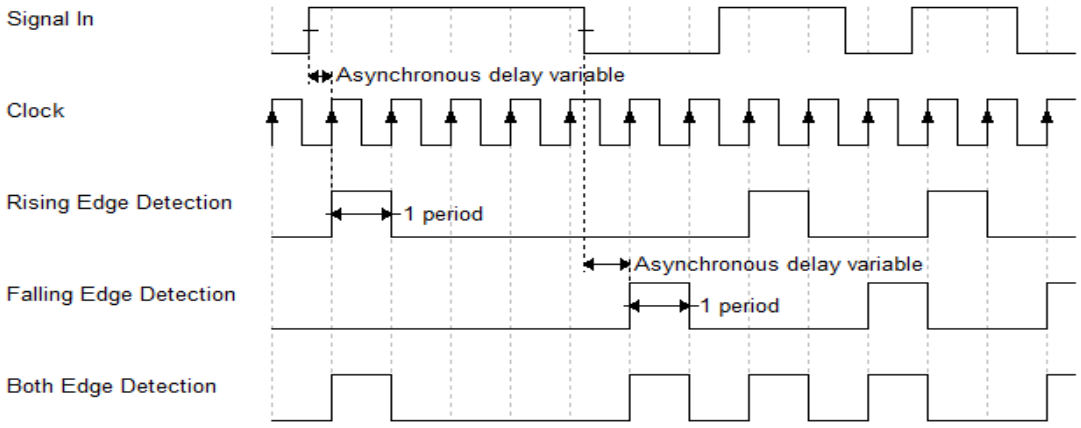


Figure 12-21. Edge Detection Mode

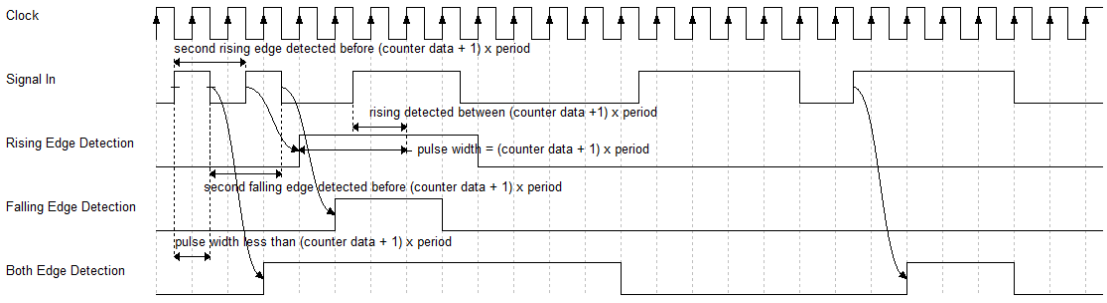


Figure 12-22. Frequency Detection Mode Counter Data = 2

12.9 Asynchronous State Machine (ASM)

The ASM module allows users to create state machines with 2 to 8 states. Users have the flexibility to define available states, state transitions, and input signals (e.g., a, b, c …) that trigger transitions from one state to another state, as illustrated below:

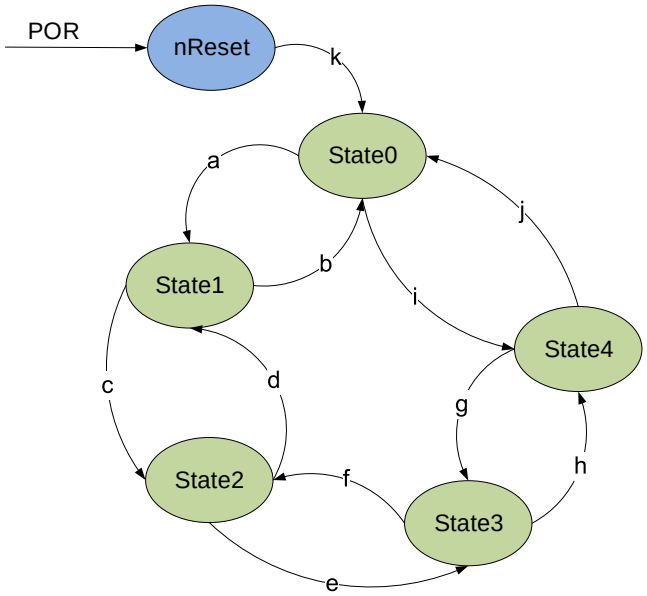


Figure 12-23. ASM State Transitions

This ASM module features a total of 25 inputs sourced from the Connection Matrix outputs. Of these 25 inputs, 24 are user-selectable for driving general state transitions. One input is dedicated to driving the ASM into the initial/reset state, which is always controlled by the power-on reset signal.

The initial/reset state can be selected from states 0 to 7. With 24 selectable inputs, a user-defined state machine can have up to 24 possible state transitions.

Additionally, the module includes an nReset input, which will drive an immediate state transition to the user-defined initial/reset state when active. This transition is highlighted in red in Figure 12-24.

The ASM module provides 8 outputs, which are routed back into the Connection Matrix inputs. These outputs can be further directed to other internal blocks or external pins. Each of the 8 possible states has user-defined outputs, and this configuration is stored in the Connection Matrix Output RAM.

The ASM module diagram is shown in the following figure:

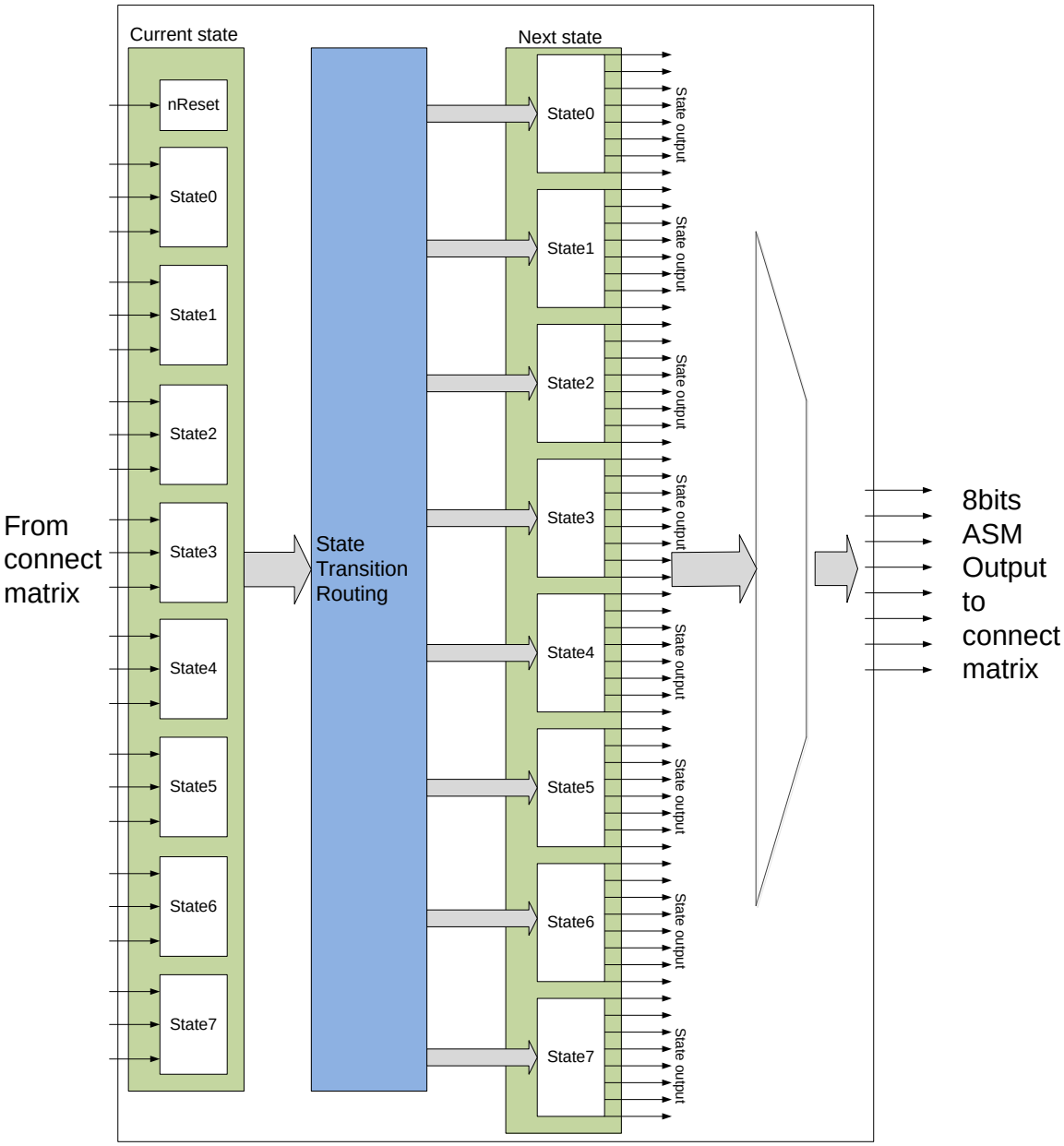


Figure 12-24. ASM Structure

The inputs of ASM are level sensitive and active high, meaning that a high-level input will drive the user-selected transition from one state to another.

12.9.1 ASM Transition

Each ASM state supports three inputs, allowing up to three different input signals to drive a state transition into a specific state. During a transition, any particular state can switch to one of seven other states.

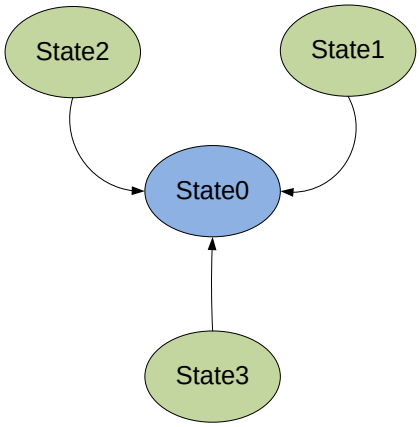


Figure 12-25. Maximum Three State Transitions into a Given State

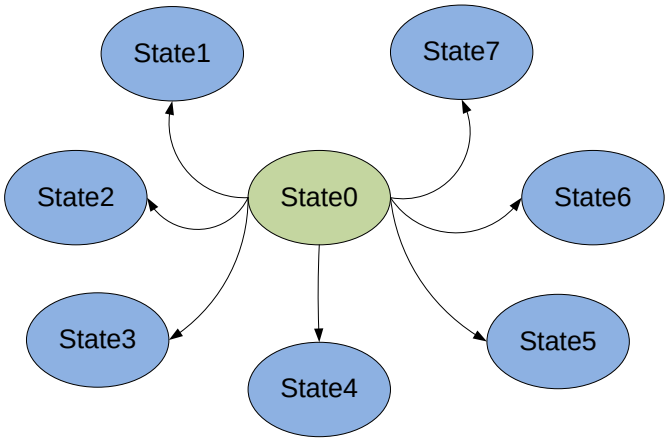


Figure 12-26. Maximum Seven State Transitions Out of a Given State

12.9.2 ASM Outputs

The 8 output values of the ASM, after transitioning into a particular state, are user defined and are routed to the Connection Matrix inputs.

The table below provides a simple example of the ASM output configuration.

State Name	ASM outputs							
	7	6	5	4	3	2	1	0
State 0	0	0	0	0	0	0	0	1
State 1	0	0	0	0	0	0	1	0
State 2	0	0	0	0	0	1	0	0
State 3	0	0	0	0	1	0	0	0
State 4	0	0		1	0	0	0	0
State 5	0	0	1	0	0	0	0	0
State 6	0	1	0	0	0	0	0	0
State 7	1	0	0	0	0	0	0	0

12.9.3 ASM Timing

The timing limitations for ASM operation are provided in the ASM specifications table and are illustrated below.

(1) Basic Transition Timing

The ASM transitions from one state into another when the input signal is at a high level. The input timing must comply with the specified limitations detailed in this specification.

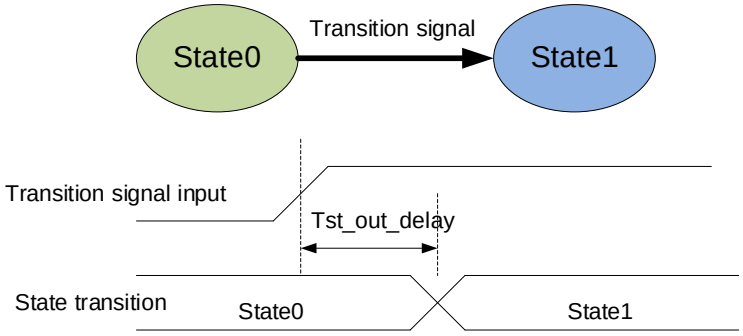


Figure 12-27. State Basic Transition Timing

(2) Pulse Input Timing

When the input operates in pulse mode, the pulse width must be longer than Tst_pulse. If the pulse width is shorter than the Tst_pulse, the state transition will not occur, and the signal will be ignored. However, this invalid input pulse will not interfere with a subsequent valid pulse that meets the minimum pulse width requirement, and can successfully trigger a state transition. The operation is shown below:

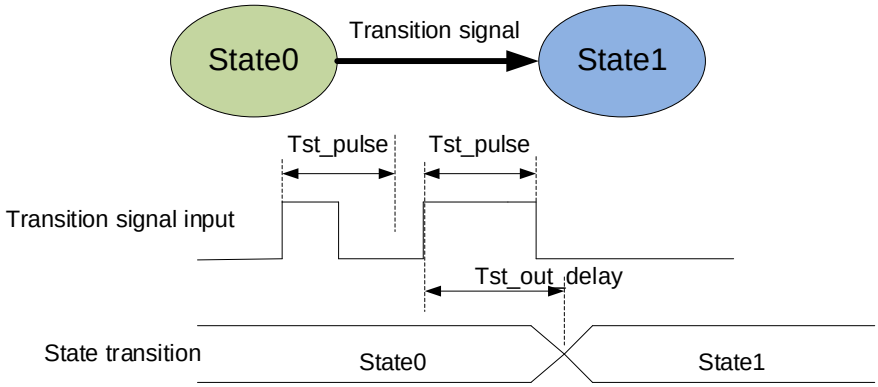
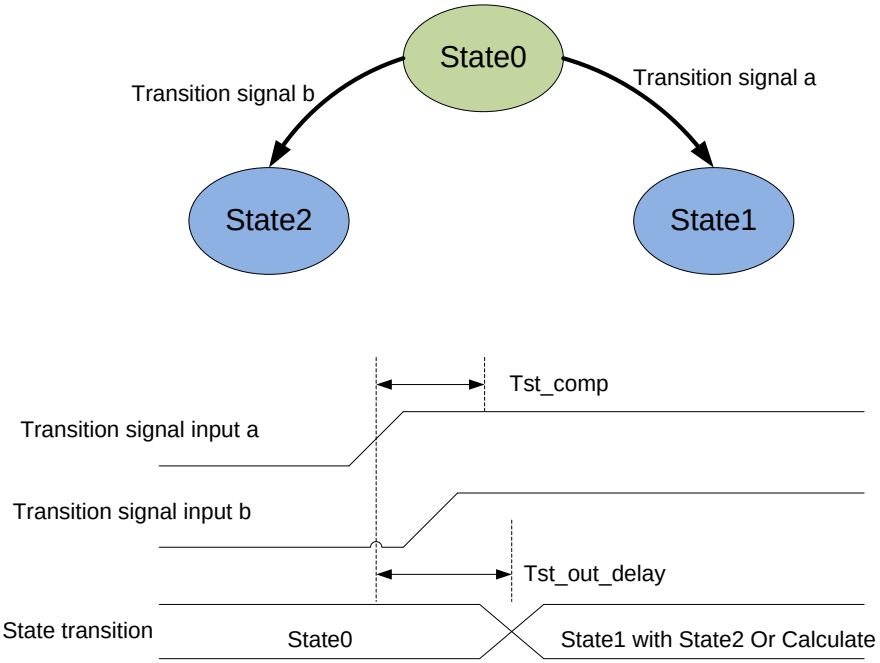


Figure 12-28. State Pulse Input Timing

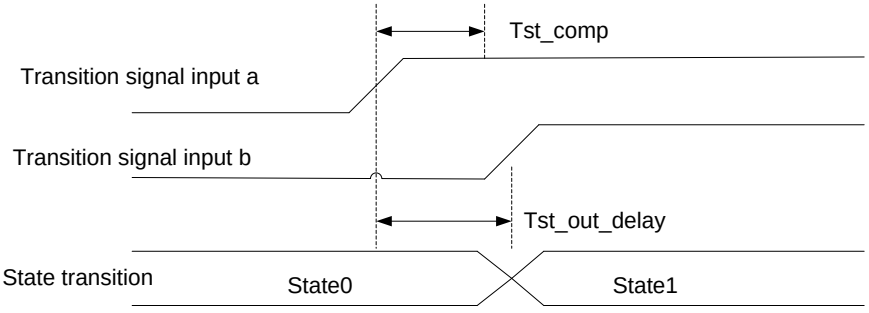
(3) Transition Competing Timing

In situations where two input signals can trigger different state transitions from the same state, these signals are considered “competing” (e.g., signals a and b in the figure below). The signal that arrives first determines the state transition that will “win” (drive the state transition). If one signal arrives at least Tst_comp before the other, it is guaranteed to win, and its corresponding state transition will be executed.

To ensure predictable behavior, competing signals should have a minimum interval of 10ns. If this interval is not maintained, the state transition may be unpredictable.



1) State transition competing: sooner will win



2) State transition competing: normal transition

Figure 12-29. State Transition Competing Timing

When the interval time between signal a and signal b is less than Tst_comp, the output will transition to State3 instead of State1 or State2 (as determined by the calculation logic).

(4) Transition Sequential Timing

A valid input signal for a state transition can become active before the current state is reached. In such cases, the block will remain in that state for only Tst_out_delay before transitioning to the next state. An example of this sequential behavior is shown below:

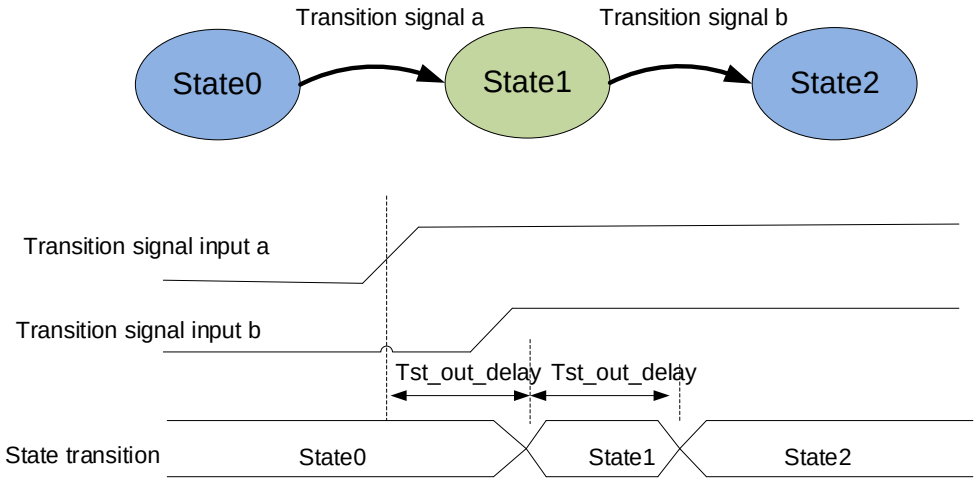
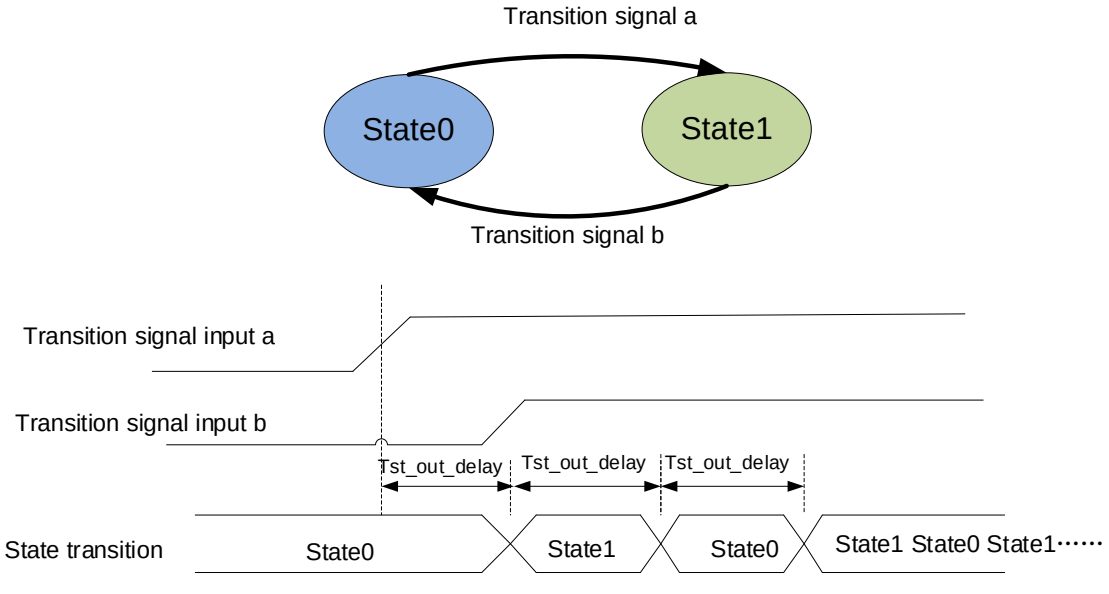


Figure 12-30. State Transition Sequential Timing

(5) Transition Closed Cycling

A closed cycle of state transitions can occur if multiple valid inputs are active at the same time. The rate of these transitions is determined by Tst_out_delay.

The example in the figure below involves cycling between two states, but a closed-cycle transition can involve any number of states from two to eight.



State transition cycling timing

Figure 12-31. State Transition Cycling Timing

12.10 Cross Bar

The Cross Bar is used to create the internal routing for internal macro cells. The Cross Bar has 64 inputs and 128 outputs which constitute a connection matrix. The input sources of the Cross Bar are hard-wired to the outputs of particular modules or macro cells, including I/O pins, LUTs, analog comparators, other digital resources, VDD, and VSS. Each Cross Bar output can be configured to select one of the 64 input sources by using a 6-bit control register.

12.10.1 Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode reg<5:0>
0	GROUND	0
1	VDD	1
2	Reset (POR)	2
3	Pin 2 (GPIO0) Digital Input	3
4	Pin 3 (GPIO1) Digital Input	4
5	Pin 4 (GPIO2) Digital Input	5
6	Pin 5 (GPIO3) Digital Input	6
7	Pin 6 (GPIO4) Digital Input	7
8	Pin 7 (GPIO5) Digital Input	8
9	Pin 8 (GPIO6) Digital Input	9
10	Pin 9 (GPIO7) Digital Input	10
11	Pin 10 (GPIO8) Digital Input	11
12	Pin 12 (GPIO9) Digital Input	12
13	Pin 13 (GPIO10) Digital Input	13
14	Pin 14 (GPIO11) Digital Input	14
15	Pin 15 (GPIO12) Digital Input	15
16	Pin 16 (GPIO13) Digital Input	16
17	Pin 17 (GPIO14) Digital Input	17
18	Pin 18 (GPIO15) Digital Input	18
19	Pin 19 (GPIO16) Digital Input	19
20	Pin 20 (GPIO17) Digital Input	20
21	LUT2_0 (with Inverter) Output	21
22	LUT2_1 (with Inverter) Output	22
23	LUT2_2 (with Inverter) Output	23
24	LUT2_3 (with Inverter) Output	24
25	LUT2_4 (with Inverter) Output	25
26	LUT2_5 (with Inverter) Output	26
27	LUT2_6 (with Inverter) Output	27
28	LUT2_7 (with Inverter) Output	28
29	LUT2_8 (with Inverter) Output	29
30	LUT3_0 Output	30
31	LUT3_1 Output	31
32	LUT3_2 Output	32
33	LUT3_3 Output	33
34	LUT3_4 Output	34
35	LUT3_5 Output	35
36	LUT3_6 Output	36
37	LUT3_7 Output	37
38	DFF/Latch_0 Output	38
39	DFF/Latch_1 Output	39
40	DFF/Latch_2 Output	40
41	DFF/Latch_3 Output	41
42	CNT/DLY_0 Output	42
43	CNT/DLY_1 Output	43
44	CNT/DLY_2 Output	44
45	CNT/DLY_3 Output	45
46	CNT/DLY_4 Output	46
47	CNT/DLY_5 Output	47
48	Deglitch Filter 0 Output	48
49	Deglitch Filter 1 Output	49

50	ACMP_0 Output	50
51	ACMP_1 Output	51
52	ACMP_2 Output	52
53	ACMP_3 Output	53
54	I2C_virtual_0 Output	54
55	I2C_virtual_1 Output	55
56	ASM-stateX-dout0/LUT3_8 Output	56
57	ASM-stateX-dout1/LUT4_0 Output	57
58	ASM-stateX-dout2 / CNT/DLY_6 Output	58
59	ASM-stateX-dout3 / CNT/DLY_7 Output	59
60	ASM-stateX-dout4 / CNT/DLY_8 Output	60
61	ASM-stateX-dout5	61
62	ASM-stateX-dout6	62
63	ASM-stateX-dout7	63

12.10.2 Matrix Output Table

Matrix Output Number	Matrix Output Signal Function	Register Address Offset
0	SM-state0-EN0	0
1	SM-state0-EN1	1
2	SM-state0-EN2	2
3	SM-state1-EN0	3
4	SM-state1-EN1	4
5	SM-state1-EN2	5
6	SM-state2-EN0	6
7	SM-state2-EN1	7
8	SM-state2-EN2	8
9	SM-state3-EN0	9
10	SM-state3-EN1	10
11	SM-state3-EN2	11
12	SM-state4-EN0	12
13	SM-state4-EN1	13
14	SM-state4-EN2	14
15	SM-state5-EN0	15
16	SM-state5-EN1	16
17	SM-state5-EN2	17
18	SM-state6-EN0	18
19	SM-state6-EN1	19
20	SM-state6-EN2	20
21	SM-state7-EN0	21
22	SM-state7-EN1	22
23	SM-state7-EN2	23
24	SM-state-RSTB	24
25	PIN 3 (GPIO1) Digital Output Source	25
26	PIN 4 (GPIO2) Digital Output Source	26
27	PIN 5 (GPIO3) Digital Output Source	27
28	PIN 6 (GPIO4) Digital Output Source	28
29	PIN 7 (GPIO5) Digital Output Source	29
30	PIN 8 (GPIO6) Digital Output Source	30
31	PIN 9 (GPIO7) Digital Output Source	31
32	PIN 10 (GPIO8) Digital Output Source	32
33	PIN 12 (GPIO9) Digital Output Source	33
34	PIN 13 (GPIO10) Digital Output Source	34
35	PIN 14 (GPIO11) Digital Output Source	35
36	PIN 15 (GPIO12) Digital Output Source	36
37	PIN 16 (GPIO13) Digital Output Source	37
38	PIN 17 (GPIO14) Digital Output Source	38
39	PIN 18 (GPIO15) Digital Output Source	39
40	PIN 19 (GPIO16) Digital Output Source	40

41	PIN 20 (GPIO17) Digital Output Source	41
42	PIN 3 (GPIO1) Digital Output Enable Source	42
43	PIN 4 (GPIO2) Digital Output Enable Source	43
44	PIN 5 (GPIO3) Digital Output Enable Source	44
45	PIN 6 (GPIO4) Digital Output Enable Source	45
46	PIN 7 (GPIO5) Digital Output Enable Source	46
47	PIN 8 (GPIO6) Digital Output Enable Source	47
48	PIN 9 (GPIO7) Digital Output Enable Source	48
49	PIN 10 (GPIO8) Digital Output Enable Source	49
50	PIN 12 (GPIO9) Digital Output Enable Source	50
51	PIN 13 (GPIO10) Digital Output Enable Source	51
52	PIN 14 (GPIO11) Digital Output Enable Source	52
53	PIN 15 (GPIO12) Digital Output Enable Source	53
54	PIN 16 (GPIO13) Digital Output Enable Source	54
55	PIN 17 (GPIO14) Digital Output Enable Source	55
56	PIN 18 (GPIO15) Digital Output Enable Source	56
57	PIN 19 (GPIO16) Digital Output Enable Source	57
58	PIN 20 (GPIO17) Digital Output Enable Source	58
59	IN0 of LUT2_0	59
60	IN1 of LUT2_0	60
61	IN0 of LUT2_1	61
62	IN1 of LUT2_1	62
63	IN0 of LUT2_2	63
64	IN1 of LUT2_2	64
65	IN0 of LUT2_3	65
66	IN1 of LUT2_3	66
67	IN0 of LUT2_4	67
68	IN1 of LUT2_4	68
69	IN0 of LUT2_5	69
70	IN1 of LUT2_5	70
71	IN0 of LUT2_6	71
72	IN1 of LUT2_6	72
73	IN0 of LUT2_7	73
74	IN1 of LUT2_7	74
75	IN0 of LUT2_8	75
76	IN1 of LUT2_8	76
77	IN0 of LUT3_0	77
78	IN1 of LUT3_0	78
79	IN2 of LUT3_0	79
80	IN0 of LUT3_1	80
81	IN1 of LUT3_1	81
82	IN2 of LUT3_1	82
83	IN0 of LUT3_2	83
84	IN1 of LUT3_2	84
85	IN2 of LUT3_2	85
86	IN0 of LUT3_3	86
87	IN1 of LUT3_3	87
88	IN2 of LUT3_3	88
89	IN0 of LUT3_4	89
90	IN1 of LUT3_4	90
91	IN2 of LUT3_4	91
92	IN0 of LUT3_5	92
93	IN1 of LUT3_5	93
94	IN2 of LUT3_5	94
95	IN0 of LUT3_6	95
96	IN1 of LUT3_6	96
97	IN2 of LUT3_6	97
98	IN0 of LUT3_7	98
99	IN1 of LUT3_7	99
100	IN2 of LUT3_7	100

101	Input of DFF_0	101
102	RST of DFF_0	102
103	CLK of DFF_0 LATCH	103
104	Input of DFF_1	104
105	RST of DFF_1	105
106	CLK of DFF_1 LATCH	106
107	Input of DFF_2 and 16bit-Counter0 Pause Input	107
108	RST of DFF_2	108
109	CLK of DFF_2 LATCH	109
110	Input of DFF_3 and 16bit-Counter1 Pause Input	110
111	RST of DFF_3	111
112	CLK of DFF_3 LATCH	112
113	Input of CNT/DLY(8bit)_0	113
114	Input of CNT/DLY(8bit)_1	114
115	Input of CNT/DLY(8bit)_2	115
116	Input of CNT/DLY(8bit)_3	116
117	Input of CNT/DLY(16bit)_0	117
118	Input of CNT/DLY(16bit)_1	118
119	Input of Deglitch_0	119
120	Input of Deglitch_1	120
121	ACMP0 PDB (Power down)	121
122	ACMP1 PDB (Power down)	122
123	ACMP2 PDB (Power down)	123
124	ACMP3 PDB (Power down)	124
125	OSC PDB (Power down)	125

12.11 EEPROM

Once the application is finalized and the configuration binary file is generated, it can be loaded into EEPROM memory by following the programming command sequence as described below.

The EEPROM supports write, erase, and read operations via I²C (or UART). The EEPROM can be erased and reloaded repeatedly up to approximately 1000 times.

For details on the EEPROM programming flow, please refer to the following figure:

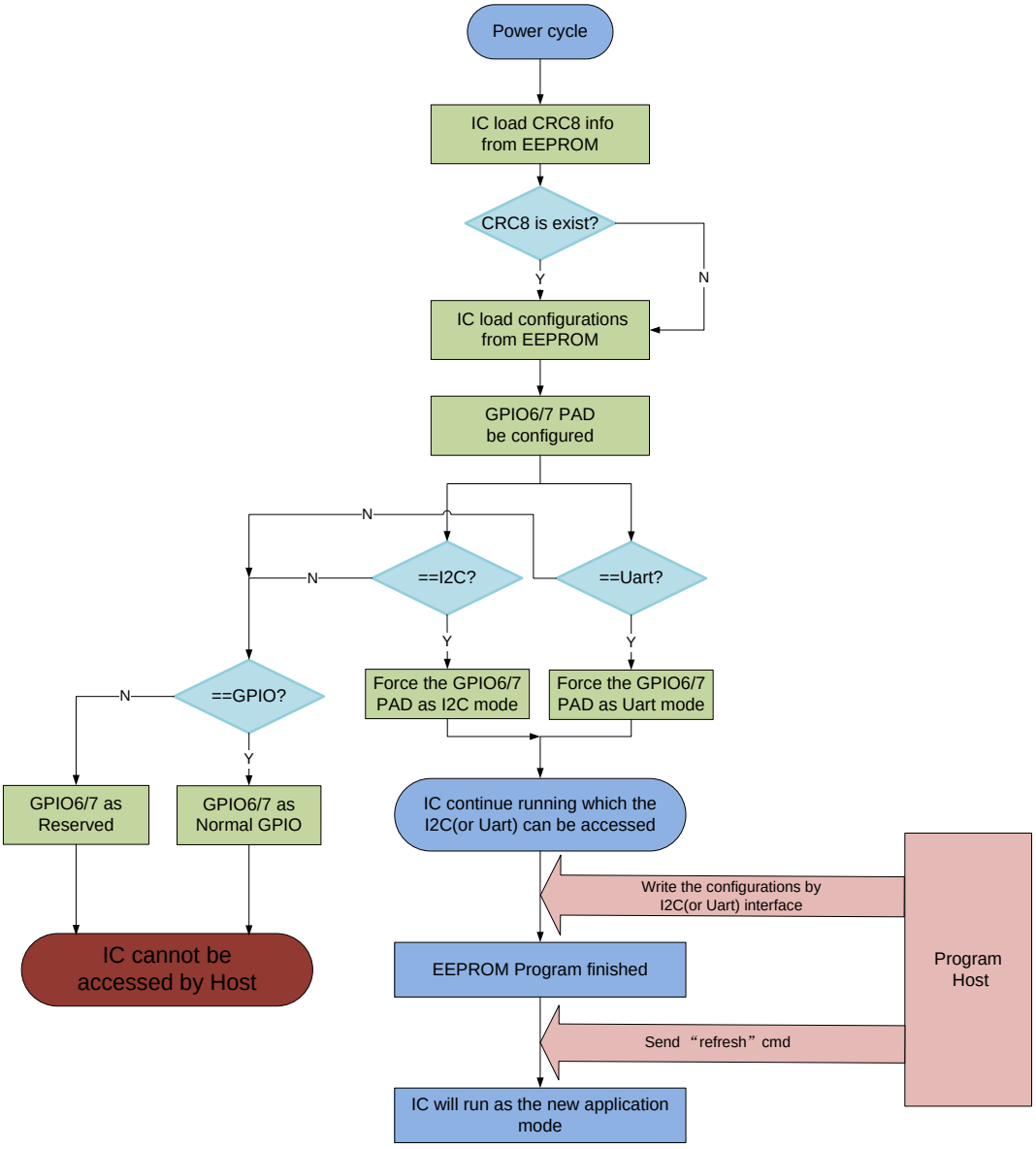


Figure 12-32. EEPROM Program Flow

12.12 The I²C/UART Communication

The device includes one I²C peripheral and one UART interface. Configure register SYS_CFG bit[1:0] to choose I²C or UART protocol for the GPIO6/7 Pins.

SYS_CFG

Bit	Name	Access	Reset	Description
1:0	GPIO6/7 Mode	RW	0x2	GPIO6/7 Share Mode 00: GPIO Mode 01: I2C Mode (GPIO6: SCL, GPIO7: SDA) 10: UART Mode (GPIO6: RXD, GPIO7: TXD) 11: Reserved

Using the protocol interface, users can access the configuration registers and retrieve information while the device is operating. This allows for real-time behavior adjustments without interrupting operation. Additionally, once the application is finalized, configurations can be written into the Non-Volatile Memory (NVM).

The communication mode operates in one of the following ways:

(1) The register configuration will be automatically loaded from NVM after power-on.

(2) Users can access the entire configuration stored in the NVM via the I²C or UART interface during operation.

(3) Register values can be modified via I²C or UART interface, which will change the behavior of the device immediately.

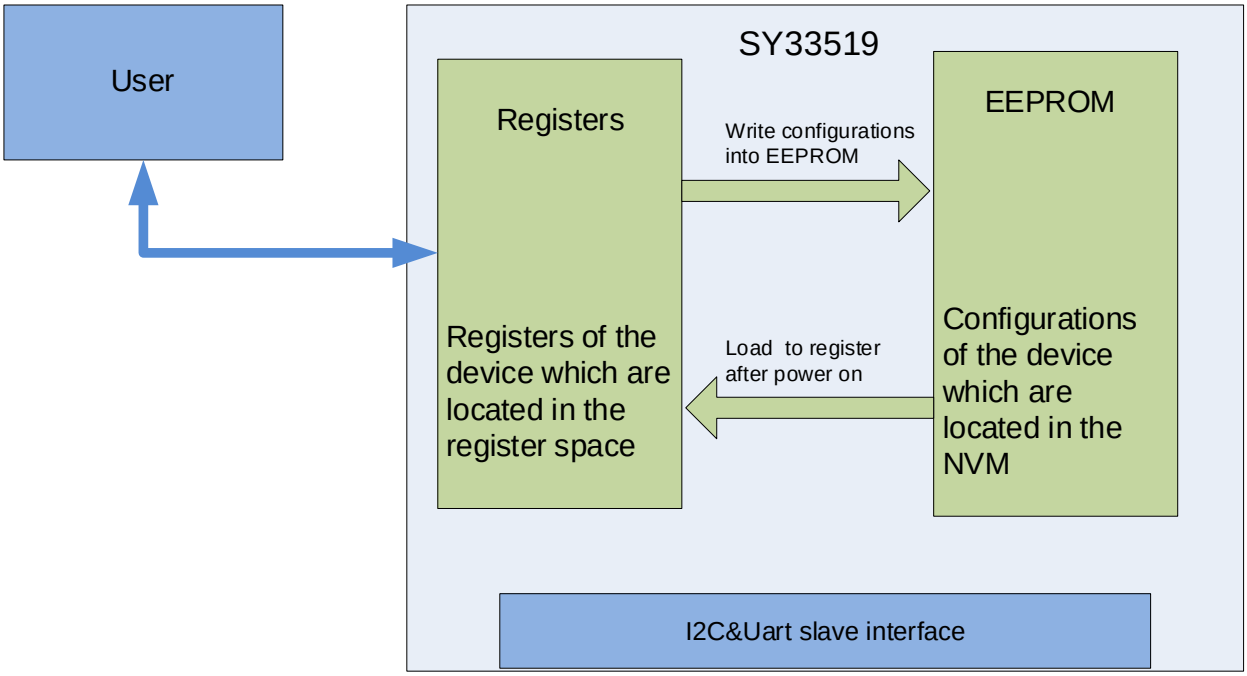


Figure 12-33. I²C Access Scenario

12.12.1 I²C Communication

The I²C peripheral address supports only 7-bit mode. The following two modes are supported: normal mode (100kHz), or fast mode (400kHz).

For this device, the register address space accessible by the I²C controller is limited to the range of 0~0xFF. If an address outside this range is accessed, read operations will be undetermined, write operations will be ignored, and the device will respond with a NAK (not acknowledge).

12.12.1.1 I2C Write

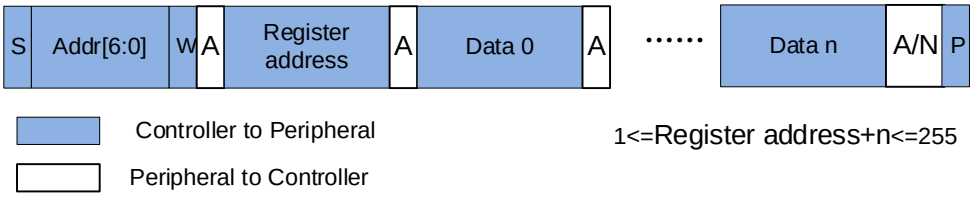


Figure 12-34. I²C Write Mode

12.12.1.2 I2C Read

The read can be one of two modes which are shown below:

Current Read Mode

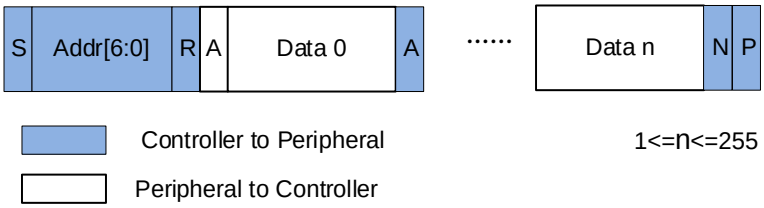


Figure 12-35. I²C Current Read Mode

Random Read Mode

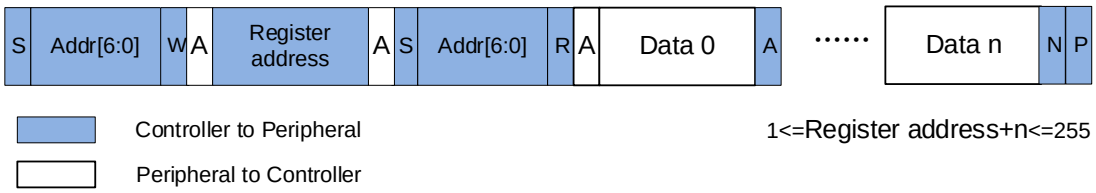


Figure 12-36. I²C Random Read Mode

12.12.2 UART Communication

The UART interface has a default baud rate of 115200bps and is configured as 8-bit, 1 stop bit, 1 start bit, and no parity. For added flexibility, the baud rate can be adjusted using the auto-baud method, supporting the following rates: 4800, 9600, 19200, 38400, 57600, and 115200bps.

When accessing the SY33519 via UART interface, users should follow the defined protocol, detailed in the sections below. Both read and write operations to SY33519 have two stages: the command stage initiated by the host, and the response stage initiated by the SY33519.

12.12.2.1 UART Write

A register write operation consists of a packet containing a header, a command and counter byte, address byte, data bytes, and checksum. When the SY33519 receives a UART write command, it validates the checksum, confirms the register address, loads the data (1~n) to the specified registers, and transmits an acknowledgement to the host.

For details on the UART write data command, refer to the following figure:

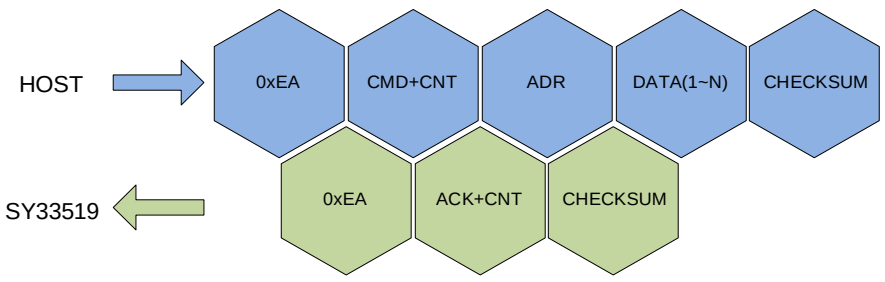


Figure 12-37. UART Write Access Scenario

HOST Command Format:

	Bit Position							
	7	6	5	4	3	2	1	0
CMD+CNT	CMD: 0 = READ 1 = WRITE	CNTS[6:0]: n = 0x01~0x04						
ADR	Register address：0x00~0xFF							
CHECKSUM	(0xEA + (CMD_CNT) + ADR + DATA(n)) & 0xFF							

SY33519 Command Format:

	Bit Position							
	7	6	5	4	3	2	1	0
ACK_CNT	ACK: 0 = OK 1 = ERROR	CNTS[6:0]: The count of received data						
CHECKSUM	(0xEA + (ACK_CNT)) & 0xFF							

12.12.2.2 UART Read

A register read operation consists of a header, a command and count byte, a start address byte, and a checksum. When the SY33519 receives the command, it validates the checksum and transmits the register data to the host.

For details on the UART write data command, refer to the following figure:

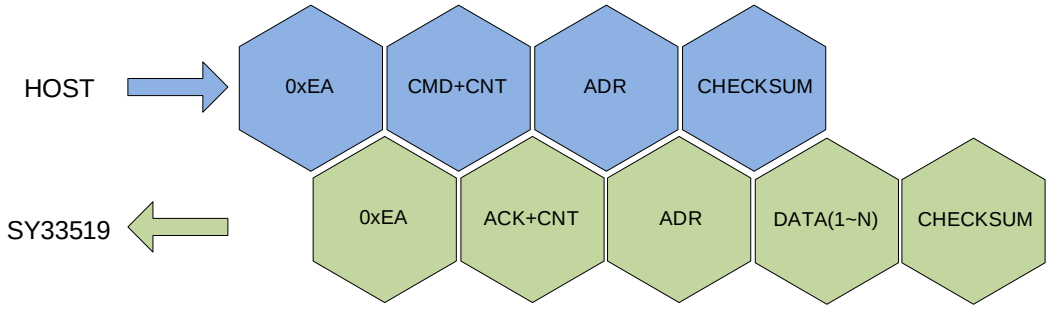


Figure 12-38. UART Access Scenario

HOST Command format:

	Bit Position							
	7	6	5	4	3	2	1	0
CMD+CNT	CMD 0=Read 1=Write	Data Length(n) n=1~5						
ADR	Start Address							
CHECKSUM	0xEA + (CMD_CNT) + (ADR)							

SY33519 Command Format:

	Bit Position							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACK_CNT	ACK 0=OK 1=Error	CNT: Data Length(n) From Host						
ADR	Start Address From Host							
Data	Data1~Datan from target register address							
CHECKSUM	0xEA + (ACK_CNT) + (SEL_ADR) + DATA(1~n)							

12.12.2.3 UART Auto Baud

The UART default baud rate is 115200bps, but it can be automatically configured to 1200, 2400, 4800, or 9600bps. After the device powers on, the host can send a message containing six consecutive 0x55 bytes to SY33519 at the target baud rate. Upon receiving this sequence, the SY33519 will automatically adjust its baud rate to match the target baud rate.

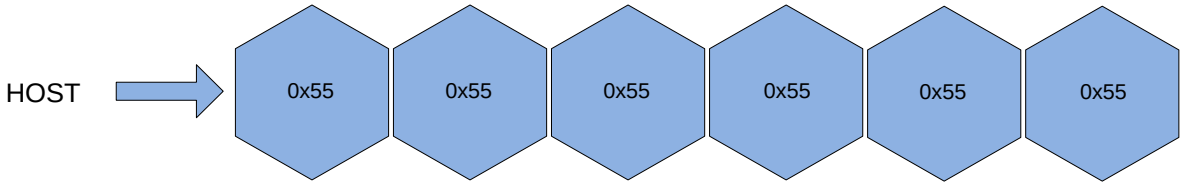


Figure 12-39. UART Auto Baud Access Scenario

13 Applications

13.1 Application 1: System Reset

The SY33519 can function as a system reset generator, activating a reset when exception events are triggered, such as failure, protection events, or reset triggers.

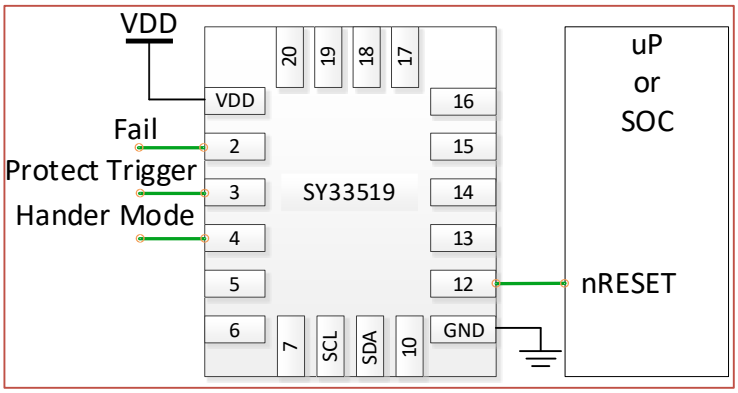


Figure 13-1. Application 1: System Reset

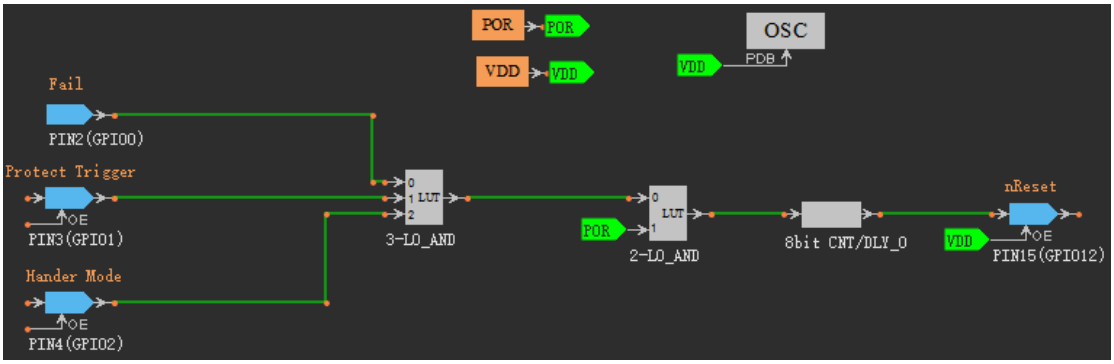


Figure 13-2. SilerVision Design Diagram

Configuration details:

Function	Configuration
GPIO0/1/2	Set as digital input.
GPIO9	Set as output and connect to the reset pin of SOC.
3-LUT 0	Configured to AND mode.
2-LUT 0	Configured to AND mode.
8-bit CNT/DLY 0	One shot mode, rising edge detection, and counter data is determined by requirement.
	Output Invert: enable the output mode if the SOC's reset is active-low.

13.2 Application 2: Multi-button Reset

Triggering a reset by pressing multiple buttons is a common method in the device. When system crashes, failures, or other abnormalities occur, a separate chip is used to implement the reset function to ensure that the system can be reset in time.

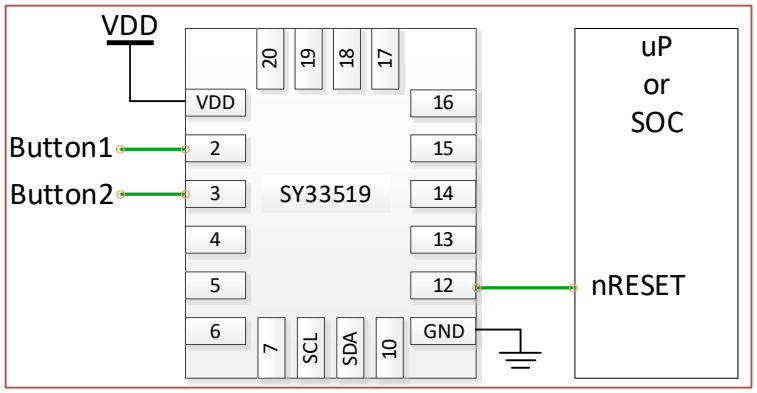


Figure 13-3. Application 2: Multi-Button Reset

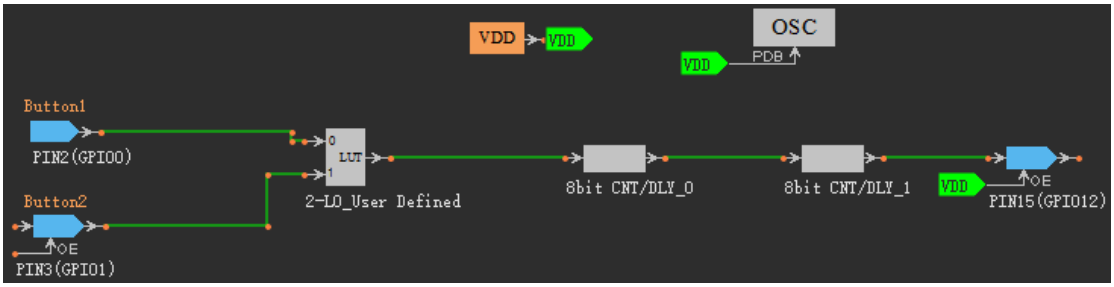


Figure 13-4. SilerVision Design Diagram

Configuration details:

Function	Configuration	
GPIO0/1	Set as digital input.	
GPIO9	Set as output and connect to the reset pin of SOC.	
LUT	Function: Converting the input signal of the button to the correct reset signal.	
	Logical relationship: determined by nReset high level or low level.	
CNT/DLY	CNT/DLY_0	Delay mode, rising edge detection.
		Counter data: determined by the required time length of the button.
		Output polarity: Inverted (pulse low level effective).
	CNT/DLY_1	One shot mode, rising edge detection.
		Counter data: determined by the required pulse width of nReset.
		Output invert: inverted (pulse low level effective).

13.3 Application 3: Basic Sequencer

When different parts of the system need to power up in a specific sequence, a power sequencer will be introduced.

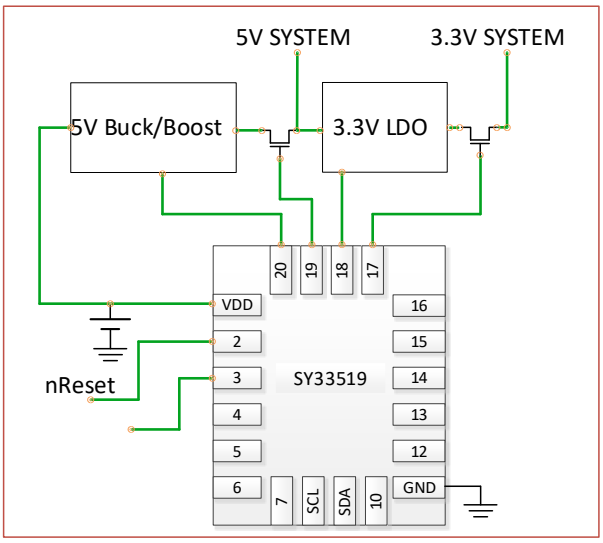


Figure 13-5. Application 3: Basic Sequencer

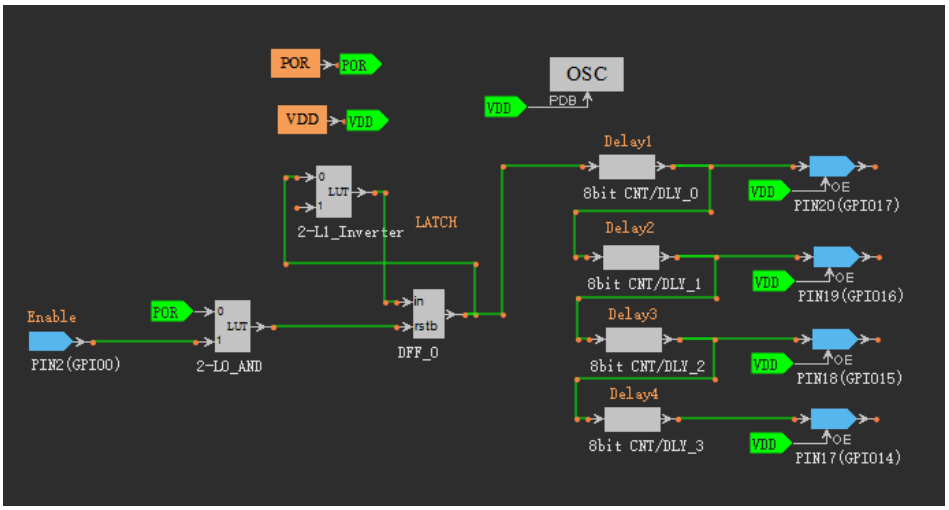


Figure 13-6. SilerVision Design Diagram

Configuration details:

Function	Configuration
GPIO 0	Set as digital input.
GPIO14/15/16/17	Set as output which has a different power-up sequence.
2 LUT	Function: converting the input signal to the correct power control signal.
	Logical relationship: determined by nReset high level or low level.
CNT/DLY	Delay mode, rising edge detection.
	Counter data: determined by the required delay time.
	Output Invert: inverted (pulse low level effective).

13.4 Application 4: Deglitch by CNT/DLY

Application Details:

Application	Analysis
Application scenario	Glitch conditions, such as button closing and opening, input voltage approaching digital input threshold without Schmitt trigger, and input voltage approaching threshold without hysteresis comparator.
Design principle	Filter out pulses shorter than the delay time when CNT/DLY is in delay mode.
Support mode (CNT/DLY)	Rising edge, falling edge, and both.

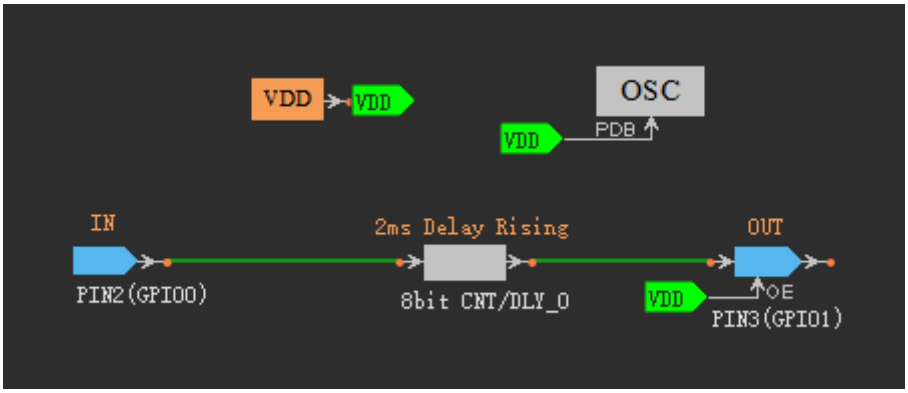


Figure 13-7. SilerVision Design Diagram

Figure 13-8. CNT/DLY Output in Rising Mode

13.5 Application 5: Ship Mode Controller

Before the product is delivered to the user, an ultra-low power MS-PLD is used to design a button monitor which is used as the power switch for the main system.

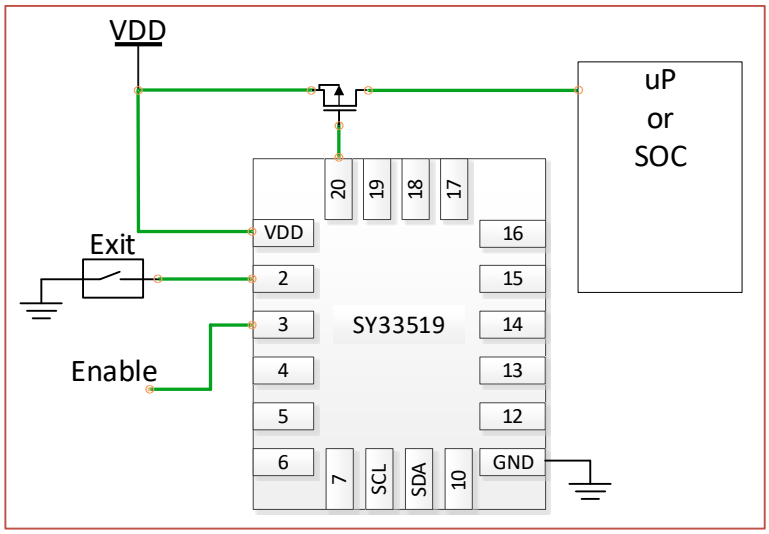


Figure 13-9. Application 5: Ship Mode Controller

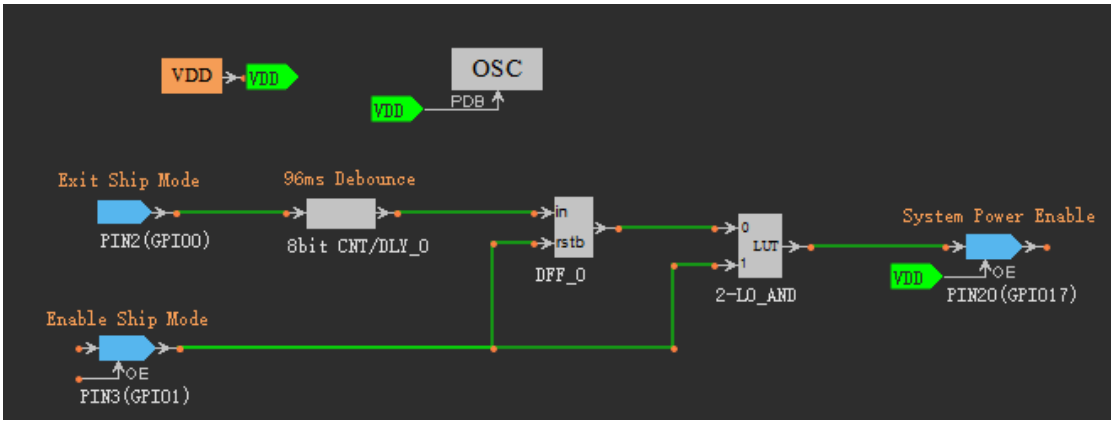


Figure 13-10. SilerVision Design Diagram

Configuration details:

Function	Configuration
GPIO 0/1	GPIO 0 Mode: Analog IO, GPIO 1 Mode: Digital Input.
GPIO17	Configure as output mode which is used as the power switch of the system.
LUT	Function: convert the input signal into the correct enable signal of system power.
	Logical relationship: determined by the output level corresponding to Entry or Exit Ship Mode.
CNT/DLY	Delay mode, rising edge detection.
	Counter data: determined by debounce.

13.6 Application 6: 4-bit Demultiplexer

A demultiplexer is used to distribute an input signal to one of several output channels.

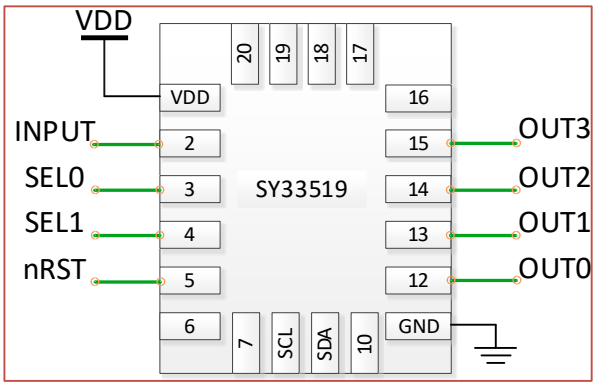


Figure 13-11. Application 6: 4-bit Demultiplexer

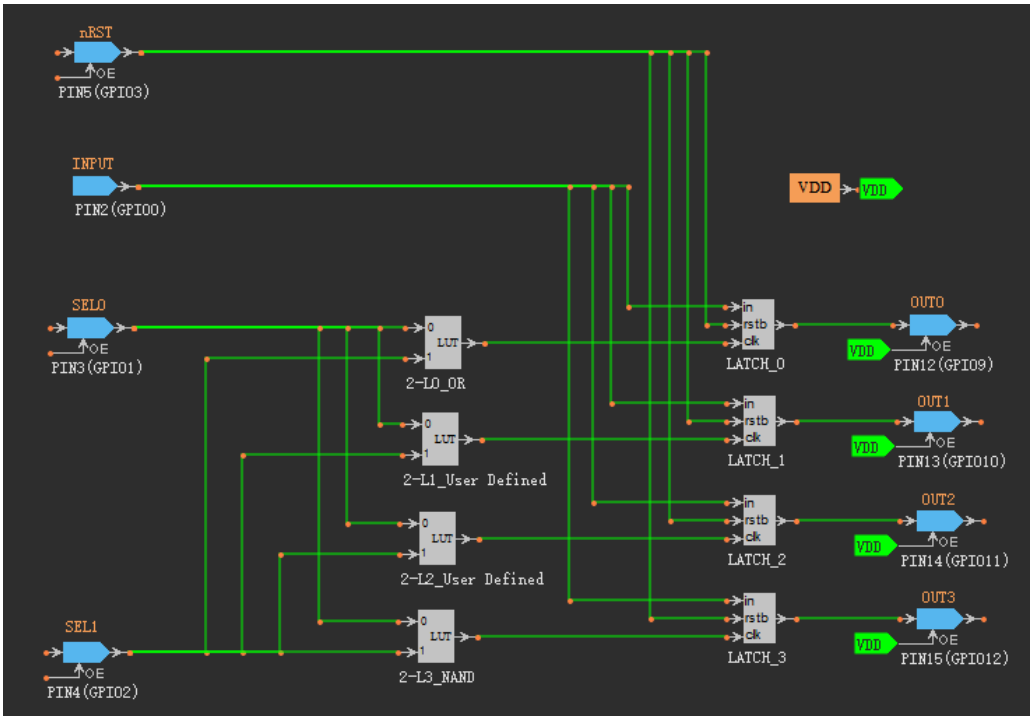
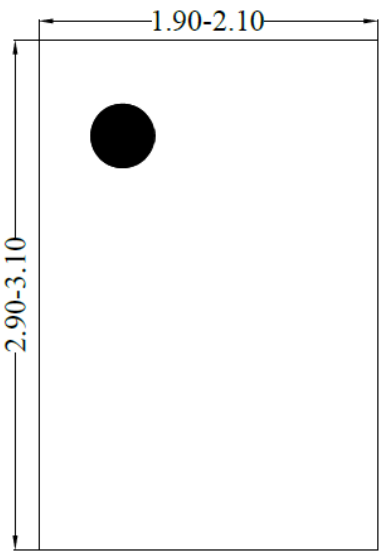


Figure 13-12. SilerVision Design Diagram

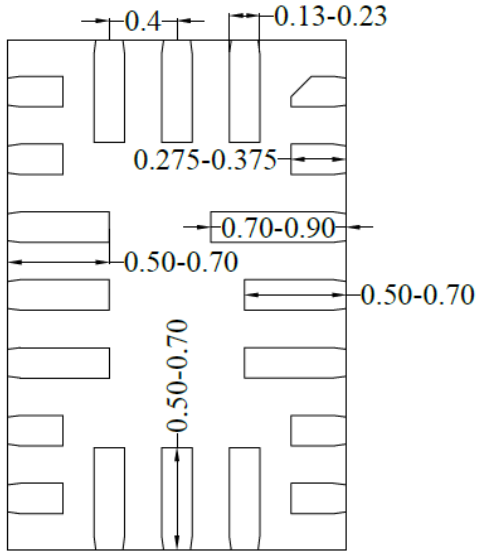
Configuration details:

Function	Configuration
LUT	Logical relationship: the combination of SEL0 and SEL1 ensures that only one LUT output value of LUT0, LUT1, LUT2, and LUT3 is low. For example, the output value of 2-L3 will be low when both SEL0 and SEL1 are low.
LATCH	Connecting LUT output to the clk of LATCH. Connecting INPUT to the in of LATCH.

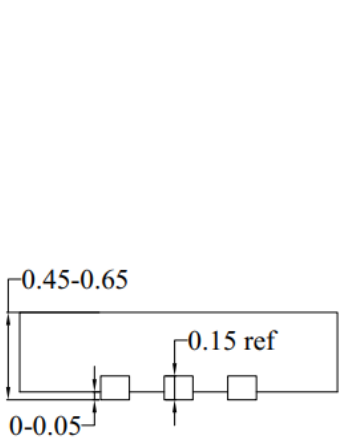
14 QFN2x3-20 Package Outline Drawing



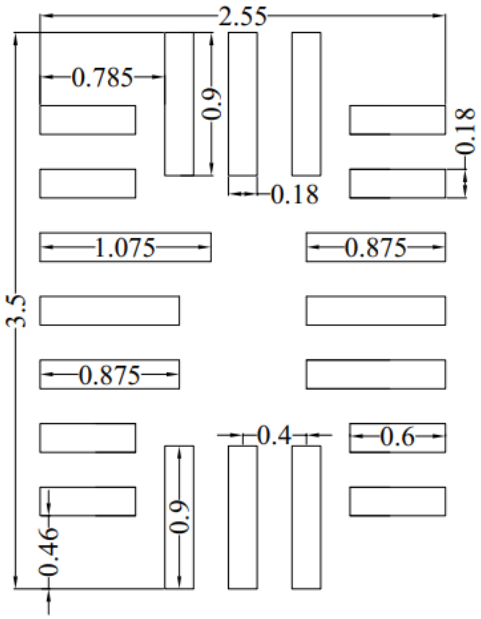
Top View



Bottom View



Side View



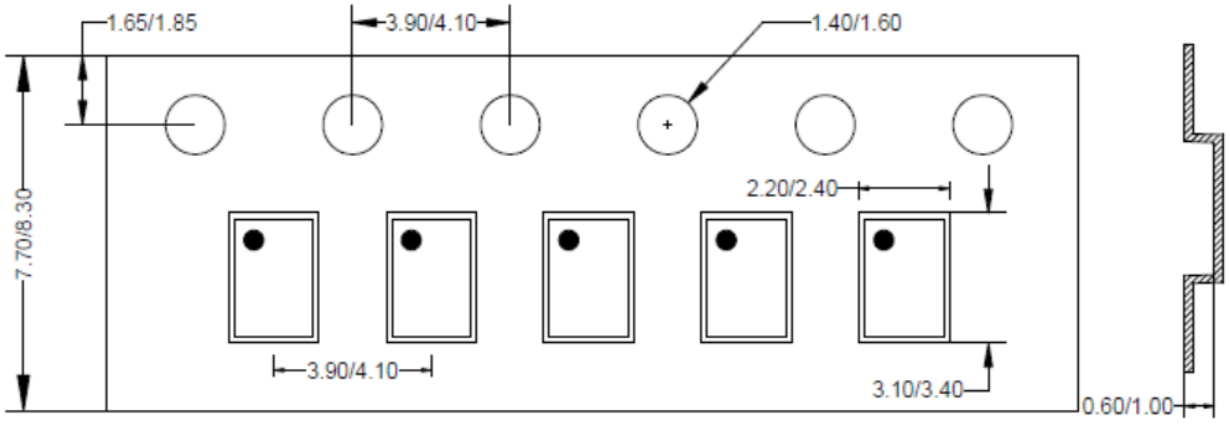
Recommended PCB Layout
(Only for reference)

Notes: All dimensions are in millimeters and exclude mold flash and metal burr.
The center line on the PCB layout refers to the chip body center.

15 Taping & Reel Specification

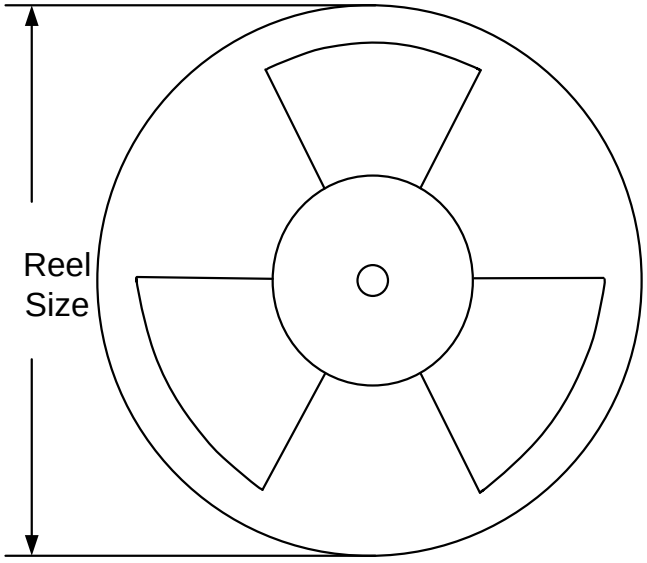
15.1 Tape Dimensions and Pin 1 Orientation

QFN2x3-20



Feeding Direction ⟶

15.2 Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN2x3-20	8	4	7"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Mar. 15, 2025	Revision 1.0	Initial Release

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