SQ25001

60V Synchronous Four-Switch Buck-Boost Controller

General Description

The SQ25001 is a synchronous four-switch buck-boost DC/DC controller that operates over a wide input voltage range of 6V to 60V. It features three operation modes: Buck, Boost, and Buck-Boost, which allow it to regulate the output voltage from an input voltage that is above, below, or equal to the output voltage. External components can be used to configure the soft-start time, 150kHz-400kHz switching frequency, and 4.5V-30V output voltage.

The SQ25001 can operate in either pulse width modulation (PWM) mode or pulse frequency modulation (PFM) mode under light load conditions, depending on the application's requirements for fast dynamic response or high efficiency. The optional spread spectrum function can help improve system EMI performance. The design features a 5V drive voltage and a peak drive current capability of over 3A, making it suitable for a wide range of industrial applications.

The SQ25001 ensures safe operation in all operating conditions, providing a power good flag, a fault indicator, input undervoltage lockout (UVLO), cycle-by-cycle (CBC) current limit protection, output undervoltage protection (UVP), output overvoltage protection (OVP), output overcurrent protection (OCP), and thermal shutdown to prevent damage to the device and ensure reliable operation.

The SQ25001 is available in a QFN5×5-32 package.

Key Features

- Four-Switch Single Inductor Architecture
- 6V to 60V Input Voltage Range
- 4.5V to 30V Output Voltage Range
- Peak Drive Current > 3A
- 0.8V ±1% Reference Voltage
- Adjustable Switching Frequency from 150kHz to 400kHz
- Adjustable Soft-Start Time
- PWM or PFM Operation Selectable in Light Load
- Smooth Pre-Biased Startup
- Spread-Spectrum Function
- Power Good Indicator
- Fault Indicator
- CBC Current Limit Protection
- Output Voltage Undervoltage, Overvoltage, and Overcurrent Protection
- Thermal Shutdown
- Package: QFN5×5-32
- MSL Rating: MSL3

Applications

- Industrial Applications
- High-Voltage DC-DC Converters

Typical Application

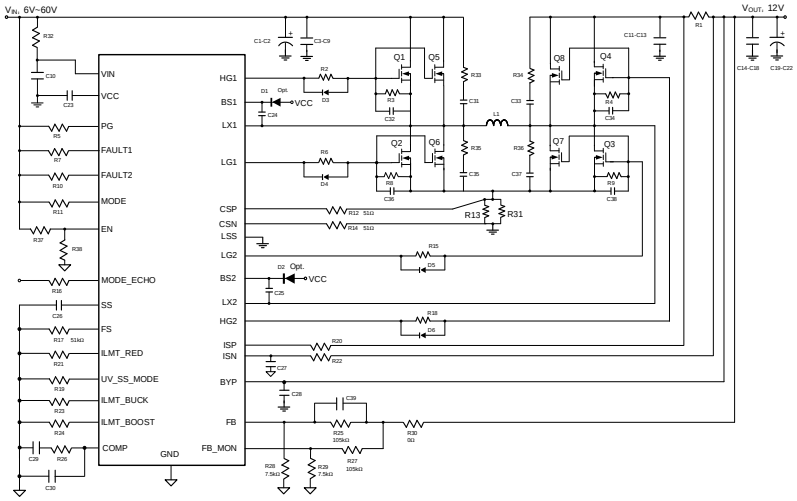


Figure 1. Schematic Diagram

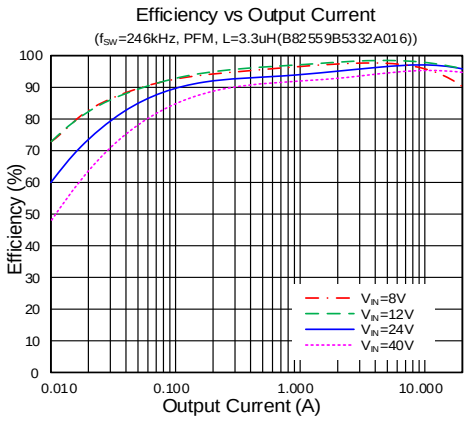


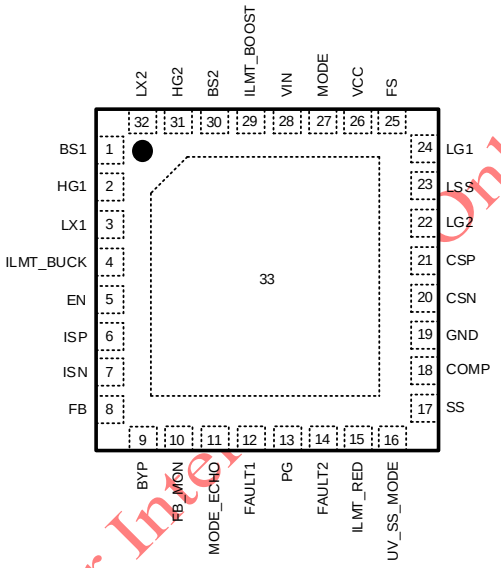
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ25001QEQ	QFN5×5-32 RoHS-Compliant and Halogen-Free	**AAPF*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN5×5-32)

Pin Description

Pin Number	Pin Name	Pin Description
1	BS1	Bootstrap pin for buck high side MOSFET driver. Connect a 0.22μF ceramic capacitor between this pin and the LX1 pin.
2	HG1	Buck high side MOSFET driver.
3	LX1	Buck side switching node. Connect to the source of SWA and the drain of SWB.
4	ILMT_BUCK	Threshold setting pin for cycle-by-cycle current limit protection and output overcurrent protection. Connect a resistor between this pin and GND to set the threshold.
5	EN	Enable control. Pull high to enable the device, pull low to disable the device. This pin can be used as an adjustable UVLO if it is connected to VIN and GND through a resistor divider. This pin has a 2MΩ internal pulldown resistor.
6	ISP	Positive input of average current sense amplifier.
7	ISN	Negative input of average current sense amplifier. To ensure accurate current sensing, ISP and ISN wiring should use Kelvin connections.
8	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: V_{OUT} = 0.8 × (1 + R25/R28). This pin can be used to monitor the output for undervoltage and overvoltage events.
9	BYP	Optional input to the VCC regulator when BYP voltage is higher than 6.5V. Connect a 1μF ceramic capacitor between this pin and GND. Do not leave floating.
10	FB_MON	Monitoring pin of output undervoltage and overvoltage protection.
11	MODE_ECHO	Mode state indicator pin. This pin outputs 3V when the MODE pin is pulled high and 0V when the MODE pin is pulled low.
12	FAULT1	Fault warning indicator, open-drain output. This pin is internally driven low when a fault is detected. Otherwise, it is in high impedance state and can be externally pulled high.
13	PG	Power good indicator, open-drain output. This pin is internally driven low when the FB pin voltage is between 90% and 110% of the reference voltage. PG is in a high impedance state, and can be externally pulled high when the FB pin voltage is lower than 85% or greater than 115% of the reference voltage.

Pin Number	Pin Name	Pin Description
14	FAULT2	Fault warning indicator, open-drain output. This pin is internally driven low when a fault is detected. Otherwise, it is in high impedance state and can be externally pulled high.
15	ILMT_RED	The threshold halved setting pin of cycle-by-cycle current limit protection and output overcurrent protection. Connect a resistor between this pin and GND to enable this function.
16	UV_SS_MODE	Configuration pin for output UVP and spread-spectrum functions.
17	SS	Soft-start time control pin. Connect a ceramic capacitor C_{SS} between this pin and GND to define the output voltage rise time t_{SS} (ms) = C_{SS} (nF) × 0.8V/10μA.
18	COMP	Compensation pin. Connect a RC network between this pin and GND.
19	GND	Ground pin.
20	CSN	Negative terminal of the low side current detection resistor.
21	CSP	Positive terminal of the low side current detection resistor. To ensure accurate current sensing, CSP and CSN wiring should use Kelvin connections.
22	LG2	Boost low side MOSFET drive.
23	LSS	Reference ground of LG1 and LG2. Connect this pin to GND on the PCB.
24	LG1	Buck low side MOSFET drive.
25	FS	Switching frequency programming pin. Connect an external resistor to GND to set the switching frequency f_{SW}. f_{SW} (kHz) = 5900/R_{FS} (kΩ) + 130 (kHz)
26	VCC	Internal LDO output pin. Decouple this pin to GND with at least a 4.7μF low ESR ceramic capacitor.
27	MODE	Mode control pin. Under light load conditions, the device is in forced CCM mode when the pin is pulled high, and in PFM mode when the pin is pulled low. This pin has a 1MΩ internal pulldown resistor.
28	VIN	Power input pin.
29	ILMT_BOOST	Threshold setting pin for peak current limit protection. Connect a resistor between this pin and GND to set the threshold.
30	BS2	Bootstrap pin for boost high side MOSFET driver. Connect a 0.22μF ceramic capacitor between this pin and the LX2 pin.
31	HG2	Boost high side MOSFET driver.
32	LX2	Boost side switching node. Connect to the source of SWD and the drain of SWC.
33	EP PAD	Exposed pad. Connect the exposed pad to GND on the PCB.

Block Diagram

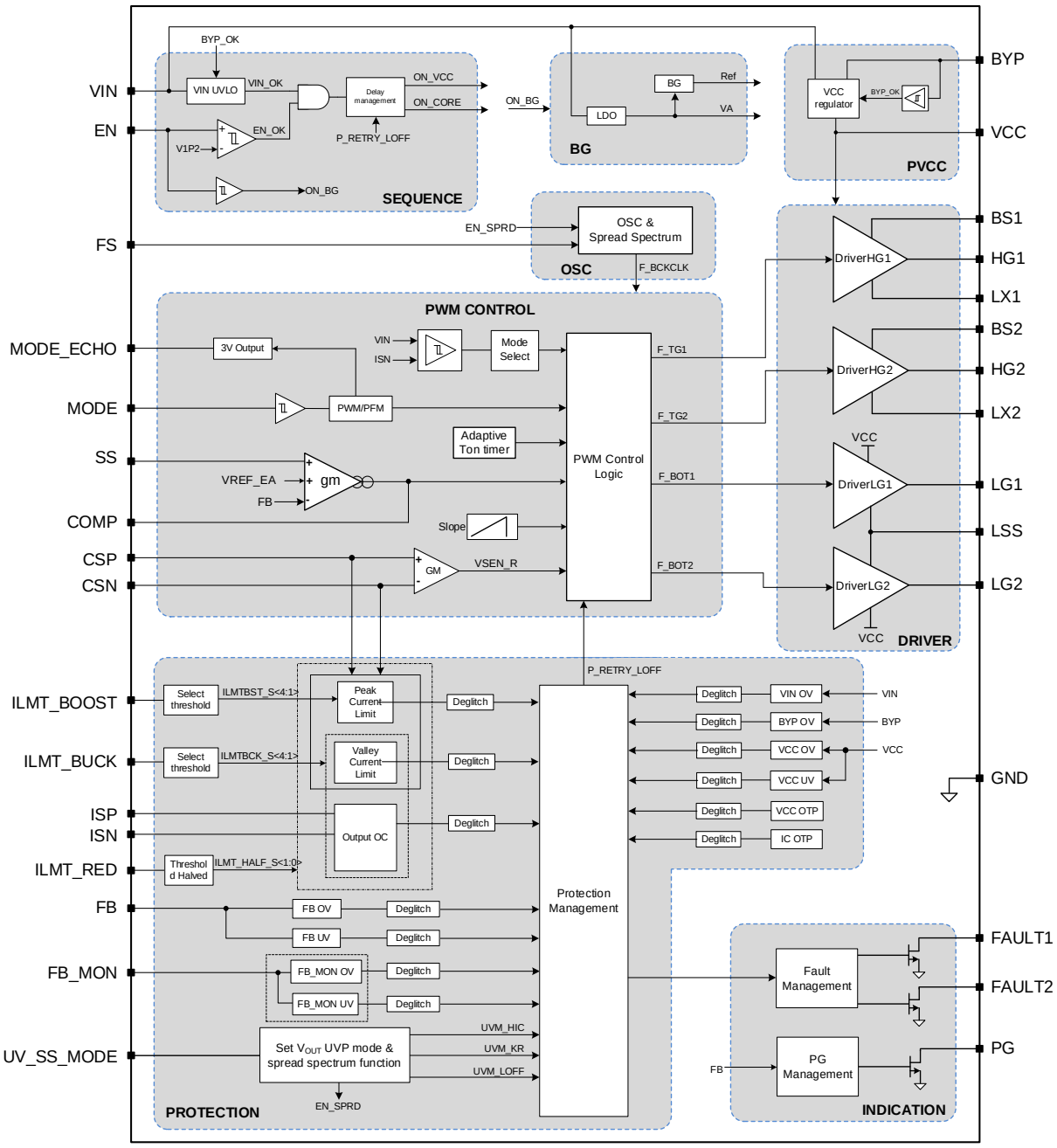


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN, EN, ISP, ISN, FB, FB_MON, FAULT1, FAULT2, PG, MODE, MODE_ECHO to GND	-0.3	65	V
LX1, LX2 to GND	-0.3	VIN+0.3	
BS1-LX1, BS2-LX2	-0.3	6	
VCC, LG1, LG2, CSN, CSP to GND	-0.3	6	
LSS to GND	-0.3	0.3	
BS1, HG1, BS2, HG2 to GND	-0.3	70	
ILMT_BUCK, ILMT_BOOST, ILMT_RED, UV_SS_MODE, FS, SS, COMP to GND	-0.3	60	
BYP to GND	-0.3	40	
Dynamic LX1, LX2 to GND voltage in 20ns Duration	-5	70	
Dynamic LX1, LX2 to GND voltage in 10ns Duration	-10	70	
Dynamic LG1, LG2, CSN, CSP, LSS to GND voltage in 20ns Duration	-5	6	
Junction Temperature Range	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-65	150	
ESD Susceptibility			
HBM (Human Body Mode)	±2000		V
CDM (Charge Device Mode) All pins	±700		

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	15	°C/W
θ_{JB} Junction-to-Board Thermal Resistance	3	
θ_{JC_TOP} Junction-to-Case (Top) Thermal Resistance	7.5	
Ψ_{JT} Junction-to-Top Characterization Parameter	0.1	
P_D Power Dissipation T_A = 25°C	6.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	6	60	V
BYP	6.5	36	
ISP, ISN to GND	4.5	30	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	125	

Electrical Characteristics

(V_{IN} = 12V, V_{EN} = 3.3V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified. These values are guaranteed by test, design, or statistical correlation. (**Note 4**))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		6		60	V
	Input UVLO Rising Threshold	V_{UVLO_R}		5.5	5.7	5.9	
	Input UVLO Falling Threshold	V_{UVLO_F}	V_{BYP} < 6.2V	5.1	5.3	5.5	
			V_{BYP} > 6.5V	3.4	3.6	3.8	
	V_{IN} Overvoltage Threshold	V_{OV_VIN}	Rising	60	62	65	
	V_{IN} Overvoltage Hysteresis	V_{OVHYS_VIN}			2		
	Quiescent Current	I_Q	V_{EN} = 0V		30	60	µA
			V_{EN} = 3.3V, no switching		2.5	4	mA
BYP	BYP Input Rising Threshold	V_{BYP_R}	BYP rising	6.2	6.5	6.8	V
	BYP Input Hysteresis	V_{BYP_HYS}			0.3		
	BYP OVP Threshold	V_{OV_BYP}		34	36	38	
	BYP OVP Hysteresis	V_{OVHYS_BYP}			1.8		
Output	V_{OUT} Voltage Range	V_{OUT}	(Note 5)	4.5		30	V
	Soft-Start Charging Current	I_{SS}		7	10	13	µA
	Startup Delay Time	t_{DELAY_SS}	Time from EN high to switching	8	13	18	ms
VCC	VCC Regulation Voltage	V_{VCC}	I_{VCC} = 0A	4.8	5	5.2	V
	VCC Load Regulation		I_{VCC} = 0mA to 100mA		1	4	%
	VCC Line Regulation		I_{VCC} = 60mA, V_{IN} = 6V to 60V		1	4	
	VCC Current Limit	I_{VCC_ILMT}	V_{VCC} = 4.5V		135		mA
	VCC Undervoltage Threshold	V_{UV_VCC}	VCC falling	3.35	3.5	3.65	V
	VCC Undervoltage Hysteresis	V_{UVHYS_VCC}	Rising-falling		0.2		
	VCC UVP Filter Time	t_{UV_VCC}			8		µs
	VCC Overvoltage Threshold	V_{OV_VCC}	VCC rising	5.75	6	6.25	V
	VCC Overvoltage Hysteresis	V_{OVHYS_VCC}	Rising-falling		0.2		
	VCC OVP Filter Time	t_{OV_VCC}			8		µs
Enable (EN)	EN Rising Threshold	V_{EN}		1.15	1.20	1.25	V
	EN Hysteresis Voltage	V_{EN_HYS}			0.3		
	EN Pulldown Resistance	R_{EN_PD}		1.5	2	3.5	MΩ
	EN Rising Filter Time	t_{EN_R}			1		ms
	EN Falling Filter Time	t_{EN_F}			10		µs
MODE	MODE Logic High Voltage	V_{MODE_H}		1.7			V
	MODE Logic Low Voltage	V_{MODE_L}				0.7	
	MODE Pulldown Resistance	R_{MODE_PD}		0.8	1	1.6	MΩ
	MODE_ECHO Output Voltage	V_{ECHO}		2.5	3	3.45	V
	MODE_ECHO Pullup Current	I_{ECHO_U}	MODE_ECHO pin force 0V		1		mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	MODE_ECHO Pulldown Current	I_{ECHO_D}	MODE_ECHO pin force 3V		1		
Frequency	Switching Frequency Range			150		400	kHz
	Switching Frequency	f_{SW}	R_{UVM} = 10kΩ, R_{FS} = 51kΩ	215	246	275	
Spread-Spectrum	Highest Spread-Spectrum above Oscillator Frequency	f_{SPRD_H}	R_{UVM} = 68kΩ		10		% f_{SW}
	Lowest Spread-Spectrum below Oscillator Frequency	f_{SPRD_L}	R_{UVM} = 68kΩ		-10		
FB Regulation	FB Reference Voltage	V_{FB}	T_J=25°C	0.792	0.8	0.808	V
			40°C≤T_J≤125°C	0.788	0.8	0.812	
	FB Line Regulation		V_{IN} = 6V to 40V, FCCM		0.5	0.8	%
	FB Load Regulation		0.1A to 20A		0.5	0.8	
	FB Voltage Regulation Amplifier g_m	g_m	Buck mode		1000		µS
			Buck-boost, boost mode		700		
	FB Input Current	I_{FB}	V_{FB} = 0.8V	-50		50	nA
	FB Overvoltage Threshold	V_{OV_FB}	Rising	0.92	0.96	1.00	V
	FB Overvoltage Hysteresis	V_{OVHYS_FB}		35	50	65	mV
	FB Undervoltage Threshold	V_{UV_FB}	Falling	0.36	0.4	0.44	V
	FB Undervoltage Hysteresis	V_{UVHYS_FB}		35	50	65	mV
	FB_MON Overvoltage Threshold	V_{OV_FBM}	Rising	0.92	0.96	1.00	V
	FB_MON Overvoltage Hysteresis	V_{OVHYS_FBM}		35	50	65	mV
	FB_MON Undervoltage Threshold	V_{UV_FBM}	Falling	0.36	0.4	0.44	V
	FB_MON Undervoltage Hysteresis	V_{UVHYS_FBM}		35	50	65	mV
	FB_MON Input Current	I_{FBM}	V_{FB} = 0.8V	-50		50	nA
Current Limit	Valley Current Limit Threshold	$V_{VY\_H\_TH1}$	R_{ILMT_BUCK} = 68kΩ	33	40	47	mV
		$V_{VY\_H\_TH2}$	R_{ILMT_BUCK} = 51kΩ	48	55	62	
		$V_{VY\_H\_TH3}$	R_{ILMT_BUCK} = 39kΩ	60	67	74	
		$V_{VY\_H\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	73	80	87	
	Valley Current Limit Reduced Threshold	$V_{VY\_L\_TH1}$	R_{ILMT_BUCK} = 68kΩ	14	20	26	
		$V_{VY\_L\_TH2}$	R_{ILMT_BUCK} = 51kΩ	21	27.5	34	
		$V_{VY\_L\_TH3}$	R_{ILMT_BUCK} = 39kΩ	29	35	41	
		$V_{VY\_L\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	36.5	42.5	48.5	
	ILMT_BUCK Pin Bias Current	I_{ILMT_BUCK}		28.2	30	31.8	µA
	ILMT_BUCK Pin Voltage Range	Open	Safe state (latch off)	3.2			V
		V_{BUK_RG1}	V_{VY_TH1} current limit	1.83	2.04	2.26	
		V_{BUK_RG2}	V_{VY_TH2} current limit	1.38	1.53	1.69	
		V_{BUK_RG3}	V_{VY_TH3} current limit	1.07	1.17	1.28	
		V_{BUK_RG4}	V_{VY_TH4} current limit	0.25	0.6	0.98	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
		Short to GND	Safe state (latch off)			0.1	
	Peak Current Limit Threshold	$V_{PK\_H\_TH1}$	R_{ILMT_BOOST} = 68kΩ	58	65	72	mV
		$V_{PK\_H\_TH2}$	R_{ILMT_BOOST} = 51kΩ	73	80	87	
		$V_{PK\_H\_TH3}$	R_{ILMT_BOOST} = 39kΩ	88	95	102	
		$V_{PK\_H\_TH4}$	R_{ILMT_BOOST} = 30kΩ/20kΩ/10kΩ	103	110	117	
	Peak Current Limit Reduced Threshold	$V_{PK\_L\_TH1}$	R_{ILMT_BOOST} = 68kΩ	26.5	32.5	38.5	
		$V_{PK\_L\_TH2}$	R_{ILMT_BOOST} = 51kΩ	34	40	46	
		$V_{PK\_L\_TH3}$	R_{ILMT_BOOST} = 39kΩ	41.5	47.5	53.5	
		$V_{PK\_L\_TH4}$	R_{ILMT_BOOST} = 30kΩ/20kΩ/10kΩ	49	55	61	
	ILMT_BOOST Pin Bias Current	I_{ILMT_BOOST}		28.2	30	31.8	μA
	ILMT_BOOST Pin Voltage Range	Open	Safe state (latch off)	3.2			V
		V_{BST_RG1}	V_{PK_TH1} current limit	1.83	2.04	2.26	
		V_{BST_RG2}	V_{PK_TH2} current limit	1.38	1.53	1.69	
		V_{BST_RG3}	V_{PK_TH3} current limit	1.07	1.17	1.28	
		V_{BST_RG4}	V_{PK_TH4} current limit	0.25	0.6	0.98	
		Short to GND	Safe state (latch off)			0.1	
	ILMT_RED Pin Bias Current	I_{ILMT_RED}		28.2	30	31.8	μA
	ILMT_RED Pin Voltage	Open	Safe state (latch off)	3.2			V
		V_{RED_TH1}	R_{ILMT_RED} = 51kΩ/39kΩ, normal threshold	1.07		1.69	
		V_{RED_TH2}	R_{ILMT_RED} = 30kΩ/20kΩ, valley/peak current limit thresholds reduced	0.44		0.98	
		V_{RED_TH3}	R_{ILMT_RED} = 10kΩ, valley/peak, output current limit thresholds reduced	0.25		0.36	
		Short to GND	Safe state (latch off)			0.1	
Output Overcurrent	Output Average Current Limit Threshold	$V_{OC\_H\_TH1}$	R_{ILMT_BUCK} = 68kΩ	18	25	32	mV
		$V_{OC\_H\_TH2}$	R_{ILMT_BUCK} = 51kΩ	33	40	47	
		$V_{OC\_H\_TH3}$	R_{ILMT_BUCK} = 39kΩ	48	55	62	
		$V_{OC\_H\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	63	70	77	
	Output Average Current Limit Reduced Threshold	$V_{OC\_L\_TH1}$	R_{ILMT_BUCK} = 68kΩ	6.5	12.5	18.5	
		$V_{OC\_L\_TH2}$	R_{ILMT_BUCK} = 51kΩ	14	20	26	
		$V_{OC\_L\_TH3}$	R_{ILMT_BUCK} = 39kΩ	21.5	27.5	33.5	
		$V_{OC\_L\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	29	35	41	
	ISP Pin Bias Current		V_{ISP} = V_{ISN} = 12V		25	35	μA
	ISP/ISN Input Common Mode Range	$V_{RANGE\_ISP/N}$		4.5		30	V
UV_SS_MODE	UV_SS_MODE Pin Bias Current	I_{UVM}		28.2	30	31.8	μA
	UV_SS_MODE Pin Voltage Range	Open	Safe state (latch off)	3.2			V
		V_{UVM_RG1}	Hiccup/SPRD on	1.83	2.04	2.26	
		V_{UVM_RG2}	Continue running/SPRD on	1.38	1.53	1.69	
		V_{UVM_RG3}	Latch off/SPRD on	1.07	1.17	1.28	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
		V_{UVM_RG4}	Hiccup/SPRD off	0.78	0.9	0.98	
		V_{UVM_RG5}	Continue running/SPRD off	0.44	0.6	0.67	
		V_{UVM_RG6}	Latch off/SPRD off	0.25	0.3	0.36	
		Short to GND	Safe state (latch off)			0.1	
Indicator	PG Threshold	V_{PG_FF}	Falling, PG from low to high	80	85	90	$\%V_{REF}$
		V_{PG_RG}	Rising, PG from high to low	85	90	95	
		V_{PG_RF}	Rising, PG from low to high	110	115	120	
		V_{PG_FG}	Falling, PG from high to low	105	110	115	
	PG Delay Time	t_{PG_DLY}		45	80	100	μs
	PG, FAULT1, FAULT2 Output Low	$V_{PG/FAULT\_L}$	I_{SINK} = 1mA			0.3	V
	PG, FAULT1, FAULT2 Leakage Current	$I_{PG/FAULT\_LK}$	V_{DS} = 3.3V			1	μA
Region Transition	Boost to Buck-Boost	f_{SW} ≤ 300kHz	V_{OUT}-V_{IN} or V_{IN}/V_{OUT}		1.7		V
					80		%
	Buck-Boost to Boost		V_{OUT}-V_{IN} and V_{IN}/V_{OUT}		2.3		V
					75.9		%
	Buck-Boost to Buck		V_{IN}-V_{OUT} and V_{OUT}/V_{IN}		2.3		V
					74		%
	Buck to Buck-Boost		V_{IN}-V_{OUT} or V_{OUT}/V_{IN}		1.7		V
					79		%
	Boost to Buck-Boost	f_{SW} > 300kHz	V_{OUT}-V_{IN} or V_{IN}/V_{OUT}		1.7		V
					75.9		%
	Buck-Boost to Boost		V_{OUT}-V_{IN} and V_{IN}/V_{OUT}		2.3		V
					71.8		%
	Buck-Boost to Buck		V_{IN}-V_{OUT} and V_{OUT}/V_{IN}		2.3		V
					63.8		%
	Buck to Buck-Boost		V_{IN}-V_{OUT} or V_{OUT}/V_{IN}		1.7		V
					68.5		%
	Buck/Boost to Buck-Boost Blanking time		(Note 5)		2		μs
	Buck-Boost to Buck/Boost Blanking time		(Note 5)		2		
Drivers	LG1, LG2 Pullup MOSFET On-Resistance	R_{LG_U}	V_{VCC} = 5V, V_{LG} = 0V		1		Ω
	LG1, LG2 Pulldown MOSFET On-Resistance	R_{LG_D}	V_{VCC} = 5V, V_{LG} = 5V		0.3		
	HG1, HG2 Pullup MOSFET On-Resistance	R_{HG_U}	$V_{(BS-LX)}$ = 5V, V_{HG} = 0V		1		
	HG1, HG2 Pulldown MOSFET On-Resistance	R_{HG_D}	$V_{(BS-LX)}$ = 5V, V_{HG} = 5V		0.3		
	LG1, LG2 Rising and Falling Time	t_{RISE_LG}	C_{TEST} = 22nF, 10% to 90%, (Note 5)		30	80	ns
		t_{FALL_LG}	C_{TEST} = 22nF, 90% to 10%, (Note 5)		15	40	
	HG1, HG2 Rising and Falling Time	t_{RISE_HG}	C_{TEST} = 22nF, 10% to 90%, (Note 5)		30	80	
		t_{FALL_HG}	C_{TEST} = 22nF, 90% to 10%, (Note 5)		15	40	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum On-Time	HG1, HG2 Minimum On-Time	$t_{ON\_HG\_MIN}$	(Note 5)	250	300	350	ns
	LG1, LG2 Minimum On-Time	$t_{ON\_TG\_MIN}$	(Note 5)	400	450	500	
OTP	Thermal Shutdown Temperature	t_{SD}	(Note 5)	150	165	180	˚C
	Thermal Shutdown Hysteresis	t_{SD_HYS}	(Note 5)		15		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in natural convection at T_A = 25°C on a 2oz four-layer Silergy evaluation board. The case temperature θ_{JC} is measured at pin 26.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions, such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

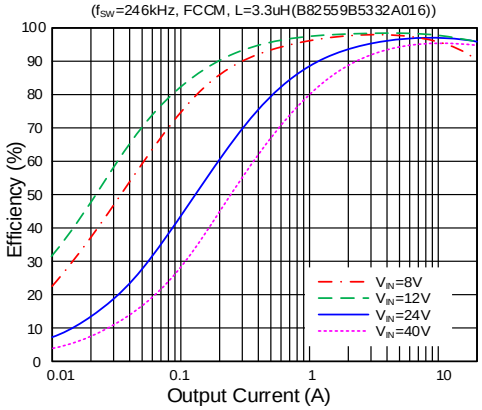
Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 12V, L = 3.3μH, C_{OUT} = 8 × 22μF/25V + 4 × 150μF/25V, f_{SW} = 246kHz, unless otherwise noted. The circuit is shown in the Application Schematic section.)

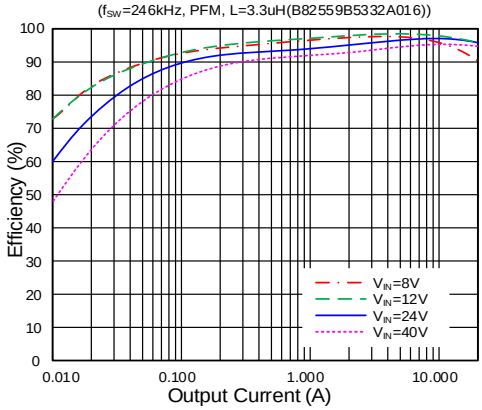
Efficiency vs Output Current

(f_{SW}=246kHz, FCCM, L=3.3uH(B82559B5332A016))



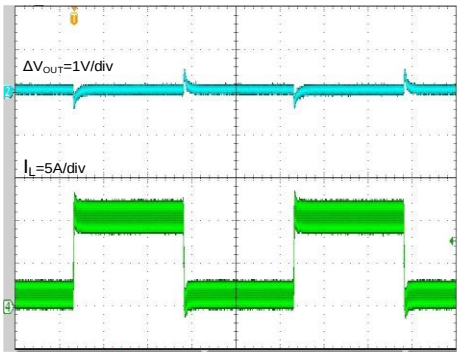
Efficiency vs Output Current

(f_{SW}=246kHz, PFM, L=3.3uH(B82559B5332A016))



Load Transient

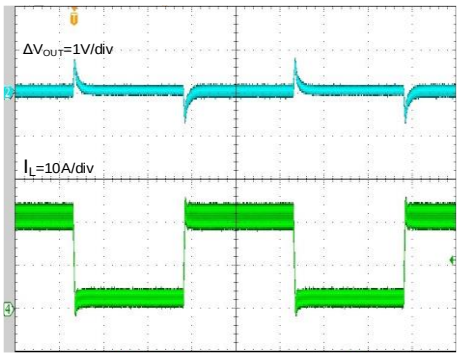
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=1~9A)



Time (4ms/div)

Load Transient

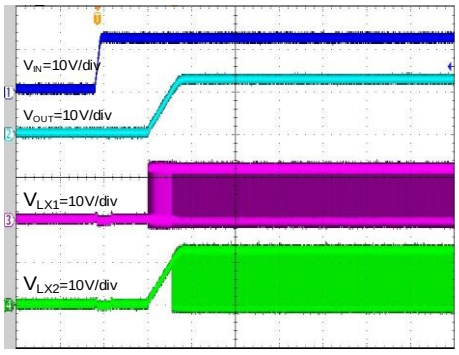
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=2~18A)



Time (4ms/div)

Startup From VIN

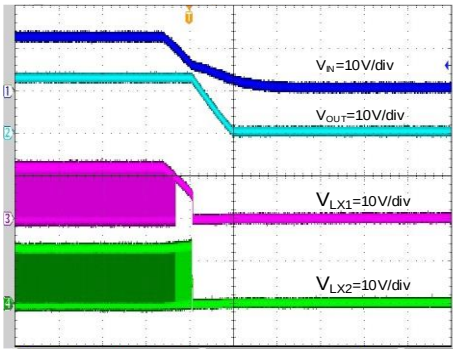
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=1A)



Time (10ms/div)

Shutdown From VIN

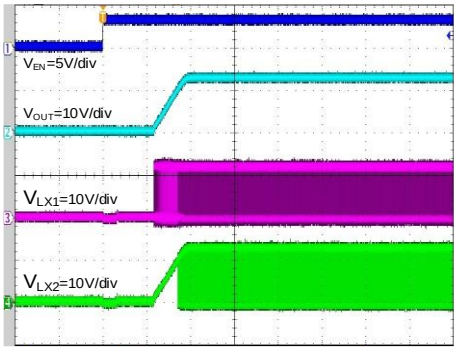
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=1A)



Time (10ms/div)

Startup From Enable

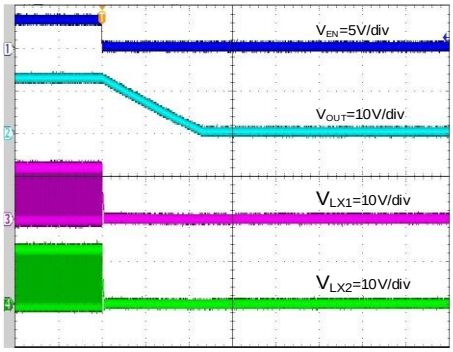
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=1A)



Time (10ms/div)

Shutdown From Enable

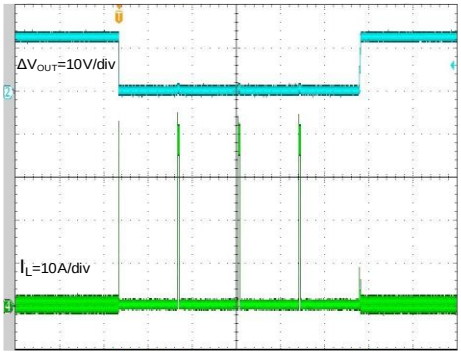
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=1A)



Time (4ms/div)

Short Circuit Protection

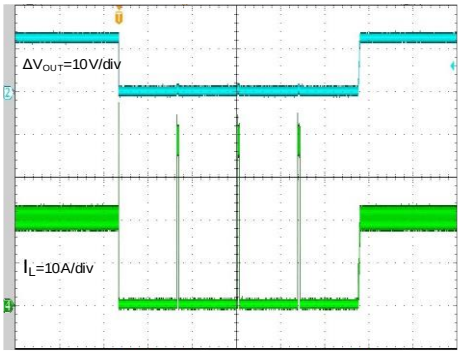
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=0A)



Time (200ms/div)

Short Circuit Protection

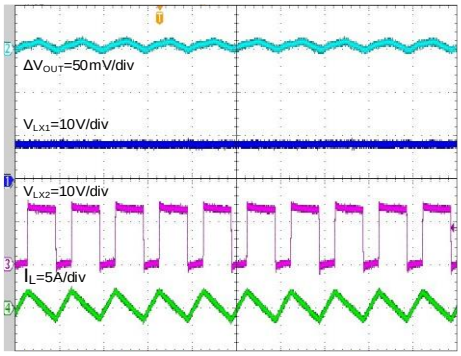
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=20A)



Time (200ms/div)

Output Ripple

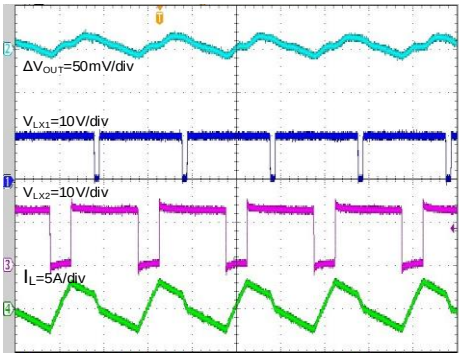
(V_{IN}=8V,V_{OUT}=12V,I_{OUT}=0A)



Time (4μs/div)

Output Ripple

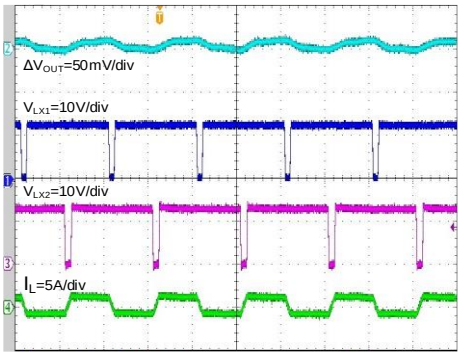
(V_{IN}=10V,V_{OUT}=12V,I_{OUT}=0A)



Time (4μs/div)

Output Ripple

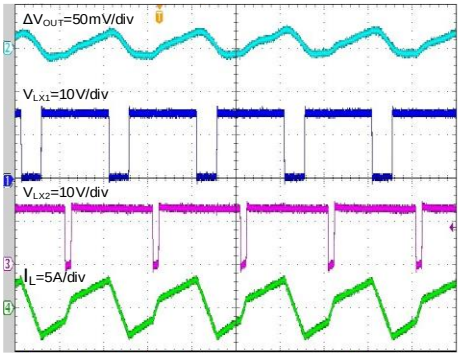
(V_{IN}=12V,V_{OUT}=12V,I_{OUT}=0A)



Time (4μs/div)

Output Ripple

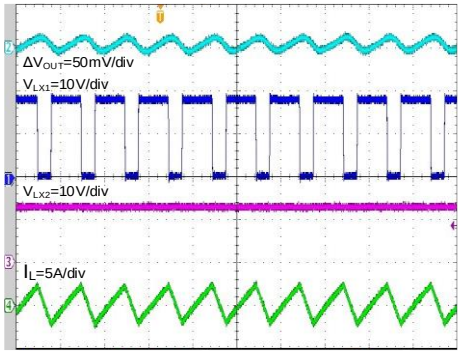
(V_{IN}=15V,V_{OUT}=12V,I_{OUT}=0A)



Time (4μs/div)

Output Ripple

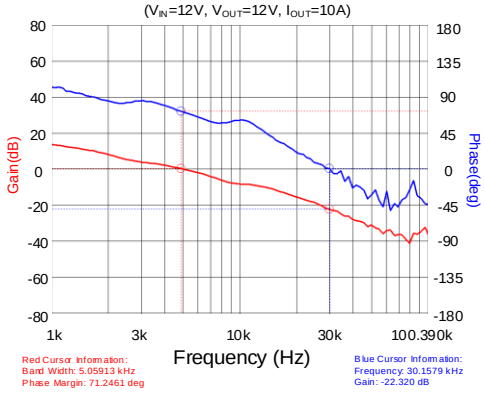
(V_{IN}=18V,V_{OUT}=12V,I_{OUT}=0A)



Time (4μs/div)

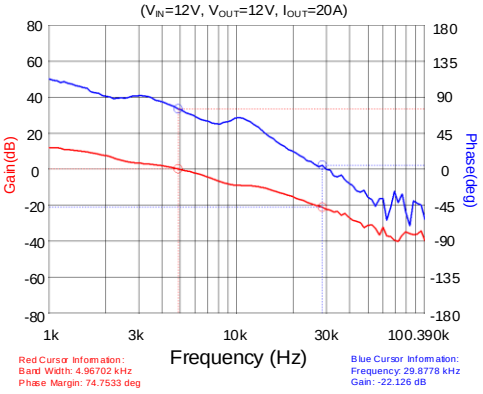
Bode Plot

(V_{IN}=12V, V_{OUT}=12V, I_{OUT}=10A)



Bode Plot

(V_{IN}=12V, V_{OUT}=12V, I_{OUT}=20A)



Functional Description

The SQ25001 is a synchronous four-switch buck-boost DC/DC controller that operates over a wide input voltage range of 6V to 60V. It features three operation modes: Buck, Boost, and Buck-Boost, which allow it to regulate the output voltage from an input voltage that is above, below, or equal to the output voltage. External components can be used to regulate the soft-start time, 150kHz-400kHz switching frequency, and 4.5V-30V output voltage.

The SQ25001 can operate in either pulse width modulation (PWM) mode or pulse frequency modulation (PFM) mode under light load conditions, depending on the application's requirement for fast dynamic response or high efficiency. The optional spread spectrum function can help improve system EMI performance. The design features a 5V drive voltage and a peak drive current capability of over 3A, making it suitable for a wide range of industrial applications.

The SQ25001 ensures safe operation in all operating conditions, providing a power good flag, a fault indicator, input undervoltage lockout (UVLO), cycle-by-cycle (CBC) current limit protection, output undervoltage protection (UVP), output overvoltage protection (OVP), output overcurrent protection (OCP), and thermal shutdown to prevent damage to the device and ensure reliable operation.

The SQ25001 is available in a QFN5×5-32 package.

Operating Mode

To obtain a continuous and stable output voltage, the controller is designed to operate according to the difference and proportion of V_{IN} and V_{OUT}, as well as the switching frequency, to ensure a successful transition among Buck, Buck-Boost, and Boost operating modes. A reasonable blanking time during mode transitions is used to prevent instability. The SQ25001 uses current-controlled architecture to guarantee the current limit, based on sensing current on the low side shunt current resistors R_{13} and R_{31}.

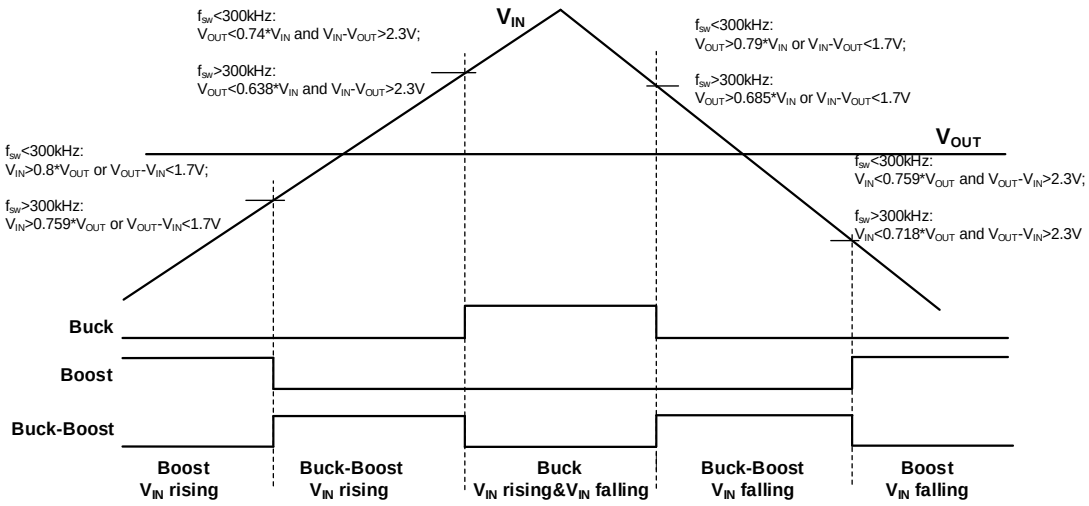
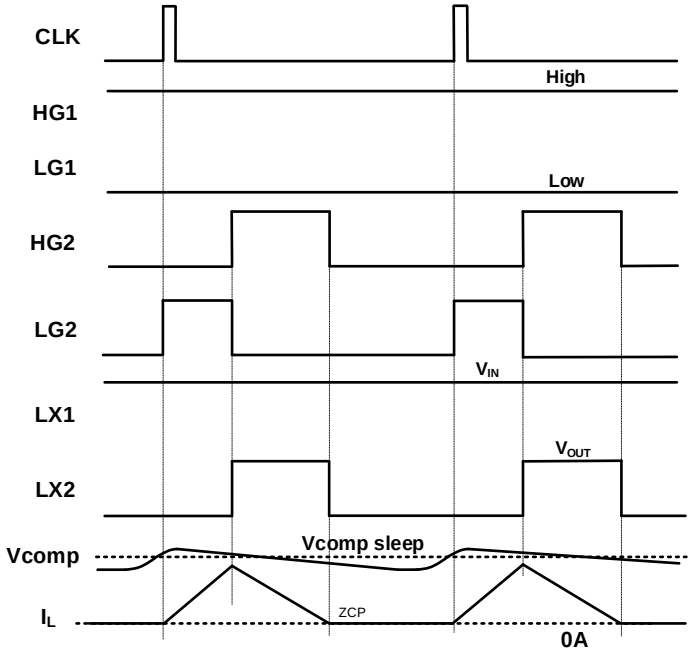


Figure 4. Operating Modes Transition

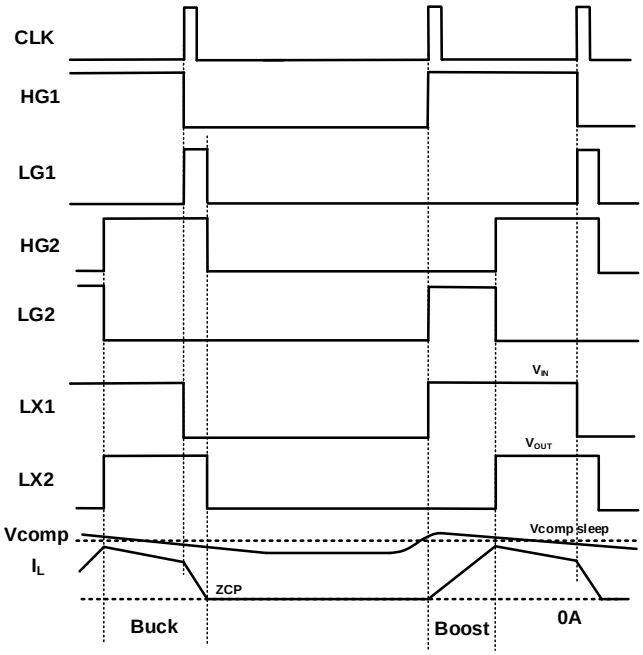
PFM Mode Operation

The SQ25001 provides two light load operation modes: pulse frequency modulation (PFM) and forced continuous current mode (FCCM). In PFM mode, the low side synchronous rectifier (SWB in Buck mode or SWD in Boost mode) is turned off when the current through the rectifier ramps to zero, thereby preventing recirculation current that can reduce efficiency under light load conditions. Additionally, the output of the error amplifier (V_{COMP}) naturally decreases, reducing the inductor current during light load conditions. When V_{COMP} decreases further with the decreasing load and reaches the preset low threshold, the device stops switching and enters sleep mode. This reduces switching power loss and quiescent current, thereby further improving light load efficiency. To prevent voltage starvation in the bootstrap capacitors during sleep mode, the SQ25001 will turn on SWB and SWC to charge the bootstrap capacitors 20μs after entering sleep mode. Switching resumes when V_{COMP} rises above the low threshold. When operating in Buck mode, the device will enter constant on-time control when zero-crossing is detected, and exit constant on-time control when zero-crossing has not been detected for 16

consecutive switching cycles. In Boost and Buck-Boost mode, only the first switching cycle is fixed on-time control when the device exits sleep mode.



(a) Boost Mode



(b) Buck-Boost Mode (V_{IN}<V_{OUT})

Power Up/Down Sequence

V_{IN} On/Off

When the V_{IN} voltage exceeds the UVLO rising threshold, the VCC voltage begins to raise after a delay time of t_{EN_FIT} + t_{VCC_DY} (where t_{EN_FIT} is the EN rising filter time and t_{BIST} is a 3ms fixed delay for self-check), and the output voltage starts to regulate after a delay time of t_{DELAY_SS}. The PG signal remains active until the output current monitor BIST is completed. Conversely, when the V_{IN} voltage falls below the UVLO falling threshold, the controller stops switching after a 5µs filter time (t_{UV_VIN}), and the PG signal is pulled up after an 80µs filter time, regardless of whether the output voltage is lower than 85% × V_{OUT}. The VCC regulator is turned off 200µs later. The device remains completely turned off until the V_{IN} voltage falls below the POR off voltage.

Note: *The PG, FAULT1, and FAULT2 signals are connected to V_{IN} through an external resistor.*

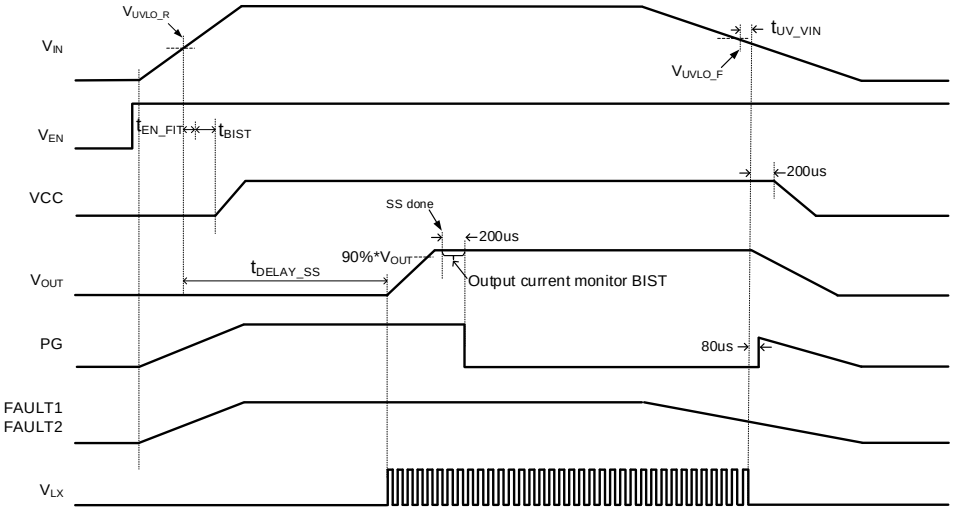


Figure 5. V_{IN} On/Off Sequence

EN On/Off

If V_{IN} powers up first, and then the EN signal is pulled from low to high, the VCC voltage begins to build up after t_{EN_FIT} + t_{BIST}, and the output voltage starts to regulate after t_{DELAY_SS}. The power-good (PG) signal is pulled down after the output current monitor BIST. When the EN pin transitions from high to low and exceeds 10µs, the controller will stop switching immediately, and the PG signal will be pulled up after an 80µs filter time, regardless of whether the output voltage is lower than 85% × V_{OUT}. The VCC regulator is turned off 200µs later. When EN is off, the FAULT1 and FAULT2 signals will not indicate any faults.

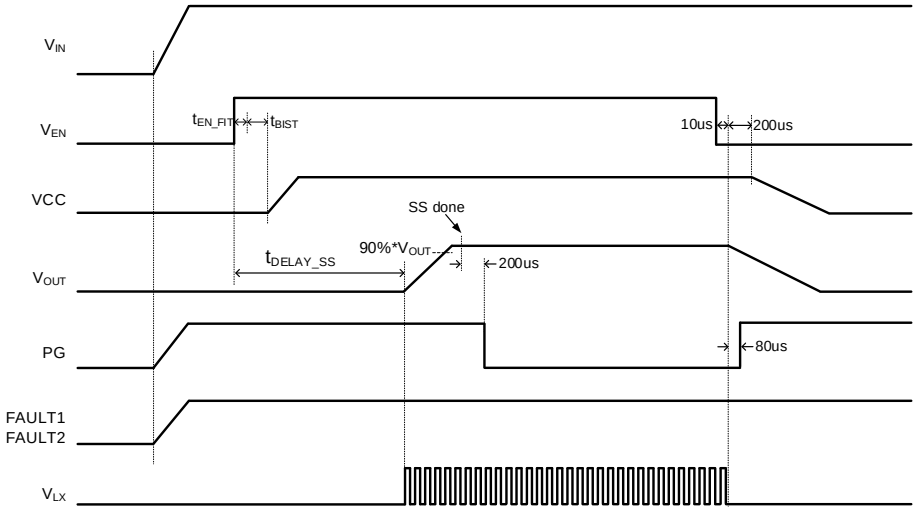


Figure 6. EN On/Off Sequence

V_{IN} Power Supply

The power supply of SQ25001 comes from the battery systems, and its working voltage range must fully meet the requirements. The part is fully compliant with 12V and 24V battery systems. The internal circuits, including bandgaps, monitoring units, and control loops, receive their power supply from V_{IN}. There is a 5.7V rising UVLO threshold and a 5.3V falling threshold voltage for the V_{IN} power supply when V_{BYP} is lower than 6.2V. The falling threshold voltage is 3.6V when V_{BYP} is higher than 6.5V. If the input voltage exceeds 62V, it will trigger overvoltage protection, force the controller to stop switching, and pull FAULT1 and FAULT2 down after a 5µs filter time.

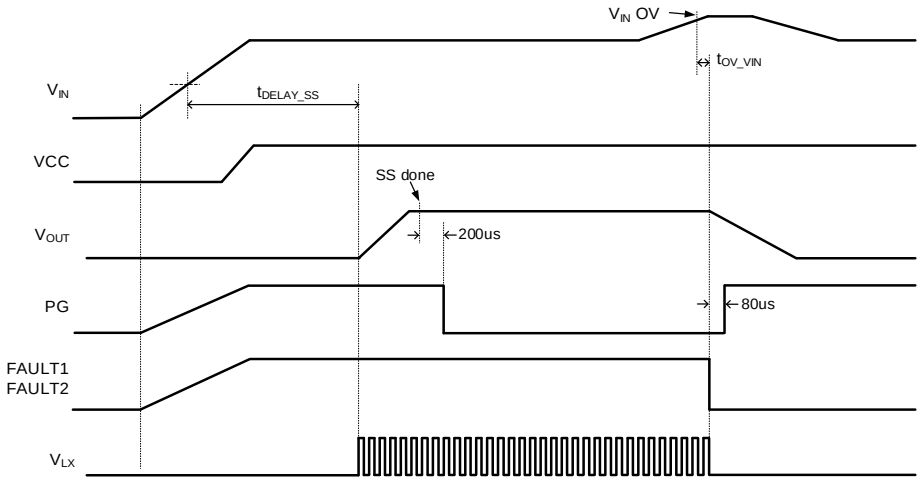


Figure 7. V_{IN} Overvoltage Protection

Enable Control

The EN input supports high voltage and logic-compatible thresholds. The input comparator design features a relatively accurate 1.2V rising threshold with 0.3V of hysteresis. When the EN input is driven above 1.2V, normal device operation is

enabled after 1ms and the converter starts switching. Conversely, when the EN voltage falls below 0.9V, the device stops switching after 10µs. This pin is equipped with a 2MΩ internal pulldown resistor.

VCC Linear Regulator and BYP Input

The 5V internal linear regulator output (VCC) provides the power supply for the drivers HG1, LG1, HG2, and LG2.

To ensure clean and stable VCC supply, connect a low ESR ceramic capacitor with a capacitance of at least 4.7µF between the VCC pin and GND, placing it close to the VCC pin using a short, direct copper trace to the nearest ground. The linear regulator has a typical 135mA current capacity, but it folds back to 65mA when VCC voltage is low to reduce power loss and device heating. The SQ25001 offers real-time detection for VCC undervoltage, overvoltage, and overtemperature. As soon as one of these faults is continuously detected for a duration longer than the 8µs filter time, the controller will stop switching and pull FAULT1 and FAULT2 down without retry.

To improve efficiency and avoid device overheating caused by high input voltage, the controller provides an additional power supply pin BYP for the linear regulator. When the voltage on the BYP pin is higher than 6.5V, the power will supply transitions from V_{IN} to V_{BYP}. It is recommended to connect BYP to V_{OUT}. If the BYP voltage continuously exceeds 36V for a duration longer than the 5µs filter time, the controller will stop switching and pull FAULT1 and FAULT2 low. The BYP pin should be decoupled to GND with a 1µF ceramic capacitor, and pulled to GND if it is not used.

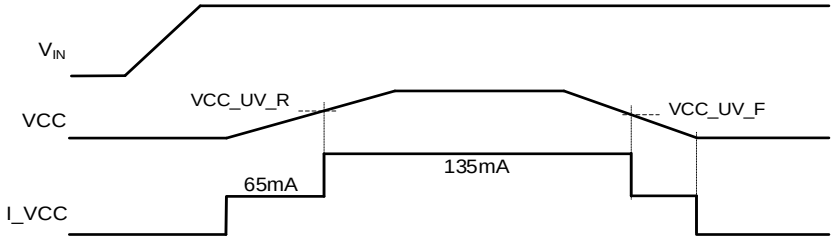


Figure 8. VCC Current Limit Fold Back

Drivers

As a synchronous four-switch buck-boost controller, the SQ25001 ensures fast pullup and pulldown drive signals for external MOSFETs. The charging current is supplied through VCC (for low side drivers) and bootstrap structures (for high side drivers), enabling the controller to support high power applications. With a typical 3A source current and 6A sink current capability, the SQ25001 can drive two parallel MOSFETs simultaneously in high power applications.

Adjustable Switching Frequency

The switching frequency can be adjusted from 150 kHz to 400 kHz using an external resistor R_{FS} connected from the FS pin to GND. It is recommended to place R_{FS} close to the FS pin to minimize noise coupling. To improve system stability, when the resistance from the FS pin to GND is larger than 500kΩ (i.e., the FS pin is open) or smaller than 10kΩ (i.e., the FS pin is shorted), the controller will stop switching and pull FAULT1 and FAULT2 low after a 3µs filter time, without retry.

Adjustable Soft-Start Time

The SS pin serves as an external interface for the internal soft-start circuitry, controlling the output voltage slope during startup to prevent excessive inrush current and unwanted voltage drops from high impedance power sources, and ensuring a controlled output voltage rise time. The internal reference rises with a slope controlled by an external capacitor connected from the SS pin to GND, which is charged by an internal 10µA current source. The capacitor is charged gradually until its voltage reaches 0.8V, at which point the reference voltage will transition to an internal fixed 0.8V voltage source. Leaving the SS pin open results in the fastest startup ramp, typically 1.5ms.

UV_SS_MODE

The UV_SS_MODE pin independently configures the following functions:

- Behavior of output UVP (hiccup, latch off, or continue running)
- Frequency spread-spectrum function (3kHz modulation frequency and ±10% modulation amplitude)

There is a relatively accurate 30µA current source delivering current through the UV_SS_MODE pin. Connect the UV_SS_MODE pin to GND with different resistances to configure the above functions. There are three different protection behaviors to choose from when the output triggers undervoltage protection: hiccup, latch off, or continue running. The

UV_SS_MODE pin can also enable the spread-spectrum function to optimize EMI performance. When the spread-spectrum function is enabled, the operating switching frequency varies by ±10% centered on the set switching frequency, with a 3kHz modulation frequency of a triangular wave.

To improve system stability, when the voltage on the UV_SS_MODE pin is higher than 3.2V (i.e., the UV_SS_MODE pin is open) or lower than 0.1V (i.e., the UV_SS_MODE pin is shorted), the controller will stop switching and pull FAULT1 and FAULT2 low after a 3μs filter time, without retry.

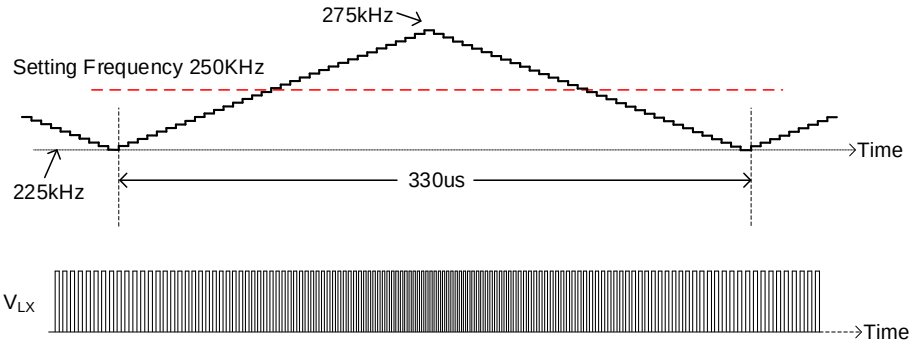


Figure 9. Spread-Spectrum Function

Mode Control

The SQ25001 provides the MODE and MODE_ECHO pins to achieve different application requirements under light load. When a fast response is required from light load to heavy load, pulling the MODE pin high selects FCCM mode, and the MODE_ECHO pin will output 3V after a 200μs delay time to indicate that the chip has entered the FCCM operating state. To achieve high efficiency at light load, pulling the MODE pin low selects PFM mode after a 100μs delay, and the MODE_ECHO pin will output 0V after a 200μs delay indicating that the chip has entered the PFM operating state. The default state of the chip is PFM mode if the MODE pin is floating, as it has a 1MΩ internal pulldown resistor.

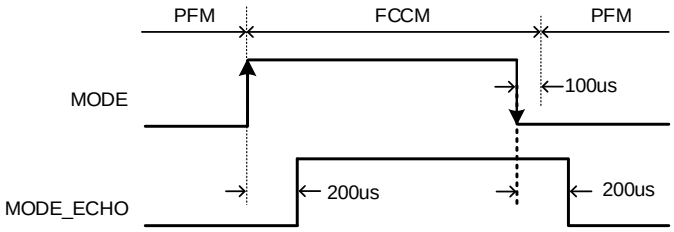


Figure 10. Mode Control

Fault Protections

Peak/Valley Current Limit Protection

The SQ25001 uses a current-control architecture to guarantee the current limits, based on measuring voltage on the low side shunt current resistors R_{13} and R_{31}. The voltage drop on R_{13} and R_{31}, which occurs between CSP and CSN, is utilized to perform the current limit operation.

While operating in Buck or Buck-Boost switching cycles, the SQ25001 uses valley current limit control. The valley current limit threshold can be configured using the external resistor R_{ILMT_BUCK} connected from the ILMT_BUCK pin to GND. If a valley overcurrent is detected once, the threshold will fold back to 95% of the set value. The controller will stop switching and pull FAULT1 and FAULT2 low when a valley overcurrent is continuously detected for a period longer than the 200μs filter time. Then, it will start an auto-retry procedure, which is repeated up to 32 times or until the fault disappears. To improve system stability, when the voltage on the ILMT_BUCK pin is higher than 3.2V (i.e., the ILMT_BUCK pin is open) or lower than 0.1V (i.e., the ILMT_BUCK pin is shorted), the controller will stop switching and pull FAULT1 and FAULT2 low after a 3μs filter time, without retry.

While operating in Boost or Buck-Boost switching cycles, the SQ25001 uses peak current limit control. The peak current limit threshold can be configured using the external resistor R_{ILMT_BOOST} connected from the ILMT_BOOST pin to GND. The controller will stop switching and pull FAULT1 and FAULT2 low when a peak overcurrent is continuously detected for a period longer than 200μs filter time. Then, it will start an auto-retry procedure, which is repeated up to 32 times or until the

fault disappears. To improve system stability, when the voltage on the ILMT_BOOST pin is higher than 3.2V (i.e., the ILMT_BOOST pin is open) or lower than 0.1V (i.e., the ILMT_BOOST pin is shorted), the controller will stop switching and pull FAULT1 and FAULT2 low after a 3μs filter time, without retry.

To adapt the application scenarios at different power levels, both the valley and peak current limit thresholds can be halved by configuring the resistor R_{ILMT_RED} connected from the ILMT_RED pin to GND. To improve system stability, when the voltage on the ILMT_RED pin is higher than 3.2V (i.e., the ILMT_RED pin is open) or lower than 0.1V (i.e., the ILMT_RED pin is shorted), the controller will stop switching and pull FAULT1 and FAULT2 low after a 3μs filter time, without retry.

A second-level current limit is implemented to provide immediate protection against a large current flowing instantaneously through R_{13} and R_{31}. When the voltage between CSP and CSN exceeds the 0.2V threshold, the controller will stop switching and immediately pull FAULT1/FAULT2 low, without retry. The controller can be reactivated by pulling the EN pin from high to low and then back to high.

Table 1. Fault Protection Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Valley Current Limit Threshold	$V_{VY\_H\_TH1}$	R_{ILMT_BUCK} = 68kΩ	33	40	47	mV
	$V_{VY\_H\_TH2}$	R_{ILMT_BUCK} = 51kΩ	48	55	62	
	$V_{VY\_H\_TH3}$	R_{ILMT_BUCK} = 39kΩ	60	67	74	
	$V_{VY\_H\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	73	80	87	
Valley Current Limit Reduced Threshold	$V_{VY\_L\_TH1}$	R_{ILMT_BUCK} = 68kΩ	14	20	26	
	$V_{VY\_L\_TH2}$	R_{ILMT_BUCK} = 51kΩ	21.5	27.5	33.5	
	$V_{VY\_L\_TH3}$	R_{ILMT_BUCK} = 39kΩ	29	35	41	
	$V_{VY\_L\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	36.5	42.5	48.5	
ILMT_BUCK Pin Bias Current	I_{ILMT_BUCK}		28.2	30	31.8	μA
ILMT_BUCK Pin Voltage Range	Open	Safe state (latch off)	3.2			V
	V_{BUK_RG1}	V_{VY_TH1} current limit	1.83	2.04	2.26	
	V_{BUK_RG2}	V_{VY_TH2} current limit	1.38	1.53	1.69	
	V_{BUK_RG3}	V_{VY_TH3} current limit	1.07	1.17	1.28	
	V_{BUK_RG4}	V_{VY_TH4} current limit	0.25	0.6	0.98	
	Short to GND	Safe state (latch off)			0.1	
Peak Current Limit Threshold	$V_{PK\_H\_TH1}$	R_{ILMT_BOOST} = 68kΩ	58	65	72	mV
	$V_{PK\_H\_TH2}$	R_{ILMT_BOOST} = 51kΩ	73	80	87	
	$V_{PK\_H\_TH3}$	R_{ILMT_BOOST} = 39kΩ	88	95	102	
	$V_{PK\_H\_TH4}$	R_{ILMT_BOOST} = 30kΩ/20kΩ/10kΩ	103	110	117	
Peak Current Limit Reduced Threshold	$V_{PK\_L\_TH1}$	R_{ILMT_BOOST} = 68kΩ	26.5	32.5	38.5	
	$V_{PK\_L\_TH2}$	R_{ILMT_BOOST} = 51kΩ	34	40	46	
	$V_{PK\_L\_TH3}$	R_{ILMT_BOOST} = 39kΩ	41.5	47.5	53.5	
	$V_{PK\_L\_TH4}$	R_{ILMT_BOOST} = 30kΩ/20kΩ/10kΩ	49	55	61	
ILMT_BOOST Pin Bias Current	I_{ILMT_BOOST}		28.2	30	31.8	μA
ILMT_BOOST Pin Voltage Range	Open	Safe state (latch off)	3.2			V
	V_{BST_RG1}	V_{PK_TH1} current limit	1.83	2.04	2.26	
	V_{BST_RG2}	V_{PK_TH2} current limit	1.38	1.53	1.69	
	V_{BST_RG3}	V_{PK_TH3} current limit	1.07	1.17	1.28	
	V_{BST_RG4}	V_{PK_TH4} current limit	0.25	0.6	0.98	
	Short to GND	Safe state (latch off)			0.1	
ILMT_RED Pin Bias Current	I_{ILMT_RED}		28.2	30	31.8	μA

ILMT_RED Pin Voltage	Open	Safe state (latch off)	3.2			V
	V_{RED_TH1}	R_{ILMT_RED} = 51kΩ/39kΩ, normal threshold	1.07		1.69	
	V_{RED_TH2}	R_{ILMT_RED} = 30kΩ/20kΩ, valley/peak current limit thresholds reduced	0.44		0.98	
	V_{RED_TH3}	R_{ILMT_RED} = 10kΩ, valley/peak, output current limit thresholds reduced	0.25		0.36	
	Short to GND	Safe state (latch off)			0.1	

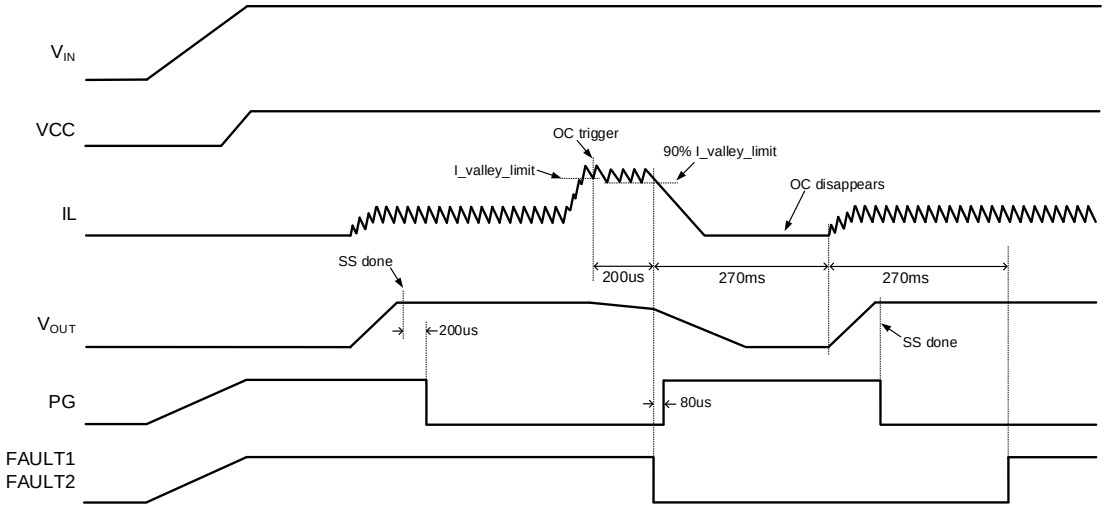


Figure 11. Valley Current Limit (Retry Once)

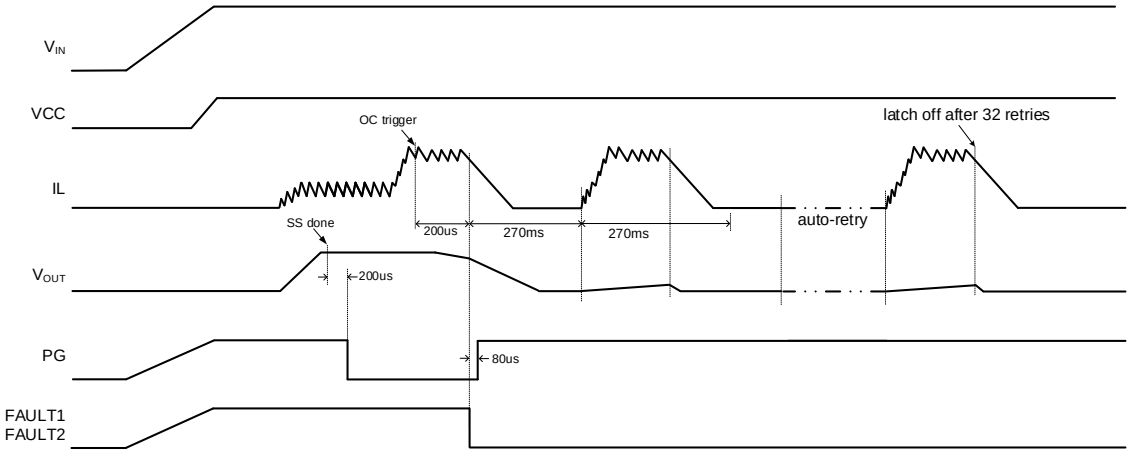


Figure 12. Valley Current Limit (Keep OC)

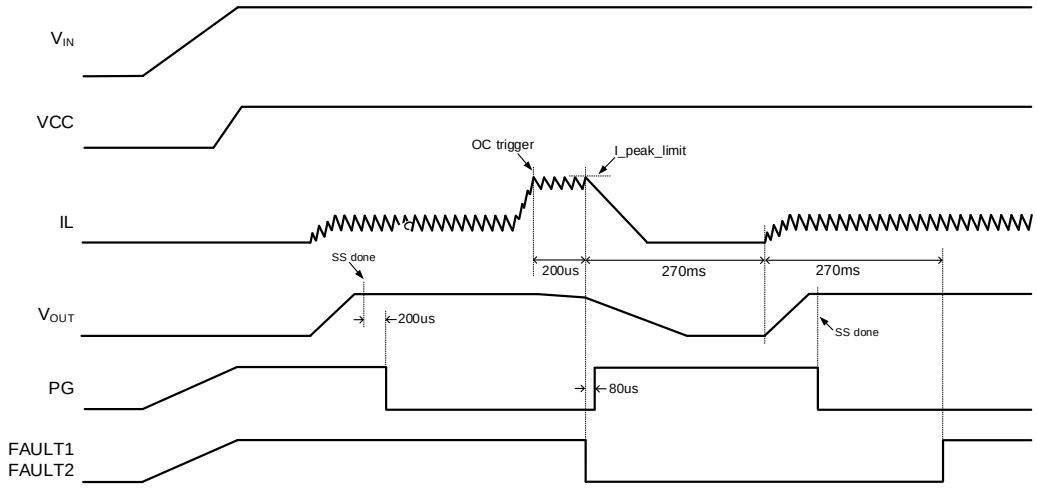


Figure 13. Peak Current Limit (Retry Once)

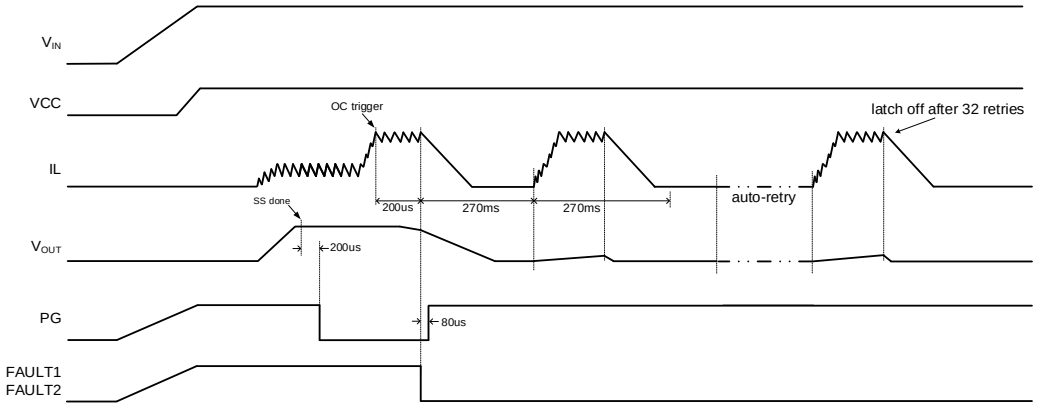


Figure 14. Peak Current Limit (Keep OC)

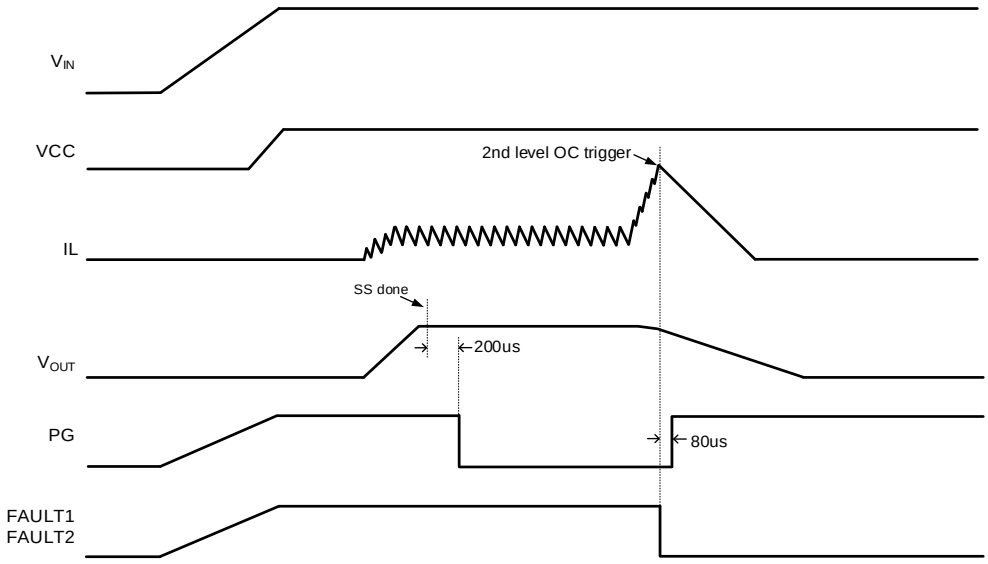


Figure 15. Second Level Current Limit

Output Overcurrent

To limit the output power of the system, the ISP and ISN pins are used to monitor the average current delivered to the load through a series resistor connected at the converter output. The output overcurrent threshold can also be configured using the external resistor R_{ILMT_BUCK} connected from the ILMT_BUCK pin to GND. If the output overcurrent is continuously detected for a duration longer than 80μs filter time, the controller will stop switching and pull both FAULT1 and FAULT2 low. Then, it will start an auto-retry procedure, which is repeated up to 32 times or until the fault disappears. The output overcurrent detection threshold can be halved by configuring the resistor R_{ILMT_RED} connected from the ILMT_RED pin to GND.

Table 2. Current Limit Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Average Current Limit Threshold	$V_{OC\_H\_TH1}$	R_{ILMT_BUCK} = 68kΩ	18	25	32	mV
	$V_{OC\_H\_TH2}$	R_{ILMT_BUCK} = 51kΩ	33	40	47	
	$V_{OC\_H\_TH3}$	R_{ILMT_BUCK} = 39kΩ	48	55	62	
	$V_{OC\_H\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	63	70	77	
Output Average Current Limit Reduced Threshold	$V_{OC\_L\_TH1}$	R_{ILMT_BUCK} = 68kΩ	6.5	12.5	18.5	
	$V_{OC\_L\_TH2}$	R_{ILMT_BUCK} = 51kΩ	14	20	26	
	$V_{OC\_L\_TH3}$	R_{ILMT_BUCK} = 39kΩ	21.5	27.5	33.5	
	$V_{OC\_L\_TH4}$	R_{ILMT_BUCK} = 30kΩ/20kΩ/10kΩ	29	35	41	

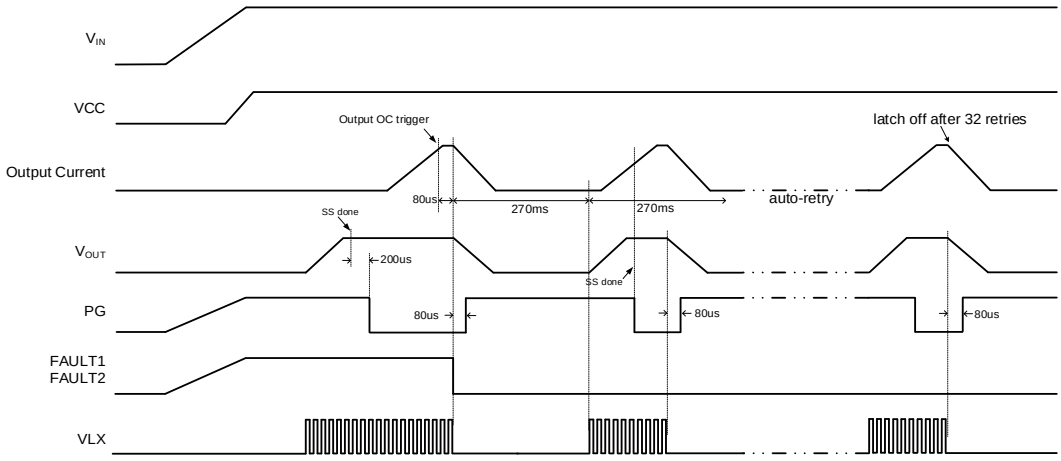


Figure 16. Output Overcurrent (Keep OC)

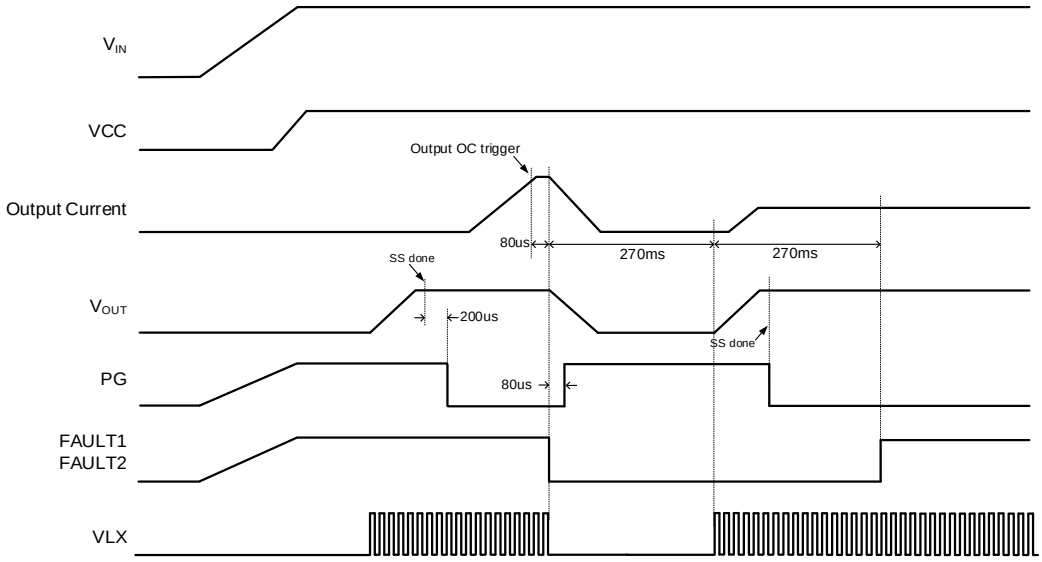


Figure 17. Output Overcurrent (Retry Once)

Output Voltage Regulation and Monitoring

The output voltage can be configured from 4.5V to 30V by connecting the FB pin to divider resistors between V_{OUT} and GND. The controller regulates the FB pin voltage to equal the internal reference voltage (0.8V), thereby generating the desired output voltage. Consequently, the controller can use the FB pin to monitor undervoltage and overvoltage of the output voltage.

- **Undervoltage (UV):** If FB voltage is continuously lower than the undervoltage threshold 0.4V for a duration longer than the 80µs filter time, the controller will pull FAULT1 and FAULT2 low and enter a fault mode that depends on UV_SS_MODE pin (three different protection modes: hiccup, latch off, or continue running).
- **Overvoltage (OV):** If FB voltage is continuously higher than the overvoltage threshold 0.96V for a duration longer than the 5µs filter time, the controller will stop switching and pull FAULT1 and FAULT2 low, without retry.
- **Power Good (PG)**: The PG pin is used to indicate the output voltage status. The PG pin switches from high level to low level when FB voltage is continuously higher than the 0.72V rising threshold and lower than the 0.88V falling threshold for a duration longer than the 80µs filter time. It switches from low level to high level when FB is continuously higher than the 0.92V rising threshold and lower than the 0.68V falling threshold for a duration longer than the 80µs filter time.

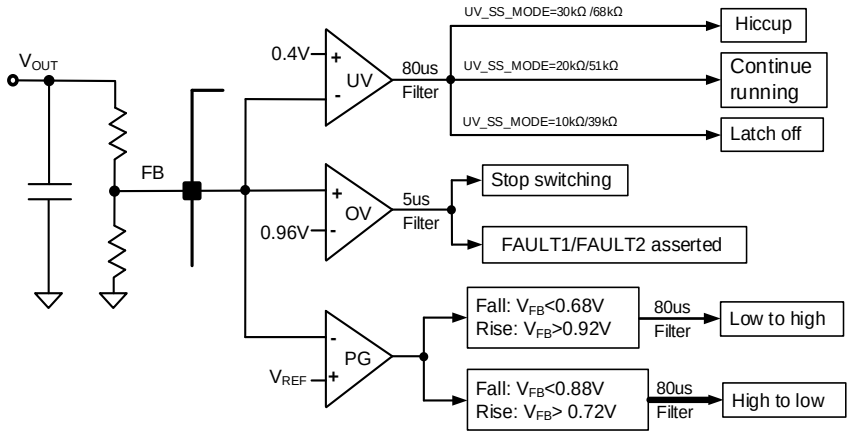


Figure 18. Output Voltage Regulation and Monitoring

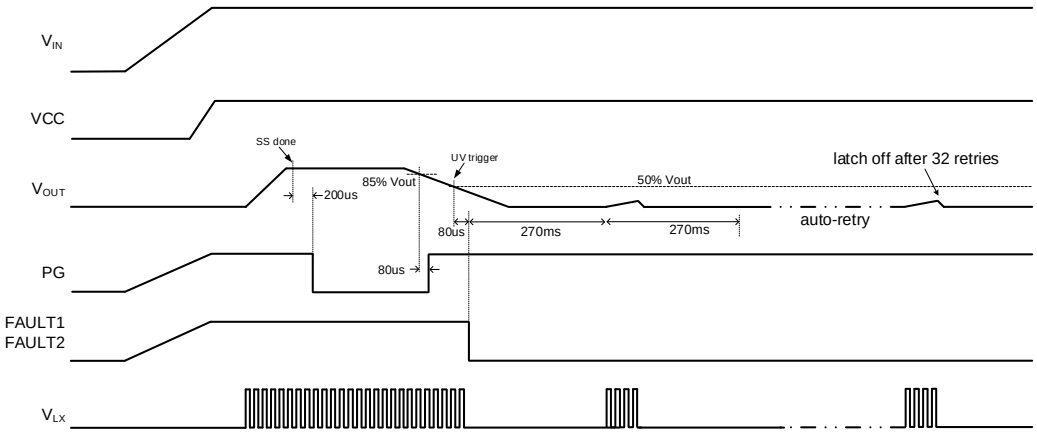


Figure 19. Output Undervoltage (Hiccup)

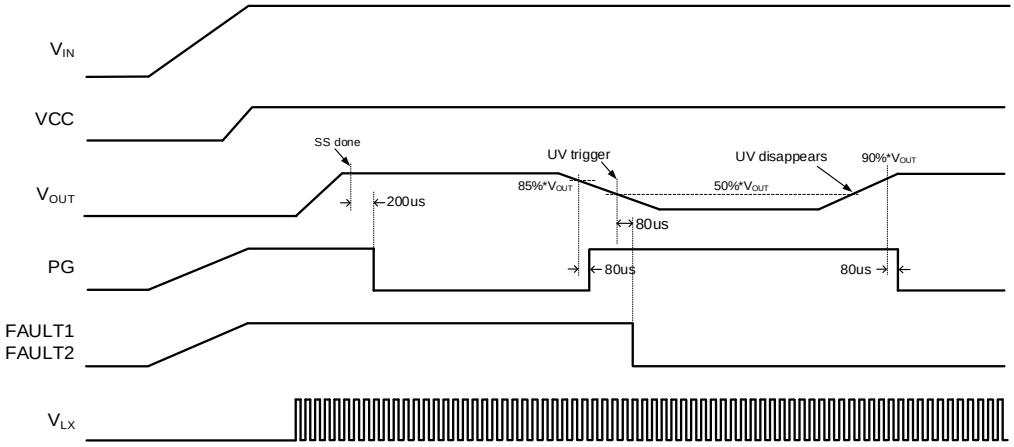


Figure 20. Output Undervoltage (Continue Running)

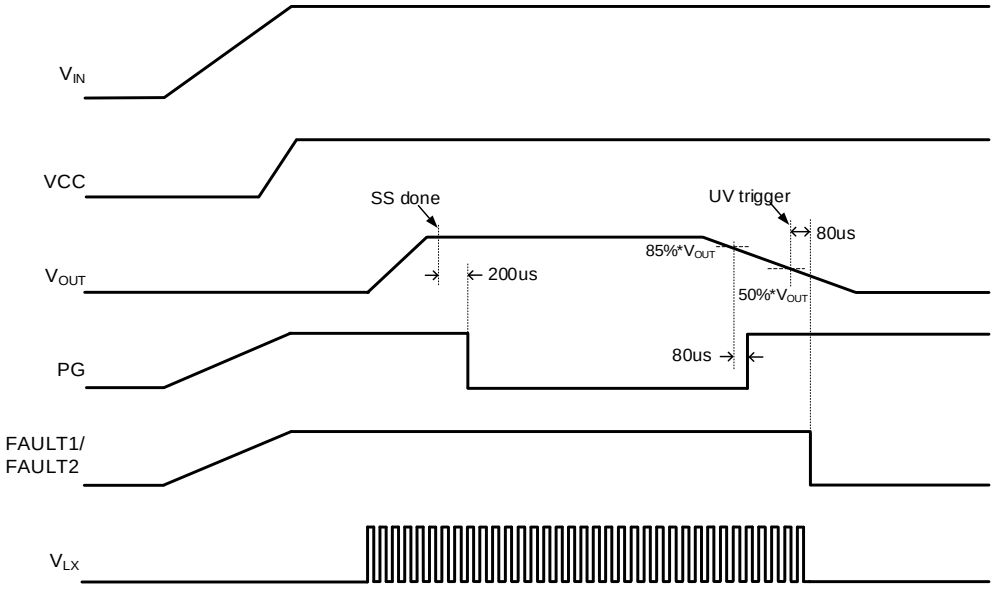


Figure 21. Output Undervoltage (Latch Off)

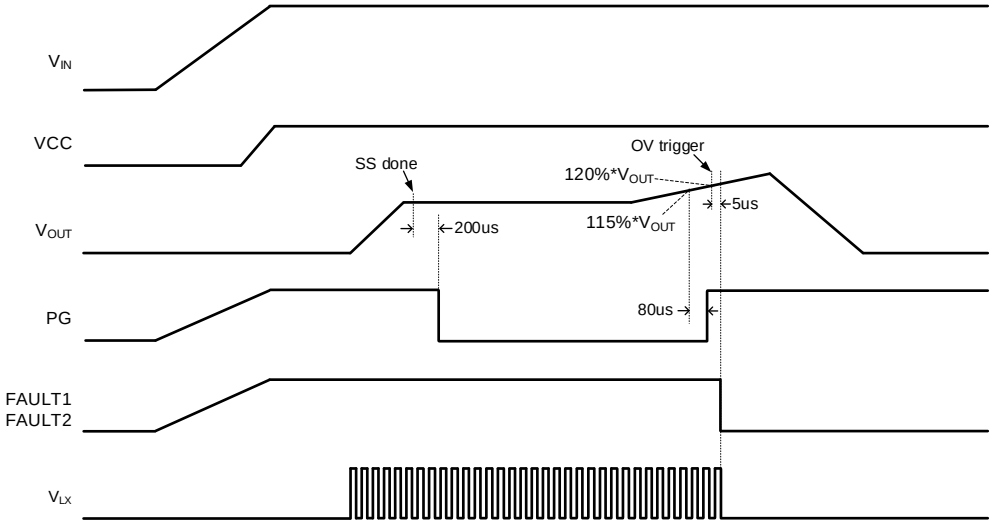


Figure 22. Output Overvoltage

Output Voltage Monitoring Redundancy

The FB_MON pin serves as a redundant pin to the FB pin, enhancing the reliability of the controller by providing the same threshold and protection behavior. The FB_MON pin is solely used to monitor the output voltage for undervoltage (UV) and overvoltage (OV) events, without participating in the closed-loop regulation. In the event of a fault occurring on FB_MON pin, the controller will take corresponding actions, as shown in Figure 29.

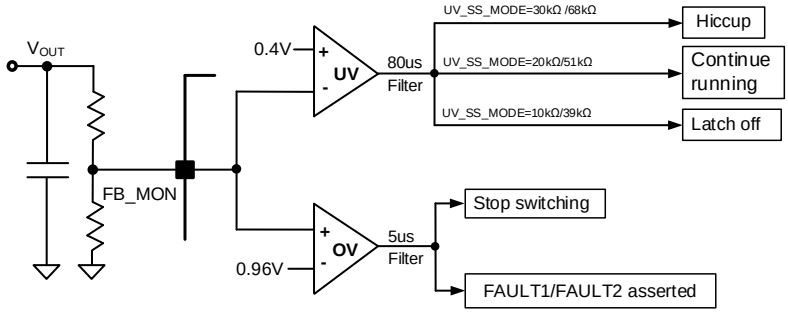


Figure 23. Output Voltage Monitoring Redundancy

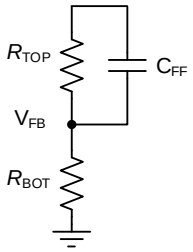
Application Information

Feedback Resistor Divider R_{TOP} and R_{BOT}

Choose R_{TOP} and R_{BOT} to program the proper output voltage. Choose larger resistor values for both R_{TOP} and R_{BOT} to minimize the power consumption under light loads. Choose lower resistor values for a more robust design and to suppress high frequency noise. A value between 10kΩ and 120kΩ is recommended for both resistors.

If V_{OUT} = 12V and R_{TOP} is chosen to be 105kΩ, R_{BOT} can be calculated as 7.5kΩ using the following equation:

$$R_{BOT} = \frac{0.8V}{V_{OUT} - 0.8V} \times R_{TOP}$$



Operating Frequency Resistor

Connect the FS pin to GND with a resistor to configure the switching frequency. In most cases, 246kHz is the recommended operating frequency. If the switching frequency (f_{SW}) is 246kHz, the value of R_{FS} can be calculated as 51kΩ using the following equation:

$$R_{FS}(\text{k}\Omega) = \frac{5900}{f_{SW}(\text{kHz}) - 130(\text{kHz})}$$

Input Capacitor Selection

Input filter capacitors are necessary to reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and minimize electromagnetic interference (EMI). When selecting an input capacitor, choose a voltage rating that is at least 20% greater than the maximum voltage of the input supply and a temperature rating that exceeds the system requirements. X7R series ceramic capacitors are often preferred due to their compact size, low cost, surge current capability, and high RMS current ratings across a wide temperature and voltage range. Systems powered by wall adapters or other long, inductive wires may be susceptible to significant inductive ringing at the device input. In these cases, consider adding bulk capacitance, such as electrolytic, tantalum, or polymer type capacitors, to mitigate this issue. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet RMS current requirements) can be particularly effective in these cases.

In the boost region, the converter's input current is continuous, whereas in the buck region, it is discontinuous. The discontinuity of the input current results in a higher RMS current. Therefore, it is essential to consider the RMS current rating of the input capacitor and, if necessary, to parallel additional capacitors to meet the calculated RMS ripple current requirement.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low equivalent series resistance (ESR) and equivalent series inductance (ESL) of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at V_{IN} = 2V_{OUT}, then

$$V_{CIN\_RIPPLECAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

Inductor Selection

The inductor is necessary to supply a constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value helps reduce size and cost, and enhances transient response, but it increases the peak inductor ripple current, thereby reducing efficiency and increasing output voltage ripple. However, the low DC resistance (DCR) of these low value inductors can help reduce DC losses and increase efficiency. In contrast, higher inductor values tend to have higher DCR and slower transient response.

A reasonable compromise between size, efficiency, and transient response can be achieved by selecting a ripple current (ΔIL) approximately 20% to 50% of the desired full output load current. The inductor for the buck mode is calculated using the equation:

$$L_{BUCK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Utilize this inductance value to determine the actual inductor ripple current (ΔI_L) and the required peak current inductor current ($I_{L,PEAK,BUCK}$) according to the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_{BUCK}}$$

$$I_{L,\,PEAK,\,BUCK} = I_{OUT,\,MAX} + \frac{\Delta I_L}{2}$$

In Boost mode, select a ripple current (ΔIL) approximately 20%–50% of the input current.

$$I_{IN,\,MAX} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,\,MIN} \times \eta}$$

where η is the efficiency.

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L}$$

Utilize this inductance value to determine the actual inductor ripple current (ΔI_L) and the required peak current inductor current ($I_{L,PEAK,BOOST}$) according to the following equations:

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times L_{BOOST}}$$

$$I_{L,\,PEAK,\,BOOST} = I_{IN,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current in excess of both $I_{L,PEAK,BUCK}$, and $I_{L,PEAK,BOOST}$.
The recommended minimum inductance is either L_{BUCK} or L_{BOOST}, whichever is higher.

Output Capacitor C_{OUT} Selection

Select the output capacitor (C_{OUT}) to handle the output ripple requirements, considering both steady-state ripple and transient requirements. When selecting this capacitor, Ceramic and Polymer Hybrid types are often preferred due to their low equivalent series resistance (ESR) and higher capacitance. To reduce the influence of AC ripple on the output current sampling resistor (R_{S_H}), it is necessary to avoid placing the majority of the output capacitors at the end of the resistor R_{S_H}.

The output capacitor ripple current is high in boost mode. The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors' equivalent series resistance (ESR ripple) as well as the stored charge (capacitive ripple). To accurately estimate the total ripple, both of these factors should be considered.

$$V_{RIPPLE,\,ESR} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} \times ESR$$

$$V_{RIPPLE,\,CAP} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{V_{OUT} \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple may be higher than the calculated value, as the effective capacitance of ceramic capacitors decreases with the voltage across their terminals. The voltage derating, typically provided as a chart in the capacitor datasheet, should be considered to recalculate the ripple after taking the target output voltage into account.

Programming Peak/Valley Current Limit

The sense resistor R_{S_L}, located between the CSP and CSN pins, provides the valley current limit in Buck mode and peak current limit in Boost mode on a cycle-by-cycle basis. It is recommended to consider a margin of 30% for headroom to accommodate load transients, etc.

In Buck mode, the current limit resistor is given by:

$$R_{CS,\,BUCK} = \frac{V_{VY\_H\_THx}}{I_{L,\,PEAK,\,BUCK} \times 1.3}$$

where $V_{VY\_H\_THx}$ represents the valley current limit minimum threshold.

In Boost mode, the current limit resistor is defined as:

$$R_{CS,\,BOOST} = \frac{V_{PK\_H\_THx}}{I_{L,\,PEAK,\,BOOST} \times 1.3}$$

where $V_{PK\_H\_THx}$ is the peak current limit threshold.

The final R_{S_L} value should be lower than the calculated values in both the R_{CS_BUCK} and R_{CS_BOOST} configurations. To attenuate noise in the CSP and CSN input lines, place a pair of resistors with values between 50Ω and 100Ω. Additionally, consider using resistors with higher precision and lower parasitic inductance.

Programming Output Current Limit

The sense resistor R_{S_H}, located between the ISP and ISN pins, provides output average current limit protection. Once the sensed signal exceeds the current limit reference voltage and remains above it for a continuous period of 135μs filter time, the controller stops switching and pulls FAULT1 and FAULT2 pins low. The current limit resistor is given by:

$$R_{SEN,\,O} = \frac{V_{IS\_THDx}}{I_{OUT} \times 1.2}$$

where V_{IS_THDx} is output average current limit threshold. A margin of 1.2 × output current is recommended.

Programming Soft-Start Time

The soft-start time is programmed by a capacitor connected between the SS (soft-start) and GND pins. The internal charge current is typically 10μA. The soft-start capacitor can be calculated by:

$$C_{SS} = \frac{t_{ss} \times 10}{0.8}$$

where t_{SS} is the desired soft-start time in milliseconds (ms) and C_{SS} is the soft-start capacitor using units of

nanofarads (nF). Typically, C_{SS} is 100nF, which results in an approximate soft-start time of 8ms.

External MOSFETs Selection

This buck-boost controller requires four external N-channel power MOSFETs.

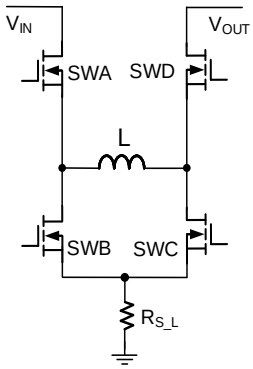


Figure 24. External MOSFET Selection

In Buck mode, the input-side switches SWA and SWB must withstand the maximum input voltage. Therefore, the breakdown voltage (V_{BR}) of the MOSFETs, SWA, and SWB should be higher than 1.5 to 2 times the maximum input voltage. Meanwhile, SWC is always in the off state, and SWD is always in the on state.

When in boost mode, the output-side switches SWD and SWC must withstand the maximum output voltage. Therefore, the breakdown voltage (V_{BR}) of the MOSFETs SWD and SWC should be higher than 1.5 to 2 times the maximum output voltage. The SWA switch is always on, while the SWB switch is always off.

SWA power loss includes two parts: switching loss and conduction loss. The approximate loss can be calculated as follows:

$$P_{CON\_SWA\_BOOST} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \times R_{DS\_ON\_SWA}$$

$$P_{CON\_SWA\_BUCK} = \frac{V_{OUT}}{V_{IN}} \times {I_{OUT}}^2 \times R_{DS\_ON\_SWA}$$

$$P_{SW\_SWA\_BUCK} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{sw}$$

The rise (t_R) and fall (t_F) times are obtained from the MOSFET datasheet. R_{DS_ON} can be selected according to the allowed temperature rise of the SWA.

SWB conduction loss in Buck mode as the synchronous rectifier can be calculated as follows:

$$P_{CON\_SWB\_BUCK} = \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times {I_{OUT}}^2 \times R_{DS\_ON\_SWB}$$

SWC power loss includes two parts: switching loss and conduction loss. The conduction loss in Boost mode can be calculated as follows:

$$P_{CON\_SWC\_BOOST} = \left(1 - \frac{V_{IN}}{V_{OUT}} \right) \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \times R_{DS\_ON\_SWC}$$

SWC switching loss in Boost mode can be calculated as follows:

$$P_{SW\_SWC\_BOOST} = \frac{1}{2} \times V_{OUT} \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \right) \times (t_r + t_f) \times f_{sw}$$

SWD power loss in Boost and Buck mode can be calculated as follows:

$$P_{CON\_SWD\_BOOST} = \left(\frac{V_{IN}}{V_{OUT}} \right) \times \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \right)^2 \times R_{DS\_ON\_SWD}$$

$$P_{CON\_SWD\_BUCK} = {I_{OUT}}^2 \times R_{DS\_ON\_SWD}$$

The total MOSFET gate charge (Q_g) should be within the following range to prevent triggering the VCC current limit:

$$Q_g < \frac{I_{VCC\_ILMT}}{f_{SW}}$$

where I_{VCC_ILMT} is VCC current limit 100mA.

External Bootstrap Capacitor

The SQ25001 integrates a floating power supply for the gate drivers, which operates the high side power switches. Connect a ceramic capacitor between BS1 and LX1, and between BS2 and LX2. The bootstrap capacitors need to store approximately 100 times the high side gate charge. In most applications, proper operation requires 100nF to 470nF low ESR ceramic capacitors.

Loop Compensation

The SQ25001 incorporates peak current mode control in the boost stage and valley current mode control in the buck stage. A compensation network on the COMP pin is necessary to achieve a balance between the stability and speed of the control loop. In most applications, the network shown in Figure 34 is used.

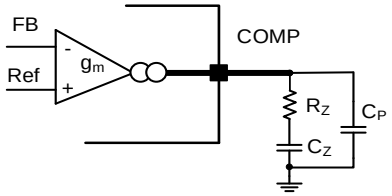


Figure 25. Loop Compensation Network

Select the crossover frequency (f_C) of the closed-loop system. The boost compensation loop is more restrictive

due to the existence of a right half-plane zero (RHPZ) in Boost mode. Choose a crossover frequency that is 1/5 of the right half-plane zero (f_{RHPZ}) and 1/10 of the switching frequency, as this tradeoff ensures both stability and transient response of the system. Note that the system exhibits a faster response at higher crossover frequencies.

For Boost mode:

$$f_{RHPZ} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}}$$

Calculate the compensation resistor Rz value of the R-C series combination connected to the COMP pin:

$$R_Z = \frac{V_{OUT}}{V_{REF}} \times \frac{A_{CS} \times R_{CS} \times C_{OUT}}{1 - D_{MAX}} \times \frac{2\pi \times f_C}{gm}$$

where A_{CS} is the current sense amplifier gain, which is typically 19. The error amplifier transconductance (g_m) is 700μS in boost mode.

The compensation zero determines the phase margin at the crossover frequency. The capacitor C_Z, along with R_Z, provides zero compensation. It is recommended to place the compensation zero f_Z between the crossover frequency f_C and the dominant pole f_P:

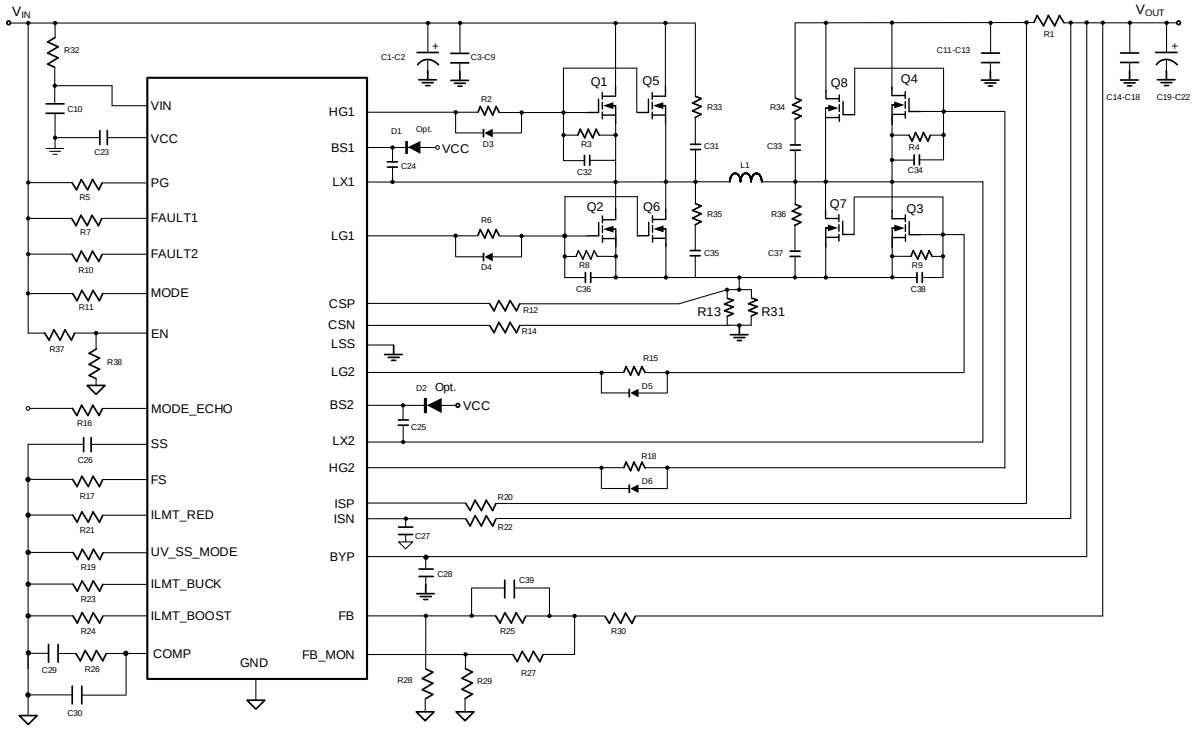
$$f_P = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

$$C_Z = \frac{1}{2\pi \times f_Z \times R_Z}$$

A high frequency pole is recommended to attenuate high frequency noise. It is advisable to position this pole to cancel the ESR zero of C_{OUT} if the output capacitor has a large capacitance or a high equivalent series resistance (ESR) value:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_Z}$$

Application Schematic (V_{OUT} = 12V, f_{SW} = 246kHz)



BOM List

Reference Designator	Description	Part Number	manufacturer
C1–C2	E-cap 100μF, 63V	EEHZU1J101P	Panasonic
C3–C7	Cap 4.7μF, 100V,1210	CNA6P1X7R2A475K250AE	TDK
C8, C9, C10	Cap 1μF, 100V, 0805	CGA4J2X7R2A104K125AE	TDK
C11–C18	Cap 22μF, 25V, 1210	CGA6P3X7R1E226M250AE	TDK
C19–C22	E-cap 150μF, 25V	EEHZC1E151P	Panasonic
C23	Cap 4.7μF, 25V, 0603	CGA4J1X7R1E475K125AE	TDK
C24, C25	Cap 0.22μF, 50V, 0603	CGA3E3X7R1H224K080AE	TDK
C26	Cap 0.1μF, 50V, 0603	CGA3E2X7R1H104K080AE	TDK
C28	Cap 1μF, 50V, 0805	CGA4J3X7R1H105K125AE	TDK
C29	Cap 22nF, 50V, 0603	CEU3E2X7R1H223K080AE	TDK
C30	Cap 220pF, 50V, 0603	CGA3E2C0G1H221J080AD	TDK
C27, C31, C32, C33, C34, C35, C36, C37, C38, C39	NC		
R1	Res 1mΩ, 2512	PA2512FKF7W0R001E	YAGEO
R2, R6, R15, R18	Res 1Ω, 0603		YAGEO
R3, R4, R5, R7, R8, R9, R10, R11, R37	Res 100kΩ, 0603		YAGEO
R12,R14	Res 51Ω, 0603		YAGEO
R13, R31	Res 2mΩ, 2512	PA2512FKF7W0R002E	YAGEO
R16, R20, R22, R30, R32	Res 0Ω, 0603		YAGEO
R17, R21, R23	Res 51kΩ, 0603		YAGEO
R19	Res 10kΩ, 0603		YAGEO
R24	Res 68kΩ, 0603		YAGEO
R25, R27	Res 105kΩ, 0603		YAGEO
R26	Res 15kΩ, 0603		YAGEO
R28, R29	Res 7.5kΩ, 0603		YAGEO
R33, R34, R35, R36, R38	NC		
D1, D2, D3, D4, D5, D6	NC		
L1	Inductor 3.3μH	SPM12565VT-3R3M-D	TDK
Q1, Q2, Q5, Q6	MOSFET	IAUC120N06S5L032	Infineon
Q3, Q4, Q7, Q8	MOSFET	IAUC100N04S6L025	Infineon

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Input Capacitors:** Place the input capacitor close to the VIN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the VIN and GND pins using wide copper connections. A 0.1μF input ceramic capacitor is recommended to reduce the high frequency noise. Minimize the loop formed by the power input capacitors, MOSFET Q1 , MOSFET Q2, and sampling resistor R_{S_L} to reduce the noise of LX1.
- **Output Capacitors:** Ensure that the C_{OUT} negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage. Minimize the loop formed by the output capacitors, MOSFET Q3 , MOSFET Q4, and sampling resistor R_{S_H} to reduce the noise of LX2.
- **VCC Capacitor:** Place the VCC capacitor close to the VCC pin using a short, direct copper trace to the nearest ground. Minimize the loop formed by the VCC capacitor and ground.
- **Feedback Network:** Place the feedback components as close to the FB pin as possible. Avoid routing the feedback line near LX, BS, or other high frequency signals, as it is noise sensitive. Use a Kelvin connection for the feedback sampling point at C_{OUT} rather than the inductor output terminal.
- **BS Capacitor:** Place the BS capacitor on the same layer as the device and keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.
- **Control Signals:** It is not recommended to connect control signals to VIN or another voltage source directly. A resistor in the range of 1kΩ to 1MΩ should be used if they are pulled high.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device to improve thermal performance. Connect the exposed pad to a larger copper area than its size, and place an adequate number of vias on it for heat dissipation.
- **LSS Pin:** Use a short, direct copper trace to connect the LSS pin to the nearest ground for better driving noise suppression.
- **PCB Board:** A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. Provide large copper areas for VIN and GND on the top land bottom layers and maximize their size. The Middle1 layer should be used as a GND layer for conducting heat and shielding the Middle2 layer signal lines from top layer crosstalk. Place signal lines on the Middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

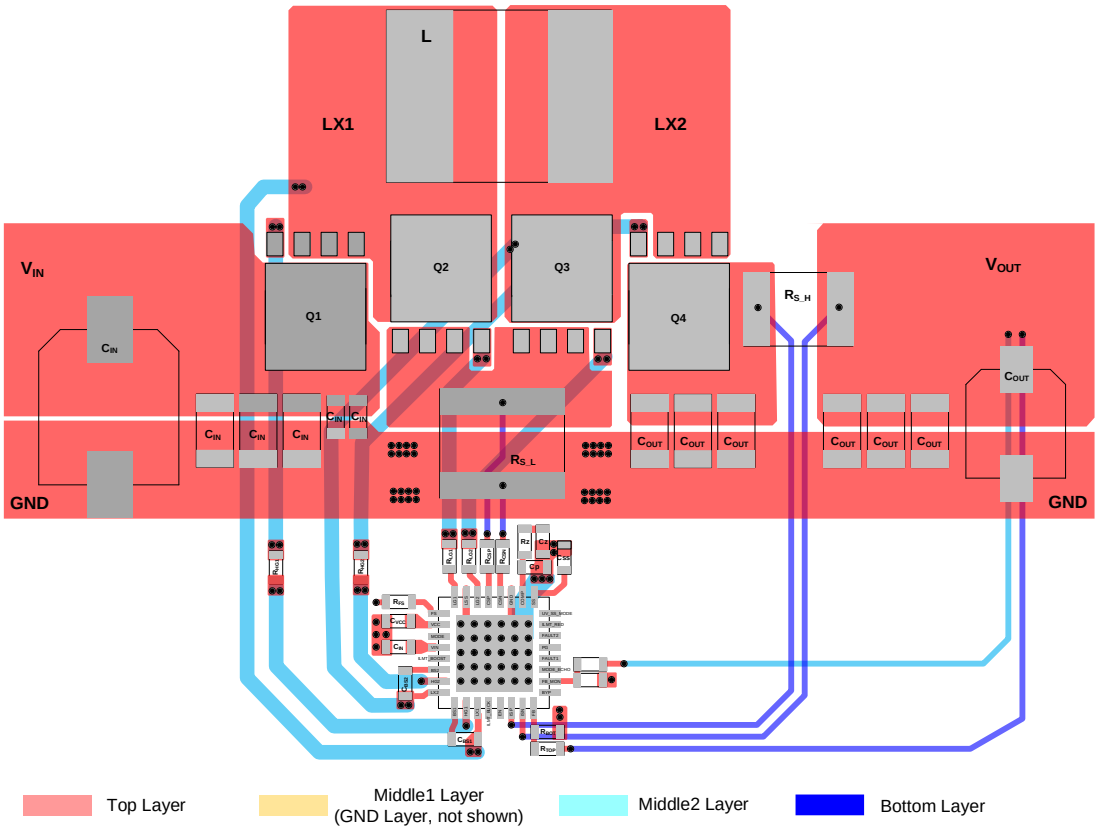
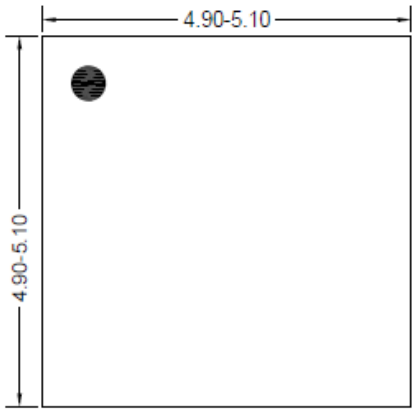
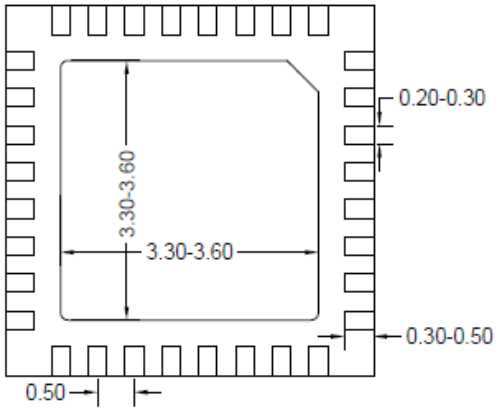


Figure 26. Suggested PCB Layout

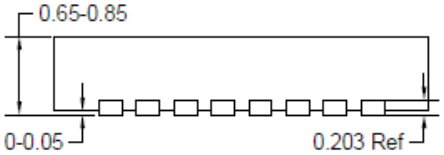
QFN5.0×5.0-32 Package Outline Drawing



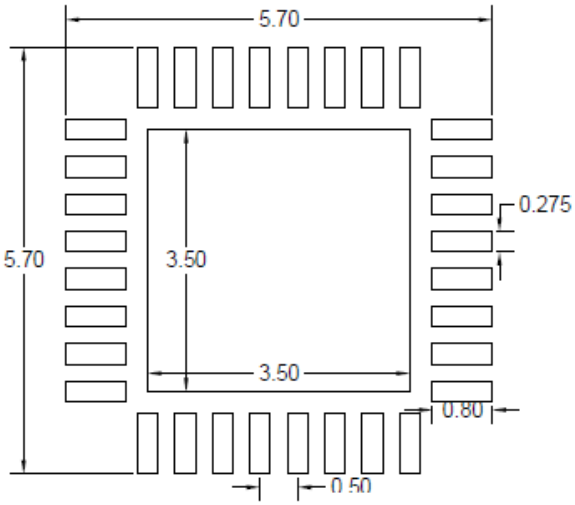
Top view



Bottom view



Side view

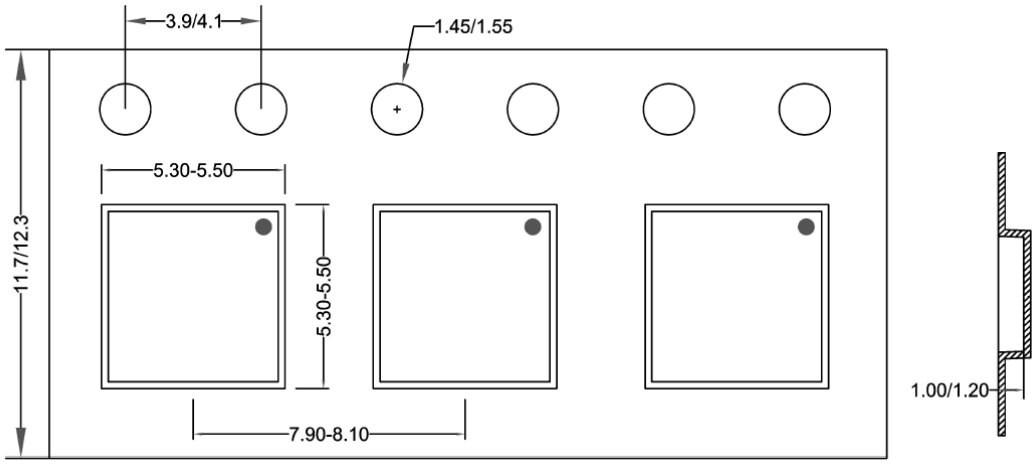


Recommended Pad Layout
(Reference Only)

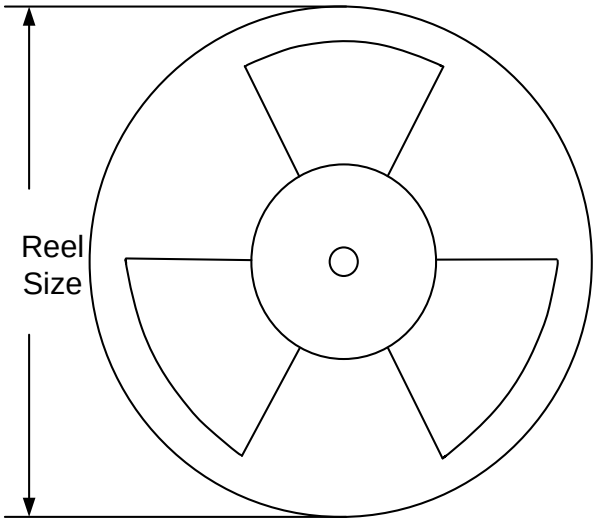
Notes: *All dimension in millimeter and exclude mold flash & metal burr.*

Tape and Reel Specification

QFN5x5-32 Tape Orientation



Reel Dimensions



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
QFN5x5-32	12	8	13"	400	400	5000

Note: *All dimensions are nominal.*

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
May.06, 2025	Revision 1.0	Initial Release	-

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