SA21904A

65V Hot swap and ORing Controller with ASIL D

General Description

The SA21904A is a high-voltage automotive controller that integrates hot swap and ORing functions internally.

The device can driver two back-to-back MOSFETs for bidirectional current control, ideal for systems with load-side energy reservoirs that must not drain back to a failed supply BUS.

The device includes programmable features such as current limit threshold and fault time during start up, overcurrent threshold, input overvoltage and undervoltage thresholds, requiring minimal external components. It offers ENOUT and FLT_N indications for downstream load control.

The SA21904A provides a range of features to support applications that need to meet functional safety requirements in accordance with Automotive Safety Integrity Level ASIL D.

Features

- AEC-Q100 Grade 1 Qualified for Automotive Applications
- Wide Input Voltage Range: 4V to 65V
- Reverse Input Protection: -65V
- 2 External N-Channel MOSFET Predrivers
  - One Hot Swap Feature
  - One ORing Feature
- Very Low Supply Current: 2.2mA@Operation, 50μA@WAKE Low
- Current Limiting for Startup
- Programmable Current Limit Fault Timer
- Integrated Charge Pump
- Input Overvoltage Protection
- Input Undervoltage Protection
- Output Overcurrent Protection
- Complies with the 16750 AC Ripple Test Requirements (50Hz-25kHz)
- Developed According to ISO26262 to Be Used in ASIL D Application

Applications

- Advanced Driving Assistance System
- Automotive Power Distribution Applications

Typical Application

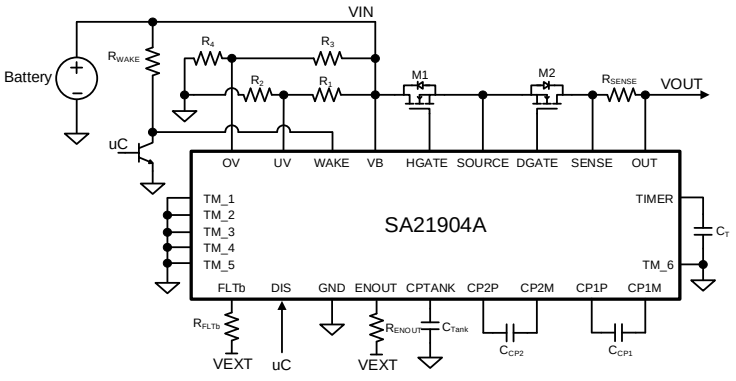


Figure1 Single Channel Typical Application

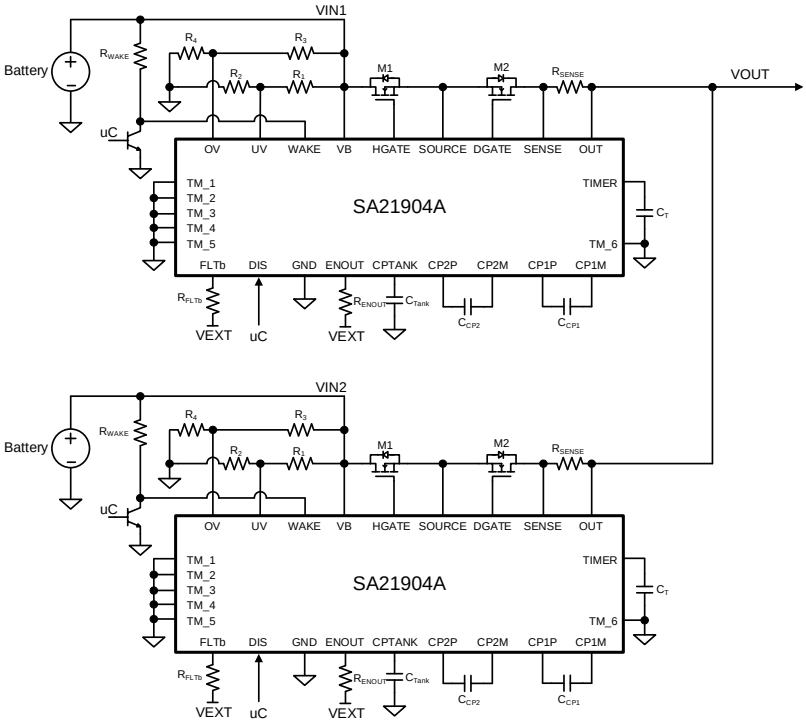


Figure 2. Dual Channel Typical Application

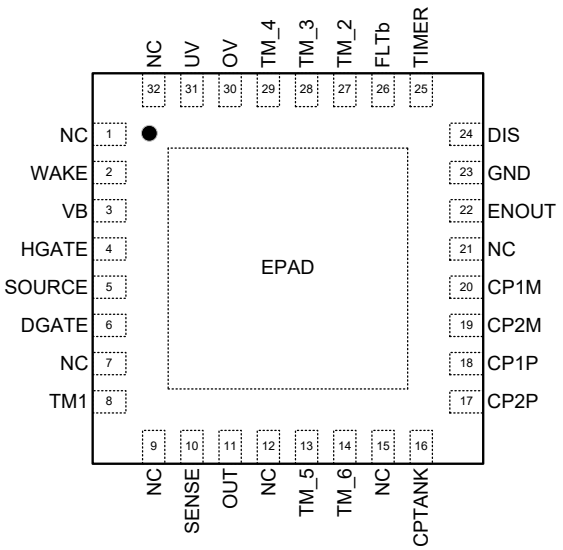
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA21904AQEQ	QFN5×5-32 RoHS Compliant and Halogen Free	**AAHR*xyz***

Device code: AAHR

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

NO.	Pin Name	TYPE	Pin Description
1	NC		Not connected.
2	WAKE	I	Shutdown control.
3	VB	SUPPLY	Input voltage.
4	HGATE	I/O	Gate drive output of Hot Swap MOS.
5	SOURCE	I/O	Common Source Input and Gate Drive Return.
6	DGATE	I/O	Diode Controller gate drive output.
7	NC		Not connected.
8	TM_1		Connect directly to GND.
9	NC		Not connected.
10	SENSE	I	Current sense pin. Connect an external current sense resistor between this pin and OUT to monitor V_{SENSE}-V_{OUT}.
11	OUT	I	External MOS drain voltage sense.
12	NC		Not connected.
13	TM_5		Connect directly to GND.
14	TM_6		Connect directly to GND.
15	NC		Not connected.
16	CPTANK	O	Charge pump output. Connect a capacitor to ground. Typical value 220nF.
17	CP2P		Charge pump pin for capacitor 2, positive side.
18	CP1P		Charge pump pin for capacitor 1, positive side.
19	CP2M		Charge pump pin for capacitor 2, negative side.
20	CP1M		Charge pump pin for capacitor 1, negative side.
21	NC		Not connected.

NO.	Pin Name	TYPE	Pin Description
22	ENOUT	O	MOSFET fully on indication output. It is an open drain, active high output that requires an external pull up resistor. Typical 4.7kΩ for 5V IO line.
23	GND	Ground	Ground.
24	DIS	I	Disable. This pin need add a <25kΩ pull down resistor.
25	TIMER		A capacitor connected from this pin to GND provides a power up fault timing function.
26	FLTb	O	FLTb output signal when fault is present. Internal Pull-down works as Open Drain Output and External resistor pull up the output. Typical 4.7kΩ for 5V IO line.
27	TM_2		Connect directly to GND.
28	TM_3		Connect directly to GND.
29	TM_4		Connect directly to GND.
30	OV	I	Input overvoltage protection. Overvoltage comparator Input.
31	UV	I	Input undervoltage protection. Undervoltage comparator Input.
32	NC		Not connected.

Block Diagram

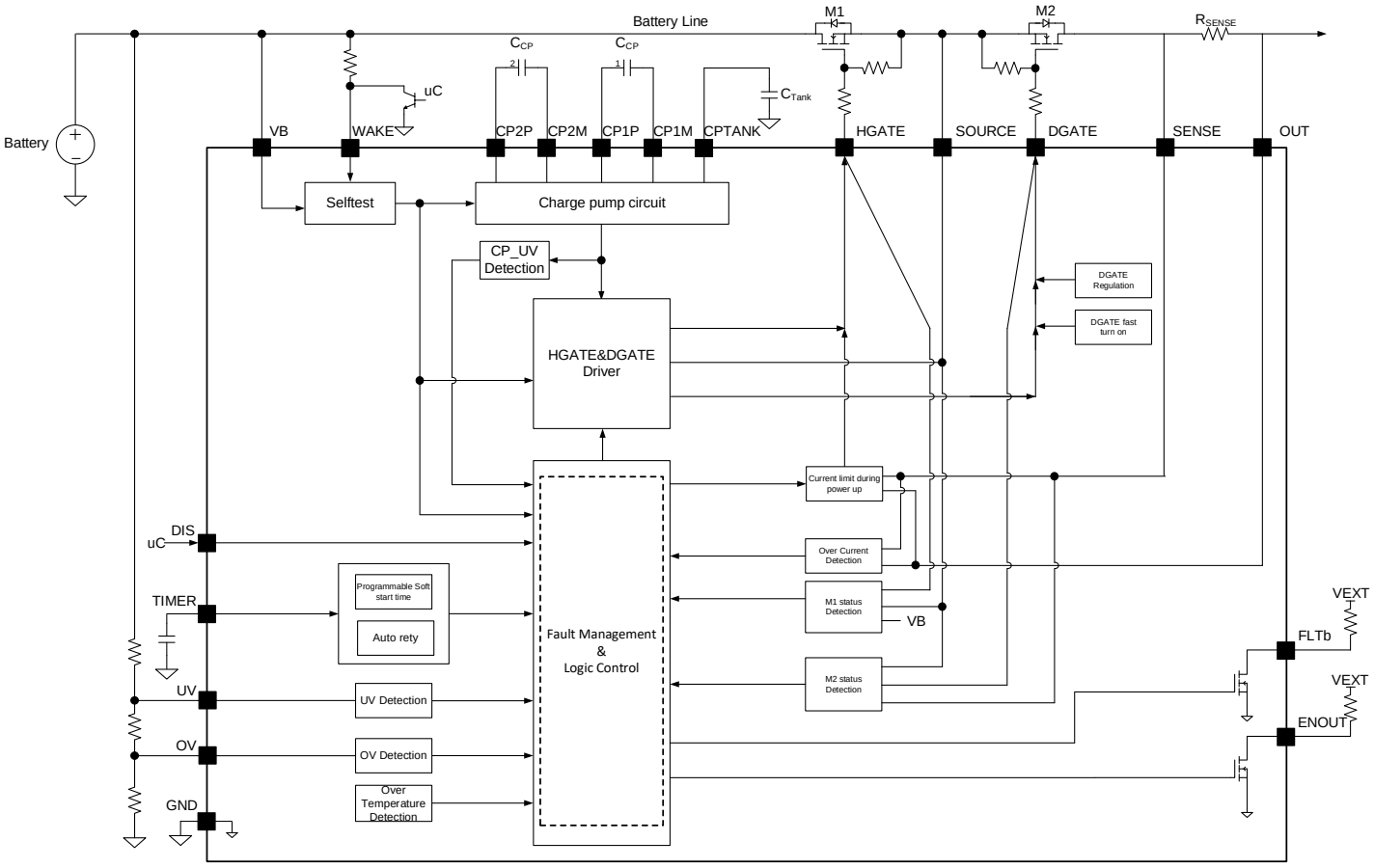


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
WAKE (Condition: VB=WAKE, all pin GND) Voltage	-65	65	V
VB (Condition: All pin GND) Voltage	-65	65	
SOURCE, OV, UV	-65	65	
HGATE, DGATE	-65	78	
CP1M, CP2M, ENOUT, DIS, FLTb, TIMER	-0.3	65	
TM_1, TM_2, TM_3, TM_4, TM_5, TM_6	-0.3	5	
SENSE, OUT	–0.3V/(-3.6V 100μs)/(-4.6V 10μs)	65	
GND	-0.3	0.3	
CPTANK, CP1P, CP2P	-0.3	78	
CPTANK-VB	-0.3	13	
CPTANK-HGATE, CPTANK-DGATE, CPTANK-SOURCE	-0.3	65	
CPTANK-CP1P, CPTANK-CP2P, CPTANK-CP1M, CPTANK-CP2M	-0.3	20	
VB-HGATE, VB-WAKE, VB-SOURCE	-0.3	65	
VB-CP1M, VB-CP2M	-0.3	6	
CP1P-CP1M	-0.3	6	
CP2P-CP2M	-0.3	13	
SENSE-SOURCE	-0.3	65	
HGATE-SOURCE, DGATE-SOURCE	-0.3	13	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	22	°C/W
θ_{JC} Junction-to-case Thermal Resistance	1.8	
Power Dissipation, P_D @ T_A=25°C	4.55	W

ESD Susceptibility

Parameter	Min	Max	Unit
HBM (Human Body Mode)			
HBM (all pins)	-2	+2	kV
CDM (Charged Device Mode)			
CDM(Corner pins)	-750	+750	V
CDM(All pins)	-500	+500	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VB, WAKE, SOURCE, DGATE, SENSE, OUT, ENOUT, DIS, FLT, OV, UV	-0.3	40	V
CP1M, CP2M, TIMER	-0.3	40	
HGATE, CPTANK, CP2P, CP1P	-0.3	50	
TM_1, TM_2, TM_3, TM_4, TM_5, TM_6, GND	-0.3	0.3	
Operating Junction Temperature	-40	150	°C
Ambient Temperature	-40	125	

Electrical Characteristics

((VB=4V to 40V, T_A=-40°C ~125°C. Typical values are at VB=14V, T_A=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.(Note 4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General Characteristics						
Wide Range AMR	$V_{B, range1}$	Full function	4 (Note 5)	14	65	V
Operating Range	$V_{B, range2}$	Full parameters	4 (Note 5)		40	V
Minimum VB to Turn On Device	$V_{B,min}$		6			V
Supply Current	I_{ON}	V_B=14V,V_B=28V, WAKE=High, DIS=Low		1.65	2.2	mA
Supply Current in Shutdown@VB=14V, T_J=125℃	I_{sd_hot}	V_B=14V, WAKE=Low			50	μA
Supply Current in Shutdown@VB=14V, T_J=25℃	I_{sd}	V_B=14V, WAKE=Low			25	μA
Supply Current in VB, UV, OV, WAKE Pin During Device Shutdown@14V, T_J=125℃ (Note 6)	I_{sdtot_hot}				55	μA
Supply Current in VB,UV, OV, WAKE Pin During Device Shutdown@14V, T_J=25℃ (Note 6)	I_{sdtot}				30	μA
VB _Slope_fast	$V_{B\_Slope\_F}$				1	V/μs
VB _Slope_fast_ON	$V_{B\_Slope\_F\_ON}$	Device ON VB>8V			5	V/μs
VB _Slope_slow	$V_{B\_Slope\_S}$		2			V/ms
WAKE Pin						
WAKE Turn ON Threshold	V_{WAKE_H}		2.1		2.7	V
WAKE Turn OFF Threshold	V_{WAKE_L}		1.4		2	V
WAKE Hysteresis	V_{WAKE}_hys		0.8		1.2	V
WAKE Input Current	I_{WAKE}	V_{WAKE}<V_{WAKE_H}-200mV	0.4		10	μA
WAKE On Filter Time (Note 6)	$t_{WAKE\ on\_flt}$			100		us
WAKE Off Filter Time (Note 6)	$t_{WAKE\ off\_flt}$			1		ms
WAKE ON Time	t_{WAKE_ON}	WAKE ON to GATE charge		2	2.5	ms
OV and UV Pins						
UV Threshold	$V_{UVth, LH}$		1.14	1.2	1.26	V
UV Threshold	$V_{UVth, HL}$		0.95	1	1.05	V
UV Filter Time (Note 6)	t_{uv_flt}				100	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OV Threshold	$V_{OVth, LH}$		1.14	1.2	1.26	V
OV Threshold	$V_{OVth, HL}$		0.95	1	1.05	V
OV Filter Time (Note 6)	t_{uv_flt}				10	μs
UV Leakage Current	$I_{UV, Iwak}$				1	μA
OV Leakage Current	$I_{OV, Iwak}$				1	μA
OC Protection						
Current Limit During Start up, (V_{SENSE}–V_{OUT})	V_{CL0}	V_{OUT}<2.8V	1.5	3	4.5	mV
Current Limit During Start up, (V_{SENSE}–V_{OUT})	V_{CL1}	V_{OUT}<50%*V_B	3	5	7	mV
Current Limit During Start up, (V_{SENSE}–V_{OUT})	V_{CL2}	50%*V_B<V_{OUT}<V_B-0.8V and V_{HGATE}-V_{SOURCE}>5.5V	8	10	12	mV
CL0 to CL1 Threshold	$V_{OUT\_CL0\ to\ CL1}$		2	2.8	3.6	V
Overcurrent Fault Threshold (V_{SENSE}–V_{OUT})	V_{OC_th}		50	57	64.5	mV
Overcurrent Fast Trip Fault Threshold (V_{SENSE}–V_{OUT})	$V_{OC\_fast\_th}$		90	101	112	mV
Overcurrent Filter Time	t_{OC_flt}		400	450	500	μs
Overcurrent Filter Time (Note 6)	$t_{OC\_fast\_flt}$		1		2.2	μs
TIMER Pin						
Sourcing Current (Note 6)	$I_{TIMER,SRC}$		8	10	12	μA
Sinking Current	$I_{TIMER,SNC1}$	V_{TIMER}=1.5V	8	10	12	μA
	$I_{TIMER,SNC2}$	V_{WAKE}=V_{DIS}=High, V_{TIMER}=1.5V	2	4.5	8	mA
Upper Threshold Voltage	$V_{TIMER,U}$		1.3	1.35	1.4	V
Lower Threshold Voltage	$V_{TIMER,L}$		0.335	0.355	0.375	V
HGATE OK Threshold Voltage	V_{HG_OK}	Raise HGATE until I_{TIMER} sinking, measure $V_{(HGATE–SOURCE)}$, V_B=V_{OUT}=14V	5	5.5	6	V
HGATE OK Voltage Filter Time	$t_{(HGATE-SOURCE)\_flt}$				120	μs
Bleed-down Resistance	$R_{TIMER,SD}$	V_B=V_{WAKE}=0V, V_{TIMER}=1.5V	70	104	142	kΩ
TIMER Short to GND Protection Voltage	V_{TIMER_S}		0.335	0.355	0.375	V
TIMER Short to GND Protection Filter Time	$t_{\_TIMER\_S\_flt}$		24	27	31	ms
ENOUT Pin						
ENOUT Output Low Voltage	V_{ENOUT_OL}	Pull up current=1mA			0.4	V
ENOUT Leakage Current	I_{ENOUT_LEAK}	V_{ENOUT}=5V, Output buffer off			10	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
(V_B–V_{OUT}) Difference in Order to Release ENOUT	V_{FULL_ON}	ENOUT from Low to High	0.5	0.8	1.1	V
Filter Time to Activate ENOUT (Note 6)	$t_{FULL\_ON,flt}$				100	μs
FLTb Pin						
FLTb Output Low Voltage	V_{FLTb_OL}	Pull up current=1mA			0.4	V
FLTb Leakage Current	I_{FLT_LEAK}	V_{FLTb}=5V, Output buffer off			10	μA
Charge Pump						
Charge Pump Voltage	V_{CP}	V_B=14V, I_{CP}=4mA	V_B+8V	V_B+9.5V	V_B+11V	V
Charge Pump Voltage	V_{CP_LOW}	V_B=4.5V, I_{CP}=4mA	V_B+6.5V			V
Charge Pump Undervoltage_L	$V_{CP\_UV\_L}$	CPTANK Pin fall from V_B+11V to V_B+0V	V_B+4.9V		V_B+5.9V	V
Charge Pump Undervoltage_H	$V_{CP\_UV\_H}$	CPTANK Pin Rise from V_B+0V to V_B+11V	V_B+5.5V		V_B+6.5V	V
Charge Pump Undervoltage Hystersis	$V_{CP\_UV\_HYS}$		0.2	0.5	0.8	V
Charge Pump Undervoltage Filter Time (Note 6)	$V_{CP\_UV\_flt}$		60		100	μs
Charge Pump Switching Frequency	f_S			385		kHz
C1 and C2 Flying Capacitor	Cfly			100		nF
Tank Output Capacitor	Ctank			220		nF
Hot Swap MOS						
HGATE Gate Drive, (V_{HGATE}−V_{SOURCE})	ΔV_{HG1_4V}	Drive voltage @V_B=4.5V	6.5			V
HGATE Gate Drive, (V_{HGATE}−V_{SOURCE})	ΔV_{HG1_12V}	Drive voltage @V_B=14V	9		13	V
HGATE Pull-Up Current	$I_{HG,PU}$		20	35	50	μA
HGATE Pull-Down Current	$I_{HG,PD}$	V_{HGATE}-V_{SOURCE}=6V	40	70	110	mA
VGS Comparator	$V_{GS\_Hotswap}$		0.5	1.5	2.2	V
VGS Comparator Filter Time (Note 6)	$t_{Hotswap\_VGS\_flt}$		0.8	0.9	1	ms
VDS on Soft Start MOS. Generate FLT if Detection Happen after ENOUT set	$V_{DS\_Hotswap}$		0.8	1	1.2	V
VDS Detection Filter Time (Note 6)	$t_{Hotswap\_VDS\_flt}$		4.45	5	5.55	ms
ORing MOS						
DGATE Gate Drive, (V_{DGATE}−V_{SOURCE})	ΔV_{DG2_4V}	Drive voltage @V_B=4.5V, M2 Fully ON	6.5			V
DGATE Gate Drive, (V_{DGATE}−V_{SOURCE})	ΔV_{DG2_12V}	Drive voltage @V_B=14V, M2 Fully ON	9		13	V
DGATE ORing Pull-Up Current, peak	$I_{DG,PU}$	V_{SOURCE}-V_{SENSE}=200mV, V_{DGATE}-V_{SOURCE}=1V	55		150	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DGATE ORing Pull-Down Current, peak	$I_{DG,PD}$	DIS=High, V_{DGATE}-V_{SOURCE}=6V	100		280	mA
Ideal Diode Regulation Voltage, (V_{SOURCE}–V_{SENSE})	ΔV_{ORing_Reg}		15	30	47	mV
(V_{SOURCE}–V_{SENSE}) for Fast Turn ON Activation Voltage	ΔV_{ORing_Fast}		60	80	130	mV
Fast Turn ON Duration Time	$t_{fast\_turn\ on}$		2.6	4	5.4	μs
Fast Turn ON Clamp voltage	$V_{DGATE-SOURCE\_F\_D}$		6	7.2	8	V
Reverse Voltage Shut Off (V_{SOURCE}-V_{SENSE})	ΔV_{ORing_Rev}		-4	-10	-15	mV
DGATE Turn off Propagation Delay (Note 6)	$t_{ORing\_Turnoff\_delay}$				0.6	μs
VGS Comparator	V_{GS_ORing}		0.15	0.27	0.37	V
VGS Comparator Filter Time(Note 6)	$t_{ORing\ \_VGS\_flt}$		8	9	10	ms
VDS on ORing MOS. Generate FLT if Detection Happens	V_{DS_ORing}		270	300	330	mV
Open Detection Filter Time (Note 6)	$t_{ORing\ \_VDS\_flt}$		0.8	0.9	1	ms
DIS Pin						
High Input Voltage Range	$V_{DIS\_in\_hl\_th}$		2			V
Low Input Voltage Range	$V_{DIS\_in\_ll\_th}$				0.8	V
Internal Pull Down Current	$I_{DIS\_in\_pd}$	Pin=3.3V	20	40	60	μA
Disable Pin Filter Time (Note 6)	t_{DIS_flt}			2	5	μs
Thermal protection(Note 6)						
Thermal Shutdown	T_{SD_TH}		150	160	170	°C
Hysteresis	T_{SD_hys}			20		°C
Thermal Filter Time	t_{TSD_filter}		8	10	12	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25°C on a highly effective four-layer test board of JEDEC51-7 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

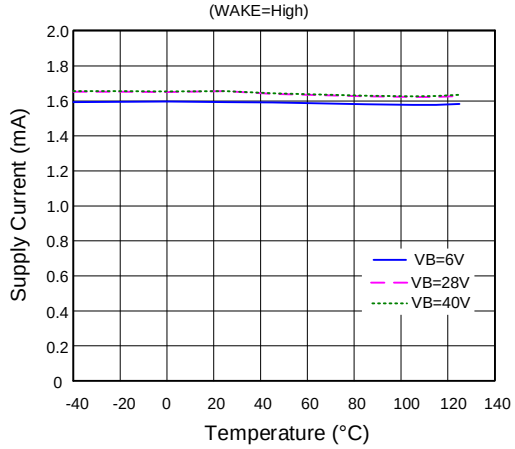
Note 5: Cranking scenario.

Note 6: Guaranteed by design or statistical correlation and not production tested.

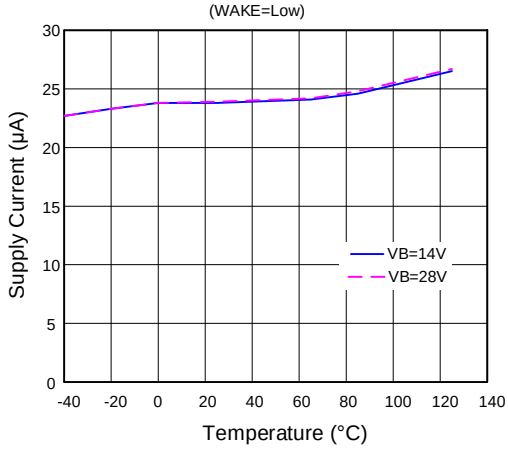
Typical Performance Characteristics

(V_B=14V, T_A=25°C, unless otherwise specified.)

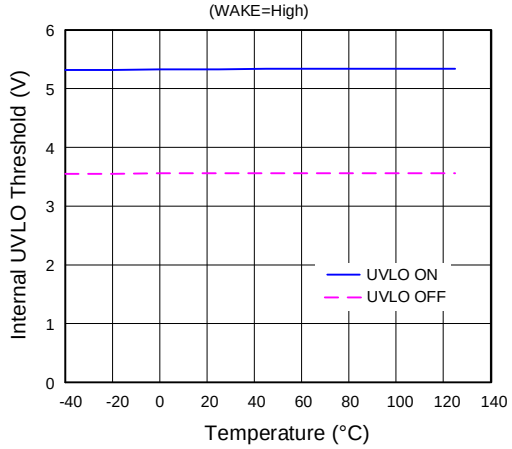
Supply Current at Normal Operation vs. Temperature
(WAKE=High)



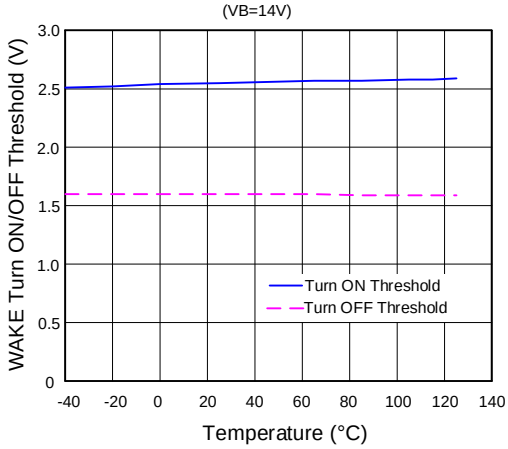
Supply Current at Shutdown vs. Temperature
(WAKE=Low)



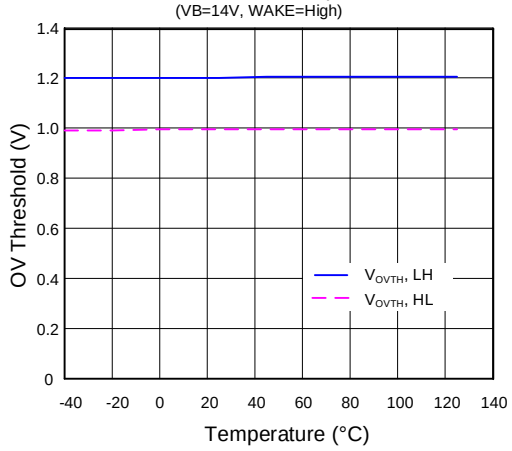
Internal UVLO Threshold vs. Temperature
(WAKE=High)



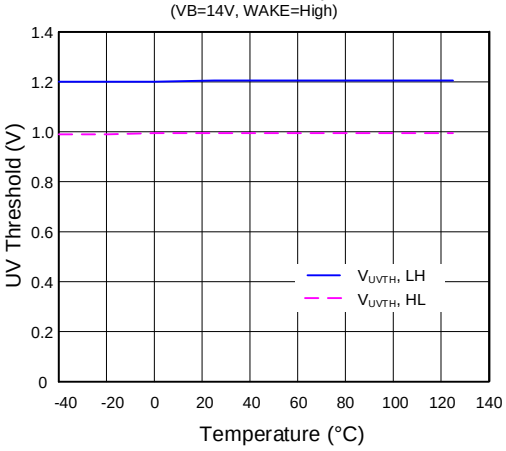
WAKE Turn ON/OFF Threshold vs. Temperature
(VB=14V)



OV Threshold vs. Temperature
(VB=14V, WAKE=High)



UV Threshold vs. Temperature
(VB=14V, WAKE=High)



Operation

The SA21904A is a controller which operates with external back-to-back connected N-channel power MOSFETs. The device can be used either for 12 V or 24 V supply rails.

The two N-channel MOSFETs are driven by the current limit function and ORing function respectively during power up. The current limit function can limit the inrush current during power-up. The ORing MOSFET is mainly used as ideal diode, and it can also block the reverse current conduction in case of fault like power source failure, brown out or input short.

Power ON Self-test Function

The device integrates the function of power-on self-test. This function is activated when the voltage of VB exceeds the internal UVLO (Under-Voltage Lockout) threshold and the voltage of WAKE exceeds the turn on threshold, V_{WAKE_H}. The entire self-test process typically takes about 2ms.

During the self-test, the internal HGATE and DGATE keep pulled low to SOURCE, and the following items are evaluated:

- Trim Code Check
- Charge Pump Clock Check
- Fault Comparator Logic Behavior Check: This includes all faults listed in Table 1 below.
- Test Mode Check
- ENOUT Logic Check
- Fast Turn on Function Check
- SOURCE pin Short to GND Check

Once the self-test is completed, HGATE and DGATE begin to be charged, and ENOUT is pulled down because the output is not established.

If any of the self-test items fail, FLTb will be pulled down at the end of the self-test process, the CPTANK will be discharged, and the HGATE and DGATE pull-down drives will remain active. The self-test failure is a latch-off fault and the self-test process can be re-initiated by re-enabling the VB or WAKE signal.

Current Limit during Power-up

The SA21904A current limitation during power-up acts sensing voltage drop across external shunt resistance, connected through SENSE and OUT pins. The Power-up mode consists of the following four states:

State 1: $V_{(SENSE-OUT)}=V_{CL0}$ when $V_{OUT}<V_{OUT\_CL0\ to\ CL1}$. TIMER begins to source current to the timer capacitor when OUT starts to build.

State 2: $V_{(SENSE-OUT)}=V_{CL1}$ when $V_{OUT\_CL0\ to\ CL1}<V_{OUT}<50\%\times V_B$. TIMER always source current to the timer capacitor.

State 3: $V_{(SENSE-OUT)}=V_{CL2}$ when $50\%\times V_B<V_{OUT}<V_B-V_{FULL\_ON}$. TIMER always source current to the timer capacitor.

State 4: When OUT OK is high, that is $V_{OUT}>V_B-V_{FULL\_ON}$, current limit loop is disabled. When power up is completed, that is $V_{OUT}>V_B-V_{FULL\_ON}$ and $V_{(HGATE-SOURCE)}>V_{HG\_OK}$, the timer capacitor starts discharging to 0V.

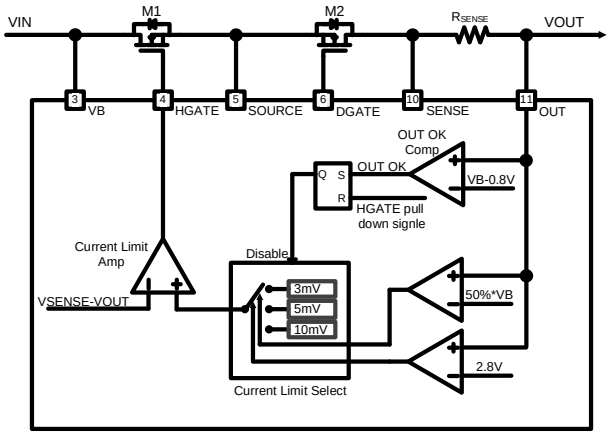


Figure 4 Partial Diagram of Current Limit Function during Power up

Power up Fail Detection

There are three scenarios that are considered to be power up fail:

- When a non-latched fault occurs during the TIMER timing process, fault type can refer to the table 1. Fault Table.
- When V_{TIMER} reaches $V_{TIMER,L}$, V_{OUT} is still less than $V_{OUT\_CL0\ to\ CL1}$.
- When V_{TIMER} reaches $V_{TIMER,U}$, the power up is not yet complete.

Once a power up fail occurs, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. Then the device goes into retry mode.

Short Circuit Protection

The SA21904A integrates over current protection and

V_{OUT} short to GND detection to protect against short circuit fault.

The device monitors load current by sensing the voltage across external shunt resistance, connected through SENSE and OUT pins. The device incorporates two distinct thresholds: a overcurrent fault threshold and a overcurrent fast-trip fault threshold. When V_{OUT} drops to negative values, the comparator used to trigger short-circuit protection cannot work normally.

If V_{OUT} falls below $V_{OUT\_CL0\ to\ CL1}$ after power up is completed, V_{OUT} short to GND is detected.

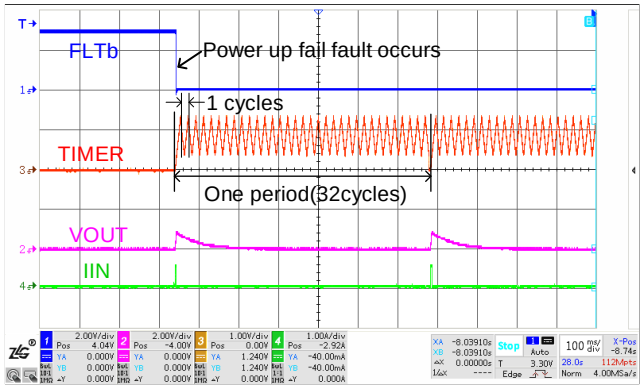
When an overcurrent or V_{OUT} short to GND event occurs, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. Then the device goes into auto-retry mode.

In the event of a short circuit, the current will increase rapidly. After triggering the protection, M_1 and M_2 are turned off, and the current will drop rapidly. If there is a long line from the battery to the drain of M1, the rapid change of current will make the drain voltage oscillate. When both M_1 and M_2 are turned off, the SOURCE may be coupled to negative values by the drain of M_1, causing overpressure from CPTANK to SOURCE. In this application, it is recommended to add a π type filter to the input and to be close to the drain of M_1.

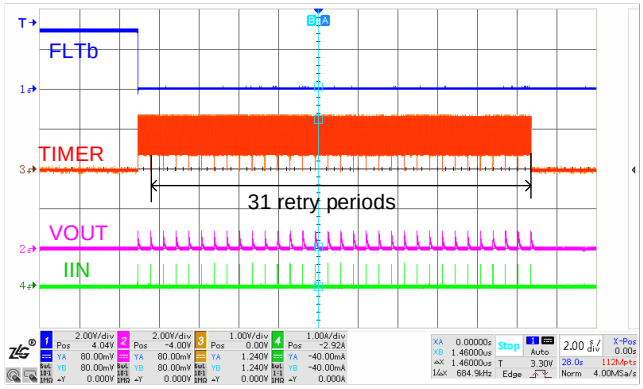
Auto-retry Mechanism

The SA21904A automatically initiates a restart after a short circuit event or Power up fail fault has caused it to turn off the external MOSFET M_1 and M_2. Internal control circuits use C_T to count 32 cycles before re-enabling M_1 and M_2 as shown in Figure 5(a). The TIMER pin is pulled to GND at the end of the 32th cycle of charging and discharging. The auto retry counter incremented if retry period is not successful, and the device should be latched after 31 auto retry periods as shown in Figure 5(b).

The timer has a 1: 1 charge-to-discharge current ratio. For the very first cycle, the TIMER pin starts from 0V and rises to the upper threshold of $V_{TIMER,U}$ and subsequently falls to $V_{TIMER,L}$ before restarting. For the following 32 cycles, $V_{TIMER,L}$ is used as the lower threshold. This small duty cycle often reduces the average short circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.



(a)



(b)

Figure 5 Auto Retry Mechanism

If one of the retry cycles is successful, the counter of retry should be reset.

TIMER Pin Short to GND Protection

The device integrates the detection of the TIMER pin short to GND during the startup process. The purpose is to prevent the situation where the MOS cannot be turned off when both the TIMER pin and the OUT pin are shorted to GND simultaneously. The detection is implemented by checking whether V_{TIMER} exceeds $V_{TIMER,L}$ within $t_{\_TIMER\_S\_flt}$. If it does not, it is considered a TIMER short to GND fault. If the device completes the power up within the $t_{\_TIMER\_S\_flt}$, the TIMER will be discharged, and this detection will also be disabled.

Once a TIMER short to GND fault occurs, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. Then the device goes into latch off mode.

A toggling on WAKE input is necessary to re-enable the device and unlatch the fault.

UV and OV Detection

The battery UV and OV trip point are adjusted using the external voltage divider network of R_1, R_2, R_3 and R_4 as connected between VB, UV, OV and GND pins of the device.

When the UV pin falls below its $V_{UVth, HL}$ threshold, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. When the UV pins rises above $V_{UVth, LH}$, both HGATE and DGATE pins are allowed to turn on if there is no other fault.

When the OV pin is above its threshold of $V_{OVth, LH}$, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. When OV falls below $V_{OVth, HL}$, both HGATE and DGATE pins are allowed to turn on if there is no other fault.

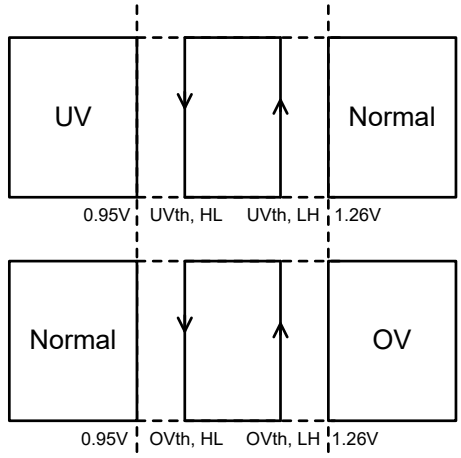


Figure 6. Under Voltage and Over Voltage Detection

External MOSFETs Status Detection

The SA21904A integrates VDS open and VGS short detection for external two MOSFETs. The VGS and VDS diagnostic are masked before power up is completed. Once VDS open or VGS short occurs, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. Then the device goes into latch off mode.

A toggling on WAKE input is necessary to re-enable the device and unlatch the fault.

ORing Function

The ORing function integrates Ideal diode function, Fast turn on function and Reverse current protection.

When the load current is small enough, the DGATE pin is actively driver to maintain ΔV_{ORing_Reg} across the ORing MOSFET ($V_{(SOURCE-SENSE)}$) by actively regulating DGATE, thus implementing ideal diode function.

In case of the forward voltage of drop across the ORing MOSFET more than ΔV_{ORing_Fast}, the DGATE pin is pulled high by a strong pull up current $I_{DG,PU}$ until $V_{(DGATE-SOURCE)}$ reachs $V_{DGATE-SOURCE\_F\_D}$ threshold voltage, and then DGATE charging current is controlled by internal ideal diode regulation loop, thus implementing fast turn on function. I_{DG_PU} duration time is up to $t_{fast\_turn\ on}$.

In case of reverse voltage of drop across the MOSFET less than ΔV_{ORing_Rev}, the DGATE is pulled down to SOURCE and the FLTb pin is not asserted, thus preventing reverse current flowing into battery line.

Reverse current protection and fast turn on function are also used in order to quickly turn on and off the ORing MOSFET, in order to sustain 16750 AC ripple test and preventing AC noise to be transferred on V_{OUT} line.

Disable Function

When the DIS pin is driver at high logic level, both HGATE and DGATE are pulled down to SOURCE and the FLTb pin is asserted. When DIS pin is driver at low logic level, both HGATE and DGATE pins are allowed to turn on if there is no other fault.

Indication function

ENOUT is an open-drain output that goes high impedance when Power up is completed ($V_{OUT}>V_B-V_{FULL\_ON}$ and $V_{(HGATE-SOURCE)}>V_{HG\_OK}$) when first power on, indicating the external MOSFETs are fully on. Once power up is completed. ENOUT pin state is only related to the VOUT, ENOUT goes low if $V_{OUT}<V_B-V_{FULL\_ON}$.

FLTb is an open-drain output that pulls low when a fault is detected, after proper filter time (depending on fault type).

Fault Management

In the following table are reported all the faults that creates an alarm on the FLTb pin, with proper filter time.

To clear a latched fault the WAKE pin has to be set to below 1.4V for its filter time(1ms) and then set again to above 2.7V for this filter time(1ms), so a new power-up sequence restart.

Table 1. Fault Table

Classifi-cation	Event	Filter Time	HGATE	DGATE	FLTb	Latched	Action for Coming Back to Operating	Scenario
Hot Swap FET	M1 VGS short detection	0.9ms	Low	Low	Active	Yes	Toggling WAKE	$V_{(HGATE-SOURCE)}$ <$V_{GS\_Hotswap}$ after Power up is completed(V_{OUT}>V_{B-} V_{FULL_ON} and $V_{(HGATE-SOURCE)}$>V_{HG_OK})
	M1 VDS open detection	5ms	Low	Low	Active	Yes	Toggling WAKE	$V_{(VB-SOURCE)}$>$V_{DS\_Hotswap}$ after Power up is completed
	Overcurrent	1/450μs	Low	Low	Active	Latched after 31 retries	Toggling WAKE	Output overcurrent
ORing FET	Reverse protection	0.6μs	High.	Low. M2 VDS and VGS Mask	Inactive	Not	$V_{(SOURCE-SENSE)}$ is above ΔV_{ORing_Rev}	Reverse voltage V_{BAT}<V_{OUT}
	M2 VGS short detection	9ms	Low	Low	Active	Yes	Toggling WAKE	$V_{(DGATE-SOURCE)}$<V_{GS_ORing} after Power up is completed
	M2 VDS open detection	0.9ms	Low	Low	Active	Yes	Toggling WAKE	$V_{(SOURCE-SENSE)}$>V_{DS_ORing} after Power up is completed
Global	CP_UV	80μs	Low	Low	Active	Not	If CP_UV disappears	UV on charge pump, VGS on MOSFETs cannot be guaranteed
	OT	10μs	Low	Low	Active	Not	If OT disappears	Over-temperature detected
	DIS	2μs	Low	Low	Active	Not	If DIS is not active	DIS pin is not asserted
	OV	10μs Max	Low	Low	Active	Not	OV disappear	Input overvoltage(internal OV pin threshold: 1.2V)
	UV	100μs Max	Low	Low	Active	Not	UV disappear	Input undervoltage(internal UV pin threshold: 1V)
	SAFETY_FAULT	-	Low	Low	Active	Yes	Toggling WAKE	Selftest fail
	Power-up fail	Programmed by TIMER	Low	Low	Active	Latched after 31 retries	Toggling WAKE	Power up is not completed
	TIMER Short to GND Protection	27ms	Low	Low	Active	Yes	Toggling WAKE	TIMER pin short to GND and Power up is not completed.

High voltage Hot Plug Application

The following diagram shows the internal simplified structure of charge pump, there is a parasitic diode between VB pin and CPTANK pin, the purpose is to pre-charge the charge pump voltage to VB minus a parasitic diode forward voltage drop before charge pump starts working.

If VB>40V for hot swapping, there is a strong current I_1 flowing through the parasitic diode to charge the hold capacitor C_{TANK} of Charge pump, which may cause IC damage. In this application, it is recommended to change the C_{TANK} negative side form GND pin to VB pin, this is shown in figure 7(b).

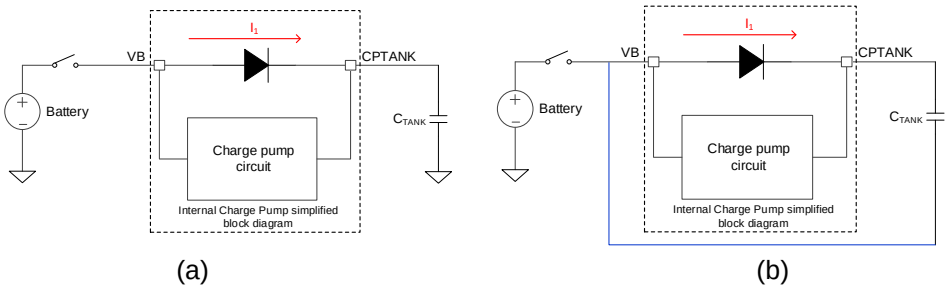


Figure 7 Charge Pump Simplified Block Diagram

Fast Line Transient Application

Due to the hold capacitor of the charge pump, when the battery voltage rises rapidly, the CPTANK voltage may not follow VB, resulting in a voltage drop in the HGATE and DGATE. When the battery voltage drops rapidly, it may cause an overvoltage between CPTANK and VB. In this application, it is recommended to change the C_{TANK} negative side form GND pin to VB pin to ensure that CPTANK can follow fast VB transient, this is shown in figure 7(b).

ORing MOSFET Reverse Protection

The reverse protection function of the ORing MOSFET is realized by detecting the voltage between SOURCE and SENSE by the comparator. When the source and sense drop rapidly, this comparator is slower to respond. In this application, it is recommended to add a minimum of 10μF capacitance at the output close to the OUT pin.

Application Information

In the Figure 8 the typical application schematic is shown.

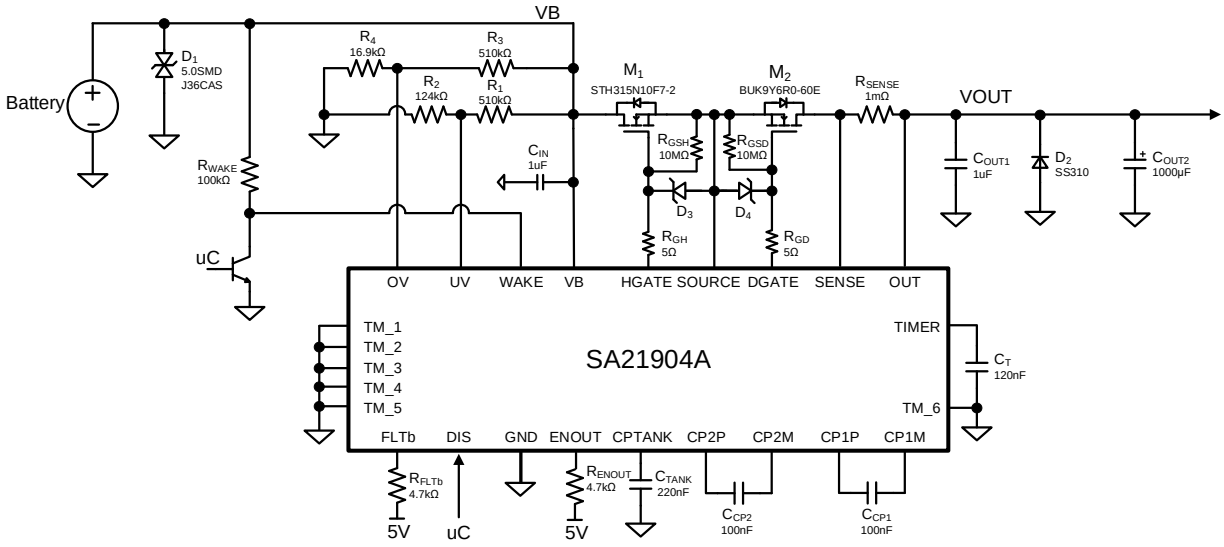


Figure8 Typical Application for 14V System

Current Sense Resistor R_{SENSE} Selection

R_{SENSE} is chosen considering the maximum operating load current. From the SA21904A electrical specifications, the Overcurrent fault threshold voltage V_{OC_th} is around 57mV. The R_{SENSE} is set by:

$$R_{SENSE} < \frac{V_{OC\_th}}{Max\ Load\ Current}$$

External Hot Swap MOSFET M_1 Selection

The hot swap MOSFET is chosen considering these main parameters:

- Maximum continuous drain current I_D. This value shall exceed the maximum continuous load current of the application.
- Maximum drain to source voltage V_{DS}. It shall be high enough to withstand the highest differential voltage in the application.
- Maximum gate to source voltage V_{GS}. It shall be higher than the maximum V_{GS} that SA21904A can drive for HGATE.
- Drain to source ON resistance R_{ON}. It is recommended a value as low as possible, to reduce the MOSFET conduction losses.
- Safe operating area SOA. It shall meet SOA of hot swap MOS when considering current limit during power up and TIMER capacitor.

User can choose the proper number of parallel MOSFETs depending on the kind of application and the expected levels of load currents. But it should be noted that the SOA should be considered as a single MOSFET.

External ORing MOSFET M_2 Selection

M_2 selection has similar requirements to M_1 selection, such as maximum I_D, V_{DS} and V_{GS}. In particular, the ORing MOSFET is also expected to be very fast during the transients of switching ON and OFF. A key parameter is the Qg (total gate charge) which is recommended to be as low as possible.

User can choose the proper number of parallel MOSFETs depending on the kind of application, the expected levels of load currents and the value of Qg.

TIMER Capacitor C_T Selection

The C_T selection is limited by the following conditions:

- It must suffice to fully charge the load capacitance C_{OUT} without triggering the fault circuitry.

- It must suffice to charge VOUT exceeds $V_{OUT\_CL0\ to\ CL1}$, which typical value is 2.8V, before V_{TIMER} reaches $V_{TIMER,L}$(typical value 0.355V).
- It shall meet SOA of hot swap MOS when considering current limit during power up.

Just as an example: normal operation voltage is 14V±2V, R_{SENSE}=1mΩ, maximum C_{OUT}=1000μF.

The maximum output voltage rise time, t_{ON}, it can be calculated by:

$$t_{ON} = \frac{C_{OUT} \times max.V_{OUT\_CL0\ to\ CL1}}{\frac{min.V_{CL0}}{R_{SENSE}}} + \frac{C_{OUT} \times (50\% \times VB_{max} - max.V_{OUT\_CL0\ to\ CL1})}{\frac{min.V_{CL1}}{R_{SENSE}}} + \frac{C_{OUT} \times 50\% \times VB_{max}}{\frac{min.V_{CL2}}{R_{SENSE}}}$$

Therefore,

$$t_{ON} = \frac{1000\mu F \times 3.6V}{1.5A} + \frac{1000\mu F \times 4.4V}{3A} + \frac{1000\mu F \times 8V}{8A} = 4.87ms$$

The maximum C_{OUT} is charged to maximum $V_{OUT\_CL0\ to\ CL1}$ time, t_{ON1}, it can be calculated by:

$$t_{ON1} = \frac{C_{OUT} \times max.V_{OUT\_CL0\ to\ CL1}}{\frac{min.V_{CL0}}{R_{SENSE}}} = \frac{1000\mu F \times 3.6V}{1.5A} = 2.4ms$$

The fault time programed by C_T needs to be greater than the t_{ON} and t_{ON1} calculated above. Considering the tolerance of TIMER sourcing current $I_{TIMER,SRC}$, upper threshold voltage $V_{TIMER,U}$ and lower threshold voltage $V_{TIMER,L}$, C_T needs to meet:

$$\begin{cases} C_T > \frac{max.I_{TIMER,SRC} \times t_{ON}}{min.V_{TIMER,U}} = \frac{12\mu A \times 4.87ms}{1.3V} \approx 45nF \\ C_T > \frac{max.I_{TIMER,SRC} \times t_{ON1}}{min.V_{TIMER,L}} = \frac{12\mu A \times 2.4ms}{0.335V} \approx 86nF \end{cases}$$

Therefore, the value of CT must be greater than 86nF.

In addition, when a start into short or retry with short circuit occurs, it is necessary to ensure that the hot swap MOSFET must be working in the SOA. The hot swap MOS in typical application is STH315N10F7-2, and its safe operating area is as follows:

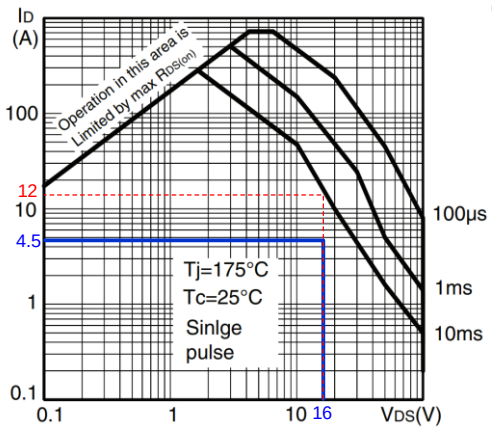


Figure 9 SOA Curve of STH315N10F7-2

As can be seen from the SOA curve, the maximum SOA limit is 192W×10ms, and the maximum power dissipation of start into short circuit in this application is 72W. Therefore, as long as the start into short circuit duration is less than 26.6ms (which is 192W×10ms/72W), the SOA requirement is sufficient, then C_T needs to meet:

$$C_T < \frac{min.I_{TIMER,SRC} \times 26.6ms}{max.V_{TIMER,U}} = \frac{8\mu A \times 26.6ms}{0.375V} \approx 567nF$$

Therefore, the value of C_T needs to meet 86nF<C_T<567nF.

External OV/UV Voltage Divider Network Selection

The external voltage divider network of R_1, R_2, R_3 and R_4 values must be chosen in the range of kΩ, to minimize the static power dissipation. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current must be chosen to be 20x greater than the leakage current expected. The values required for setting the undervoltage and overvoltage are calculated solving the following equations:

$$\begin{cases} VB\_OV = \frac{V_{OVth,LH} \times (R_3 + R_4)}{R_4} \\ VB\_UV = \frac{V_{UVth,HL} \times (R_1 + R_2)}{R_2} \end{cases}$$

VGS Discharge Resistor of External MOSFET Selection

In order to minimize the impact of the VGS discharge resistance on the accuracy of internal current limiting loop and regulation loop, it is recommended that the resistor be greater than 5MΩ.

Charge Pump Capacitors Selection

The sourcing current capability for the charge pump must guarantee proper turn on and turn off timings for ORing MOSFET also in case of AC ripple on the supply line. So, external capacitors must be connected to the device. For a proper operation fly capacitors shall be 100nF, and output hold capacitor 220nF, with a tolerance of 20%.

External Diodes D_1, D_2, D_3, D_4 Selection

As shown in Figure 8 some helpful external diodes are connected to the device.

- VB clamp diode, D_1: A sudden change in the input current may cause VB has a large ring, add a TVS diode from battery line to GND can clamp the VB voltage within the normal operation range.
- OUT clamp diode, D_2: Inductive loads on the output may drive the OUT pin below GND when the device is turned off. The OUT pin ratings can be satisfied by connecting a diode from OUT to GND. The diode should be selected to control the negative voltage at the full short circuit current. Schottky diodes are generally recommended for this application.

VGS clamp diode, D_3 and D_4: Zener diodes are connected between HGATE (or DGATE) and SOURCE pins, allowing to realize a clamp on the VGS voltage for both FETSs. It helps to protect the FETs in case of fast transients. Their connection is strongly recommended since the internal structure cannot guarantee a fast reaction.

External Pull-up Resistors for Digital Outputs Selection

Both digital outputs (FLTb and ENOUT) are realized as open drain. Pull-up resistor shall be connected between FLTb (or ENOUT) and a 5 V external supply line, for forcing high voltage level in case of no-faults. Recommended values for these pull-up resistors are in the order of kΩ.

PCB Layout Guide

The SA21904A applications require careful attention to layout to ensure proper performance and to minimize susceptibility to transients and noise. In general, all traces should be as short as possible, but the following list deserves first consideration:

- Decoupling capacitors on VB pin should have minimal trace lengths to the pin and to GND.
- Traces to SENSE and OUT must be short and run side-by-side to maximize common-mode rejection. Kelvin connections should be used at the points of contact with R_{SENSE}. (see Figure 10).
- Power path connections should be as short as possible and sized to carry at least twice the full load current, more if possible.
- Protection devices such as snubbers, TVS, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, the protection Schottky diode D_2 shown in the typical application diagram on the front page of this data sheet should be physically close to the OUT pin.

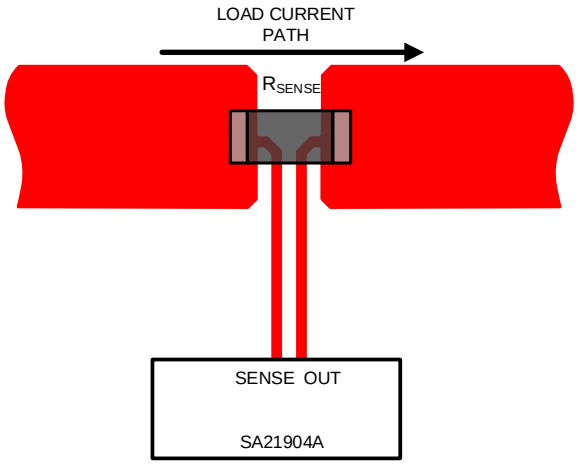
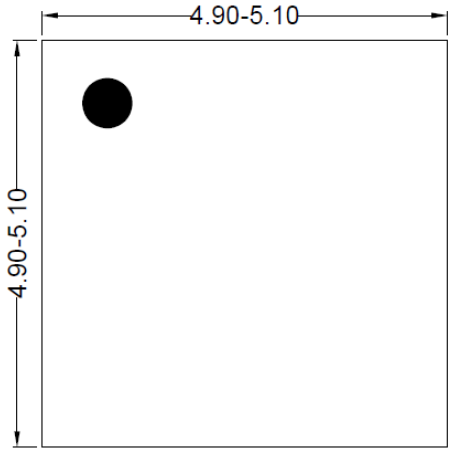
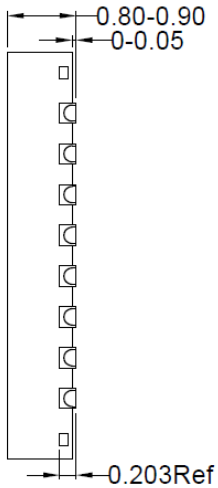


Figure 10. PCB Layout Guide

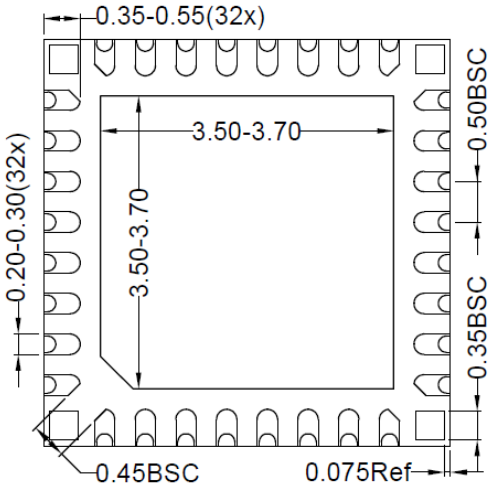
QFN5.0×5.0-32 Package Outline Drawing



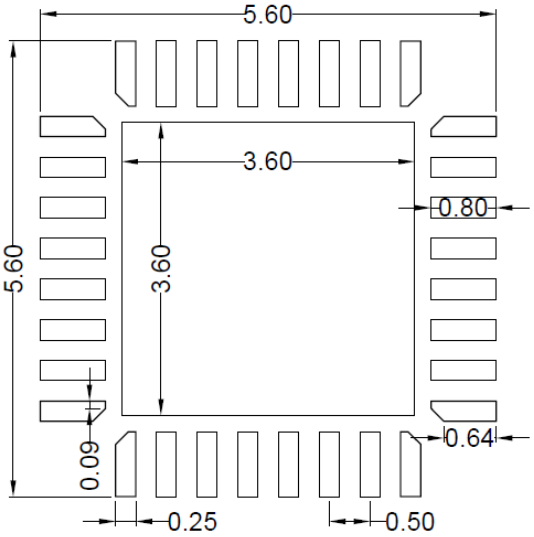
Top View



Side View



Bottom View

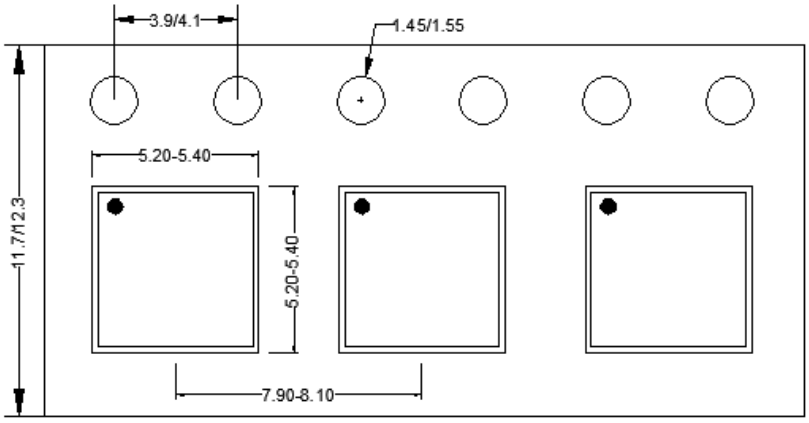


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.

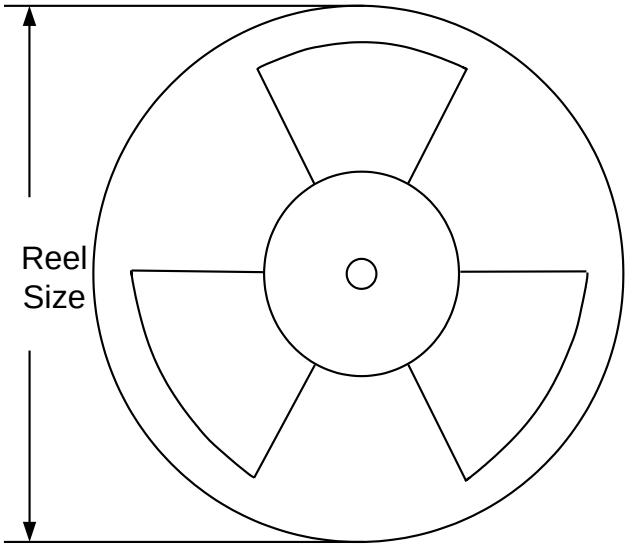
Tape and Reel Information

1. Tape Dimensions and Pin1 Orientation



Direction of Feed ⟶

2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Feb.13, 2025	Revision 1.0	Initial Release

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