SQ24905C

Hot Swap Controller with Digital Power, Energy Monitor and PMBus Interface

General Description

The SQ24905CQEQ is a hot swap controller designed to facilitate the safe removal and insertion of a live circuit board into a backplane. It includes a 12-bit analog-to-digital converter (ADC) for monitoring current, power, voltage and temperature via a PMBus interface. The load current is measured using an internal current sense amplifier, with a default current limit of 20mV that can be adjusted as needed.

This controller limits the current through the power path using an external N-channel MOSFET, controlled by the GATE pin. It also features overvoltage and undervoltage protection and a PWRGD signal to monitor the output supply. Additionally, it includes fast internal overcurrent detection and a RETRY pin for configuring automatic retry or latch-off in the event of an overcurrent fault.

The SQ24905CQEQ is available in a 32-lead QFN5x5 package.

Applications

- Servers and Datacenters
- Power Distribution Systems
- Telecommunication Equipment and Switches

Features

- 4.5V to 20V Input Voltage Range
- ±0.6% Accurate, 12-Bit ADC for V_{IN}, V_{OUT}, I_{OUT}, and Temperature Measurement
- Split Hot Swap and Power Monitor Inputs for Additional External ADC Filtering
- 320ns Response Time to Short-Circuit Events
- Resistor-Programmable Current Limit of 5mV to 25mV V_{SENSE}
- Programmable Start-Up Current Limit
- 1% Accurate UV, OV, and PWRGD Thresholds
- Remote Temperature Sensing with Configurable Warning and Shutdown Thresholds
- Shutdown After Detecting MOSFET Health Faults
- FAULT_N Open Drain Output
- Multi-functional GPO Output Pin:
  - SMBAlert Mode
  - General-purpose Digital Output Mode
  - Digital Comparator Mode
  - CONV Function Mode
- Reports Power and Energy Consumption Over Time
- Peak Detection Registers for Voltage, Current, and Power Monitoring
- PROCHOT Power Throttling Capability for Precise Control of System Power Usage
- PMBus Fast-Mode Compliant Interface and SPI Interface
- Moisture Sensitivity Level (MSL): 3
- QFN 5x5-32 Package

Typical Application

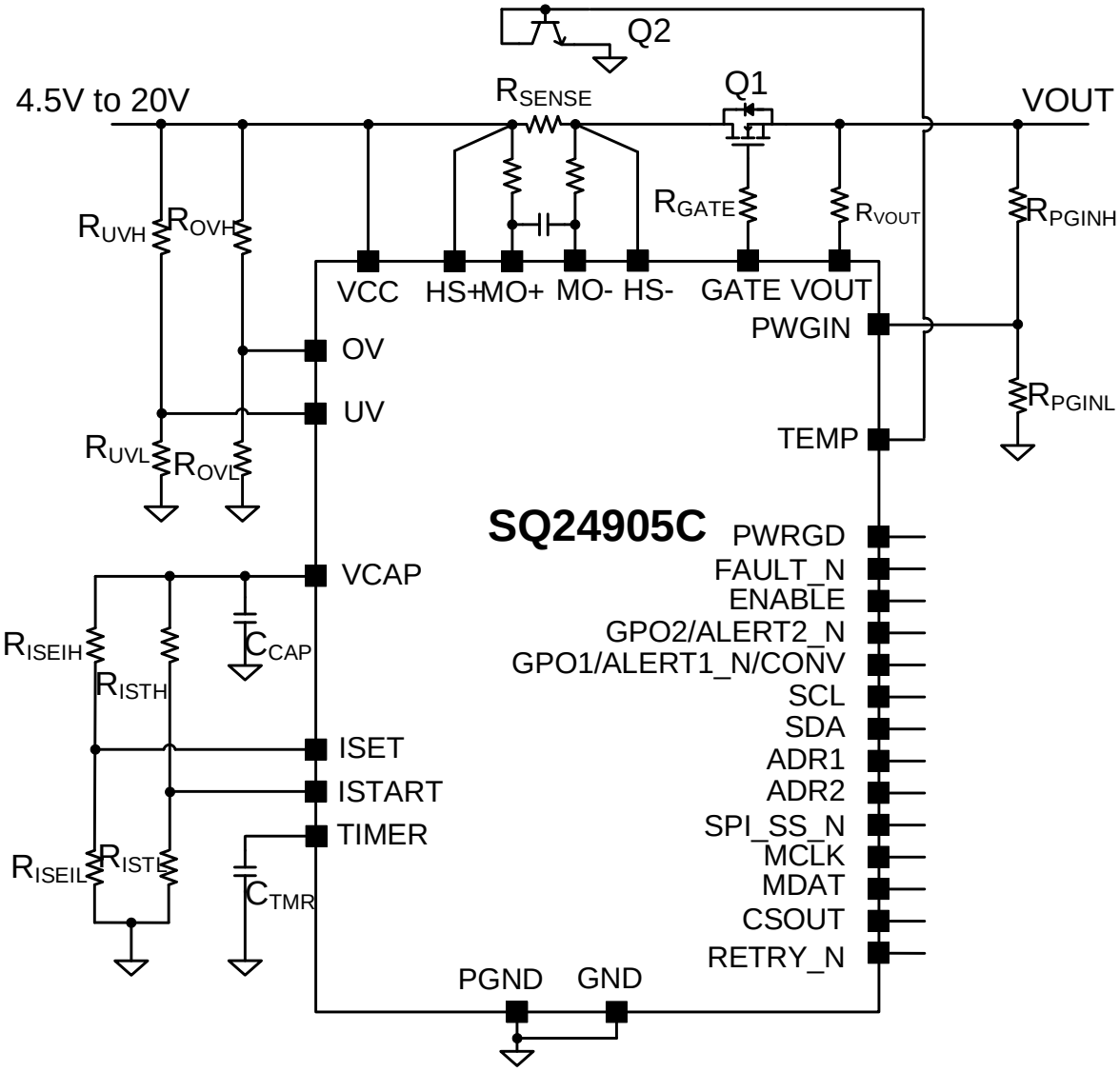


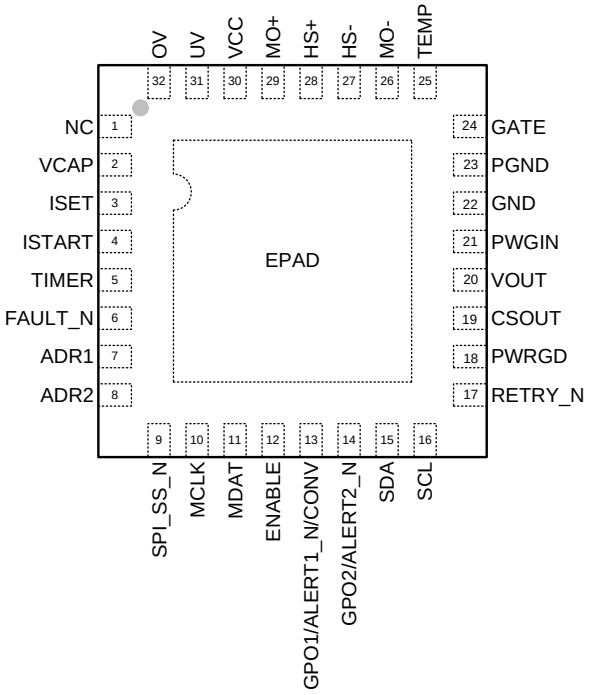
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ24905CQEQ	QFN5×5-32 RoHS Compliant and Halogen Free	**KHR*xyz***

Device code: KHR
x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Description

Pin Name	Pin Number	Description
NC	1	Not internally connected.
VCAP	2	Internal regulated supply. Place a 1μF or greater capacitor on this pin. This pin can be used as a reference to program the ISET/ISTART pin voltage.
ISET	3	Current limit setting input. Use a resistor divider to VCAP to program the current limit threshold. The default current limit can be set by connecting directly to VCAP. The current limit threshold can also be programmed by connecting an external reference.
ISTART	4	Start current limit setting input. This pin programs the current limit during the start-up stage. Connect a resistor divider to VCAP to set the start-up current limit. The start-up current limit is only active while PWRGD is low. The start-up current limit can also be set over PMBus using the STRT_UP_IOUT_LIM register. Start-up current limit = VISET × (STRT_UP_IOUT_LIM / 16). The lowest of all the active current limits always takes priority.
TIMER	5	Timer. Connect an external capacitor, C_{TIMER}, to set the initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin surpasses the upper threshold.
FAULT_N	6	Fault output. This pin asserts low and latches after a fault occurs. Faults that can trigger this pin include an overcurrent fault (causing the TIMER pin voltage to exceed the upper threshold), an overtemperature fault, and a MOSFET health fault. This is an open-drain output pin.
ADR1, ADR2	7, 8	PMBus device address. These pins can be tied to VCAP, tied to GND, left floating, or tied low through a resistor, providing 16 unique PMBus device addresses (refer to the Device Addressing section).

Pin Name	Pin Number	Description
SPI_SS_N	9	Slave Select. When pulled low, this pin begins to transfer data on the MDAT line.
MCLK	10	Master Clock. The MCLK signal outputs data on the MDAT line. This pin is clocked by an external device.
MDAT	11	Master Data Output. Open-drain output requiring an external pull-up resistor. The MDAT pin is an output-only pin used to stream data from the ADC. It provides current, voltage, and temperature data in a fixed format without requiring header information. This pin is high impedance when not transmitting data.
ENABLE	12	Device Enable. Pull high to enable the device. If the ENABLE pin is held low, the hot swap controller is kept off.
GPO1/ALERT1_N/CONV	13	General-Purpose Digital Output (GPO1) / Alert (ALERT1_N) / Conversion (CONV) This pin can be configured for multiple functions: GPO1: General-purpose digital output. ALERT1_N: Generates an alert signal when one or more fault or warning conditions are detected. CONV: Used as an input signal to control the start of a power monitor ADC sampling cycle. The GPO1/ALERT1_N/CONV pin defaults to an alert output at power-up and is an open-drain output pin.
GPO2/ALERT2_N	14	General-Purpose Digital Output (GPO2) / Alert (ALERT2_N) This pin can be configured for multiple functions: GPO2: General-purpose digital output. ALERT2_N: Generates an alert signal when one or more fault or warning conditions are detected. The GPO2/ALERT2_N pin defaults to an alert output at power-up and is an open-drain output pin.
SDA	15	Serial Data Input/Output. Open-drain input/output requiring a pull-up resistor. If not used, tie to GND or connect via a pull-up resistor to VCAP or another supply.
SCL	16	Serial Clock. Open-drain input requiring a pull-up resistor. If not used, tie to GND or connect via a pull-up resistor to VCAP or another supply.
RETRY_N	17	Retry input. The RETRY_N pin has an internal pull-up resistor. This pin can be pulled low to enable a 10-second auto retry following an overcurrent fault.
PWRGD	18	Power Good Output. Open-drain output pin. This pin indicates that no faults have been detected, the supply is within tolerance (PWGIN input), and the hot swap is enabled with the gate fully biased.
CSOUT	19	Current Sense Output. The VSENSE_HS voltage is amplified to provide an output voltage corresponding to the load current. To ensure accurate readings, the circuit connected to this pin has to offer a high input impedance.
VOUT	20	Output Voltage Feedback. Connect a 1kΩ resistor in series between the source of a MOSFET and the VOUT pin. This pin is used to sense the VOUT voltage.
PWGIN	21	Power Good Feedback. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the MOSFET (VOUT). The PWRGD output signal is not asserted high until the output voltage is above the threshold set by this pin.
GND	22	Ground. This pin is the ground connection for all sensitive analog nodes. Isolate this ground connection from the main high current path and any large transients. It is recommended that a ground island be created around the SQ24905CQEQ device and its supporting small signal components. Connect this ground island to the main ground plane at a single point as close to the SQ24905CQEQ GND pin as possible.

Pin Name	Pin Number	Description
PGND	23	Power Ground. This pin is the ground return path for the strong gate pull-down current. It is also the ground return for the external transistor used for temperature measurements.
GATE	24	Gate Driver Output. This pin is the high-side gate drive for an external N-channel MOSFET. The MOSFET drive controller uses a charge pump to provide pull-up current to charge the MOSFET gate pin. It regulates the maximum load current by controlling the GATE pin. When the supply is below the undervoltage lockout threshold (UVLO), the GATE pin is held low.
TEMP	25	Temperature Sense Input. An external NPN device can be placed near the MOSFETs and connected to the TEMP pin to report temperature. The voltage at the TEMP pin is measured by the internal ADC.
MO-	26	Negative Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage used by the ADC to measure load current. Additional filtering can be added between the MO+ and MO− pins if needed.
HS-	27	Negative Current Sense Input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. During hot swap operation, the SQ24905CQEQ regulates the external MOSFET gate to maintain the sense voltage (VHS+ − VHS−).
HS+	28	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the HS+ and HS− pins sets the analog current limit. During hot swap operation, the SQ24905CQEQ controls the external MOSFET gate to maintain the sense voltage (VHS+ − VHS−). Additionally, this pin is used to measure the supply input voltage using the ADC.
MO+	29	Positive Power Monitor Input. A sense resistor between the MO+ and MO− pins sets the sense voltage used by the ADC to measure load current internally. Additional filtering can be added between the MO+ and MO− pins if necessary.
VCC	30	Positive Supply Input. A UVLO circuit resets the device when a low supply voltage is detected. The GATE is held low when the supply is below the UVLO threshold. During normal operation, it is recommended that this pin be equal to HS+ and MO+ to ensure adherence to specifications. No sequencing is required.
UV	31	Undervoltage Input. An external resistor divider is connected from the input supply to this pin, allowing an internal comparator to detect if the supply voltage is below the UV limit.
OV	32	Overvoltage Input. An external resistor divider is connected from the input supply to this pin, enabling an internal comparator to detect if the supply voltage exceeds the OV limit.
EPAD		Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. It can be connected to ground.

Block Diagram

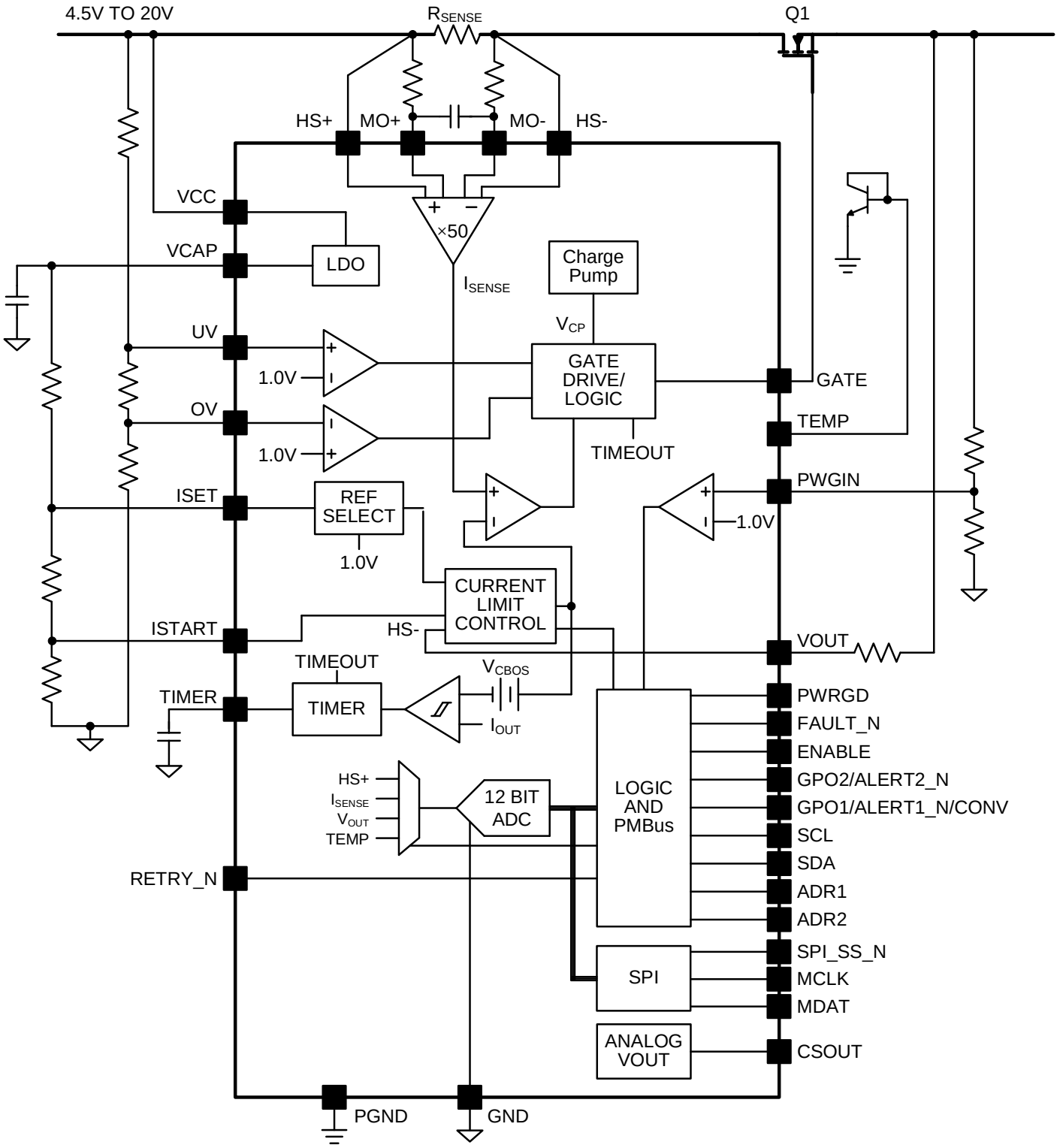


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC, FAULT_N, ENABLE, GPO1/ALERT1_N/CONV, GPO2/ALERT2_N, PWRGD, VOUT, HS+, HS, MO+, MO-	-0.3	25	V
UV, OV, ISTART, VCAP, ISET, RETRY_N, PWGIN, SPI_SS_N, MCLK, MDAT	-0.3	4	
TIMER, TEMP	-0.3	VCAP + 0.3	
SCL, SDA, ADR1, ADR2	-0.3	6.5	
GATE (Internal Supply Only) (Note 6)	-0.3	36	
PGND	-0.3	0.3	
V_{SENSE_HS} (V_{HS+}− V_{HS-})	-0.3	0.3	
V_{SENSE_MO} (V_{MO+}− V_{MO-})	-0.3	0.3	
CSOUT Short-Circuit Duration	Indefinite		
Continuous Current into Any Pin	-10	10	mA
Lead Temperature (Soldering, 10 sec.)		300	°C
Junction Temperature, Operating	-40	105	
Storage Temperature	-65	125	
Operating Temperature	-40	85	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	25	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	16.9	
P_D Power Dissipation T_A = 25°C	4	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC, VOUT	4.5	20	V
Ambient Temperature	-40	85	°C

Electrical Characteristics

(V_{CC} = 4.5V to 20V, $V_{CC} \geq V_{HS+}$ and V_{MO+}, V_{HS+} = 2V to 20V, $V_{SENSE\_HS} = (V_{HS+} - V_{HS-}) = 0V$, T_A = −40°C to +85°C, unless otherwise specified (Note 4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Operating Voltage Range	V_{CC}		4.5		20	V
UVLO	V_{UVLO_VCC}	V_{CC} Rising	2.3		3	V
UVLO Hysteresis	$V_{UVLO\_VCC,hyst}$	Hysteresis		200	400	mV
Quiescent Current	I_{CC}	GATE on and power monitor running			5.5	mA
UV Pin						
Input Current	I_{UV}	UV ≤ 3.6V			50	nA
UV Threshold	UV_{TH}	UV falling	0.99	1.0	1.01	V
UV Threshold Hysteresis	UV_{HYST}		45	60	75	mV
UV Glitch Filter (Note 5)	UV_{GF}	50mV overdrive	2		7	µs
UV Propagation Delay	UV_{PD}	UV low to GATE pull-down active		5	10	µs
OV Pin						
Input Current	I_{OV}	OV ≤ 3.6V			50	nA
OV Threshold	OV_{TH}	OV rising	0.99	1.0	1.01	V
OV Threshold Hysteresis	OV_{HYST}		45	60	75	mV
OV Glitch Filter (Note 5)	OV_{GF}	50mV overdrive	1.5		3.5	µs
OV Propagation Delay	OV_{PD}	OV high to GATE pull-down active		3	6	µs
HS+ And HS- Pins						
Input Current	I_{SENSEx}	Per individual pin: V_{HS+}, V_{HS-} = 20V		135		µA
Input Imbalance	$I_{\Delta SENSE}$	$I_{\Delta SENSE} = (I_+ - I_-)$	-8		8	µA
MO+ And MO- Pins						
Input Current	$I_{MO\pm}$	Per individual pin: V_{MO+}, V_{MO-} = 20V			30	µA
VCAP Pin						
Internally Regulated Voltage	V_{VCAP}	0µA ≤ I_{VCAP} ≤ 100µA; C_{VCAP} = 1µF	2.68	2.7	2.72	V
ISET Pin						
Reference Select Threshold	$V_{ISETRSTH}$	If $V_{ISET} > V_{ISETRSTH}$, an internal 1V reference (V_{CLREF}) is used	1.35	1.5	1.65	V
Internal Reference	V_{CLREF}	Accuracies included in total sense voltage accuracies		1		V
Gain of Current Sense Amplifier	AV_{CSAMP}	Accuracies included in total sense voltage accuracies		50		V/V
Recommended Maximum Operating Range	V_{ISET}	5mV to 25mV V_{SENSE} current limit	0.25		1.25	V
Input Current	I_{ISET}	$V_{ISET} \leq V_{VCAP}$			100	nA
GATE Pin						
GATE Drive Voltage	ΔV_{GATE}	Maximum voltage on the gate is always clamped to ≤31V $\Delta V_{GATE} = V_{GATE} - V_{OUT}$				
		20V ≥ V_{CC} ≥ 8V; I_{GATE} ≤ 5µA	10	12	14	V
		V_{HS+} = V_{CC} = 5V; I_{GATE} ≤ 5µA	8		14	V
		V_{HS+} = V_{CC} = 4.5V; I_{GATE} ≤ 1µA	7		14	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
GATE Pull-Up Current	I_{GATEUP}	V_{GATE} = 0V	-20		-30	μA
GATE Pull-Down Current	I_{GATEDN}					
Regulation	I_{GATEDN_REG}	V_{GATE} ≥ 2V; V_{ISET} = 1.0V. (V_{HS+} − V_{HS-}) = 30mV	45	60	75	μA
Slow	I_{GATEDN_SLOW}	V_{GATE} ≥ 2 V	5	10	15	mA
Fast	I_{GATEDN_FAST}	V_{GATE} ≥ 12V; V_{CC} ≥ 12V	600	1500	2250	mA
GATE Hold-off Resistance		V_{CC} = 0V, V_{GATE} = 2V		100		Ω
HOT SWAP SENSE VOLTAGE						
Hot Swap Sense Voltage Current Limit	$V_{SENSECL}$	V_{ISET} > 1.65V; V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0μA	19.75	20	20.25	mV
Normal Current Limit		V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0μA; V_{DS} = (HS−) −V_{OUT}				
		V_{ISET} = 1.25V	24.75	25	25.25	mV
		V_{ISET} = 1.0V	19.75	20	20.25	mV
		V_{ISET} = 0.75V	14.75	15	15.25	mV
Start-Up Current Limit	$V_{ISTARTCL}$	STRT_UP_IOUT_LIM = 3; V_{ISET} > 1.65V	4.7	5	5.3	mV
		V_{ISTART} = 0.2V	3.7	4	4.3	mV
Start-Up Current-Limit Clamp	$V_{ISTARTCL\_CLAMP}$	V_{ISTART} = 0V or STRT_UP_IOUT_LIM = 0	1.6	2	2.4	mV
Circuit Breaker Offset	V_{CBOS}	Circuit breaker trip voltage, V_{CB} = $V_{SENSECL}$ − V_{CBOS}	0.3	0.88	1.5	mV
SEVERE OVERCURRENT						
Voltage Threshold	$V_{SENSEOC}$	V_{ISET} > 1.65V; optional select PMBus (125%)	23	25	27	mV
		V_{ISET} > 1.65V; optional select PMBus (150%)	28	30	32	mV
		V_{ISET} > 1.65V; optional select PMBus (200%)	38	40	42	mV
		V_{ISET} > 1.65V; default at power-up (225%)	43	45	47	mV
Short Glitch Filter Duration (Note 5)		V_{SENSE_HS} step = 18mV to (2mV above $V_{SENSEOC\_MAX}$)	100		220	ns
Long Glitch Filter Duration (Note 5)		V_{SENSE_HS} step = 18mV to (2mV above $V_{SENSEOC\_MAX}$)	530		900	ns
Short Glitch Filter Response Time		V_{SENSE_HS} step = 18mV to (2mV above $V_{SENSEOC\_MAX}$)	100		350	ns
Long Glitch Filter Response Time		V_{SENSE_HS} step = 18mV to (2mV above $V_{SENSEOC\_MAX}$)	350		1200	ns
ISTART Pin						
Active Range		Tie ISTART to VCAP to disable start-up current limit	0.1		1.25	V
Gain of Current Sense Amplifier	AV_{CSAMP}	Accuracies included in total sense voltage accuracies		50		V/V
Input Current	I_{START}	V_{ISTART} ≤ V_{VCAP}			100	nA
TIMER Pin						
TIMER Pull-Up Current						
Power-On Reset (POR)	$I_{TIMERUPPOR}$	Initial power-on reset; V_{TIMER} = 0.5V	-2	-3	-4	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Overcurrent (OC) Fault	$I_{TIMERUPFLT}$	Overcurrent fault; 0.2V ≤ V_{TIMER} ≤ 1V	-57	-60	-63	µA
TIMER Pull-Down Current						
Retry	$I_{TIMERDNRT}$	After fault when GATE is off; V_{TIMER} = 0.5V	1.7	2	2.3	µA
Hold	$I_{TIMERDNHOLD}$	Holds TIMER at 0 V when inactive; V_{TIMER} = 0.5V		100		µA
TIMER High Threshold	V_{TIMERH}	Test at overcurrent fault condition	0.97	1.0	1.02	V
TIMER Low Threshold	V_{TIMERL}	Test at overcurrent fault condition	0.18	0.2	0.22	V
TIMER Glitch Filter	$TIMER_{GF}$			10		µs
Minimum POR Duration		Minimum initial insertion delay regardless of C_{TIMER} value		27		ms
VOUT Pin						
Input Current					40	µA
FAULT_N Pin						
Output Low Voltage	V_{OL_LATCH}	I_{FAULT} = 1mA			0.4	V
		I_{FAULT} = 5mA			1.5	V
Leakage Current		V_{FAULT} ≤ 2V; FAULT_N output high-Z			100	nA
		V_{FAULT} = 20V; FAULT_N output high-Z			1	µA
ENABLE Pin						
Input High Voltage	V_{IH}		1.1			V
Input Low Voltage	V_{IL}				0.8	V
Glitch Filter (Note 5)				1		µs
RETRY_N Pin						
Input High Voltage	V_{IH}	Latch off when high; internal pull-up sets this as the default	1.1			V
Input Low Voltage	V_{IL}	10-second automatic retry when pin pulled low			0.8	V
Glitch Filter (Note 5)				1		µs
Internal Pull-Up Current				8		µA
CSOUT Pin						
CSOUT Gain		CSOUT = V_{SENSE_HS} × 350; VCC > CSOUT + 2V		350		V/V
Total Output Error		V_{SENSE_HS} = 20mV; C_{CSOUT} = 1nF; I_{CSOUT}=0mA	-4		+4	%
		V_{SENSE_HS} = 10mV; C_{CSOUT} = 1nF; I_{CSOUT}=0mA	-8		+8	%
Output Swing to GND				40		mV
Current Limiting		CSOUT short-circuit current		1		mA
GPO1/ALERT1_N/CONV Pin						
Output Low Voltage	V_{OL_GPO1}	I_{GPO1} = 1mA			0.4	V
		I_{GPO1} = 5mA			1.5	V
Leakage Current		V_{GPO1} ≤ 2V; GPO1 output high-Z			100	nA
		V_{CC}=20V; V_{GPO1} = 20V; GPO1 output high-Z			1	µA
Input High Voltage	V_{IH}	Configured as CONV	1.1			V
Input Low Voltage	V_{IL}	Configured			0.8	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Glitch Filter (Note 5)		Configured		1		µs
GPO2/ALERT2_N Pin						
Output Low Voltage	V_{OL_GPO2}	I_{GPO2} = 1mA			0.4	V
		I_{GPO2} = 5mA			1.5	V
Leakage Current		V_{GPO2} ≤ 2V; GPO2 output high-Z			100	nA
		V_{CC}=20V; V_{GPO2} = 20V; GPO2 output high-Z			1	µA
PWRGD Pin						
Output Low Voltage	V_{OL_PWRGD}	I_{PWRGD}= 1mA			0.4	V
		I_{PWRGD}= 5mA			1.5	V
VCC That Guarantees Valid Output		I_{SINK} = 100µA; V_{OL_PWRGD} = 0.4V	1.1			V
Leakage Current		V_{PWRGD} ≤ 2V; PWRGD output high-Z			100	nA
		V_{PWRGD} = 20V; PWRGD output high-Z			1	µA
PWGIN Pin						
Input Current	I_{PWGIN}	PWGIN ≤ 3.6V			50	nA
PWGIN Threshold	$PWGIN_{TH}$	PWGIN falling	0.99	1.0	1.01	V
PWGIN Threshold Hysteresis	$PWGIN_{HYST}$		50	60	70	mV
Glitch Filter (Note 5)		Asserting and deasserting of the PWRGD pin		1		µs
CURRENT AND VOLTAGE MONITORING		See Table 12 for power monitor accuracy specifications.				
ADC Conversion Time		Includes time for power multiplication				
		I_{OUT} sampling time, measured from the receipt of the command to valid data in the register		104		µs
		V_{IN} sampling time, measured from the receipt of the command to valid data in the register		52		µs
		V_{OUT} sampling time, measured from the receipt of the command to valid data in the register		52		µs
ADRx Pins						
Address Set to 00		Connected to GND	0		0.8	V
Input Current for Address Set to 00		V_{ADRx} = 0V to 0.8V	-40	-22		µA
Address Set to 01		Resistor to GND	135	150	165	kΩ
Address Set to 10		No connect state: maximum allowable leakage current	-1		+1	µA
Address Set to 11		Connected to VCAP	2			V
Input Current for Address Set to 11		V_{ADRx} = 2.0V to VCAP. Must not exceed the maximum allowable current draw from VCAP		3	10	µA
TEMP Pin		External transistor is MMBT3904				
Operating Range		Limited by external diode	-55		+150	℃

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Accuracy (Note 5)		$T_A = T_{DIODE}$ = −40℃ to +85℃		±3.6		℃
Resolution (Note 5)		LSB size		0.25		℃
Output Current Source						
Low Level				5		μA
Medium Level				30		μA
High Level				105		μA
Maximum Series Resistance for External Diode	R_S	For < ±0.5℃ additional error, C_P = 0F			100	Ω
Maximum Parallel Capacitance for External Diode	C_P	R_S = 0Ω			1	nF
SPI DIGITAL INPUTS (SPI_SS_N, MCLK, MDAT)						
Compatible with SPI Mode 0. MDAT is the output data pin and is high impedance when not transmitting.						
Input High Voltage	V_{IH}		1.25			V
Input Low Voltage	V_{IL}				0.45	V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Leakage	$I_{LEAK-PIN}$				1	μA
Data Rate					1	MHz
SERIAL BUS DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}		1.25			V
Input Low Voltage	V_{IL}				0.45	V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Leakage	$I_{LEAK-PIN}$		-10		+10	μA
		Device is not powered	-5		+5	μA
Nominal Bus Voltage	V_{DD}	3V to 5V ± 10%	2.7		5.5	V
Capacitance for SDA, SCL Pins (Note 5)	C_{PIN}			5		pF
Input Glitch Filter (Note 5)	t_{SP}		0		50	ns

Power Monitoring Accuracy Specifications

(V_{CC} = V_{MO+} = 12V, 128-sample averaging, unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Current Sense Absolute Error	V_{SENSE_MO} = 25mV			±0.6	%
	V_{SENSE_MO} = 20mV		±0.04	±0.7	
	V_{SENSE_MO} = 20mV; 16-sample averaging			±1	
	V_{SENSE_MO} = 20mV; one-sample averaging			±2.2	
	V_{SENSE_MO} = 15mV			±0.8	
	V_{SENSE_MO} = 10mV			±1.1	
	V_{SENSE_MO} = 5mV			±2	
	V_{SENSE_MO} = 2.5mV			±4.3	
HS+/VOUT Absolute Error	V_{HS+}, V_{OUT} = 10V to 20V			±0.6	
	V_{HS+}, V_{OUT} = 5V			±1	
Power Absolute Error	V_{SENSE_MO} = 20mV, V_{HS+} = 12V			±1.3	

Serial Bus Timing Characteristics

(Figure3, Note 7)

Parameter	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{SCLK}			1000	kHz
Bus Free Time	t_{BUF}	0.5			μs
Start Hold Time	$t_{HD;STA}$	0.26			μs
Start Setup Time	$t_{SU;STA}$	0.26			μs
Stop Setup Time	$t_{SU;STO}$	0.26			μs
SDA Hold Time	$t_{HD;DAT}$	300		900	ns
SDA Setup Time	$t_{SU;DAT}$	50			ns
SCL Low Time	t_{LOW}	0.5			μs
SCL High Time	t_{HIGH}	0.26			μs
SCL, SDA Rise Time (Note 7)	t_R (t_R = ($V_{IL(MAX)}$ − 0.15) to (V_{IH3V3} + 0.15), V_{IH3V3} = 2.1V, V_{DD} = 3.3V)	20		120	ns
SCL, SDA Fall Time (Note 7)	t_F (t_F = 0.9 V_{DD} to ($V_{IL(MAX)}$ − 0.15), V_{IH3V3} = 2.1V, V_{DD} = 3.3V)	20		120	ns

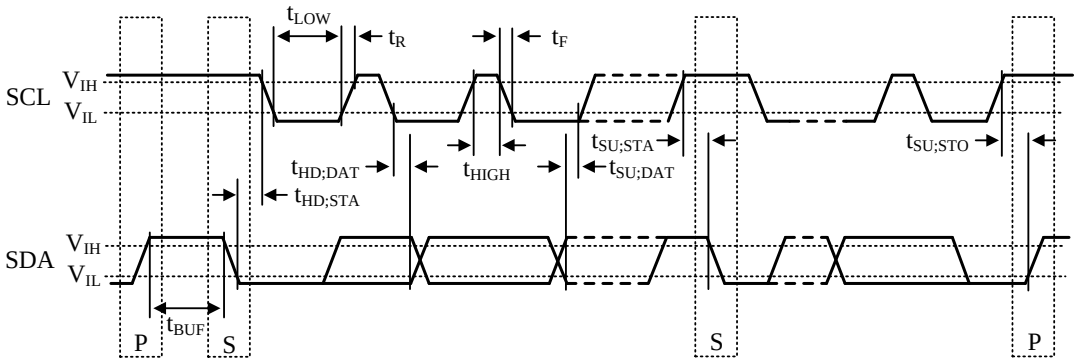


Figure 3. Serial Bus Timing Diagram

SPI Timing Characteristics

(Figure 4, Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SPI_SS_N Falling Edge to MCLK Rising Edge Setup Time (Note 5)	t_S		50			ns
MCLK High Time (Note 5)	t_{HIGH}		180			ns
MCLK Low Time (Note 5)	t_{LOW}		180			ns
MCLK Cycle Time (Note 5)	t_{CLK}		1			µs
Hold Time Between SPI_SS_N and MCLK (Note 5)	t_H		1			µs
Hold Time Between New Data Valid and MCLK Falling Edge	t_V	Track capacitance = 120pF; I_{OL} = 4mA	110		260	ns
SPI_SS_N Falling Edge to MDAT Active Time	t_{ON}	Track capacitance = 120pF; I_{OL} = 4mA	130		240	ns
Bus Relinquish Time after SPI_SS_N Rising Edge	t_{OFF}	Track capacitance = 120pF; I_{OL} = 4mA	130		280	ns

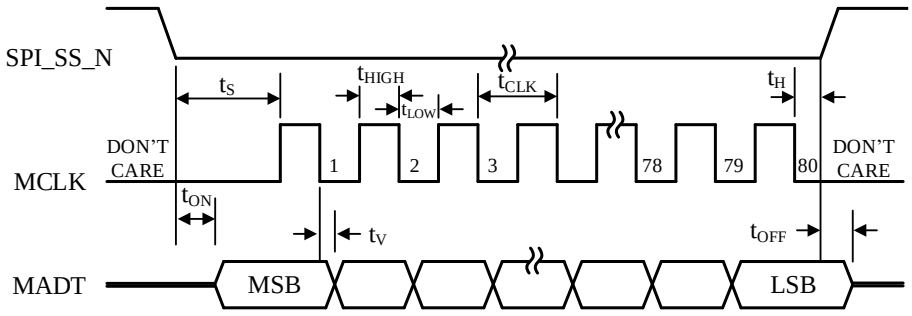


Figure 4. SPI Timing Diagram

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at T_A = 25°C on a Silergy test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

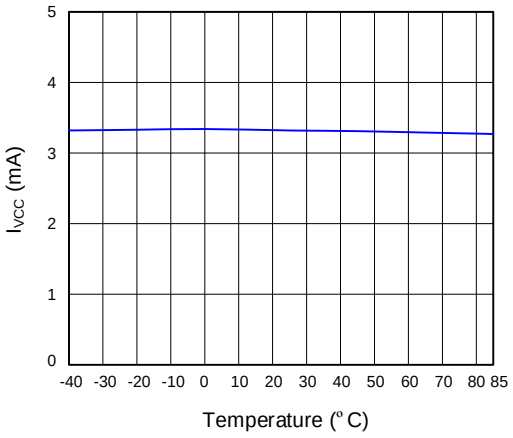
Note 6: The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with gate-to-source voltage, VGSMAX = 20V, and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Note 7: V_{IH3V3} is the input high voltage when V_{DD} = 3.3V

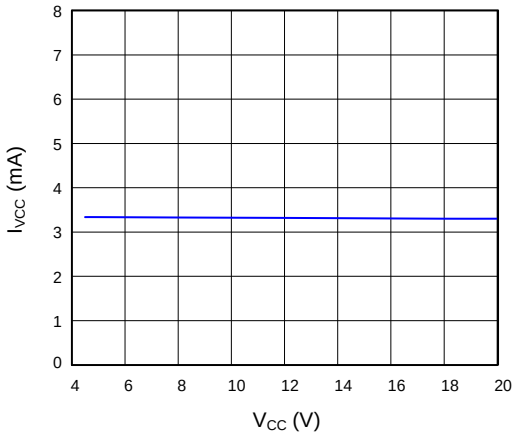
Typical Performance Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified.)

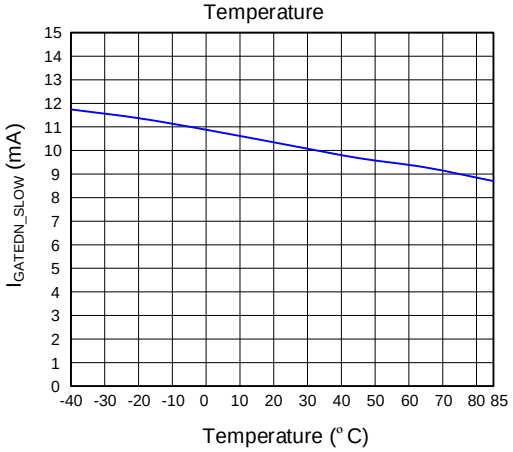
Supply Current (I_{VCC}) vs. Temperature



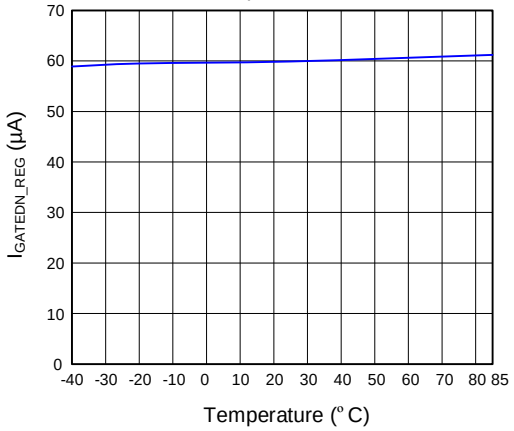
Supply Current (I_{VCC}) vs. V_{CC}



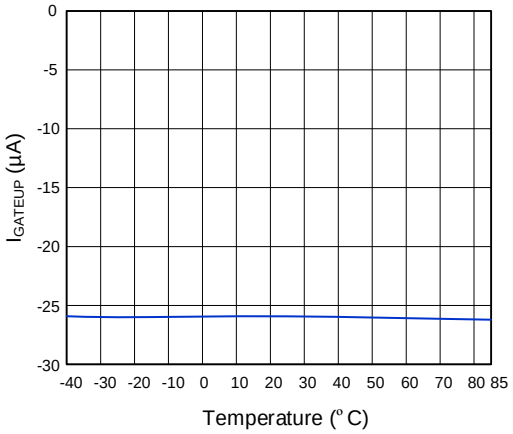
GATE Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature



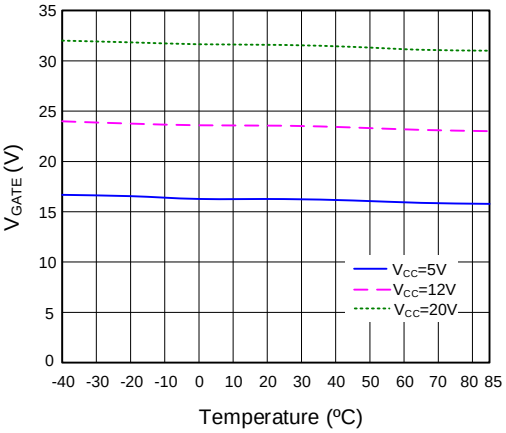
GATE Pull-Down Current (I_{GATEDN_REG}) vs. Temperature



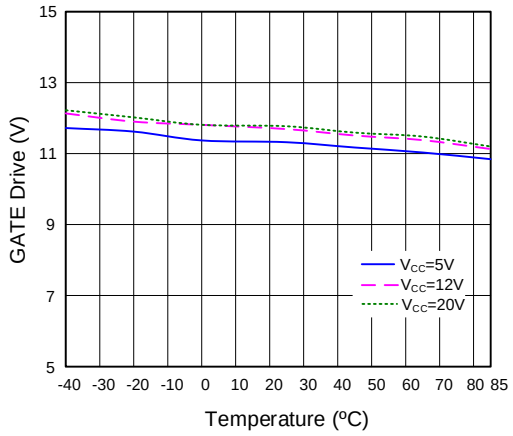
GATE Pull-Up Current (I_{GATEUP}) vs. Temperature



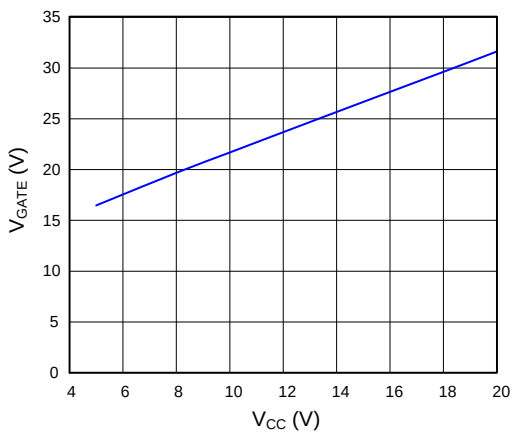
V_{GATE} (5µA Load) vs. Temperature



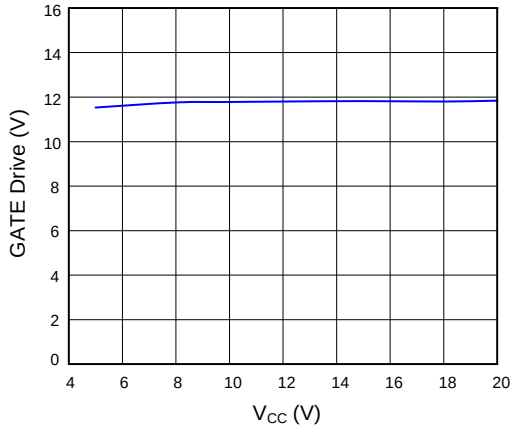
GATE Drive (5μA Load) vs. Temperature



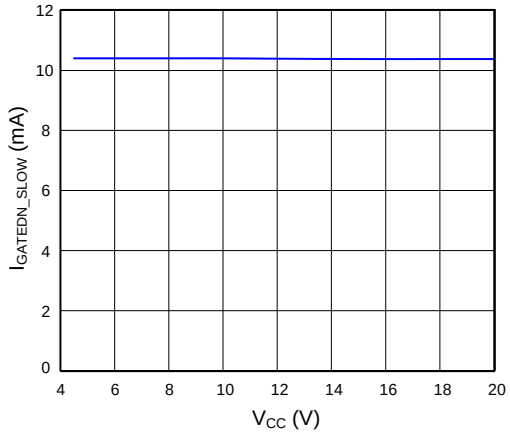
V_{GATE} (5μA Load) vs. VCC



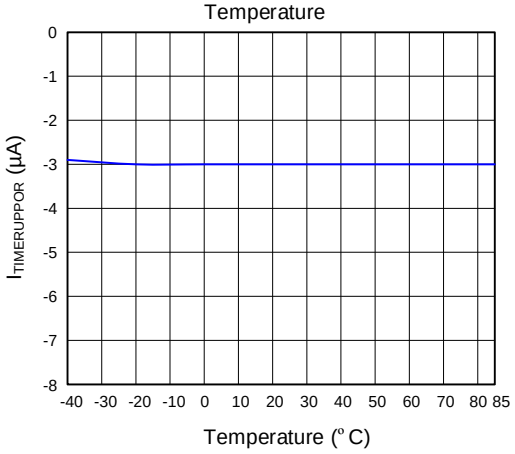
GATE Drive vs. VCC



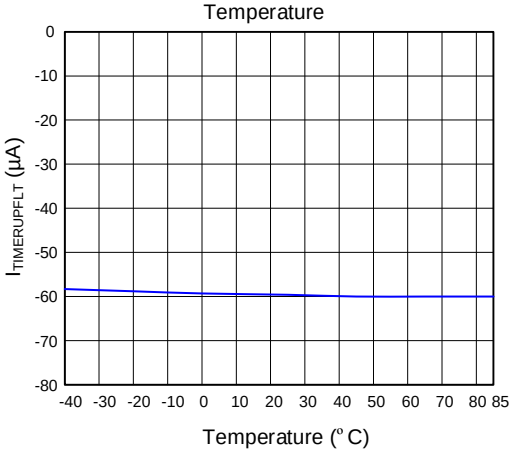
I_{GATEDN_SLOW} vs. VCC



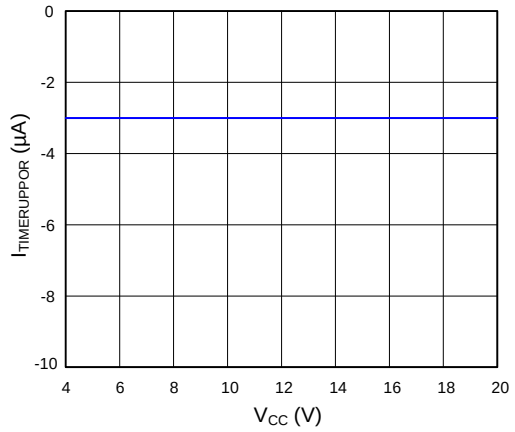
TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs. Temperature



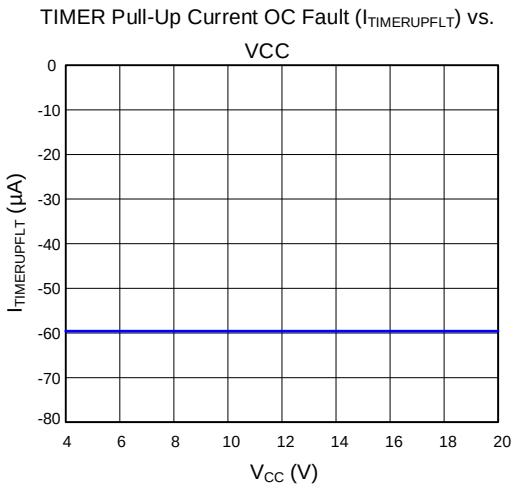
TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs. Temperature



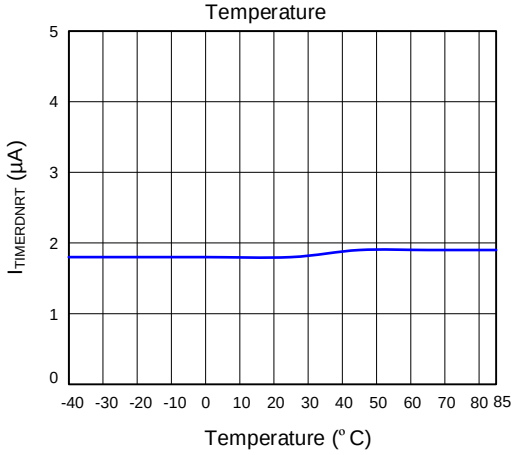
TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs. VCC



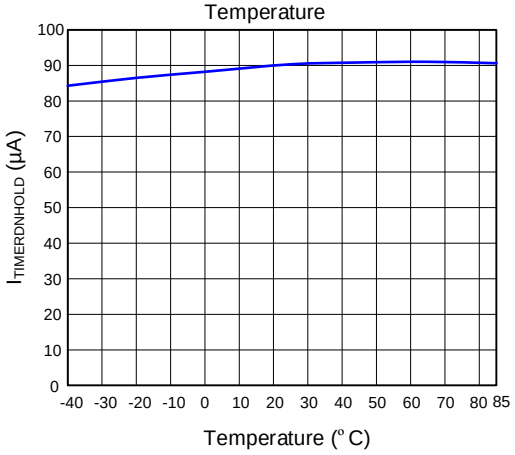
TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs. VCC



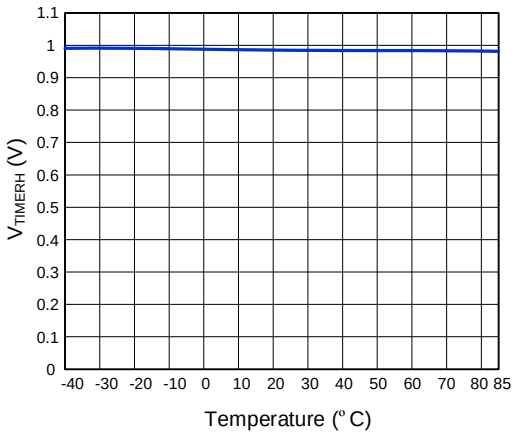
TIMER Pull-Down Current Retry ($I_{TIMERDNRT}$) vs. Temperature



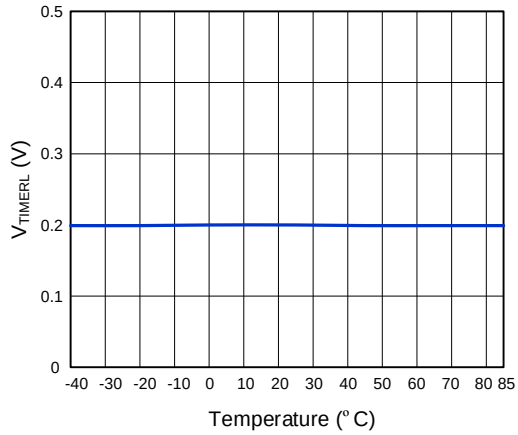
TIMER Pull-Down Current Hold ($I_{TIMERDNHOLD}$) vs. Temperature



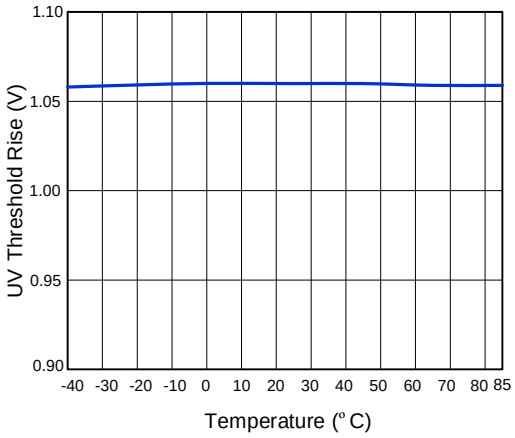
TIMER High Threshold (V_{TIMERH}) vs. Temperature



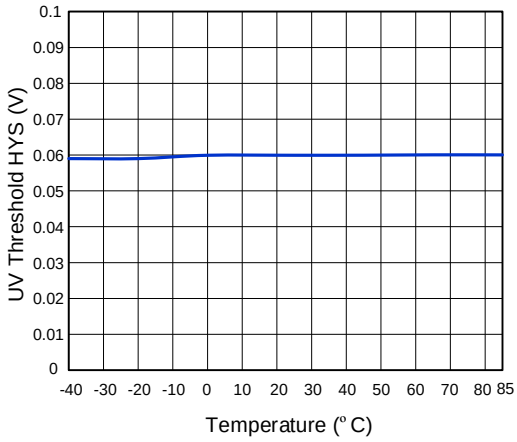
TIMER Low Threshold (V_{TIMERL}) vs. Temperature



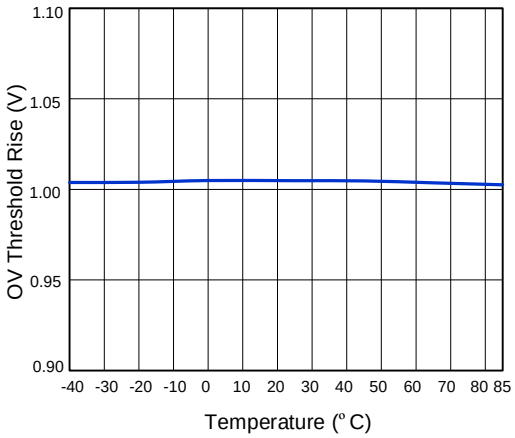
UV Threshold vs. Temperature



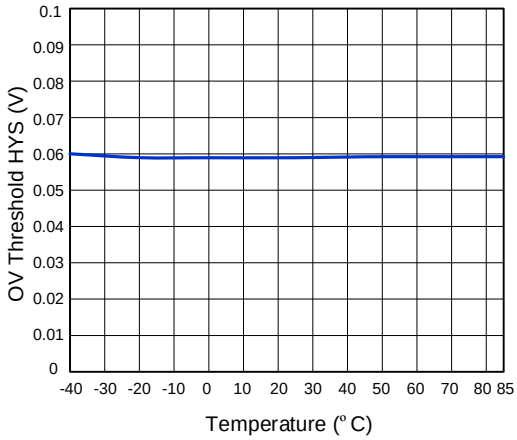
UV Hysteresis vs. Temperature



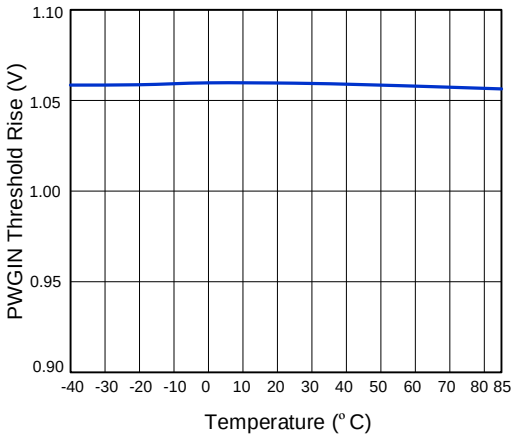
OV Threshold vs. Temperature



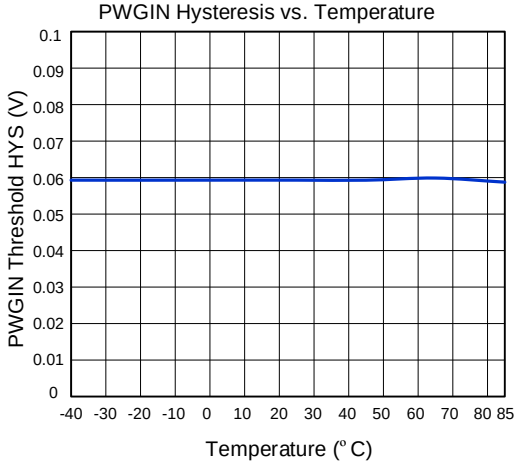
OV Hysteresis vs. Temperature



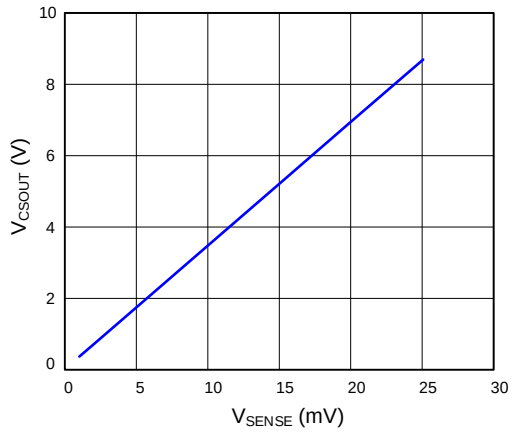
PWGIN Threshold vs. Temperature



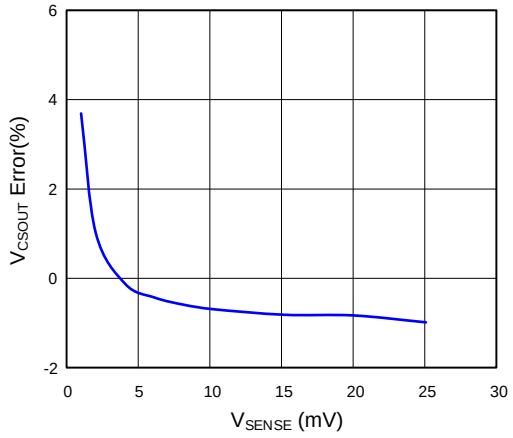
PWGIN Hysteresis vs. Temperature



CSOUT Voltage vs. V_{SENSE}

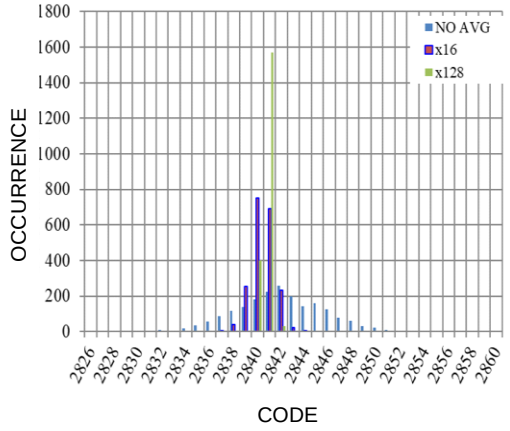


CSOUT Error vs. VSENSE

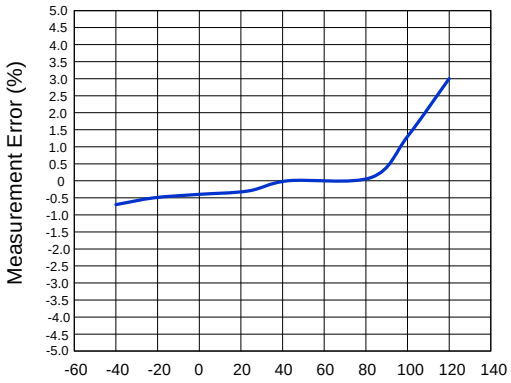


ADC Code Histogram

(V_{SENSE} = 10 mV, 2000 Measurements)

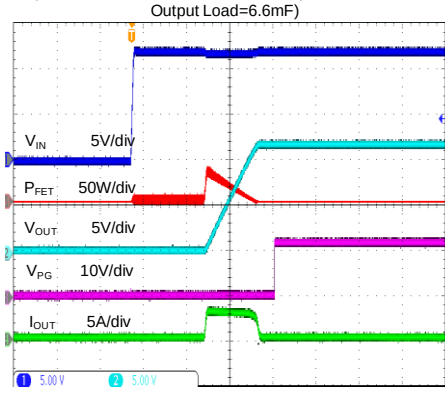


Measurement Error vs. External Transistor Temperature



Power Up Test

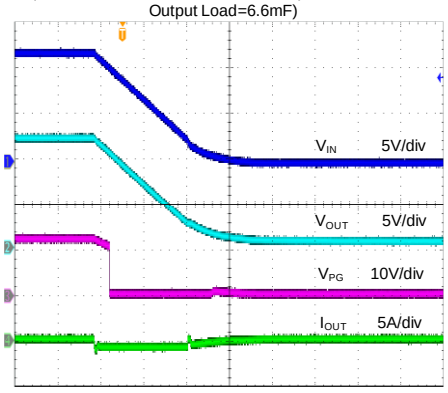
(V_{IN}=12V, R_{SENSE}=0.25mΩ, C_{TIMER}=22μF, C_{GATE}=47nF, Output Load=6.6mF)



Time (20ms/div)

Power Down Test

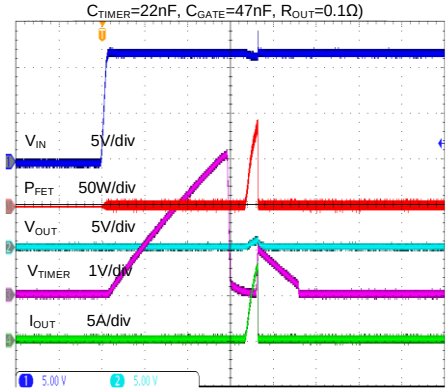
(V_{IN}=12V, R_{SENSE}=0.25mΩ, C_{TIMER}=22μF, C_{GATE}=47nF, Output Load=6.6mF)



Time (20ms/div)

Power Up With Overload

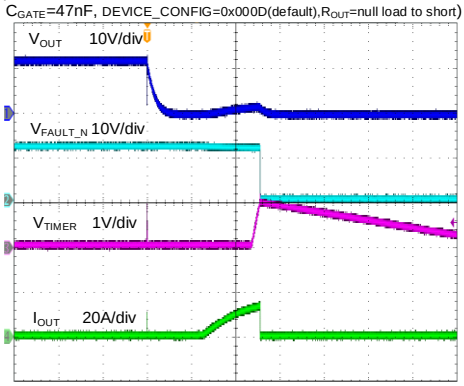
(V_{IN}=12V, R_{SENSE}=0.25mΩ, V_{ISET}=1V, V_{ISTART}=0.2V, C_{TIMER}=22nF, C_{GATE}=47nF, R_{OUT}=0.1Ω)



Time (10ms/div)

Hard short Test

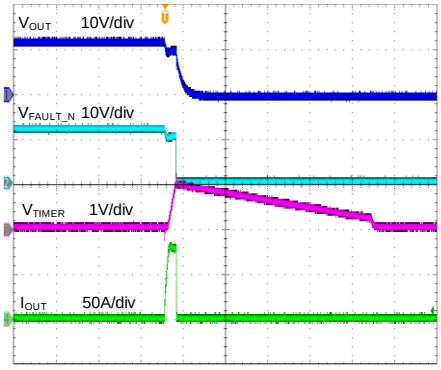
(V_{IN}=12V, R_{SENSE}=0.25mΩ, V_{ISET}=1V, V_{ISTART}=0.2V, C_{TIMER}=22nF, C_{GATE}=47nF, DEVICE_CONFIG=0x000D(default),R_{OUT}=null load to short)



Time (4ms/div)

Current Limit during Normal Operation

(V_{IN}=12V, R_{SENSE}=0.25mΩ, V_{ISET}=1V, V_{ISTART}=0.2V, C_{TIMER}=22nF, C_{GATE}=47nF, R_{OUT}=null load to 0.1Ω)



Time (4ms/div)

Application Information

The SQ24905C can be mounted on either the backplane or a removable board. It controls the system power supply with a current limit, allowing a board to be safely removed from or inserted into a live backplane.

Power Supply

The required supply voltage range of SQ24905C is 4.5V to 20V.

The VCC pin voltage should be equal to the voltages at the HS+ and MO+ pins to ensure proper operation of the device. The HS+ pin can operate normally with voltages equal to or greater than 2V, provided the VCC pin is at least 4.5V. It is recommended to connect the VCC and HS+ pins to the same voltage rail, but through separate traces, to prevent loss of accuracy in the current sense voltage measurement (refer to Figure 5).

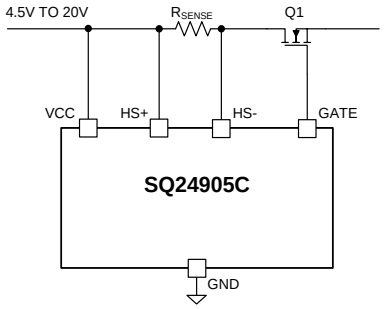


Figure 5. Powering the SQ24905C

Current Sense Inputs

The internal ADC has separate input pins for measuring load current and for hot swap circuitry. This allows extra filtering on the power monitor pins without affecting the response time to an overcurrent event.

Schematic diagrams showing configurations without and with external filtering are shown in Figure 6 and Figure 7, respectively.

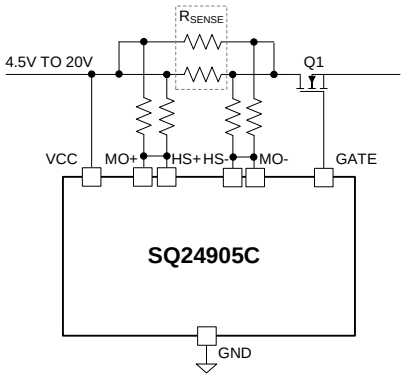


Figure 6. Power Monitor, No External Filtering

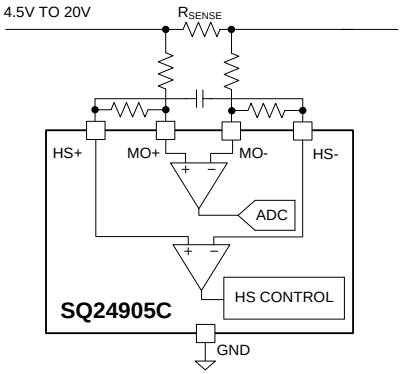


Figure 7. Power Monitor Current Sense Filtering

Current Limit Reference Selection

The ISET and ISTART current limit reference voltages determine the active current limit level during an overcurrent event. ISET is used during normal operation, while ISTART is used during startup or fault conditions.

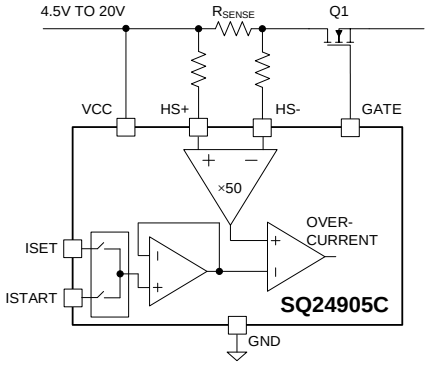


Figure 8. Current-Limit Reference Selection

The start-up current limit voltage input to the internal comparator is clamped to 100mV ($V_{SENSECL}$=2mV) to prevent almost zero current flow due to excessively low voltage at the ISTART pin. Figure 9 illustrates how ISTART and ISET voltages interact during startup.

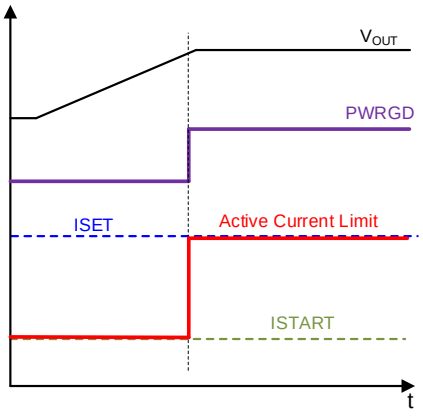


Figure 9. Interaction of ISTART and ISET Current Limits

After VOUT short to GND quickly, IC will retry once. The lower of ISTART and ISET pin voltage determines the active current limit during this retry time. It can also be configured to latch after the VOUT short event by using the PMBus register (DEVICE_CONFIG, 0xD8[1]: OC_RETRY_DIS).

Current Limit Setting for Normal Operation (ISET)

The SQ24905C allows the voltage of the ISET pin to be adjusted to set the current limit. A resistor divider is required to set a reference voltage on the ISET pin to program the limited sense voltage, as shown in Figure 10. VCAP can be used as a 2.7V pull-up supply to the resistor divider. The VCAP can also be used for setting other pins but should not be loaded by more than 100μA.

If the ISET pin voltage exceeds approximately 1.5V, an internal 1V reference will be used, resulting in a default current sense limit value of 20mV. The simplest method to achieve this fixed 20mV current sense limit is by connecting the ISET pin to the VCAP pin, as shown in Figure 11.

Set the ISET voltage as follows:

$$V_{ISET} = V_{SENSCL} \times 50$$

Where: $V_{SENSECL}$ is the current sense voltage limit

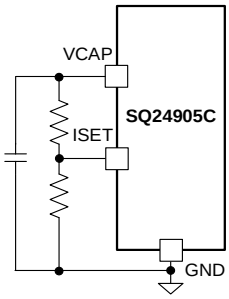


Figure 10. Adjustable Current Sense Limit

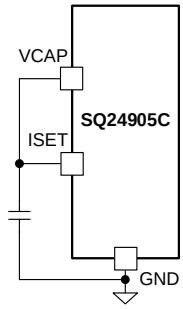


Figure 11. Fixed 20 mV Current Sense Limit

Current Limit Setting for Start-up (ISTART)

The start-up current limit is only active during start up. It is enabled while PWRGD is deasserted and is disabled when PWRGD is asserted. It can be programmed via the ISTART pin or PMBus register (STRT_UP_IOUT_LIM, 0xF6 [3:0]). If both are configured, the lower value will be selected as the active limit. The clamp level in both scenarios is a 2mV current sense limit. If configured with the ISTART pin, the start-up current limit is:

$$I_{STARTUP\_CL} = \frac{V_{ISTART}}{R_{SENSE} \times 50}$$

At the same time, the circuit breaker level is:

$$I_{STARTUP\_CB} = \frac{\frac{V_{ISTART}}{50} - 0.88mV}{R_{SENSE}}$$

To avoid triggering the start-up current limit during normal power-up, set the circuit breaker level higher than the maximum expected inrush current. The ISTART pin can be connected to VCAP to disable the start-up current limit. The PMBus register start-up current limit value is set to the maximum by default.

When configuring the start-up current limit using the PMBus register, the value is calculated as a fraction of the ISET current limit. Using four register bits, the start-up current limit can be adjusted from 1/16th to 16/16th of the normal current limit (set by ISET).

If configured using PMBus, the ISTART voltage is:

$$V_{STARTUP\_CL} = \left(\frac{START\_UP\_IOUT\_LIM + 1}{16}\right) \times V_{ISET}$$

The start-up circuit breaker and current limits can be calculated based on the effective ISTART voltage.

Setting Soft Start at Start-up

The SQ24905C enables a linear voltage ramp on the output during the startup phase to reduce inrush currents. It is important to verify that the dissipated MOSFET power in the meets the safe operating area (SOA) requirements. For this function, an extra component, C_{GATE}, is required on the GATE pin, as shown in Figure 12.

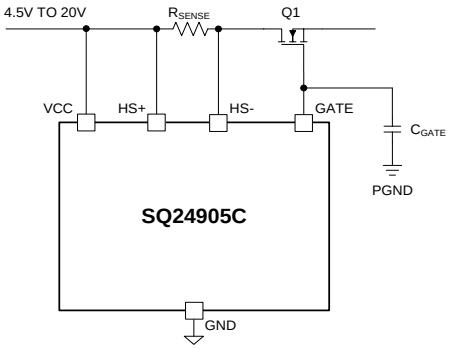


Figure 12. DV/DT Power-Up Configuration

To prevent inrush current from reaching or exceeding the active current-limit level, set the output voltage ramp by selecting the appropriate CGD value.

$$C_{GATE} = C_{LOAD} \times \frac{I_{GATEUP}}{I_{INRUSH}}$$

Where: I_{GATEUP} is the gate pull-up current specified and C_{LOAD} is the total output capacitance.

Add extra margin and account for tolerances to ensure that the target is met across all the operating conditions. Subtract the datasheet MOSFET C_{GD} value to obtain the external capacitance required.

The start-up ramp time can be approximated by:

$$t_{RAMP} = \frac{V_{IN} \times C_{LOAD}}{I_{INRUSH}} = \frac{V_{IN} \times C_{GATE}}{I_{GATEUP}}$$

The Safe Operating Area (SOA) of the MOSFET should be considered when configuring the startup TIMER. A typical hot swap start-up scenario is illustrated in Figure 13, with the gate capacitor configured for linear output voltage ramp.

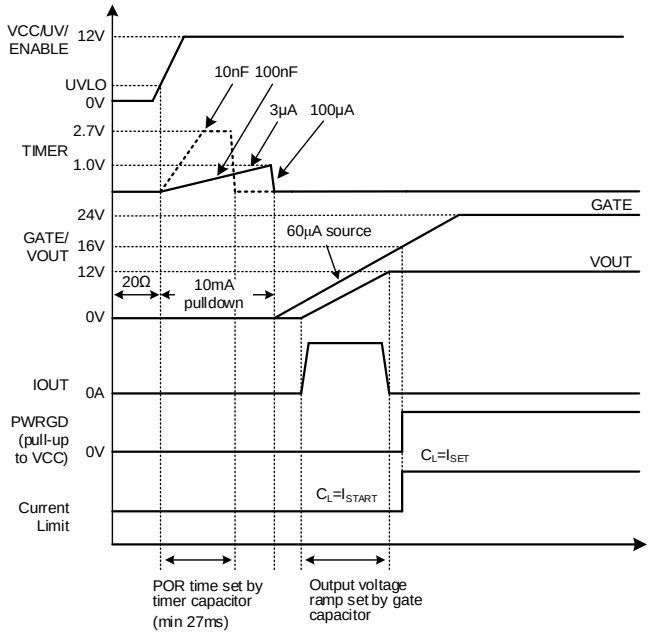


Figure 13. Linear Voltage Ramp Power-Up

TIMER

The TIMER pin controls timing functions with an external capacitor, C_{TIMER}. It has two comparator thresholds: V_{TIMERL} (0.2V) and V_{TIMERH} (1V). There are four timing constant current sources: a 3µA pull-up, a 60µA pull-up, a 2µA pull-down, and a 100µA pull-down.

The TIMER pin capacitor value is calculated using the following equation:

$$C_{TIMER} = \frac{t_{ON} \times 60\mu A}{V_{TIMERH}}$$

Where: tON is the time that MOSFET can regulate at the set current limit. The MOSFET selection is driven by its ability to meet the SOA requirements based on tON and maximum current.

The SQ24905C goes through an initial timing cycle, where a 3µA current pulls up the TIMER pin until it reaches the VTIMERH threshold (1.0V). After that, a 100µA current source pulls down the TIMER pin until it reaches VTIMERL (0.2V). The minimum duration for this cycle is approximately 27ms for MOSFET health checks. If the initial TIMER cycle is set shorter than 27ms by the TIMER capacitor, the TIMER pin will continue to be pulled up to the VCAP voltage level until the 27ms period has expired.

The duration of the initial timing cycle is determined by CTIMER using the following equation:

$$t_{INTTIAL} = Max\left\{\frac{C_{TIMER} \times V_{TIMERH}}{3\mu A} + \frac{C_{TIMER} \times (V_{TIMERH} - V_{TIMERL})}{3\mu A}, 27ms\right\}$$

When the sense resistor voltage reaches the circuit breaker trip voltage (VCB), a 60µA pull-up current activates, causing the TIMER pin to begin ramping up while the gate starts regulating the current at the current limit. If the sense voltage drops below the circuit breaker trip voltage before reaching V_{TIMERH}, the 60µA pull-up stops, and a 2µA pull-down is activated.

However, if the overcurrent situation persists and the sense voltage remains above the circuit breaker trip voltage, the 60µA pull-up current continues until the TIMER pin reaches the V_{TIMERH} threshold (1.0V). After that, a 2µA current source pulls down the TIMER pin until it reaches the V_{TIMERL} threshold (0.2V).

Note that the circuit breaker trip voltage differs from the hot swap sense voltage current limit by a small offset (V_{CBOS}). This means the TIMER pin starts ramping up slightly before the current reaches the defined current limit.

Hot Swap Retry

The RETRY_N pin configures the device to latch-off or enter auto-retry mode after an overcurrent fault. It has an internal current source. Leaving the pin floating will activate latch-off mode. Connect to GND to activate a 10-second auto-retry mode.

MOSFET Gate Driver

The charge pump on the GATE pin can drive this pin to (VCC+12V) to avoid exceeding the MOSFET's VGS maximum rating.

Fast Response to Severe Overcurrent

The SQ24905C includes a high bandwidth current sense amplifier designed to detect severe overcurrent events, such as short circuits, and respond quickly to cut off output current within 1.2µs. The device provides four threshold options for severe overcurrent (ranging from 125% to 225%) and two glitch filter options for severe overcurrent, all selectable via the PMBus registers (DEVICE_CONFIG, 0xD8[3:2]:OC_TRIP_SELECT).

Undervoltage and Overvoltage (UV & OV)

The SQ24905C monitors supply voltage for undervoltage (UV) and overvoltage (OV) conditions using internal voltage comparators with a 1V reference. External resistor dividers connected to the UV and OV pins enable adjusting the thresholds as required by the application. A fixed 60mV hysteresis is applied to the UV and OV thresholds for stable operation.

When the voltage connected to the UV pin falls below 1V, an undervoltage event is detected, and a 10mA sink current shuts down the gate for the external MOSFET. Similarly, if the voltage at the OV pin exceeds 1V, indicating an overvoltage event, the gate is also shut down by the same 10mA pull-down current.

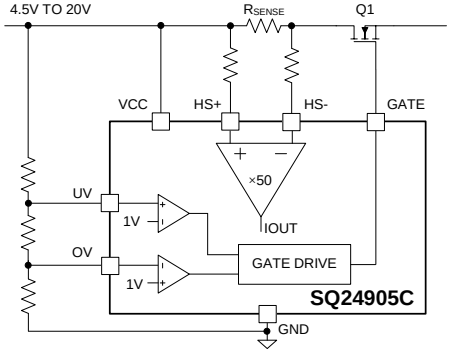


Figure 14. Undervoltage and Overvoltage Supply Monitoring

Power Good

The power-good (PWRGD) output indicates whether the output voltage is above a user-defined threshold. A resistor divider on the PWGIN pin sets an accurate power-good threshold relative to the output voltage. The PWRGD pin is an open-drain output that pulls low when the voltage at the PWGIN pin is below 1.0V. The PWRGD pin goes high when the voltage at the PWGIN pin is above this threshold (1.0V) plus a fixed hysteresis of 60mV.

PWRGD logic is shown in the following diagram:

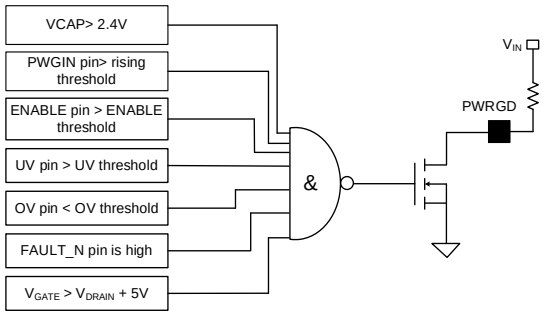


Figure 15. PWRGD Logic Diagram

The PWRGD pin is set to high impedance when all specified conditions are met and is valid for VCC ≥ 1.1V. If any PWRGD conditions are no longer met, it is immediately deasserted.

FAULT_N Pin

The FAULT_N pin is activated when any of the following three faults occur: MOSFET health fault, overcurrent fault, or overtemperature fault.

When the FAULT_N pin is latched by MOSFET health fault or overcurrent fault, it can only be cleared by one of the following actions, provided no faults are still active: a rising edge on the ENABLE pin, a PMBus OPERATION command from the off state, or a POWER_CYCLE command.

It's important to note that the fault registers can only be cleared by the PMBus OPERATION off-to-on command or the CLEAR_FAULTS command. The ENABLE pin or POWER_CYCLE command cannot clear them.

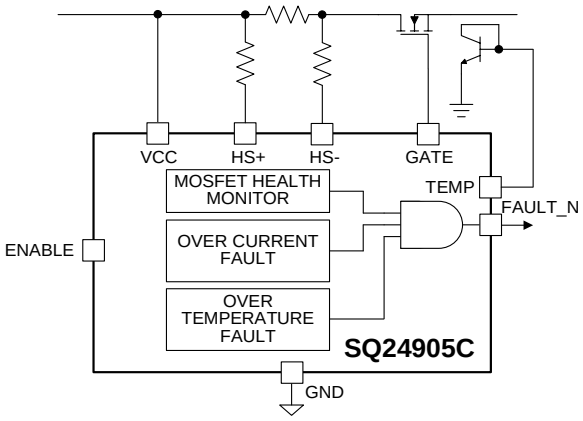


Figure 16. FAULT_N Pin Operation

Current Sense Output (CSOUT)

The SQ24905C offers a CSOUT pin voltage proportional to the V_{SENSE_HS} voltage:

$$V_{CSOUT} = V_{SENSE\_HS} \times 350$$

The CSOUT voltage represents the main system current flowing through RSENSE in analog form. To ensure accurate readings, the circuit connected to this pin has to offer a high input impedance. In the case where an ADC is used for monitoring, an operational amplifier connected as a not inverting buffer can be used. When this pin drives a comparator input, ensure that its input impedance is higher than 5MΩ.

The response time of the CSOUT pin to changes in VSENSE voltage is very fast, making it suitable for applications requiring quick response times, such as power throttling.

VOUT Measurement

The VOUT pin measures the output voltage after the MOSFET, determining the VDS of the MOSFET and calculating power loss at the MOSFET. This pin can also provide an alternate voltage for power monitoring. Users can measure either the input voltage at the HS+ pin or the output voltage at the VOUT pin.

MOSFET Health

The SQ24905C provides comprehensive detection of defective pass MOSFETs. It detects Gate-to-Source, Gate-to-GND, Gate-to-Drain or Drain-to-Source shorts event and Gate, Drain, Source opens event. Additionally, MOSFET health detection can be disabled via the PMBus register (DEVICE_CONFIG, 0xD8[11]: FHDIS).

MOSFET Health Logic diagram is shown below:

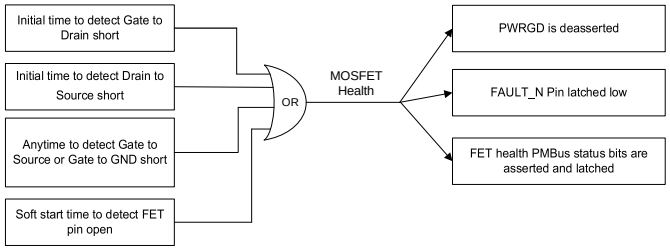


Figure 17. MOSFET Health Logic

Power Throttling

The SQ24905C can configure an alert pin for processor power throttling using the PMBus register (ALERT1_CONFIG, 0xD5[4]: HS_INLIM_EN1 or ALERT2_CONFIG, 0xD6[4]: HS_INLIM_EN2). A latched alert is triggered within a few microseconds after the output current exceeds the circuit breaker threshold. Subsequently, the processor can decrease the system current level below the circuit breaker threshold.

The CSOUT pin can also be used for power throttling. This pin can be connected to an input of a comparator (via a resistor divider) to program the analog threshold of the system current. The comparator's output can be utilized to throttle the processor once the set threshold is exceeded. It is important to consider the accuracy of the CSOUT pin when defining the power throttling threshold.

Power Monitor

The SQ24905C integrates an ADC to accurately measure the current sense voltage, input voltage, output voltage, and remote temperature using an external transistor. The measured input voltage and current are multiplied together to calculate the power value, which can be read back.

Commands like PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE can be used to read the highest value since the last reset.

The device provides an averaging function for voltage, current, and power. The number of samples that can be averaged is 2^N, where N ranges from 0 to 7, which is configured by PMbus register (PMON_CONFIG, 0xD4 [13:11] PWR_AVG and 0xD4[10:8] VI_AVG).

The power monitor has two basic operation modes: single shot and continuous. In single shot mode, the ADC samples the input voltage and current and returns a single value. In continuous mode, the power monitor continuously samples the voltage and current and provides the most recent sample value.

To trigger single-shot mode, select single-shot mode using the PMON_CONFIG (0xD4) command and the PMON_CONTROL (0xD3) command. The convert bit of the PMON_CONTROL command can be written as part of a PMBus group command, allowing multiple devices on the same I²C bus to be written in a single transaction. This enables all devices to execute the command simultaneously.

The input power can be read from the device using the READ_PIN command. Simultaneously, the calculated power value is added to a power accumulator register, and the power sample counter increments. If the value exceeds the maximum accumulator value, a rollover counter is incremented.

The power accumulator and power sample counter are both read using the READ_EIN command to ensure that the accumulated value and sample count are from the same time point. When reading the data, the bus host assigns a time stamp, calculates the time difference between consecutive uses of READ_EIN, and determines the delta power consumed.

Remote Temperature Sense

The SQ24905C can measure temperature remotely using a single discrete NPN or PNP transistor. The temperature value can be accessed via the PMBus. The temperature warning and fault thresholds can be set by PMBus registers. If a fault threshold is exceeded, the controller will shut off the MOSFET, deassert the PWRGD pin, and assert the FAULT_N pin.

The external transistor is usually positioned near the main pass MOSFET. If the transistor is placed on the opposite side of the PCB, use multiple vias to ensure optimal heat transfer from the MOSFET to the transistor.

The SQ24905C measures VBE change at three different currents, with the third current automatically canceling resistances in series with the external temperature sensor. It requires 25ms to obtain a new temperature measurement from the ADC. If filter mode is enabled by setting the TSFILT command (PMON_CONFIG, 0xD4[15]) to 1, the required time for data acquisition increases to 200ms.

The temperature sensor can be either a PNP or NPN transistor connected as a diode. For an NPN transistor, connect the collector and base to the TEMP pin and the emitter to PGND. For a PNP transistor, connect the collector and base to PGND and the emitter to TEMP. The best accuracy is achieved by selecting devices based on the following table. Transistors such as 2N3904 and 2N3906 in SOT-23 packages are suitable for use in most applications.

Table 1. Optimal Transistor Characteristics

NO.	Transistor Characteristics for Best Accuracy
1	At the highest operating temperature, the base-emitter voltage is greater than 0.25V at 6μA.
2	At the lowest operating temperature, the base-emitter voltage is less than 0.95V at 100μA.
3	Base resistance is less than 100Ω
4	Small variation in h_{FE} (50 to 150) indicates tight control of V_{BE} characteristics.

When RETRY_N is floating or connected to VCAP, the FAULT_N pin will be latched after over temperature fault. The FAULT_N can only be cleared by one of the following actions, provided over temperature fault is NOT active: a rising edge on the ENABLE pin, a PMBus OPERATION command or a POWER CYCLE command from the off state.

Noise Filtering

Temperature sensors often need a capacitor across the temperature pins to reduce noise in noisy environments. However, large capacitances can affect accuracy, so using a maximum capacitor value of 1000pF is recommended. Figure 18 illustrates a low-pass R-C-R filter with values of R=100Ω and C =1nF.

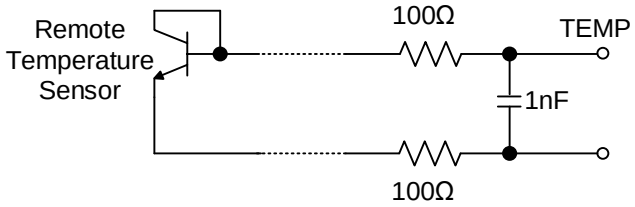


Figure 18. Filter Between Remote Sensor and SQ24905C

SPI Interface

The serial peripheral interface (SPI) allows users to output raw data from the ADC as soon as new data is available. It is a 3-pin serial interface capable of operating at speeds up to 1MHz.

If SPI is not needed, connect the SPI input pins (SPI_SS_N, MCLK) to VCAP and either leave the SPI output pin (MDAT) floating or tie it to GND.

The SPI_SS_N is the slave select pin. When SPI_SS_N is held low, the MCLK pin can clock data out on the MDAT serial output pin. The SPI pins are compatible with SPI Mode 0 (CPOL=CPHA =0). The interface characteristics are shown in the following table:

Table 2: SPI Interface Characteristics

NO.	SPI Interface Characteristics
1	MDAT is controlled by SQ24905C (master input, slave output). SPI_SS_N and MCLK are controlled by the user, such as a baseboard management controller (BMC).
2	No header or ID information is needed. The 80-bit data format remains fixed (see Figure 19).
3	The falling edge of SPI_SS_N activates the serial interface, allowing MCLK to clock out data on MDAT. To avoid duplicate data, the time between SPI_SS_N falling edges must be greater than or equal to the maximum ADC sampling time.
4	Use single shot mode for ADC sampling triggered by the falling edge of SPI_SS_N to trigger ADC sampling (ADC convert start signal)
5	Maximum clock speed (MCLK) is around 1MHz
6	The output stream can be stopped at any point in the output frame via a rising edge on the SPI_SS_N pin.
7	The MSB of each sample is output first.
8	The output data line is high impedance when not transmitting.

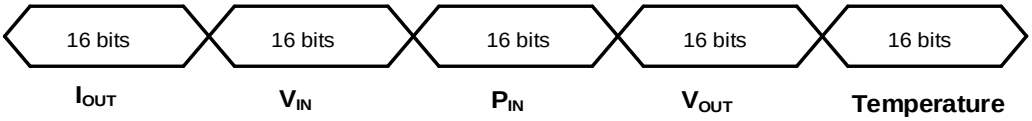


Figure 19. SPI Output Data Format

PMBus Command Reference

The SQ24905C integrates a PMBus 1.2 compatible interface. When communicating with multiple devices using the PMBus interface, each device must have its unique address so the host can distinguish between them.

The ADR1 and ADR2 pins determine the seven-bit device address of the SQ24905C. The following table shows that the device can be programmed to any of 16 possible addresses.

Table 3. ADRx Pin Connection

ADRx State	ADRx Pin connection
Low	Connect to GND
Resistor	150 kΩ resistor to GND
High-Z	No connection (floating)
High	Connect to VCAP

Table 4. PMBus Address Decode (7-bit Address)

ADR2 State	ADR1 State	Device Address
Low	Low	0x10
Low	Resistor	0x11
Low	High-Z	0x12
Low	High	0x13
Resistor	Low	0x40
Resistor	Resistor	0x41
Resistor	High-Z	0x42
Resistor	High	0x43
High-Z	Low	0x44
High-Z	Resistor	0x45
High-Z	High-Z	0x46
High-Z	High	0x47
High	Low	0x50
High	Resistor	0x51
High	High-Z	0x52
High	High	0x53

All I²C transactions on the SQ24905C are performed using SMBus-defined bus protocols. The SQ24905C PMBus interface supports packet error checking (PEC) byte as defined in the SMBus standard.

SMBus Message Formats

Figures 20 to 28 illustrate the SMBus protocols supported by the SQ24905C, including the PEC variant. Unshaded cells indicate the host is driving the bus, while shaded cells indicate that SQ24905C is driving the bus.

The SQ24905C can use group commands to simultaneously send commands or data to multiple devices in a single bus transaction. Each device is addressed separately using its unique address, as there is no specific group command address. A group command transaction can only contain write commands that send data to a device.

Flag	Meaning
S	Start condition
Sr	Repeated start condition
P	Stop condition
$\overline{W}$	Read bit
A	Acknowledge bit (0)
$\overline{A}$	Acknowledge bit (1)

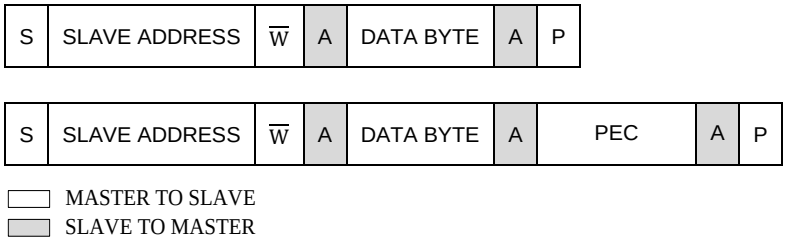


Figure 20. Send Byte and Send Byte with PEC

Note: The send byte and send byte with PEC protocols are only allowed for use with the clear_faults command and the power_cycle command. The send byte must not be used for any other commands.

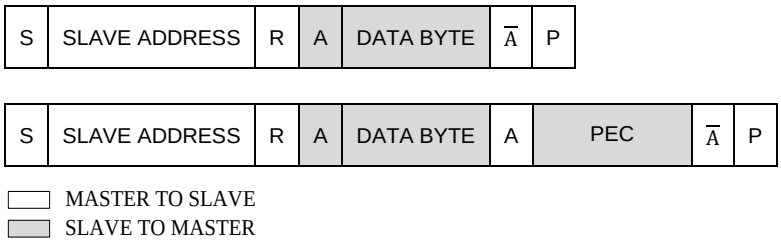


Figure 21. Receive Byte and Receive Byte with PEC

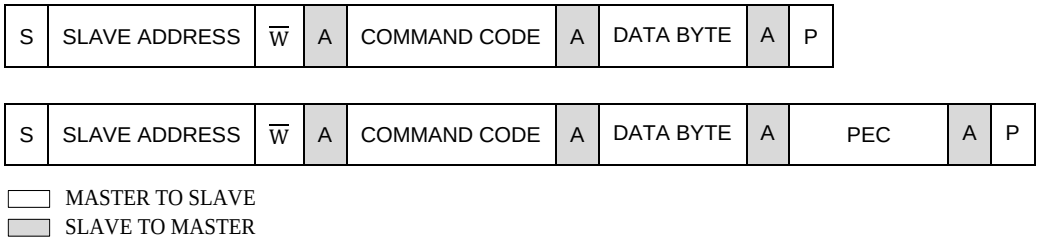


Figure 22. Write Byte and Write Byte with PEC

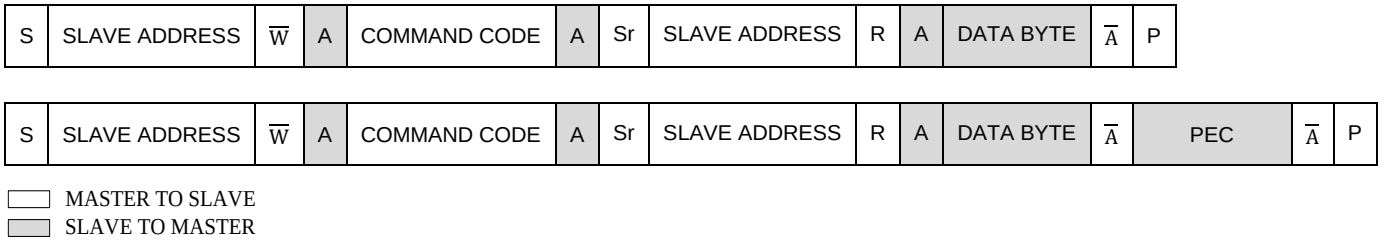


Figure 23. Read Byte and Read Byte with PEC

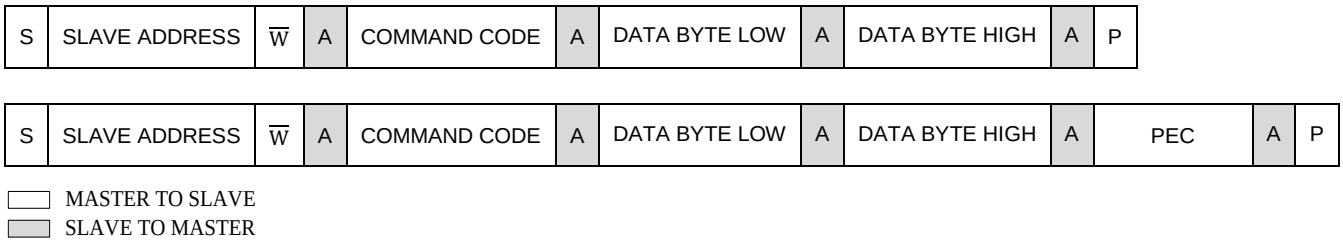


Figure 24. Write Word and Write Word with PEC

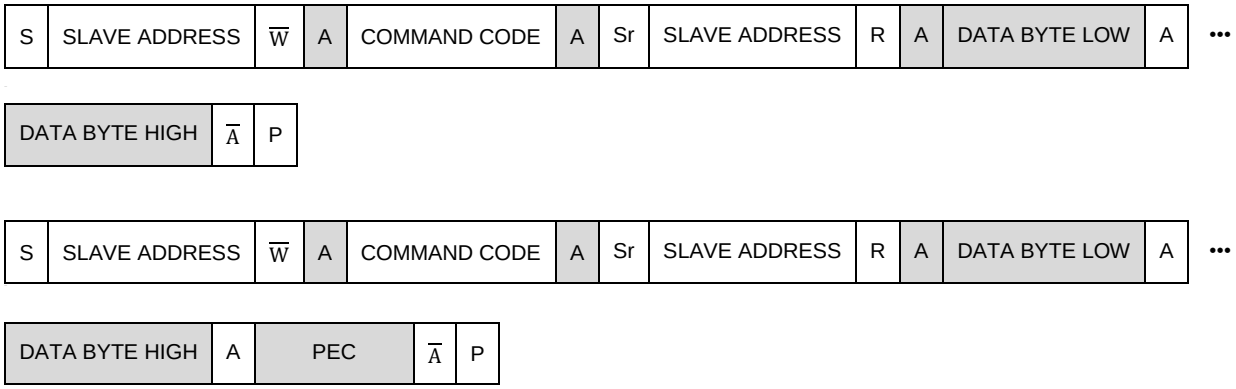


Figure 25. Read Word and Read Word with PEC

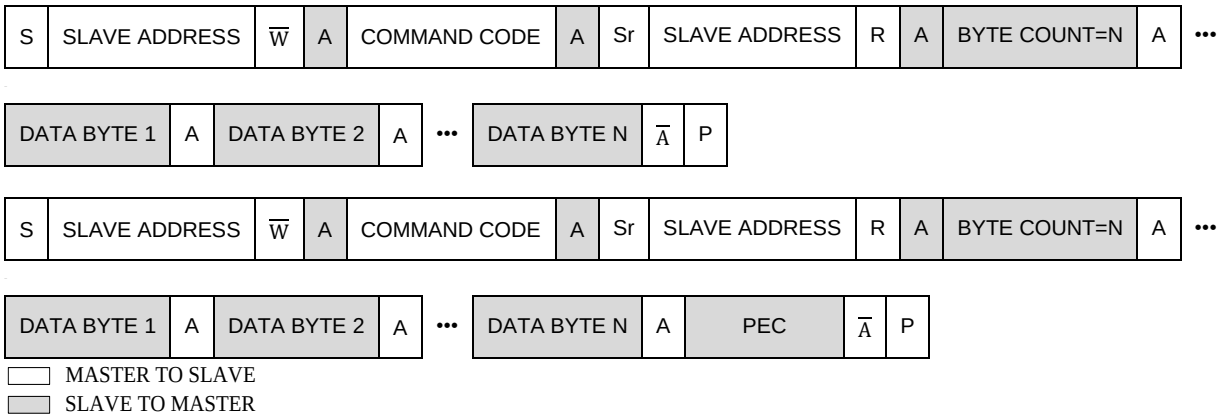


Figure 26. Block Read and Block Read with PEC

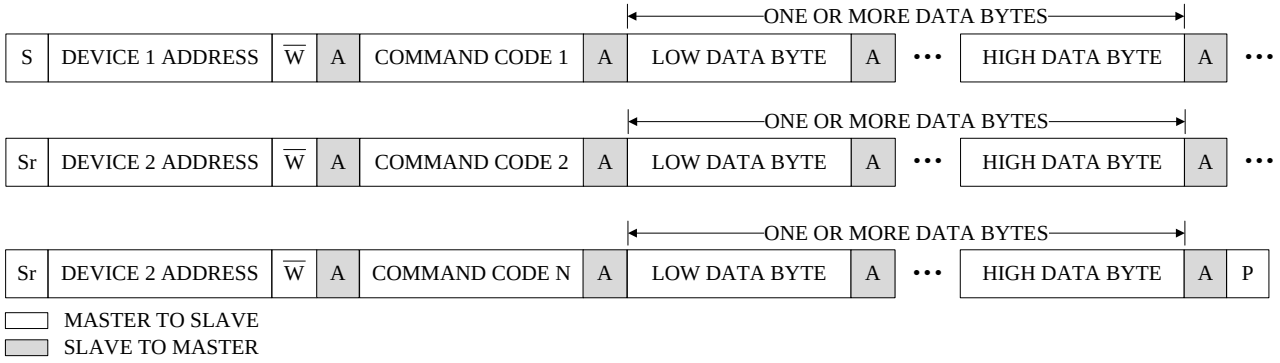


Figure 27. Group Command

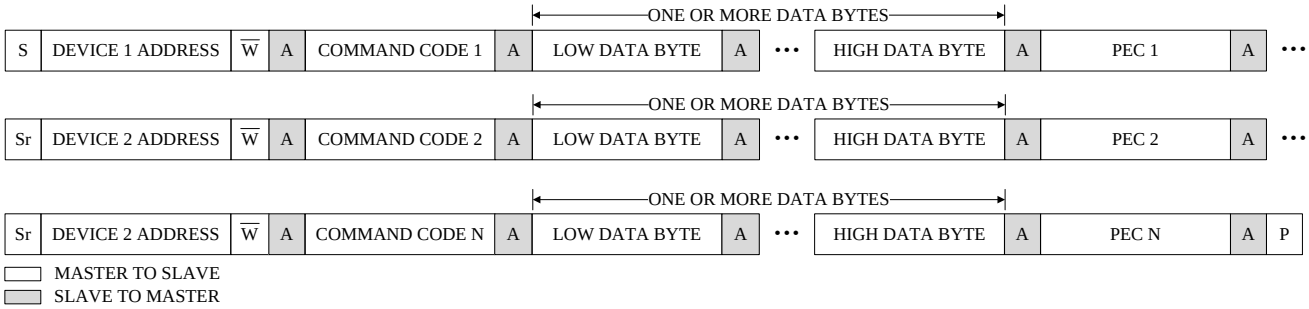


Figure 28. Group Command with PEC

Note: Group commands are single bus transactions that send commands or data to multiple devices simultaneously. Each device is addressed individually using its unique address, as there is no specific group command address. A group command transaction can only include write commands that send data to a device. It is not possible to use a group command to read data from devices.

PMBus Command Reference

Register addresses are in hexadecimal format.

Table 5. PMBus Command Summary

Address	Name	SMBus Transaction Type	Number of Data Bytes	Reset
0x01	OPERATION	Read/write byte	1	0x80
0x03	CLEAR_FAULTS	Send byte1	0	Not applicable
0x19	CAPABILITY	Read byte	1	0xD0
0x42	VOUT_OV_WARN_LIMIT	Read/write word	2	0x0FFF
0x43	VOUT_UV_WARN_LIMIT	Read/write word	2	0x0000
0x4A	IOUT_OC_WARN_LIMIT	Read/write word	2	0x0FFF
0x4F	OT_FAULT_LIMIT	Read/write word	2	0x0FFF
0x51	OT_WARN_LIMIT	Read/write word	2	0x0FFF
0x57	VIN_OV_WARN_LIMIT	Read/write word	2	0x0FFF
0x58	VIN_UV_WARN_LIMIT	Read/write word	2	0x0000
0x6B	PIN_OP_WARN_LIMIT	Read/write word	2	0x7FFF
0x78	STATUS_BYTE	Read byte	1	0x00
0x79	STATUS_WORD	Read word	2	0x0000
0x7A	STATUS_VOUT	Read byte	1	0x00
0x7B	STATUS_IOUT	Read byte	1	0x00
0x7C	STATUS_INPUT	Read byte	1	0x00
0x7D	STATUS_TEMPERATURE	Read byte	1	0x00
0x80	STATUS_MFR_SPECIFIC	Read byte	1	0x00
0x86	READ_EIN	Block read	6	0x000000000000
0x88	READ_VIN	Read word	2	0x0000
0x8B	READ_VOUT	Read word	2	0x0000
0x8C	READ_IOUT	Read word	2	0x0000
0x8D	READ_TEMPERATURE_1	Read word	2	0x0000
0x97	READ_PIN	Read word	2	0x0000
0x98	PMBUS_REVISION	Read byte	1	0x33
0x99	MFR_ID	Block read	2	0x5359(ASCII=SY)
0x9A	MFR_MODEL	Block read	10	0x4D43303943
0x9B	MFR_REVISION	Block read	1	0x00
0x9D	MFR_DATE	Block read	6	ASCII=YYMMDD
0xD0	PEAK_IOUT	Read/write word	2	0x0000
0xD1	PEAK_VIN	Read/write word	2	0x0000
0xD2	PEAK_VOUT	Read/write word	2	0x0000
0xD3	PMON_CONTROL	Read/write byte	1	0x01
0xD4	PMON_CONFIG	Read/write word	2	0x0714
0xD5	ALERT1_CONFIG	Read/write word	2	0x0000
0xD6	ALERT2_CONFIG	Read/write word	2	0x0000
0xD7	PEAK_TEMPERATURE	Read/write word	2	0x0000
0xD8	DEVICE_CONFIG	Read/write word	2	0x000D
0xD9	POWER_CYCLE	Send byte1	0	Not applicable

Address	Name	SMBus Transaction Type	Number of Data Bytes	Reset
0xDA	PEAK_PIN	Read/write word	2	0x0000
0xDB	READ_PIN_EXT	Block read	3	0x000000
0xDC	READ_EIN_EXT	Block read	8	0x0000000000000000
0xF2	HYSTERESIS_LOW	Read/write word	2	0x0000
0xF3	HYSTERESIS_HIGH	Read/write word	2	0xFFFF
0xF4	STATUS_HYSTERESIS	Read byte	1	0x00
0xF6	STRT_UP_IOUT_LIM	Read/write word	2	0x000F

Control Commands

Table 6. Control Commands

Address	Name	Description
0x01	OPERATION	The OPERATION command can be used to turn on the hot swap output, but only if the UV pin voltage exceeds the threshold. This command can also clear any latched faults in the status registers by setting the on bit to 0 and then resetting it to 1. Additionally, it clears the latched FAULT_N pin.
0xD8	DEVICE_CONFIG	Refer to the Register Details section for more information.
0xD9	POWER_CYCLE	The POWER_CYCLE command can turn off the SQ24905C for approximately 5 seconds (default) and then turn it back on. The turn-off time can be programmed from 5 to 80 seconds using the PMBus register (DEVICE_CONFIG, 0xD8[14:12]: POWER_CYCLE_SELECT).

Information Commands

Table 7. Information Commands

Address	Name	Description
0x19	CAPABILITY	The SMBus interface capabilities of the device, including PEC support, maximum bus speed, and SMBAlert support
0x98	PMBUS_REVISION	The PMBus revision that the device supports (ASCII string)
0x99	MFR_ID	The Manufacturer ID of the device (ASCII string)
0x9A	MFR_MODEL	The specific model of the device (ASCII string)
0x9B	MFR_REVISION	The hardware revision of the device (ASCII string)
0x9D	MFR_DATE	The production test date of the device (ASCII string)

Status Commands

The SQ24905C provides several status bits to report faults and warnings from the hot swap controller and the power monitor. The STATUS_BYTE and STATUS_WORD commands provide 8 bits and 16 bits of important information, respectively.

Table 8. Status Commands

Address	Name	Description
0x78	STATUS_BYTE	The STATUS_BYTE commands obtain a snapshot of the overall device status. These commands indicate whether it is necessary to read more detailed information using the other status commands.
0x79	STATUS_WORD	The low byte of the word returned by the STATUS_WORD command is the same byte returned by the STATUS_BYTE command. The high byte of the word returned by the STATUS_WORD command provides another bits that determine which of the other status commands needs to be issued to obtain all active status bits.
0x7A	STATUS_VOUT	Relating to voltage warnings on the output supply.
0x7B	STATUS_IOUT	Relating to current faults and warnings on the output supply.
0x7C	STATUS_INPUT	Relating to voltage faults and warnings on the input supply as well as the overpower warning.
0x7D	STATUS_TEMPERATURE	Relating to temperature faults and warnings at the external transistor
0x80	STATUS_MFR_SPECIFIC	The contents of the byte returned are specific to the SQ24905C; refer to the Register Details section for more information.

Address	Name	Description
0x03	CLEAR_FAULTS	The CLEAR_FAULTS command clears fault and warnings bits when they are set.

GPO and Alert Pin Setup Commands

The SQ24905C provides two multipurpose pins: GPO1/ALERT1_N/CONV and GPO2/ALERT2_N. These pins can be configured in one of four modes using the DEVICE_CONFIG register (GPOx_MODE).

- Output for generating an SMBAlert (default)
- General-purpose digital output
- Digital comparator

Pin 13 (GPO1/ALERT1_N/CONV) can also be configured as a convert (CONV) input pin.

SMBAlert Mode

GPOx_MODE of DEVICE_CONFIG register is 00.

Any one or more of the faults and warnings can be enabled by the ALERT2_CONFIG register and cause an alert, making the corresponding GPO1/ALERT1_N/CONV or GPO2/ALERT2_N pin active and latched. By default, the active state of the GPO1/ALERT1_N/ CONV and GPO2/ALERT2_N pins are low. The active state can be changed by configuring the DEVICE_CONFIG register (GPOx_INVERT).

When enabled faults or warnings occur, the corresponding pin becomes active to signal an interrupt to the processor. Subsequently, the processor issues an SMBus alert response address (ARA:0x0C) command to determine which device asserted the SMBAlert line. The processor then reads the status bytes from that device and issues a CLEAR_FAULTS command.

General-Purpose Digital Output Mode

GPOx_MODE of DEVICE_CONFIG register is 01.

GPO1 and GPO2 can be used as a general-purpose digital output pin. Use the GPOx_INVERT bit to change the output state.

Digital Comparator Mode

GPOx_MODE of DEVICE_CONFIG register is 11.

The GPO1/ALERT1_N/CONV and GPO2/ALERT2_N pins can be configured to indicate if the measured value is above or below the user-defined threshold. Configuring digital comparator mode is similar to configuring SMBAlert mode. The difference is that in digital comparator mode, the output pin is active and not latched when a fault or warning event occurs.

Hysteretic Comparison Setting

The current or power value is compared with the user-defined threshold in SMBAlert mode or digital comparator mode. The output will be active when the value exceeds the threshold. If the hysteretic comparison function is required, consider the following items:

- Set GPOx_MODE of the DEVICE_CONFIG register to 00 or 11.
- Select Current or Power to be compared using PWR_HYST_EN of the DEVICE_CONFIG register.
- Set the HYSTERETIC_ENx bit of the ALERTx_CONFIG register to 1.
- Set the user-defined threshold using the HYSTERESIS_LOW register (0xF2) and HYSTERESIS_HIGH register (0xF3).
- If needed, set the invert mode for the output pin using GPOx_INVERT in the DEVICE_CONFIG register.

Table 9. Commands Related to GPO and Alert Pin Set

Address	Name	Description
0xD8	DEVICE_CONFIG	1. Configure Pin 13 or Pin 14 working mode (GPOx_MODE) 2. Configure invert mode when the SMBAlert mode or GPO mode is configured (GPOx_INVERT) 3. Select current or power to compare with the threshold set by HYSTERESIS_LOW and HYSTERESIS_HIGH command (PWR_HYST_EN)
0xD5	ALERT1_CONFIG	Select different combinations of faults and warnings to be configured on the GPO1 output
0xD6	ALERT2_CONFIG	Select different combinations of faults and warnings to be configured on the GPO2 output
0xF2	HYSTERESIS_LOW	Set the low threshold
0xF3	HYSTERESIS_HIGH	Set the high threshold
0xF4	STATUS_HYSTERESIS	This command reports whether the hysteretic comparison is above or below the user defined thresholds

Power Monitor Commands

The SQ24905C provides a high-accuracy, 12-bit current, voltage, and temperature power monitor. The power monitor can be configured in different operation modes, either continuous or single-shot. Additionally, it supports different sample averaging, which is configured using the PMON_CONFIG command (0xD4).

Table 10. Power Monitor Commands

Address	Name	Description
0xD3	PMON_CONTROL	Starts and stops the power monitor.
0xD4	PMON_CONFIG	This command configures the power monitor, including sampling mode, sampling average mode, enabling or disabling channels, and other settings.
0x86	READ_EIN	Read the energy metering registers in a single operation to ensure time-consistent data.
0x88	READ_VIN	Reads the input voltage, V_{IN}.
0x8B	READ_VOUT	Reads the output voltage, V_{OUT}.
0x8C	READ_IOUT	Reads the output current, I_{OUT}.
0x8D	READ_TEMPERATURE_1	Reads the temperature measured by the device.
0x97	READ_PIN	Reads the calculated input power, P_{IN}.
0xDB	READ_PIN_EXT	Reads the extended precision version of the calculated input power, P_{IN}.
0xDC	READ_EIN_EXT	Read the extended precision energy metering registers in a single operation to ensure time-consistent data.
0xD0	PEAK_IOUT	Report the maximum peak output current value since the peak value was last cleared.
0xD1	PEAK_VIN	Report the maximum peak input voltage value since the peak value was last cleared.
0xD2	PEAK_VOUT	Report the maximum peak output voltage value since the peak value was last cleared.
0xD7	PEAK_TEMPERATURE	Report the maximum peak temperature value since the peak value was last cleared.
0xDA	PEAK_PIN	Report the maximum peak power value since the peak value was last cleared.

Warning Limit Commands

Using status commands, the SQ24905C power monitor can simultaneously monitor multiple warning conditions and report any values exceeding user-defined thresholds for current, voltage, power, or temperature.

At power-up, all threshold limits are set to either minimum scale (for undervoltage) or maximum scale (for overvoltage, overcurrent, overpower, or overtemperature conditions) to make sure there are no warnings by default.

Table 11. Warning Limit Commands

Address	Name	Description
0x42	VOUT_OV_WARN_LIMIT	Set the overvoltage warning limit for the voltage measured on the VOUT pin
0x43	VOUT_UV_WARN_LIMIT	Set the undervoltage warning limit for the voltage measured on the VOUT pin
0x4A	IOUT_OC_WARN_LIMIT	Set the overcurrent warning limit for the current measured between the MO+ and the MO- pins
0x4F	OT_FAULT_LIMIT	Set the overtemperature fault limit for the temperature measured on the TEMP pin
0x51	OT_WARN_LIMIT	Set the overtemperature warning limit for the temperature measured on the TEMP pin
0x57	VIN_OV_WARN_LIMIT	Set the overvoltage warning limit for the voltage measured on the HS+ pin
0x58	VIN_UV_WARN_LIMIT	Set the undervoltage warning limit for the voltage measured on the HS+ pin
0x6B	PIN_OP_WARN_LIMIT	Set the overpower warning limit for the power calculated based on VIN × IOUT

PMBus Data Format Conversion

The following equations must be used to convert between direct format value and real-world quantities. Equation 1 converts real-world quantities to PMBus direct values, and Equation 2 converts PMBus direct format values to real-world values.

$$Y = (mX + b) \times 10^{R} \quad (1)$$

$$X = \frac{1}{m} \times (Y \times 10^{-R} - b) \quad (2)$$

Where:

- Y is the value in PMBus direct format.
- X is the real-world value.
- m is the slope coefficient: a 2-byte, two's-complement integer.
- b is the offset: a 2-byte, two's-complement integer.
- R is a scaling exponent: a 1-byte, two's-complement integer.

The same equations are used for voltage, power, current, and temperature conversions. The only differences are the values of the m, b, and R coefficients. Table 12 lists all the coefficients required for the SQ24905C.
The maximum positive value of m coefficients is 32,767, defined as a 2-byte, two's complement number in the PMBus standard. If the m value exceeds this maximum, divide the m coefficient by 10 and increase the R coefficient by 1. For example, with a 10mΩ sense resistor, the m coefficient for power is 6123, and the R coefficient is -1.

Table 12. PMBus Conversion to Real-World Coefficients

Coefficient	Voltage (V)	Current (A)	Power (W)	Temperature (°C)
m	+19599	+800×R_{SENSE} (in mΩ)	+6123×R_{SENSE} (in mΩ)	+42
b	0	+20475	0	+31880
R	-2	-1	-2	-1

The direct voltage and current values obtained from the READ_VIN, READ_VOUT, and READ_IOUT commands are the

raw data output of the ADC. These 12-bit ADC output codes can be converted to real-world values using the LSB size information of the ADC.

Use the following formulas to convert an ADC code to current in amperes:

$V_{SENSE\_MO} = LSB_{CURRENT} \times (I_{ADC} - 2048)$

$I_{OUT} = V_{SENSE\_MO}/(R_{SENSE} \times 0.001)$

Where:

- V_{SENSE_MO} = (V_{MO+}) – (V_{MO-}).
- $LSB_{CURRENT}$ = 12.5μV.
- I_{ADC} is the 12-bit ADC code. I_{OUT} is the measured current value in amperes. R_{SENSE} is the value of the sense resistor in milliohms.

Use the following formula to convert an ADC code to voltage in volts:

$V_M = LSB_{VOLTAGE} \times (V_{ADC} + 0.5)$

Where:

- V_M is the measured value in volts.
- $LSB_{VOLTAGE}$ = 5.102mV.
- V_{ADC} is the 12-bit ADC code.

Use the following formulas to convert a current in amperes to a 12-bit value:

$V_{SENSE\_MO} = I_A \times R_{SENSE} \times 0.001$

$I_{CODE} = 2048 + (V_{SENSE_{MO}}/LSB_{CURRENT})$

Where:

- V_{SENSE_MO} = (V_{MO+}) – (V_{MO-}).
- I_A is the current value in amperes.
- R_{SENSE} is the value of the sense resistor in milliohms.
- I_{CODE} is the 12-bit ADC code.
- $LSB_{CURRENT}$ = 12.5μV.

Use the following formula to convert voltage in volts to a 12-bit value:

$V_{CODE} = (V_A/LSB_{VOLTAGE}) - 0.5$

Where:

- V_{CODE} is the 12-bit ADC code.
- V_A is the voltage value in volts.
- $LSB_{VOLTAGE}$ = 5.102 mV.

REGISTER DETAILS

OPERATION REGISTER

This command initiates turning the hot swap on and off. When activating the hot swap, it clears status bits for any inactive faults or warnings.

Table 13. Bit Descriptions for Operation

OPERATION Address: 0x01, Reset: 0x80				Setting	Description
Name	Bit NO.	Type	Reset		
ON	7	R/W	0x1	0	Hot swap output disabled.
				1	Hot swap output enabled.
RESERVED	[6:0]	Reserved	0x00		Reserved

CLEAR FAULTS REGISTER

Address: 0x03, Send Byte, No Data, Name: CLEAR_FAULTS

This command clears fault and warning bits in all status registers. Active faults are not cleared and remain set. Warnings and OT_FAULT generated by the power monitor are cleared but may be reasserted if they remain active after the next power monitor conversion cycle. This command does not require any data.

PMBUS CAPABILITY REGISTER

Enables the host system to identify the SMBus interface capabilities of the device.

Table 14. Bit Descriptions for Capability

CAPABILITY Address: 0x19, Reset: 0xD0				Setting	Description
Name	Bit NO.	Type	Reset		
PEC_SUPPORT	7	R	0x1	1	Always reads as 1. PEC is supported.
MAX_BUS_SPEED	[6:5]	R	0x2	10	Always reads as 02. Maximum supported bus speed is 1000 kHz.
SMBALERT_SUPPORT	4	R	0x1	1	Always reads as 1. Device supports SMBAlert and ARA.
RESERVED	[3:0]	Reserved	0x0		Always reads as 0000.

V_{OUT} OV WARNING LIMIT REGISTER

This register establishes the overvoltage warning threshold for the voltage measured at the VOUT pin.

Table 15. Bit Descriptions for VOUT_OV_WARN_LIMIT

VOUT_OV_WARN_LIMIT Address: 0x42, Reset: 0x0FFF				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000
VOUT_OV_WARN_LIMIT	[11:0]	R/W	0xFFF		The overvoltage warning threshold for the VOUT pin measurement is expressed in direct format.

V_{OUT} UV WARNING LIMIT REGISTER

This register establishes the undervoltage warning threshold for the voltage measured at the VOUT pin.

Table 16. Bit Descriptions for VOUT_UV_WARN_LIMIT

VOUT_UV_WARN_LIMIT Address: 0x43, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000
VOUT_UV_WARN_LIMIT	[11:0]	R/W	0x000		The undervoltage warning threshold for the VOUT pin measurement is expressed in direct format.

I_{OUT} OC WARNING LIMIT REGISTER

This register establishes the overcurrent warning limit for the current measured between the MO+ and the MO- pins.

Table 17. Bit Descriptions for IOUT_OC_WARN_LIMIT

IOUT_OC_WARN_LIMIT Address: 0x4A, Reset: 0x0FFF				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000
IOUT_OC_WARN_LIMIT	[11:0]	R/W	0xFFF		The overcurrent warning threshold for the IOUT measurement is expressed in direct format.

OT FAULT LIMIT REGISTER

This register establishes the overtemperature fault limit for the temperature measured on the TEMP pin.

Table 18. Bit Descriptions for OT_FAULT_LIMIT

OT_FAULT_LIMIT Address: 0x4F, Reset: 0x0FFF				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
OT_FAULT_LIMIT	[11:0]	R/W	0xFFF		The overtemperature fault threshold for the TEMP pin measurement is expressed in direct format.

OT WARNING LIMIT REGISTER

This register establishes the overtemperature warning limit for the temperature measured on the TEMP pin.

Table 19. Bit Descriptions for OT_WARN_LIMIT

OT_WARN_LIMIT Address: 0x51, Reset: 0x0FFF				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.

OT_WARN_LIMIT	[11:0]	R/W	0xFFF		Overtemperature warning threshold for the TEMP pin measurement, expressed in direct format.

V_{IN} OV WARNING LIMIT REGISTER

This register establishes the overvoltage warning limit for the voltage measured on the HS+ pin.

Table 20. Bit Descriptions for VOUT_OV_WARN_LIMIT

VIN_OV_WARN_LIMIT Address: 0x57, Reset: 0x0FFF				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
VIN_OV_WARN_LIMIT	[11:0]	R/W	0xFFF		Overvoltage warning threshold for the HS+ pin measurement, expressed in direct format.

V_{IN} UV WARNING LIMIT REGISTER

This register establishes the undervoltage warning limit for the voltage measured on the HS+ pin.

Table 21. Bit Descriptions for VIN_UV_WARN_LIMIT

VIN_UV_WARN_LIMIT Address: 0x58, Reset: 0x0000				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
VIN_UV_WARN_LIMIT	[11:0]	R/W	0x000		Undervoltage warning threshold for the HS+ pin measurement, expressed in direct format.

P_{IN} OP WARNING LIMIT REGISTER

This register establishes the overpower warning limit for the power calculated based on $V_{IN} \times I_{OUT}$.

Table 22. Bit Descriptions for PIN_OP_WARN_LIMIT

PIN_OP_WARN_LIMIT Address: 0x6B, Reset: 0x7FFF				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	15	Reserved	0x0		Always reads as 0.
PIN_OP_WARN_LIMIT	[14:0]	R/W	0x7FFF		Overpower warning threshold for the $V_{IN} \times I_{OUT}$ power calculation, expressed in direct format.

STATUS BYTE REGISTER

This register provides status information for critical faults and specific top-level status commands in the device. It also represents the lower byte returned by STATUS_WORD. A bit set to 1 indicates the occurrence of a fault or warning.

Table 23. Bit Descriptions for STATUS_BYTE

STATUS_BYTE Address: 0x78, Reset: 0x00				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	7	Reserved	0x0		Always reads as 0.
HOTSWAP_OFF	6	R	0x0	0	The hot swap gate drive output is enabled.
				1	The hot swap gate drive output is disabled, and the GATE pin is pulled down. This can be due to, for example, an overcurrent fault that causes the device to latch off, an undervoltage condition on the UV pin, or the use of the OPERATION command to turn the output off. This bit is live.
RESERVED	5	Reserved	0x0		Always reads as 0.
IOUT_OC_FAULT	4	R	0x0	0	No overcurrent output fault detected.
				1	The hot swap controller detected an overcurrent condition, and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down. This bit is latched.
VIN_UV_FAULT	3	R	0x0	0	No undervoltage input fault detected on the UV pin.
				1	An undervoltage input fault was detected on the UV pin. This bit is latched.
TEMP_FAULT	2	R	0x0	0	There are no active status bits to be read by STATUS_TEMPERATURE. (Temperature fault or warning)
				1	There are one or more active status bits to be read by STATUS_TEMPERATURE (temperature fault or warning). This bit is live.
CML_FAULT	1	R	0x0	0	No communications error detected on the I^2C/PMBus interface.
				1	An error was detected on the I^2C/PMBus interface. Detected errors include unsupported commands, invalid PEC bytes, and incorrectly structured messages. This bit is latched.
NONEABOVE_STATUS	0	R	0x0	0	No other active status bit reported by any other status command.
				1	Active status bits are waiting to be read by one or more status commands. This bit is live.

STATUS WORD REGISTER

Provides status information for critical faults and all top-level status commands in the device. The lower byte is also returned by the STATUS_BYTE.

Table 24. Bit Descriptions for STATUS_WORD

STATUS_WORD Address: 0x79, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
VOUT_STATUS	15	R	0x0	0	There are no active status bits to be read by the STATUS_VOUT register.
				1	There are one or more active status bits to be read by STATUS_VOUT. This bit is live.
IOUT_STATUS	14	R	0x0	0	There are no active status bits to be read by the STATUS_IOUT register.
				1	There are one or more active status bits to be read by the STATUS_IOUT register. This bit is live.
INPUT_STATUS	13	R	0x0	0	There are no active status bits to be read by the STATUS_INPUT register.
				1	There are one or more active status bits to be read by STATUS_INPUT. This bit is live.
MFR_STATUS	12	R	0x0	0	There are no active status bits to be read by the STATUS_MFR_SPECIFIC register.
				1	There are one or more active status bits to be read by the STATUS_MFR_SPECIFIC register. This bit is live.
PGB_STATUS	11	R	0x0	0	Output power is good. The voltage on the PWGIN pin is above the threshold.
				1	Output power is bad. The voltage on the PWGIN pin is below the threshold. This bit is live.
RESERVED	[10:9]	Reserved	0x0		Always reads as 00.
FET_HEALTH_FAULT	8	R	0x0	0	No MOSFET faults have been detected.
				1	A fault condition has been detected on the MOSFET. This bit is latched.
RESERVED	7	Reserved	0x0		Always set to 0.
HOTSWAP_OFF	6	R	0x0		Duplicate of corresponding bit in the STATUS_BYTE register.
RESERVED	5	Reserved	0x0		Always set to 0.
IOUT_OC_FAULT	4	R	0x0		Duplicate of corresponding bit in the STATUS_BYTE register.
VIN_UV_FAULT	3	R	0x0		Duplicate of corresponding bit in the STATUS_BYTE register.
TEMP_FAULT	2	R	0x0		Duplicate of corresponding bit in the STATUS_BYTE register.
CML_FAULT	1	R	0x0		Duplicate of corresponding bit in the STATUS_BYTE register.
NONEABOVE_STATUS	0	R	0x0		Duplicate of corresponding bit in the STATUS_BYTE register.

V_{OUT} STATUS REGISTER

Provides status information for warnings related to V_{OUT}.

Table 25. Bit Descriptions for STATUS_VOUT

STATUS_VOUT Address: 0x7A, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	7	Reserved	0x0		Always reads as 0.
VOUT_OV_WARN	6	R	0x0	0	No overvoltage condition on the output supply detected by the power monitor.
				1	An overvoltage condition on the output supply was detected by the power monitor. This bit is latched.
VOUT_UV_WARN	5	R	0x0	0	No undervoltage condition on the output supply detected by the power monitor.
				1	An undervoltage condition on the output supply was detected by the power monitor. This bit is latched.
RESERVED	[4:0]	Reserved	0x00		Always reads as 00000.

I_{OUT} STATUS REGISTER

Provides status information for faults and warnings related to I_{OUT}.

Table 26. Bit Descriptions for STATUS_IOUT

STATUS_IOUT Address: 0x7B, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
IOUT_OC_FAULT	7	R	0x0	0	No overcurrent output fault detected.
				1	The hot swap controller detected an overcurrent condition, and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down. This bit is latched.
RESERVED	6	Reserved	0x0		Always reads as 0.
IOUT_OC_WARN	5	R	0x0	0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.
				1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command. This bit is latched.
RESERVED	[4:0]	Reserved	0x00		Always reads as 00000.

INPUT STATUS REGISTER

Provides status information for faults and warnings related to V_{IN} and P_{IN}.

Table 27. Bit Descriptions for STATUS_INPUT

STATUS_INPUT Address: 0x7C, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
VIN_OV_FAULT	7	R	0x0	0	No overvoltage detected on the OV pin.
				1	An overvoltage was detected on the OV pin. This bit is latched.
VIN_OV_WARN	6	R	0x0	0	No overvoltage warning condition on the input supply detected by the power monitor.
				1	An overvoltage warning condition on the input supply was detected by the power monitor. This bit is latched.
VIN_UV_WARN	5	R	0x0	0	No undervoltage warning condition on the input supply detected by the power monitor.
				1	An undervoltage warning condition on the input supply was detected by the power monitor. This bit is latched.
VIN_UV_FAULT	4	R	0x0	0	No undervoltage detected on the UV pin.
				1	An undervoltage was detected on the UV pin. This bit is latched.
RESERVED	[3:1]	Reserved	0x0		Always reads as 000.
PIN_OP_WARN	0	R	0x0	0	No overpower warning condition on the input supply detected by the power monitor.
				1	An overpower warning condition on the input supply was detected by the power monitor. This bit is latched.

TEMPERATURE STATUS REGISTER

Provides status information for faults and warnings related to temperature.

Table 28. Bit Descriptions for STATUS_TEMPERATURE

STATUS_TEMPERATURE Address: 0x7D, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
OT_FAULT	7	R	0x0	0	No overtemperature fault detected by the ADC.
				1	An overtemperature fault was detected by the ADC. This bit is latched.
OT_WARNING	6	R	0x0	0	No overtemperature warning detected by the ADC.
				1	An overtemperature warning was detected by the ADC. This bit is latched.
RESERVED	[5:0]	Reserved	0x00		Always reads as 000000.

MANUFACTURER SPECIFIC STATUS REGISTER

Provides status information for manufacturer specific faults and warnings.

Table 29. Bit Descriptions for STATUS_MFR_SPECIFIC

STATUS_MFR_SPECIFIC Address: 0x80, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
FET_HEALTH_FAULT	7	R	0x0	0	No MOSFET health problems have been detected.
				1	An MOSFET health fault has been detected. This bit is latched.
UV_CMP_OUT	6	R	0x0	0	Input voltage to UV pin is above threshold.
				1	Input voltage to UV pin is below threshold. This bit is live.
OV_CMP_OUT	5	R	0x0	0	Input voltage to OV pin is below threshold.
				1	Input voltage to OV pin is above threshold. This bit is live.
SEVERE_OC_FAULT	4	R	0x0	0	A severe overcurrent has not been detected by the hot swap.
				1	A severe overcurrent has been detected by the hot swap. This bit is latched.
HS_INLIM_FAULT	3	R	0x0	0	The hot swap has not actively limited the current into the load.
				1	The hot swap has actively limited current into the load. This bit differs from the IOUT_OC_FAULT bit in that the HS_INLIM_FAULT bit is set immediately, whereas the IOUT_OC_FAULT bit is not set unless the time limit set by the capacitor on the TIMER pin elapses. This bit is latched.
HS_SHUTDOWN_CAUSE	[2:0]	R	0x0	000	The hot swap is either enabled and working correctly, or has been shut down using the OPERATION command.
				001	An OT_FAULT condition occurred that caused the hot swap to shut down. This bit is latched.
				010	An IOUT_OC_FAULT condition occurred that caused the hot swap to shut down. This bit is latched.
				011	An FET_HEALTH_FAULT condition occurred that caused the hot swap to shut down. This bit is latched.
				100	A VIN_UV_FAULT condition occurred that caused the hot swap to shut down. This bit is latched.
				110	A VIN_OV_FAULT condition occurred that caused the hot swap to shut down. This bit is latched.

READ E_{IN} REGISTER

Reads the energy metering registers in a single operation to guarantee time-consistent data.

Table 30. Bit Descriptions for READ_EIN

READ_EIN Address: 0x86, Reset: 0x000000000000				Setting	Description
Name	Bit NO.	Type	Reset		
SAMPLE_COUNT	[47:24]	R	0x000000		This is the total number of PIN samples acquired and accumulated in the energy count accumulator. This is an unsigned 24- bit binary value. Byte 5 is the high byte, Byte 4 is the middle byte, and Byte 3 is the low byte.
ROLLOVER_COUNT	[23:16]	R	0x00		Number of times that the energy count has rolled over from 0x7FFF to 0x0000. This is an unsigned 8-bit binary value.
ENERGY_COUNT	[15:0]	R	0x0000		Energy accumulator value in PMBus direct format. Byte 1 is the high byte, and Byte 0 is the low byte. Internally, the energy accumulator is a 24-bit value, but only the most significant 16 bits are returned with this command. Use the READ_EIN_EXT register to access the nontruncated version.

READ V_{IN} REGISTER

Reads the input voltage (V_{IN}) from the device.

Table 31. Bit Descriptions for READ_VIN

READ_VIN Address: 0x88, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
READ_VIN	[11:0]	R	0x000		Input voltage from the HS+ pin measurement after averaging, expressed in direct format.

READ V_{OUT} REGISTER

Reads the output voltage (VOUT) from the device.

Table 32. Bit Descriptions for READ_VOUT

READ_VOUT Address: 0x8B, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
READ_VOUT	[11:0]	R	0x000		Input voltage from the VOUT pin measurement after averaging, expressed in direct format.

READ I_{OUT} REGISTER

Reads the output current (IOUT) from the device.

Table 33. Bit Descriptions for READ_IOUT

READ_IOUT Address: 0x8C, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
READ_IOUT	[11:0]	R	0x000		Output current derived from MO+/MO- sense pin voltage measurement after averaging, expressed in direct format.

READ TEMPERATURE 1 REGISTER

Reads the temperature measured by the device.

Table 34. Bit Descriptions for READ_TEMPERATURE_1

READ_TEMPERATURE_1 Address: 0x8D, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
READ_TEMPERATURE_1	[11:0]	R	0x000		Temperature from the TEMP pin measurement after averaging, expressed in direct format.

READ P_{IN} REGISTER

Reads the calculated input power (PIN) from the device.

Table 35. Bit Descriptions for READ_PIN

READ_PIN Address: 0x97, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
READ_PIN	[15:0]	R	0x0000		Input power calculation, using $V_{IN} \times I_{OUT}$, after averaging, expressed in PMBus direct format. PIN values are calculated for each $V_{IN} \times I_{OUT}$ sample, all PIN values are then averaged before the value is returned to the READ_PIN register.

PMBUS REVISION REGISTER

Allows the system to read the PMBus revision that the device supports.

Table 36. Bit Descriptions for PMBUS_REVISION

PMBUS_REVISION Address: 0x98, Reset: 0x33				Setting	Description
Name	Bit NO.	Type	Reset		
PMBUS_P1_REVISION	[7:4]	R	0x3	0011	PMBus Part I Support. Revision 1.3.
PMBUS_P2_REVISION	[3:0]	R	0x3	0011	PMBus Part II Support. Revision 1.3.

MANUFACTURER ID REGISTER

Returns a string that identifies the device manufacturer.

Table 37. Bit Descriptions for MFR_ID

MFR_ID Address: 0x99, Reset: 0x5359(ASCII: SY)				Setting	Description
Name	Bit NO.	Type	Reset		
MFR_ID	[15:0]	R	0x5359		String identifying manufacturer as Silergy (SY).

MANUFACTURER MODEL REGISTER

Returns a string that identifies the specific device model.

Table 38. Bit Descriptions for MFR_MODEL

MFR_MODEL Address: 0x9A, Reset: 0x4D43303941				Setting	Description
Name	Bit NO.	Type	Reset		
MFR_MODEL	[79:0]	R	0x4D43303941		String identifying model.

MANUFACTURER REVISION REGISTER

Returns a string that identifies the device hardware revision.

Table 39. Bit Descriptions for MFR_REVISION

MFR_REVISION Address: 0x9B, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
MFR_REVISION	[7:0]	R	0x00		String identifying the hardware revision, for example, "0".

MANUFACTURER DATE REGISTER

Returns a string that identifies the device production test date.

Table 40. Bit Descriptions for MFR_DATE

MFR_DATE Address: 0x9D, Reset: ASCII = YYMMDD				Setting	Description
Name	Bit NO.	Type	Reset		
DATE	[47:0]	R	(TBD)		String identifying the test date in YYMMDD format.

PEAK I_{OUT} REGISTER

Reports the peak output current (I_{OUT}). Writing 0x0000 with this command resets the peak value.

Table 41. Bit Descriptions for PEAK_IOUT

PEAK_IOUT Address: 0xD0, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.

PEAK_IOUT	[11:0]	R	0x000		Peak output current measurement expressed in direct format.

PEAK V_{IN} REGISTER

Reports the peak output current (V_{IN}). Writing 0x0000 with this command resets the peak value.

Table 42. Bit Descriptions for PEAK_VIN

PEAK_VIN Address: 0xD1, Reset: 0x0000				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
PEAK_VIN	[11:0]	R	0x000		Peak input voltage measurement expressed in direct format.

PEAK V_{OUT} REGISTER

Reports the peak output current, (V_{OUT}). Writing 0x0000 with this command resets the peak value.

Table 43. Bit Descriptions for PEAK_VOUT

PEAK_VOUT Address: 0xD2, Reset: 0x0000				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
PEAK_VOUT	[11:0]	R	0x000		Peak output voltage measurement expressed in direct format.

POWER MONITOR CONTROL REGISTER

This command initiates and halts the power monitor.

Table 44. Bit Descriptions for PMON_CONTROL

PMON_CONTROL Address: 0xD3, Reset: 0x01				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
RESERVED	[7:1]	Reserved	0x00		Always reads as 0000000.
CONVERT	0	R/W	0x1	0	Power monitor is not running.
				1	The power monitor is sampling by default. In single-shot mode, this bit clears itself after one complete cycle. In continuous mode, this bit must be written to 0 to stop sampling. A rising edge on the conversion input (CONV function of Pin 13) or a falling edge on SPI_SS_N sets this bit to 1. During sampling, additional conversion edges on these pins are ignored.

POWER MONITOR CONFIGURATION REGISTER

This command configures the power monitor. Various channel combinations can be included in the sampling sequence, and averaging can be configured for different measurements.

Table 45. Bit Descriptions for PMON_CONFIG

PMON_CONFIG Address: 0xD4, Reset: 0x0714				Setting	Description
Name	Bit NO.	Type	Reset		
TSFILT	15	Reserved	0x0	0	Temperature sensor filter disabled.
				1	Temperature sensor filter enabled. Datasheet specifications assume the temperature sensor filter is disabled.
SIMULTANEOUS	14	R/W	0x0	0	Simultaneous sampling disabled.
				1	Simultaneous sampling enabled. Power monitoring accuracy is reduced. Datasheet specifications assume simultaneous sampling is disabled.
PWR_AVG	[13:11]	R/W	0x0	000	Disables sample averaging for power.
				001	Sets sample averaging for power to 2 samples.
				010	Sets sample averaging for power to 4 samples.
				011	Sets sample averaging for power to 8 samples.
				100	Sets sample averaging for power to 16 samples.
				101	Sets sample averaging for power to 32 samples.
				110	Sets sample averaging for power to 64 samples.
				111	Sets sample averaging for power to 128 samples.
VI_AVG	[10:8]	R/W	0x7	000	Disables sample averaging for V_{IN}, V_{OUT}, and I_{OUT}.
				001	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 2 samples.
				010	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 4 samples.
				011	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 8 samples.
				100	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 16 samples.
				101	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 32 samples.
				110	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 64 samples.
				111	Sets sample averaging for V_{IN}, V_{OUT}, and I_{OUT} to 128 samples.
RESERVED	[7:5]	Reserved	0x0		Always reads as 000.
PMON_MODE	4	R/W	0x1	0	The conversion mode is single-shot sampling.
				1	The conversion mode is continuous sampling.
TEMP1_EN	3	R/W	0x0	0	Temperature sampling disabled.
				1	Temperature sampling enabled.
VIN_EN	2	R/W	0x1	0	V_{IN} sampling disabled.
				1	V_{IN} sampling enabled.
VOUT_EN	1	R/W	0x0	0	V_{OUT} sampling disabled.
				1	V_{OUT} sampling enabled.
RESERVED	0	Reserved	0x0		Always reads as 0.

ALERT 1 CONFIGURATION REGISTER

This command configures the GPO1 output of the GPO1/ALERT1_N/CONV pin for various combinations of faults and warnings. The DEVICE_CONFIG command sets the pin's operating modes.

Table 46. Bit Descriptions for ALERT1_CONFIG

ALERT1_CONFIG Address: 0xD5, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
FET_HEALTH_FAULT_EN1	15	R/W	0x0		MOSFET health fault enable.
IOUT_OC_FAULT_EN1	14	R/W	0x0		I_{OUT} overcurrent fault enable.
VIN_OV_FAULT_EN1	13	R/W	0x0		V_{IN} overvoltage fault enable.
VIN_UV_FAULT_EN1	12	R/W	0x0		V_{IN} undervoltage fault enable.
CML_ERROR_EN1	11	R/W	0x0		Communications error enable.
IOUT_OC_WARN_EN1	10	R/W	0x0		I_{OUT} overcurrent warning enable.
HYSTERETIC_EN1	9	R/W	0x0		Hysteretic output enable.
VIN_OV_WARN_EN1	8	R/W	0x0		V_{IN} overvoltage warning enable.
VIN_UV_WARN_EN1	7	R/W	0x0		V_{IN} undervoltage warning enable.
VOUT_OV_WARN_EN1	6	R/W	0x0		V_{OUT} overvoltage warning enable.
VOUT_UV_WARN_EN1	5	R/W	0x0		V_{OUT} undervoltage warning enable.
HS_INLIM_EN1	4	R/W	0x0		Hot swap in-limit enable.
PIN_OP_WARN_EN1	3	R/W	0x0		P_{IN} overpower warning enable.
OT_FAULT_EN1	2	R/W	0x0		Overtemperature fault enable.
OT_WARN_EN1	1	R/W	0x0		Overtemperature warning enable.
RESERVED	0	Reserved	0x0		Always reads as 0.

ALERT 2 CONFIGURATION REGISTER

This command configures the GPO2 output of the GPO2/ALERT2_N pin for various combinations of faults and warnings. The DEVICE_CONFIG command sets the pin's operating modes.

Table 47. Bit Descriptions for ALERT2_CONFIG

ALERT2_CONFIG Address: 0xD6, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
FET_HEALTH_FAULT_EN2	15	R/W	0x0		MOSFET health fault enable.
IOUT_OC_FAULT_EN2	14	R/W	0x0		I_{OUT} overcurrent fault enable.
VIN_OV_FAULT_EN2	13	R/W	0x0		V_{IN} overvoltage fault enable.
VIN_UV_FAULT_EN2	12	R/W	0x0		V_{IN} undervoltage fault enable.
CML_ERROR_EN2	11	R/W	0x0		Communications error enable.
IOUT_OC_WARN_EN2	10	R/W	0x0		I_{OUT} overcurrent warning enable.
HYSTERETIC_EN2	9	R/W	0x0		Hysteretic output enable.
VIN_OV_WARN_EN2	8	R/W	0x0		V_{IN} overvoltage warning enable.
VIN_UV_WARN_EN2	7	R/W	0x0		V_{IN} undervoltage warning enable.
VOUT_OV_WARN_EN2	6	R/W	0x0		V_{OUT} overvoltage warning enable.
VOUT_UV_WARN_EN2	5	R/W	0x0		V_{OUT} undervoltage warning enable.
HS_INLIM_EN2	4	R/W	0x0		Hot swap in-limit enable.
PIN_OP_WARN_EN2	3	R/W	0x0		P_{IN} overpower warning enable.
OT_FAULT_EN2	2	R/W	0x0		Overtemperature fault enable.
OT_WARN_EN2	1	R/W	0x0		Overtemperature warning enable.
RESERVED	0	Reserved	0x0		Always reads as 0.

PEAK TEMPERATURE REGISTER

Reports the peak temperature measured. Writing 0x0000 with this command resets the peak value.

Table 48. Bit Descriptions for PEAK_TEMPERATURE

PEAK_TEMPERATURE Address: 0xD7, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:12]	Reserved	0x0		Always reads as 0000.
PEAK_TEMPERATURE	[11:0]	R	0x000		Peak temperature measurement, expressed in direct format.

DEVICE CONFIGURATION REGISTER

This command configures the hot swap overcurrent threshold, filtering, GPO1/GPO2 output modes, and power cycle period. Note that dual-function pin names are referenced only by their relevant function. For example, GPO2 refers to the general-purpose output function of the GPO2/ALERT2_N pin (see the Pin Configurations and Function Descriptions section for full pin descriptions).

Table 49. Bit Descriptions for DEVICE_CONFIG

DEVICE_CONFIG Address: 0xD8, Reset: 0x000D				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	15	Reserved	0x0		Always reads as 0.
POWER_CYCLE _SELECT	[14:12]	R/W	0x0	000	Power cycle time: 5s (default)
				001	Power cycle time: 10s
				010	Power cycle time: 20s
				011	Power cycle time: 40s
				100	Reserved
				101	Power cycle time: 80s
				110	Power cycle time: 5s
				111	Power cycle time: 5s
FHDIS	11	R/W	0x0	0	MOSFET health checks enabled.
				1	MOSFET health checks disabled.
PWR_HYST_EN	10	R/W	0x0	0	The general-purpose output alert hysteresis functions refer to power or current: Current hysteresis mode
				1	The general-purpose output alert hysteresis functions refer to power or current: Power hysteresis mode
GPO2_MODE	[9:8]	R/W	0x0	00	Default. GPO2 is configured to generate SMBAlerts.
				01	GPO2 can be used as a general-purpose digital output pin. Use the GPO2_INVERT bit to change the output state.
				10	Reserved.
				11	This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert.

GPO2_INVERT	7	R/W	0x0	0	GPO2: In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low.
				1	GPO2: In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high.
GPO1_MODE	[6:5]	R/W	0x0	00	Default. GPO1 is configured to generate SMBAlerts.
				01	GPO1 can be used as a general-purpose digital output pin. Use the GPO1_INVERT bit to change the output state.
				10	(CONV) input pin.
				11	This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert.
GPO1_INVERT	4	R/W	0x0	0	GPO1: In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low.
				1	GPO1: In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high.
OC_TRIP_SELECT	[3:2]	R/W	0x3	00	Severe overcurrent threshold: 125%
				01	Severe overcurrent threshold: 150%
				10	Severe overcurrent threshold: 200%
				11	Severe overcurrent threshold: 225%, default.
OC_RETRY_DIS	1	R/W	0x0	0	Retry once immediately after severe overcurrent event.
				1	Latch off after a severe overcurrent event.
OC_FILT_SELECT	0	R/W	0x1	0	Severe overcurrent filter: 200ns
				1	Severe overcurrent filter: 900ns, default.

POWER CYCLE REGISTER

Address: 0xD9, Send Byte, No Data, Name: POWER_CYCLE

This command allows a processor to request the hot swap to turn off and then back on after approximately five seconds (default) or 10s/20s/40s/60s/80s, which can be selected by using POWER_CYCLE _SELECT command (DEVICE_CONFIG: 0xD8[14:12])). This is useful when the hot swap output is powering the processor. This command does not require any data.

Don't ENABLE OFF/ON or use operation command during power cycle time

PEAK P_{IN} REGISTER

Reports the peak input power (PIN). Writing 0x0000 with this command resets the peak value.

Table 50. Bit Descriptions for PEAK_PIN

PEAK_PIN Address: 0xDA, Reset: 0x0000				Setting	Description
Name	**Bit NO.**	**Type**	**Reset**		
PEAK_PIN	[15:0]	R	0x0000		Peak input power calculation, PIN, expressed in direct format.

READ P_{IN} (EXTENDED) REGISTER

Reads the extended precision version of the calculated input power, P_{IN}, from the device.

Table 51. Bit Descriptions for READ_PIN_EXT

READ_PIN_EXT Address: 0xDB, Reset: 0x000000				Setting	Description
Name	Bit NO.	Type	Reset		
READ_PIN_EXT	[23:0]	R	0x000000		Extended precision version of peak input power calculation, PIN, expressed in PMBus direct format.

READ E_{IN} (EXTENDED) REGISTER

Reads the extended precision energy metering registers in one operation to ensure time-consistent data.

Table 52. Bit Descriptions for READ_EIN_EXT

READ_EIN_EXT Address: 0xDC, Reset: 0x0000000000000000				Setting	Description
Name	Bit NO.	Type	Reset		
SAMPLE_COUNT	[63:40]	R	0x000000		This is the total number of PIN samples acquired and accumulated in the energy count accumulator. This is an unsigned 24- bit binary value. Byte 7 is the high byte, Byte 6 is the middle byte, and Byte 5 is the low byte.
ROLLOVER_EXT	[39:24]	R	0x0000		Number of times that the energy count has rolled over from 0x7FFFFF to 0x000000. This is an unsigned 16-bit binary value. Byte 4 is the high byte, and Byte 3 is the low byte.
ENERGY_EXT	[23:0]	R	0x000000		Extended precision energy accumulator value in PMBus direct format. Byte 2 is the high byte, Byte 1 is the middle byte, and Byte 0 is the low byte

HYSTERESIS LOW LEVEL REGISTER

This sets the lower threshold for the hysteretic output signal, which can be available on a general-purpose output pin.

Table 53. Bit Descriptions for HYSTERESIS_LOW

HYSTERESIS_LOW Address: 0xF2, Reset: 0x0000				Setting	Description
Name	Bit NO.	Type	Reset		
HYSTERESIS_LOW	[15:0]	R/W	0x0000		Value setting the lower hysteresis threshold, expressed in direct format.

HYSTERESIS HIGH LEVEL REGISTER

This sets the higher threshold for the hysteretic output signal, which can be available on a general-purpose output pin.

Table 54. Bit Descriptions for HYSTERESIS_HIGH

HYSTERESIS_HIGH Address: 0xF3, Reset: 0xFFFF				Setting	Description
Name	Bit NO.	Type	Reset		
HYSTERESIS_HIGH	[15:0]	R/W	0xFFFF		Value setting the higher hysteresis threshold, expressed in direct format.

HYSTERESIS STATUS REGISTER

This status register reports whether the hysteretic comparison is above or below the user-defined thresholds and the IOUT_OC_WARNING status.

Table 55. Bit Descriptions for STATUS_HYSTERESIS

STATUS_HYSTERESIS Address: 0xF4, Reset: 0x00				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[7:4]	Reserved	0x0		Always reads as 0000.
IOUT_OC_WARN	3	R	0x0	0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.
				1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command.
HYST_STATE	2	R	0x0	0	Hysteretic comparison output: output low.
				1	Hysteretic comparison output: output high.
HYST_GT_HIGH	1	R	0x0	0	Compared value is below upper threshold.
				1	Compared value is above upper threshold.
HYST_LT_LOW	0	R	0x0	0	Compared value is above lower threshold.
				1	Compared value is below lower threshold.

START-UP I_{OUT} LIMIT REGISTER

This sets the initial current limit while the hot swap turns on the MOSFET.

Table 56. Bit Descriptions for STRT_UP_IOUT_LIM

STRT_UP_IOUT_LIM Address: 0xF6, Reset: 0x000F				Setting	Description
Name	Bit NO.	Type	Reset		
RESERVED	[15:4]	Reserved	0x00		Always reads as 0x00.
STRT_UP_IOUT_LIM	[3:0]	R/W	0xF	0000	Current limit during startup: 1/16 × ISET.
				0001	Current limit during startup: 2/16 × ISET.
				0010	Current limit during startup: 3/16 × ISET.
				0011	Current limit during startup: 4/16 × ISET.
				0100	Current limit during startup: 5/16 × ISET.

				0101	Current limit during startup: 6/16 × ISET.
				0110	Current limit during startup: 7/16 × ISET.
				0111	Current limit during startup: 8/16 × ISET.
				1000	Current limit during startup: 9/16 × ISET.
				1001	Current limit during startup: 10/16 × ISET.
				1010	Current limit during startup: 11/16 × ISET.
				1011	Current limit during startup: 12/16 × ISET.
				1100	Current limit during startup: 13/16 × ISET.
				1101	Current limit during startup: 14/16 × ISET.
				1110	Current limit during startup: 15/16 × ISET.
				1111	Current limit during startup: 1 × ISET.

Application and Implementation

Typical Application

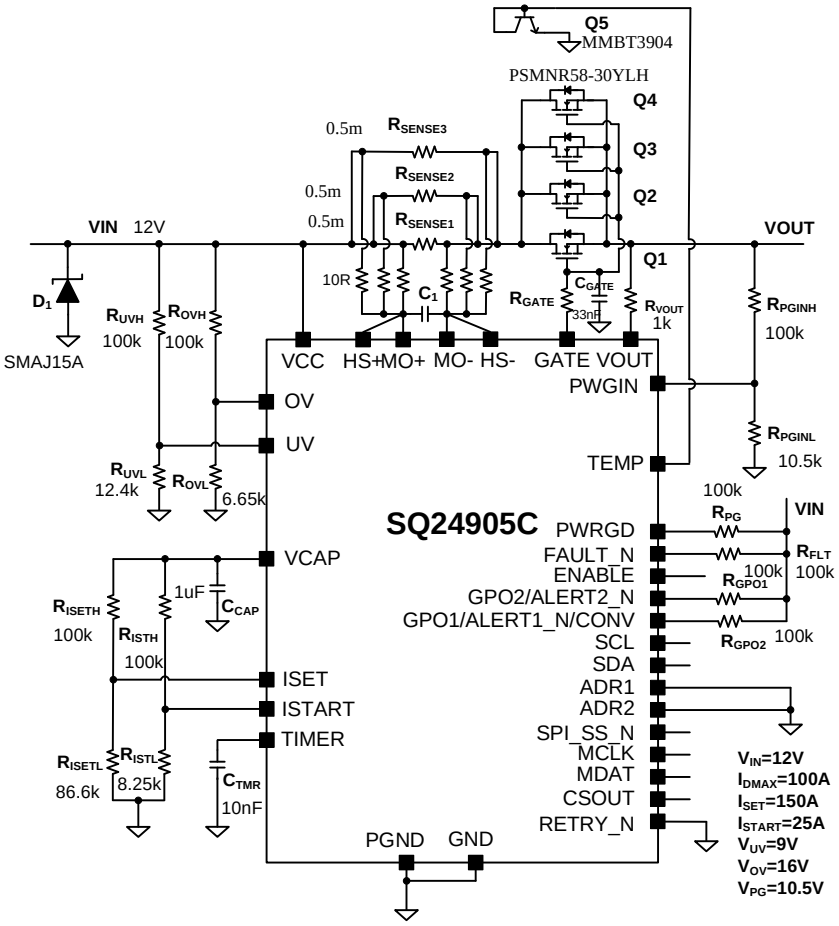


Figure 29. Typical Application Circuit (V_{IN}=12V, I_{OUT}=100A)

Design Requirements

For this design example, use the parameters shown below:

Table 57. System Parameters for Detailed Design

Design Parameter	Example Value
Input supply voltage, V_{IN}	12V
Maximum operating load current, I_{OUT}	100A
Total load capacitance, C_{LOAD}	8800μF
Operating temperature	0℃~60℃
Current Limit at Normal operation, I_{SET}	150A
INRUSH current	10A
Current Limit at start-up operation, I_{START}	25A
Undervoltage falling threshold, V_{UV}	9V
Overvoltage rising threshold, V_{OV}	16V
Power Good Target at VOUT, VPG	10.5V

Detailed Design Procedure

Step 1: Choose the Current Sense Resistance

For higher sampling accuracy, the current sense voltage should be around 20mV to 25mV when the output current reaches the current limit value (I_{SET}).

The current sense resistance can be calculated as follows:

$$R_{SENSE\_MIN} = 20mV/150A = 0.133m\Omega$$
$$R_{SENSE\_MAX} = 25mV/150A = 0.166m\Omega$$

If a resistance of 0.16mΩ is selected for the peak current limit of 150A, it will dissipate 3.7W at 150A, exceeding the rated power (1W) of a typical 2512 package sense resistor. Additionally, a 0.16mΩ resistor is difficult to acquire from manufacturers. Three 0.5mΩ, 1% accuracy, 3W rated power, 2512 package sense resistors are suitable for this system.

The power dissipation of each sense resistor at the peak 150A current and rated 100A current is 1.25W (41.6% of rated power) and 0.544W (18% of rated power), respectively, calculated as follows:

$$P_{SENSE\_PEAK\ CURRENT} = 50A \times 50A \times 0.5 = 1.25W$$
$$P_{SENSE\_RATED\ CURRENT} = 33A \times 33A \times 0.5 = 0.544W$$

If using more than one sense resistor, each sense resistor should have its own separate Kelvin sample trace.

Step 2: Choose the MOSFET(s)

The SQ24905C is designed to use an N-channel MOSFET with a gate-to-source voltage rating of 20V. Devices with lower gate-to-source voltage ratings can be used if a Zener diode is connected to limit the maximum gate-to-source voltage across the transistor.

The next factor that needs to be considered is the MOSFET's drain-to-source voltage rating, VDS(MAX). Although the MOSFET only sees 12V DC, it may experience much higher transient voltages during extreme conditions, such as the abrupt shutoff during a fast trip. A TVS may be required to limit inductive transients under such conditions. A transistor with a $V_{DS(MAX)}$ rating of at least twice the nominal input power-supply voltage is recommended regardless of whether a TVS is used.

Next, select the on-resistance of the transistor, R_{DSON}. Consider the effect of R_{DSON} on the maximum operating temperature T_{JMAX} of the MOSFET. Most manufacturers list $R_{DSON\ (MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived.

The following equation computes the value of $R_{DSON(MAX)}$ at a junction temperature of $T_{J(MAX)}$:

$$R_{DSON(MAX)} = \frac{T_{JMAX} - T_{AMAX}}{I_{MAX}^2 \times R_{\theta JA}}$$

Taking these factors into consideration, the N-channel 30V, 0.67mΩ, 380A MOSFET (PSMNR58-30YLH) is selected for this application. The value of $R_{DSON(MAX)}$ at the maximum junction temperature can be computed using the above equation.

$$R_{DSON(MAX)} = \frac{175℃ - 60℃}{150A^2 \times 42℃/W} = 0.12m\Omega$$

However, the maximum R_{DSON} of PSMNR58-30YLH at 175℃ junction temperature is 1.41mΩ. Therefore, more than one MOSFET is required for this application. The calculations for using one to five MOSFETs are shown in the following table:

Table 58. The Required $R_{DSON(MAX)}$ at T_{JMAX} for 1 to 5 MOSFETs When T_A=60℃

Number of MOSFETs	Current for each MOSFET/A	The required $R_{DSON(MAX)}$ at T_{JMAX} for each MOSFET/mΩ	The evaluated T_J of each MOSFET/°C
1	150	0.12	1392
2	75	0.49	393
3	50	1.10	208
4	37.5	1.95	143
5	30	3.04	113

Therefore, four or five MOSFETs (PSMNR58-30YLH) suit this application.

Step 3: Set the Current Limit at Normal Operation by the ISET Pin

The output current limit during normal operation is 150A. The difference between the current limit at normal operation (I_{SET}) and the circuit breaker trip current (I_{CB}) creates a voltage gap (V_{CBOS}).

The value of I_{CB} can be calculated as follows:

$$I_{CB} = I_{SET} - \frac{V_{CBOS}}{R_{SENSE}} = 150A - \frac{1.5mV}{0.166m\Omega} = 141A$$

There is a margin of 41A for the maximum operation output current, which is 100A. The above equation uses the maximum value (1.5mV) of VCBOS for the design margin.

Next, calculate the necessary ISET pin voltage with the following equation:

$$V_{ISET} = I_{SET} \times R_{SENSE} \times 50 = 150A \times 0.166m\Omega \times 50 = 1.25V$$

The VCAP is utilized as the source of the ISET divider resistor circuit, as shown in Figure 29. The divider resistance should be greater than 10kΩ to guarantee the high accuracy of the VCAP.

Assuming that the R_{ISETH} is 100kΩ, the resistance of R_{ISETL} can be calculated as follows:

$$\frac{V_{ISET}}{V_{CAP}} = \frac{R_{ISETL}}{R_{ISETH} + R_{ISETL}}$$

$$R_{ISETL} = \frac{R_{ISETH}}{\frac{V_{CAP}}{V_{ISET}} - 1} = \frac{100k}{\frac{2.7V}{1.25V} - 1} = 86.2k$$

Therefore, an 86.6kΩ, 1% resistor is selected for R_{ISETL}.

Step 4: Select C_{GATE} and calculate the Output Voltage Ramp Time.

The SQ24905C enables a linear voltage ramp on the output during the startup phase to reduce inrush currents by using an extra component, C_{GATE}. Set the output voltage ramp by choosing the appropriate CGATE value to prevent inrush current from reaching or exceeding the active current-limit level. Assuming that only the load capacitance draws current during start-up, the C_{GATE} value can be calculated as follows:

$$C_{GATE} = C_{LOAD} \times \frac{I_{GATEUP}}{I_{INRUSH}} = 8.8mF \times 1.2 \times \frac{26uA}{10A} = 27.5nF$$

Where:

- I_{GATEUP} is the specified gate pull-up current.
- I_{INRUSH} is the user-desired constant load current during the load capacitance charging time.

The previous equation uses the maximum possible load capacitance (1.2 times the typical value) to provide design margin.

The GATE capacitance should be larger than the calculated value. A 33nF capacitor is selected for C_{GATE} in this example.

The resulting output voltage ramp time can be calculated as follows:

$$t_{RAMP} = \frac{V_{IN} \times C_{GATE}}{I_{GATEUP}} = \frac{12V \times 33nF}{26uA} = 15.2ms$$

The real max inrush current is:

$$I_{INRUSH\_MAX} = \frac{V_{IN} \times C_{LOAD}}{t_{RAMP}} = \frac{12V \times 8.8mF \times 1.2}{15.2ms} = 8.33A$$

Therefore, a 33nF capacitor is suitable for C_{GATE}.

Step 5: Set the Current Limit at Start-Up by the ISTART Pin

The current limit at start-up (I_{START}) can be set by the user. If this current limit is not desired, connect the ISTART pin to the VCAP. For this application, the current limit at start-up, I_{START}, is 25A.

Next, check the margin between the circuit breaker trip current (I_{CB_ST}) of I_{START} and the inrush current.

$$I_{CB\_ST} = I_{START} - \frac{V_{CBOS}}{R_{SENSE}} = 25A - \frac{1.5mV}{0.166m\Omega} = 16A$$

The circuit breaker trip current (I_{CB_ST}) of I_{START} exceeds the maximum inrush current by a margin of 7.67A.

Similar to the calculation method of ISET, the ISTART pin voltage can be calculated as follows:

$$V_{ISTART} = I_{START} \times R_{SENSE} \times 50 = 25A \times 0.166m\Omega \times 50 = 0.208V$$

It is recommended that the divider resistance is greater than 10kΩ to guarantee the high accuracy of the VCAP voltage. Assuming that the R_{ISTH} is 100kΩ, the resistance of R_{ISTL} can be calculated as:

$$R_{ISTL} = \frac{R_{ISTH}}{\frac{V_{CAP}}{V_{ISTART}} - 1} = \frac{100k}{\frac{2.7V}{0.208V} - 1} = 8.3k$$

Therefore, an 8.25kΩ, 1% resistor is selected for R_{ISTL}.

Step 6: Choose TIMER Capacitance

The safe operating area (SOA) chart of the MOSFET is crucial for designing TIMER capacitance. The following chart displays the SOA of the PSMNR58-30YLH.

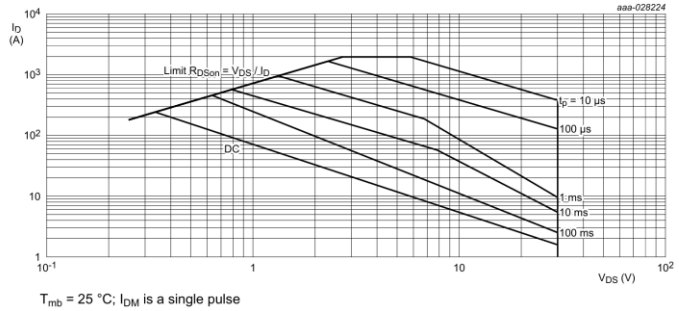


Figure 30. SOA of the MOSFET

The worst-case scenario for the MOSFET occurs when only a single MOSFET is active, the input voltage is close to the OV threshold, and the device starts up with the output shorted to GND. In this scenario, V_{DS} equals $V_{IN,}$ and the start-up current limit is triggered. From the SOA chart of the PSMNR58-30YLH, the critical time is approximately 2ms under the conditions V_{DS}=16V (OV voltage) and I_D=25A. The fault duration time must be less than 2ms; for instance, 800µs is selected.

The TIMER capacitance can be calculated as follows:

$$C_{TIMER} = \frac{I_{TIMERUP\_FLT} \times t_{DURATION}}{V_{th}} = \frac{60uA \times 800us}{1V} = 48nF$$

After considering all the tolerances it can be determined that a 10nF capacitor，which result in a timer fault time of 167µs，can provide maximum FET protection. If a longer fault filter time is desired then a 22nF or 33nF TIMER capacitor will also provide sufficient protection.

Therefore, the TIMER capacitance, CTMR, can be set to 10nF.

Step 7: Set Undervoltage and Overvoltage (UV & OV)

The user can set the undervoltage (UV) and overvoltage (OV) thresholds. For this application, the UV falling threshold is 9V, and the OV rising threshold is 16V. A reference voltage of 1V is used to compare with the voltage at the UV and OV pins.

Assuming R_{UVH} and R_{OVH} are 100kΩ, the resistances of R_{UVL} and R_{OVL} can be calculated as follows:

$$R_{UVL} = \frac{100k}{\frac{9V}{1V} - 1} = 12.5k$$

$$R_{OVL} = \frac{100k}{\frac{16V}{1V} - 1} = 6.66k$$

A 12.4kΩ, 1% resistor is selected for R_{UVL} and a 6.65kΩ, 1% resistor is selected for R_{OVL}.

Step 8: Set Power Good Input Threshold

The user can set the power good voltage at VOUT. For this example, the power good falling threshold is 10.5V. The reference voltage to compare with the voltage at the PWGIN pin is 1V.

If R_{PGINH} is set to 100kΩ, the R_{PHINL} resistance can be calculated as follows:

$$R_{PHINL} = \frac{100k}{\frac{10.5V}{1V} - 1} = 10.5k$$

Step 9: Choose Temperature Sensor

The temperature sensor can be either a PNP or NPN transistor connected as a diode. For an NPN transistor, connect the collector and base to the TEMP pin and the emitter to PGND. For a PNP transistor, connect the collector and base to PGND and the emitter to TEMP. Transistors like 2N3904, 2N3906, and MMBT3904 with SOT-23 packages are suitable.

Step 10: Choose R_{GATE}, R_{PG}, R_{FLT}, R_{GPO1}, and R_{GPO2}

In the typical application diagram on the front page, the gate resistor, R_{GATE}, is intended to suppress high frequency oscillations. A resistor of 10Ω is suitable for this application. Applications with larger MOSFETs and very short wiring may not require R_{GATE}.

The resistors, R_{PG}, R_{FLT}, R_{GPO1}, and R_{GPO2}, serve as pullups for the open-drain output drivers. 100kΩ resistor values are recommended for these resistors.

Step 11: Power Supply Recommendations

A 10-nF to 1-µF ceramic capacitor bypasses the VCC pin to GND. When the input bus power feed is inductive (the trace is long between power sources to SQ24905C), a transient voltage suppressor (TVS) may also be required. The maximum clamping voltage (V_C) at I_{pp} must be lower than the VCC absolute maximum voltage of SQ24905C (30V). Considering this the above, a TVS diode, SMAJ15A, with a maximum clamping voltage of 24.4V is chosen for this application.

Application Schematic

(V_{IN}=12V, I_{OUT}=100A, I_{SET}=150A, I_{START}=25A)

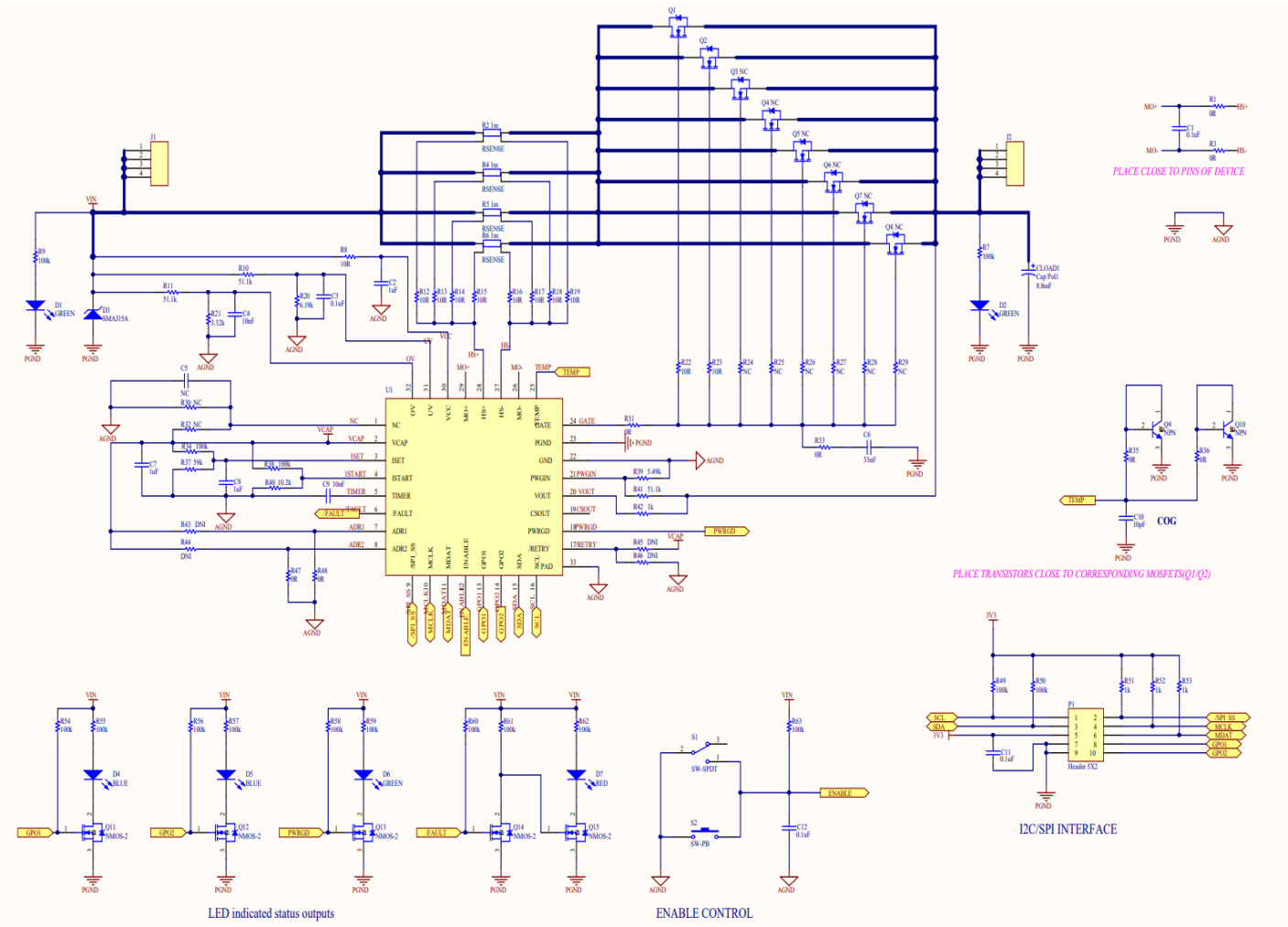


Figure 31. Schematic Diagram

BOM List

Designator	Description	Value
U1	SQ24905CQEQ	
C1, C3, C11, C12	Cap, 50 V, 0603	0.1μF
C2, C7, C8	Cap, 25 V, 0805	1μF
C4, C9	Cap, 50 V, 0603	10nF
C5	NC	
C10	Cap, 50 V, 0603	10pF
C6	Cap, 50 V, 0603	33nF
CLOAD1	Cap Poly	8.8mF (NC)
D1, D2, D4, D5, D6	LED, BLUE	
D3	TVS Diode, SMAJ15A	
D7	LED, RED	
P1	Header 2X5	
Q1, Q2	MOSFET, N-channel 30V, 0.67mΩ, 380A, PSMNR58-30YLH	
Q9, Q10	NPN transistor, SOT-23 MMBT3904	
Q3, Q4, Q5, Q6, Q7, Q8	NC	
Q11, Q12, Q13, Q14, Q15	MOSFET, N-Ch, 60 V, 0.115 A, SOT23 2N7002-7-F	
R1, R3, R8, R31, R33, R35, R36, R47, R48	Res, 0.1W, 0603	0Ω
R2, R4, R5, R6	RSENSE, 3W, 1%, 2512	1mΩ
R10, R11, R41	Res, 0.1W, 0603	51.1k
R12, R13, R14, R15, R16, R17, R18,R19, R22, R23	Res, 0.1W, 0603	10Ω
R24, R25, R26, R27, R28, R29	NC	
R20	Res, 0.1W, 0603	6.19k
R21	Res, 0.1W, 0603	3.32k
R30, R32	NC	
R37	Res, 0.1W, 0603	59k
R39	Res, 0.1W, 0603	5.49k
R40	Res, 0.1W, 0603	10.2k
R42, R51, R52, R53	Res, 0.1W, 0603	1k
R43, R44, R45, R46	Res, 0.1W, 0603	DNI
R7, R9, R34, R38, R49, R50, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63	Res, 0.1W, 0603	100k
S1	SPDT slide switch (NC)	
S2	Push button	

PCB Layout Guide

For optimal performance of the SQ24905C, the following guidelines must be followed:

1. The HS+ and HS- pins require a Kelvin sense connection to the current sense resistor. If multiple sense resistors are used, each should have its own separate Kelvin sampling trace.
2. The MO+ and MO- pins should be connected to HS+ and HS- correspondingly, as close to the device as possible.
3. The filtering capacitors on MO+ and MO- should be placed as close to the device as possible.
4. Place a 1μF or greater ceramic decoupling capacitor between the VCC pin and GND, as close to the device as possible.

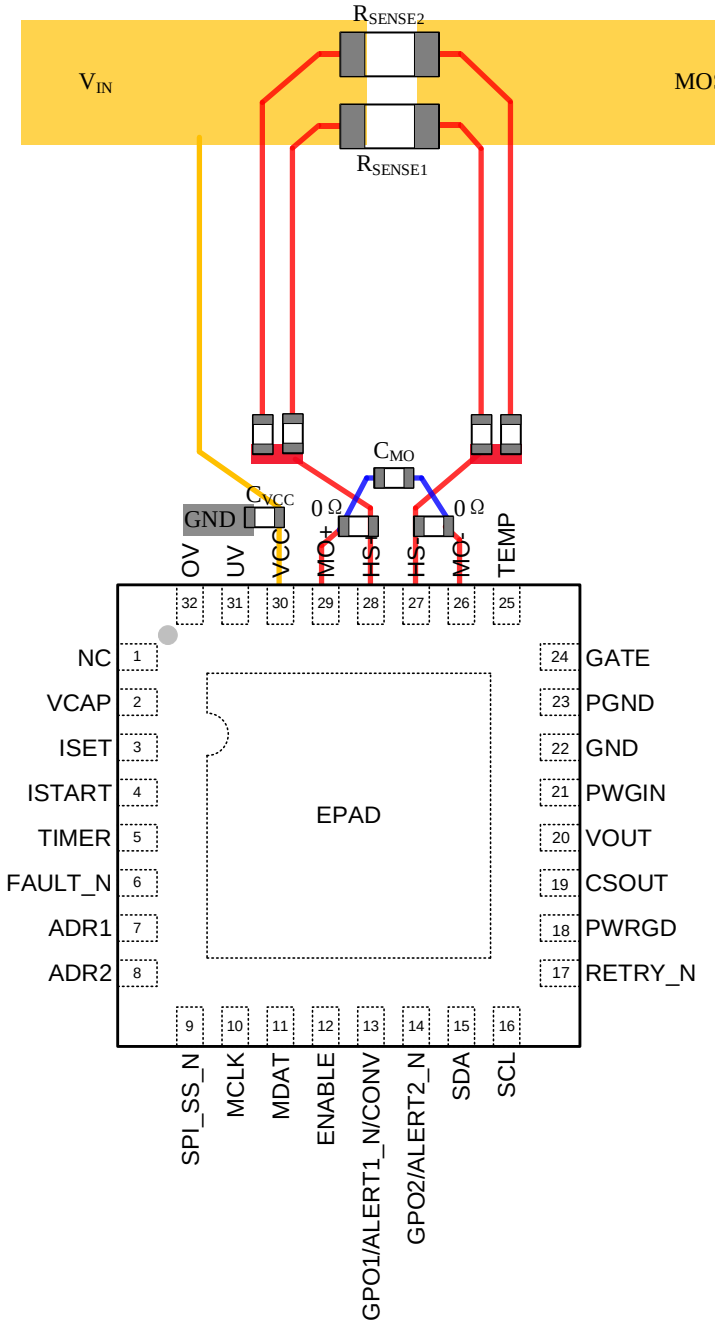
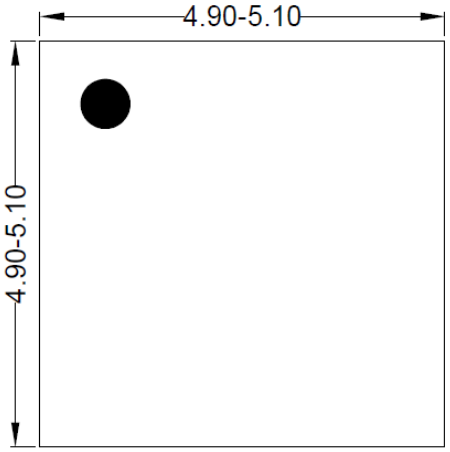
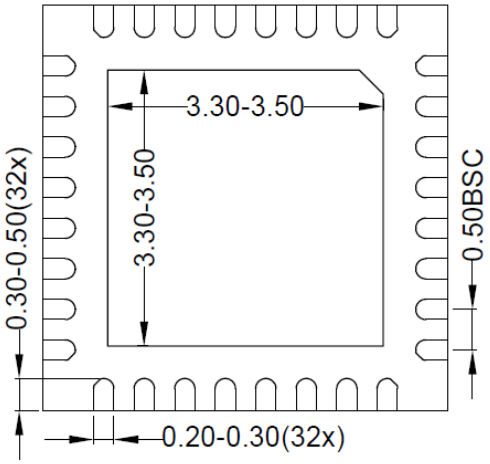


Figure 32. PCB Layout Suggestion

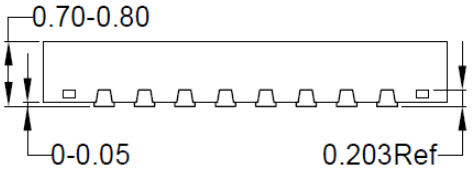
QFN5×5-32 Package Outline & PCB Layout



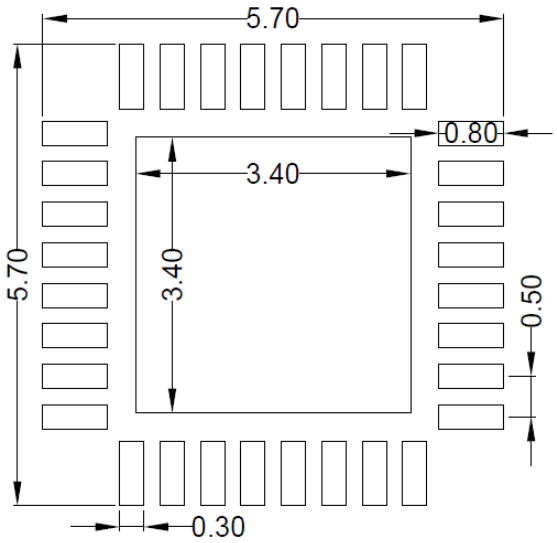
Top View



Bottom View



Front View

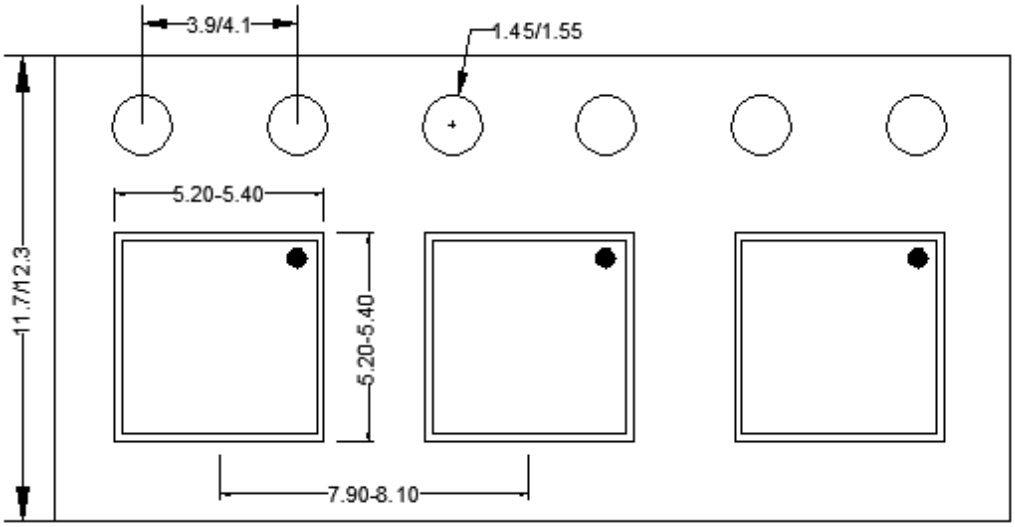


Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

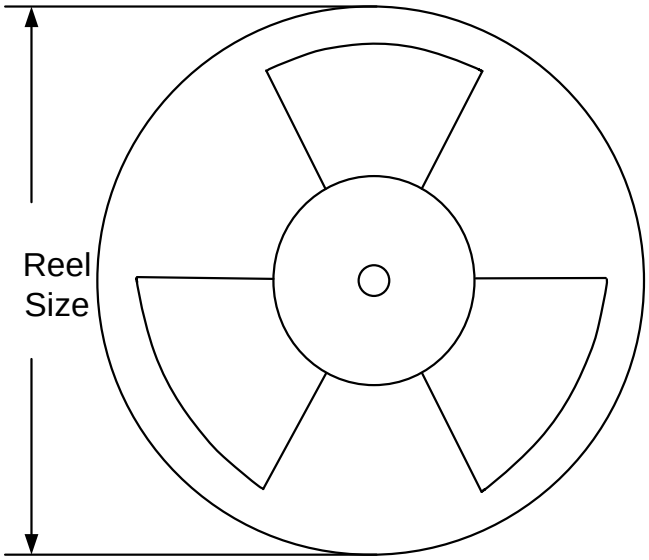
Tape and Reel Information

QFN5×5-32 Tape Dimensions and Pin1 Orientation



Feed Direction →

Reel Dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
QFN5×5-32	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 21, 2025	Revision 1.0A	Change the Pin1 Orientation from the first quadrant to the second quadrant.
Apr. 07, 2025	Revision 1.0	Initial Release

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