SY26151

High Efficiency Fast Response, 1.5A, 18V Input Synchronous Buck Converter

General Description

The SY26151 high efficiency 750kHz synchronous Buck converter operates over a wide input voltage range from 4.5V to 18V, and can deliver up to 1.5A output current. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss.

The SY26151 adopts constant on-time and valley current control to achieve fast transient response for applications with high step-down ratios and high efficiency at light loads. It also provides cycle-by-cycle current limit and over temperature protection.

The SY26151 is highly integrated, so only the input and output capacitors, the inductor, and the feedback resistors need to be selected for the targeted application specifications.

The SY26151 is available in a compact DFN2x2-8 package.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 80mΩ Top, 40mΩ Bottom
- Wide Input Voltage Range: 4.5V ~ 18V
- Up to 1.5A Output Current
- ±1.5% Reference Accuracy
- Internal Soft-Start Limits the Inrush Current
- 750kHz Switching Frequency
- Constant On-Time and Valley Current Control to Achieve Fast Transient Response.
- Cycle-by-Cycle Peak and Valley Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- Startup from Pre-Biased Output
- Power Good Indicator
- RoHS Compliant and Halogen Free
- MSL Rating: MSL1 (DFN2x2-8)

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Application

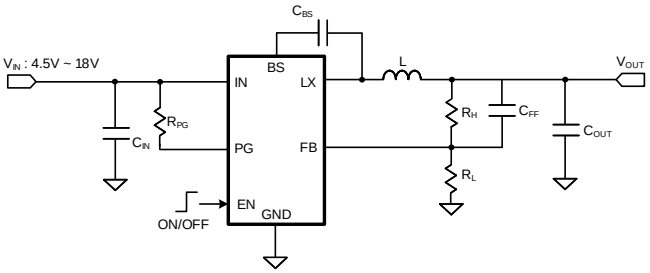


Figure1. Schematic Diagram

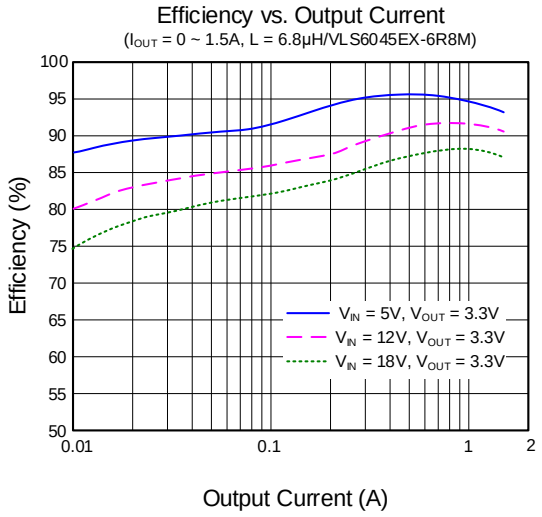


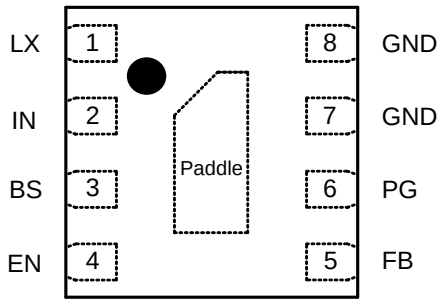
Figure2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26151DFD	DFN2x2-8 RoHS Compliant and Halogen Free	**2h*xyz***

x=year code, y=week code, z= lot number code

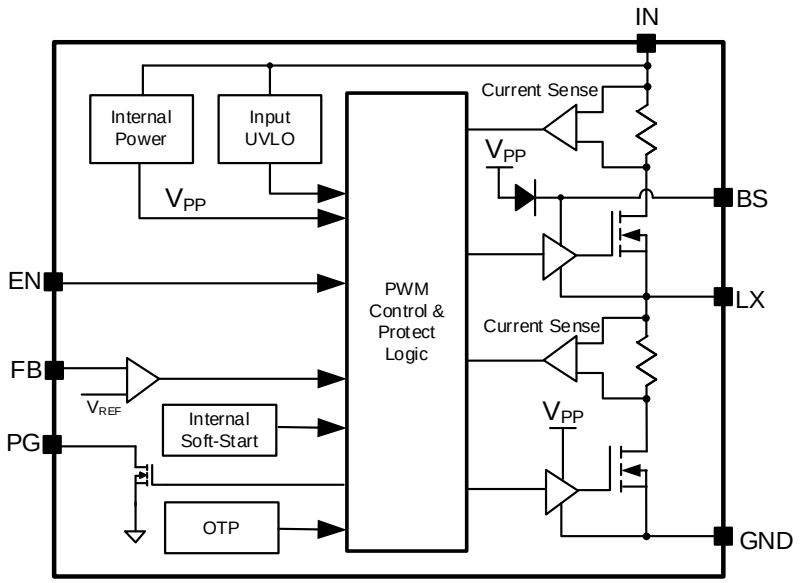
Pinout (top view)



Pin Description

Pin Number	Pin Name	Pin Description
1	LX	Inductor pin. Connect this pin to the switching node of the inductor.
2	IN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
3	BS	Boot-strap pin. Supply high side gate driver. Connect a 0.01μF ceramic capacitor between the BS pin and the LX pin.
4	EN	Enable control pin of the device. Pull this pin high to turn on the device. Pull this pin low to turn off the device. Do not leave this pin floating.
5	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure1) to program the output voltage: $V_{OUT} = 0.8 \times (1 + R_H / R_L)$.
6	PG	Power good indicator pin. Open drain output when the output voltage is higher than 94% of regulated value.
7, 8	GND	Ground pin.
Paddle	NC	Not connected network, layout with GND copper for good heat dissipation.

Block Diagram



Figue3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	19	V
EN, LX, PG	-0.3	IN + 0.3	
LX, 10ns duration	GND - 5	IN + 3	
BS	LX - 0.3	LX + 4	
FB	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	65	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	10	
P_D Power Dissipation T_A = 25°C	1.54	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4.5	18	V
Output Current		1.5	A
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified.(note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		4.5		18	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	T_J = -40°C to + 85°C			4.5	
	UVLO Hysteresis	$V_{IN,HYS}$			0.3		
	Quiescent Current	I_Q	I_{OUT} = 0A, EN = High, V_{FB} = V_{REF} × 105%		140		µA
	Shutdown Current	I_{SHDN}	EN = Low, T_J = 25°C		5	10	
	Feedback Reference Voltage	V_{REF}	T_J = 25°C	788	800	812	mV
	FB Input Current	I_{FB}	V_{FB} = 1V, T_J = 25°C	-50		50	nA
	Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching (Note5)		300		µs
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET}		1		ms
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			80		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			40		
	Top FET Current Limit Threshold	$I_{LMT,TOP}$		2.5	3.7	5	A
	Bottom FET Current Limit Threshold	$I_{LMT,BOT}$		1.5	3	4.5	
Enable(EN)	Input Voltage High	$V_{EN,H}$		1.5			V
	Input Voltage Low	$V_{EN,L}$				0.4	
PG	Rising Threshold	$V_{PG,R}$	V_{FB} rising (good)		94		%V_{REF}
	Hysteresis	$V_{PG,HYS}$			4		
Frequency	Switching Frequency	f_{SW}	T_J = 25°C, V_{OUT} = 3.3V, CCM	650	750	900	kHz
	Min On-Time	$t_{ON,MIN}$			60		ns
	Min Off-Time	$t_{OFF,MIN}$			200		
OTP	Temperature	T_{OTP}	(Note5)		150		°C
	Temperature Hysteresis	T_{HYS}	(Note5)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 6cm×6cm size, two-layer Silergy Evaluation Board with 2-oz copper. Paddle of DFN2x2-8 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

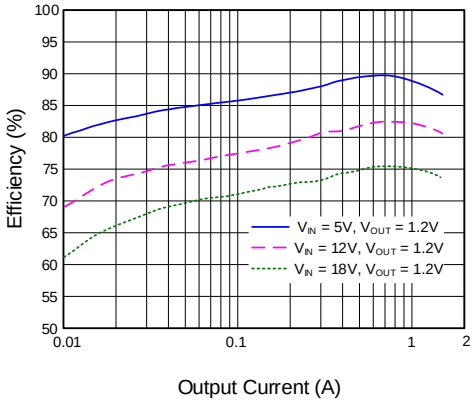
Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

(SY26151, T_A = 25°C, V_{IN} = 12V, V_{OUT} = 3.3V, L = 6.8µH, C_{OUT} = 44µF, unless otherwise noted)

Efficiency vs. Output Current

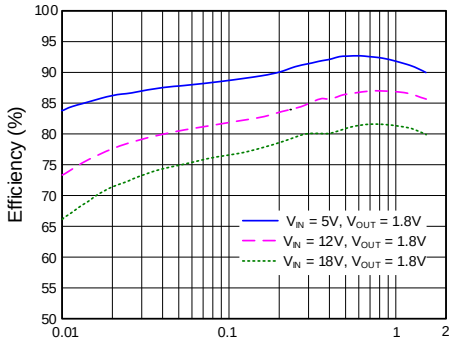
(I_{OUT} = 0 ~ 1.5A, L = 2.2µH/VLS6045EX-2R2N)



Output Current (A)

Efficiency vs. Output Current

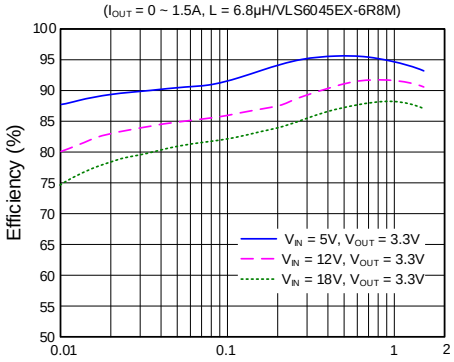
(I_{OUT} = 0 ~ 1.5A, L = 3.3µH/VLS6045EX-3R3N)



Output Current (A)

Efficiency vs. Output Current

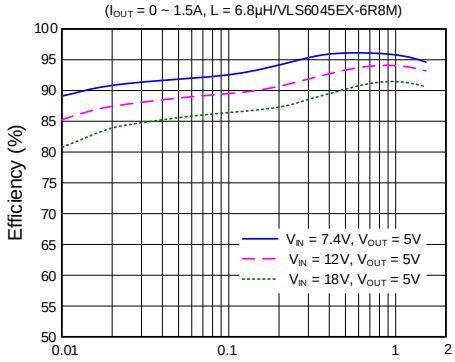
(I_{OUT} = 0 ~ 1.5A, L = 6.8µH/VLS6045EX-6R8M)



Output Current (A)

Efficiency vs. Output Current

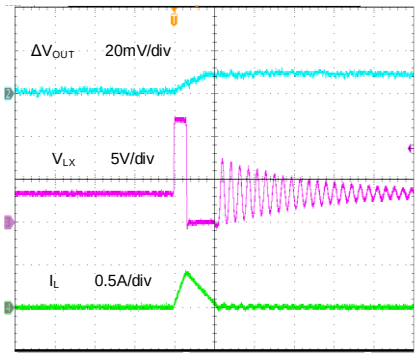
(I_{OUT} = 0 ~ 1.5A, L = 6.8µH/VLS6045EX-6R8M)



Output Current (A)

Output Ripple

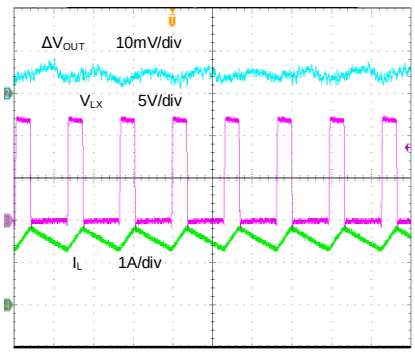
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A)



Time(1µs/div)

Output Ripple

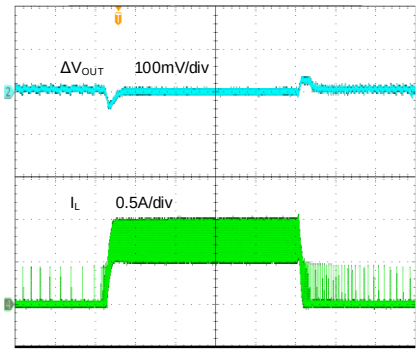
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A)



Time(1µs/div)

Load Transient

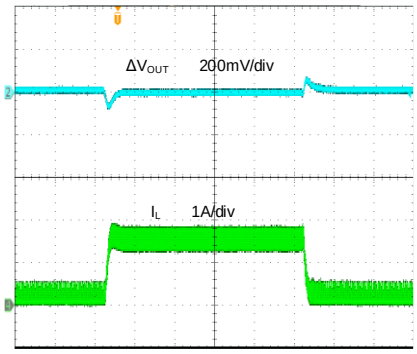
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 0.75A)



Time(100μs/div)

Load Transient

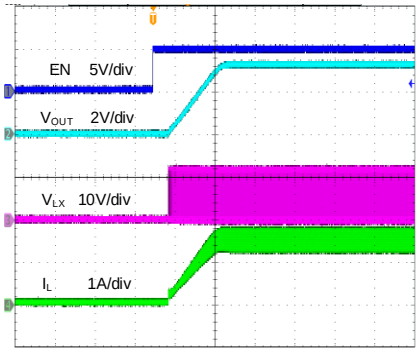
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.15A ~ 1.5A)



Time(100μs/div)

Startup from Enable

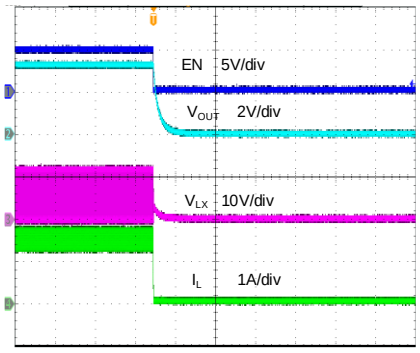
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A)



Time(800μs/div)

Shutdown from Enable

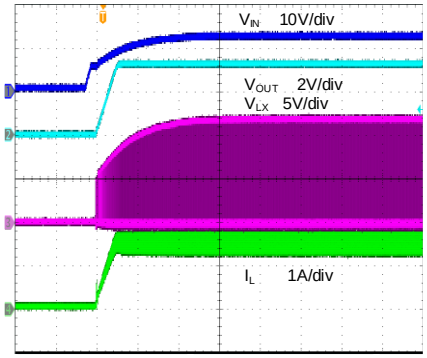
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A)



Time(800μs/div)

Startup from V_{IN}

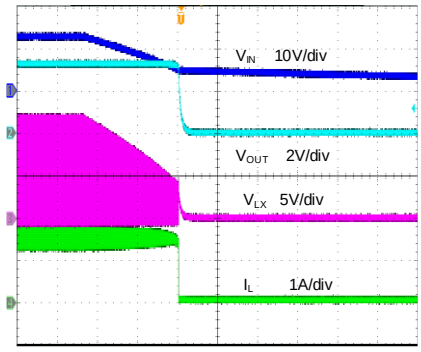
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A)



Time(2ms/div)

Shutdown from V_{IN}

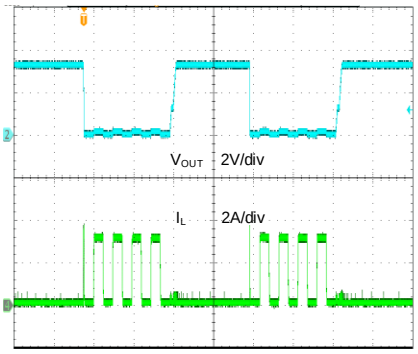
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A)



Time(2ms/div)

Short Circuit Protection

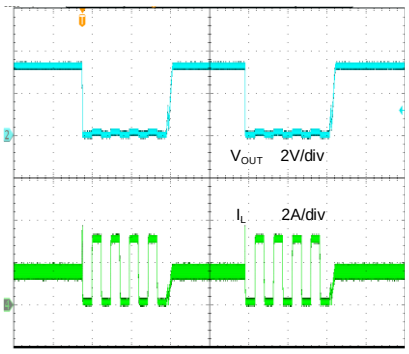
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ short)



Time(10ms/div)

Short Circuit Protection

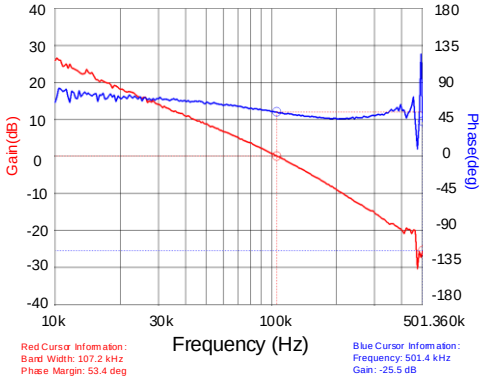
(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A ~ short)



Time(10ms/div)

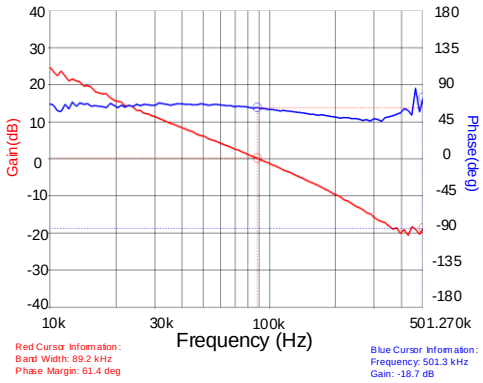
Bode Plot

(V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 1.5A)



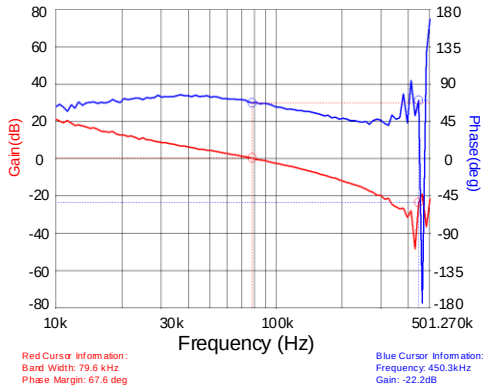
Bode Plot

(V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 1.5A)



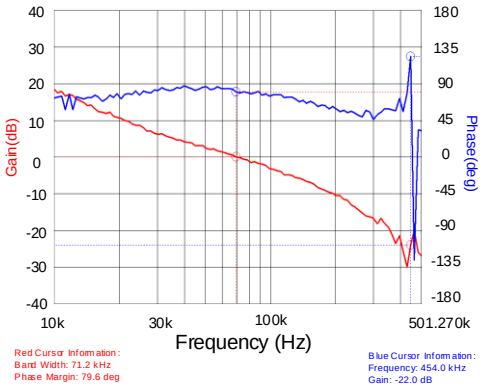
Bode Plot

(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A)

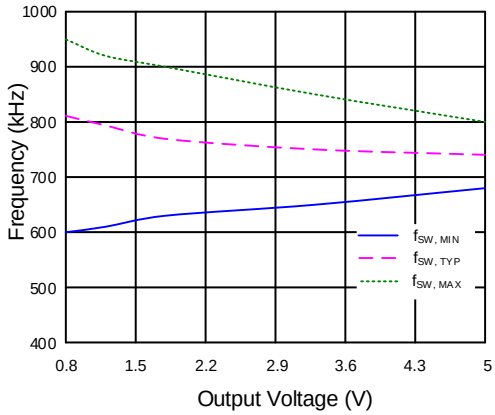


Bode Plot

(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.5A)



Switching Frequency vs. Output Voltage
(V_{IN} = 12V, V_{OUT} = 0.8V ~ 5V, CCM)



Detailed Description

The SY26151 high efficiency 750kHz synchronous Buck converter operates over a wide input voltage range from 4.5V to 18V, and can deliver up to 1.5A output current. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss.

The SY26151 adopts constant on-time and valley current control to achieve fast transient response for applications with high step-down ratios and high efficiency at light loads. It also provides cycle-by-cycle current limit and over temperature protection.

The SY26151 employs a constant on-time and valley current mode control strategy. When the bottom FET's current-sense signal reaches internal V_{COMP}, the top FET turns on for a fixed period of time (constant t_{ON}). t_{ON} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

The bottom FET turns on after a period of t_{ON}.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on-time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under T_J = -40℃ ~ 125℃ condition, the device can support up to 60% duty cycle operation .

Input Under Voltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the top FET and bottom FET can be sufficiently enhanced, the SY26151 incorporates one input under voltage lockout protection. The device remains in a low current state and LX switching actions are inhibited until V_{IN} exceeds its own UVLO (rising) threshold. At that time, if EN is enabled, the device will startup by initiating a soft-start ramp. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX switching actions will again be suppressed.

Enable Control

The EN input is a high-voltage-capable input with logic-compatible threshold. When EN is driven > 1.5V, normal device operation will be turned on. When driven < 0.4V, the device will be turned off, reducing the input current to < 10μA.

It is not recommended to connect EN pin and V_{IN} directly. A resistor in a range of 1kΩ to 1MΩ should be used if EN is pulled high by V_{IN}.

Soft-Start

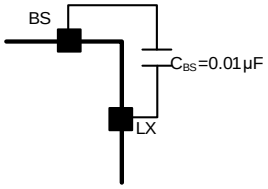
The SY26151 incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup.

Output Power Good Indicator

The power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG FET is turned on so that PG is pulled to GND before output voltage is ready. After feedback voltage V_{FB} reaches $V_{PG,R}$ for typical 30μs, PG is pulled high. When V_{FB} drops to $V_{PG,R}$ – $V_{PG,HYS}$ for typical 4μs , PG is pulled low.

External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top FET. Proper operation requires a 0.01μF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top FET.



Fault Protection Modes

Output Current Limit

If the top FET current exceeds the top current limit threshold, the top FET will be turned off and the bottom FET will be turned on. If the bottom FET current exceeds the bottom current limit threshold, the bottom FET will keep turning on until the bottom FET current decreases below the bottom current limit threshold.

Output Short Circuit Protection

With output current increasing, as soon as the bottom FET current exceeds the bottom current limit threshold, the output voltage drops. If the load current continues to increase, when the output voltage falls below 33% of the regulated level, the output under voltage protection will be

activated and the device will operate in hiccup mode. The hiccup on-time is 2.4ms, and the hiccup off-time is 2.4ms. If the hard short condition is removed, the device will return to normal operation.

Over Temperature Protection (OTP)

The device includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

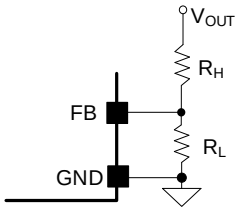
Application Information

The following paragraphs describe the selection process for the feedback resistors (R_H and R_L), input capacitor C_{IN}, output inductor L, output capacitor C_{OUT}, and feedforward capacitor C_{FF}.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R_H and R_L to minimize power consumption under light loads. If V_{OUT} is 3.3V, a value of 100kΩ is chosen for R_H, then using the following equation, R_L can be calculated as 32kΩ, a standard 1% 32.4kΩ resistor is selected.

$$R_L = \frac{0.8V}{V_{OUT} - 0.8V} \times R_H$$



Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 25V rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by CIN and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$I_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst case condition occurs at D = 0.5, then

$$I_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient in most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance value is calculated as:

$$\mathrm{L} = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 0.4}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY26151 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor

with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 44μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor-current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

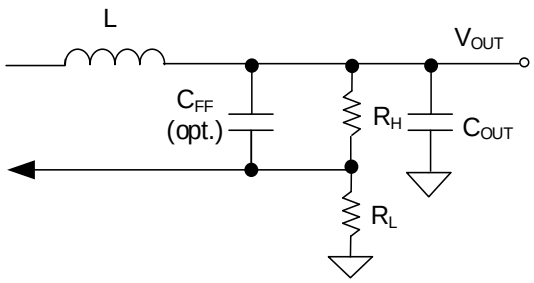
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

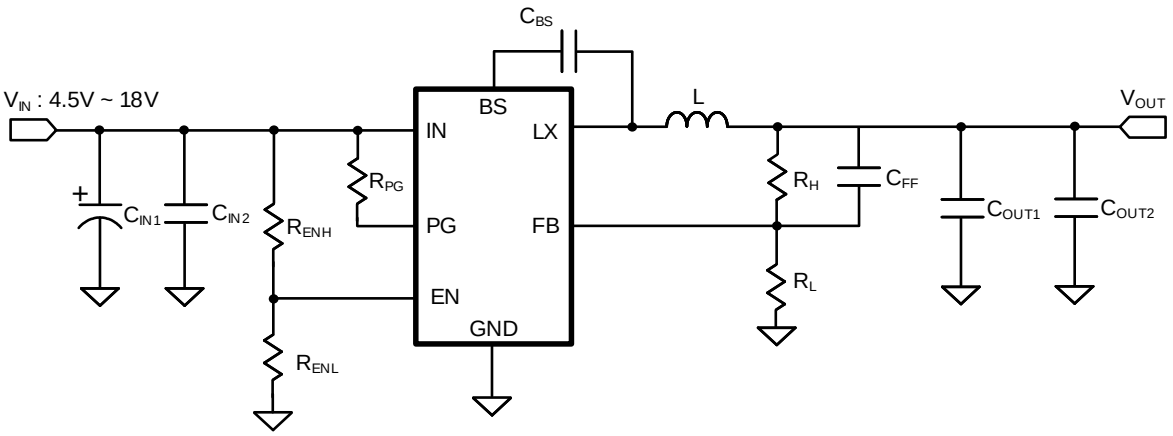
The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Load Transient Considerations

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic capacitor in parallel with R_H may further speed up the load transient response. It is recommended for applications with large load transient step requirements if the phase margin is sufficient.



Application Schematic (V_{OUT} = 3.3V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47µF/50V Electrolytic Capacitor		
C_{IN2}	10µF/25V/X5R, 1206	GRM319R61E106KA12D	muRata
C_{FF}	47pF/50V/C0G, 0603	GRM1885C1H470JA01D	muRata
C_{OUT1}	22µF/16V/X5R, 1206	GRM31CR61C226ME15L	muRata
C_{OUT2}	22µF/16V/X5R, 1206	GRM31CR61C226ME15L	muRata
C_{BS}	0.01µF/50V/X5R, 0603	GRM188R71H103KA01D	muRata
L	6.8µH	VLS6045EX-6R8M	TDK
R_H	100kΩ, 1%, 0603		
R_L	32.4kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		

Recommend Components for Typical Applications

V_{OUT} (V)	R_H (kΩ)	R_L (kΩ)	C_{FF} (pF)	L/Part Number	C_{OUT}
1.2	100	200	22	2.2µH/VLS6045EX-2R2N	2 × 22µF/16V/X5R, 1206
1.8	100	80.6	22	3.3µH/VLS6045EX-3R3N	2 × 22µF/16V/X5R, 1206
3.3	100	32.4	47	6.8µH/VLS6045EX-6R8M	2 × 22µF/16V/X5R, 1206
5	100	19.1	47	6.8µH/VLS6045EX-6R8M	2 × 22µF/16V/X5R, 1206

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND by wide copper plane.

Output Capacitors: Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

Feedback Network: Place the feedback components (R_H, R_L, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

EN Signal: It is not recommended to connect EN signal directly to V_{IN}. A resistor in a range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.

PCB Board: To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

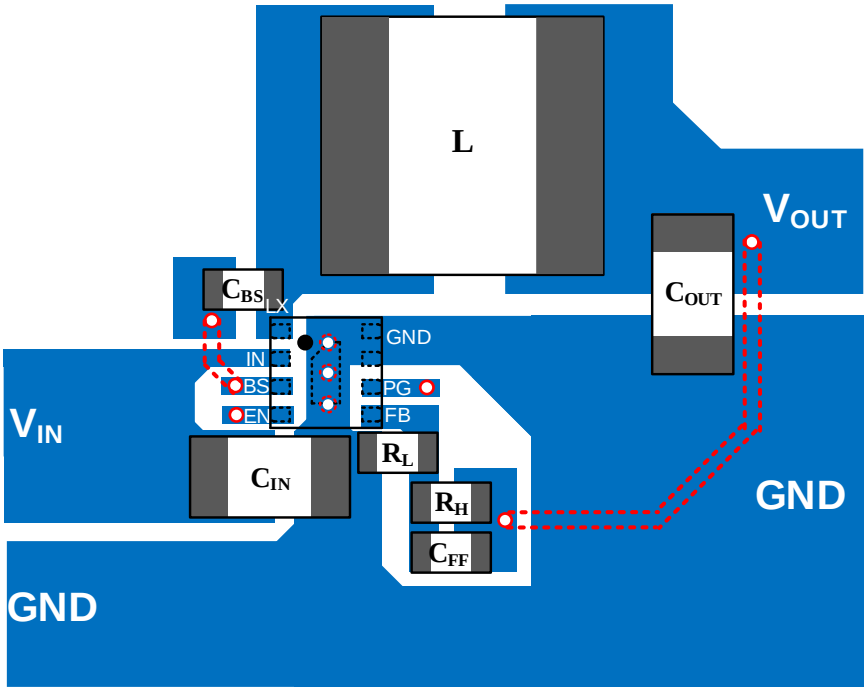
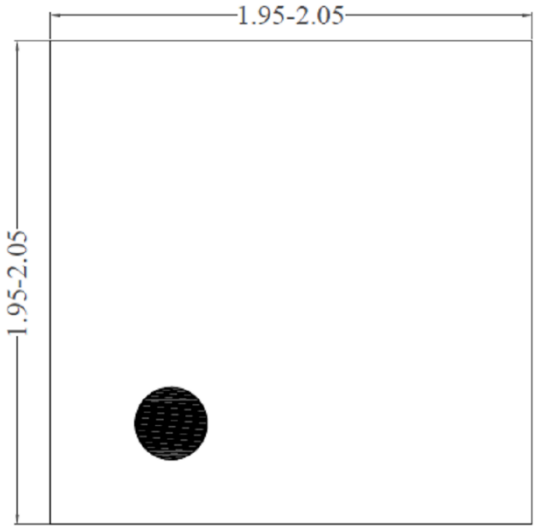
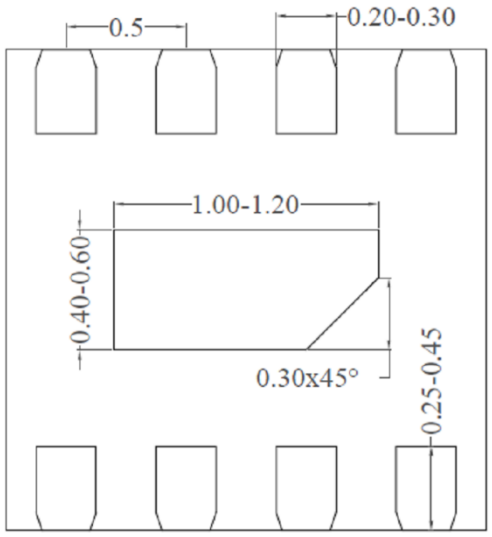


Figure4. Recommended PCB Layout

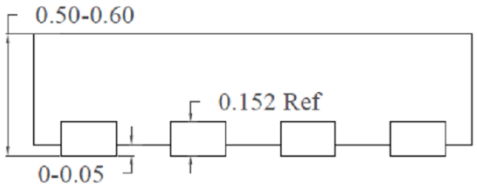
DFN2×2-8 Package Outline Drawing



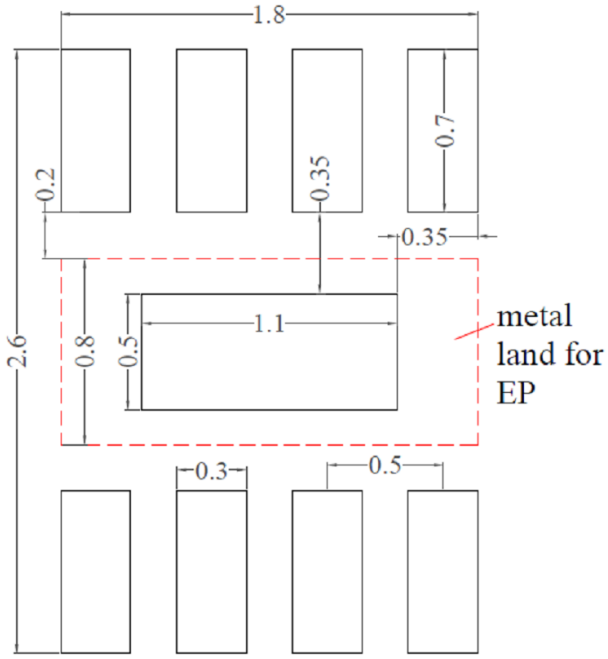
Top View



Bottom View



Side View

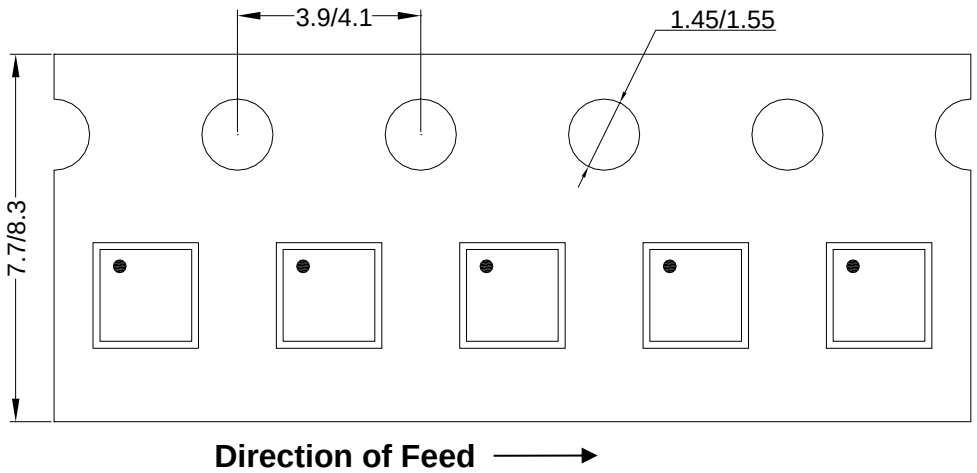


Recommended PCB layout
(Reference only)

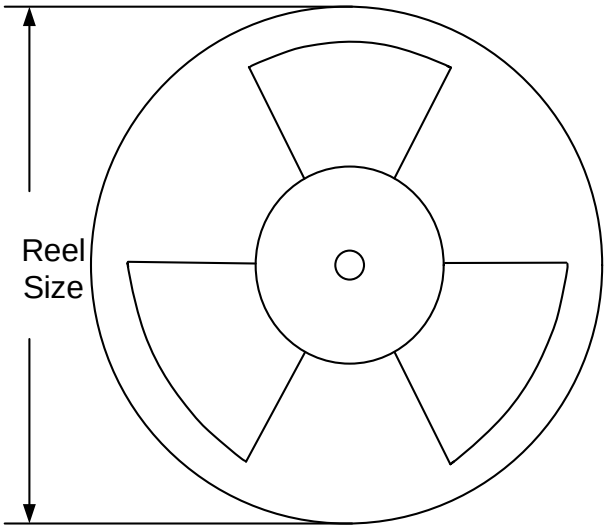
Notes: All dimensions are in millimeters and don't include mold flash & metal burr.

Tape and Reel Information

1. Tape Dimensions and Pin1 Orientation



2. Reel Dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel （pcs）
DFN2×2	8	4	7	400	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Mar. 18, 2025	1.0	Initial Release.	-

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