SA25903

High-Efficiency, 6V, 3A 2.2MHz Synchronous Step-Down Regulator

General Description

The SA25903 is a high-efficiency 2.2MHz synchronous step-down converter that operates over an input voltage range of 2.8V to 6V, and can deliver an output current of up to 3A. It integrates very low $R_{DS(ON)}$ main and synchronous MOSFETs to minimize conduction loss. The 2.2MHz constant switching frequency reduces the required external inductor and capacitor values.

The SA25903 utilizes a constant frequency peak current mode control architecture to achieve stable operation across a wide range of conditions. It also provides cycle-by-cycle current limit protection, output short-circuit protection, and overtemperature protection.

The SA25903 is available in a space-saving SOT583 package.

Features

- 2.8V~6V Input Voltage Range
- Up to 3A Output Current Capability
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 65mΩ/25mΩ
- Constant Frequency Peak Current Mode Control
- 35µA Quiescent Current (Typ.)
- 2.5µA Shutdown Current (Typ.)
- ±1% 0.6V Reference Over -40°C to +150°C
- 2.2MHz Switching Frequency
- Internal Soft-Start Limits Inrush Current
- Forced PWM or PFM Operation Selectable in Light Load
- 100% Duty Cycle Dropout Operation
- Spread Spectrum Clocking
- Power-Good Indicator
- Hiccup Mode for Short-Circuit Protection
- Compact SOT583 Package
- Automotive AEC-Q100 Grade 1 Qualified
- MSL Rating: MSL1

Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Display

Typical Application

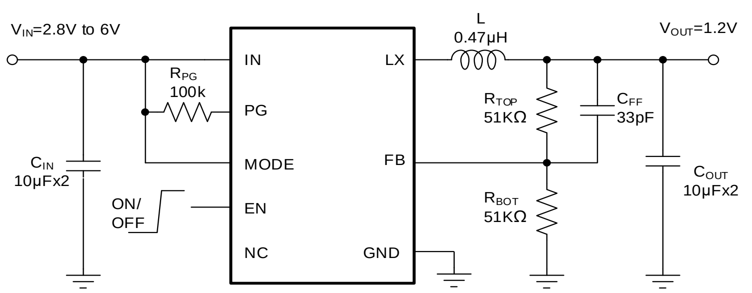


Figure 1. Schematic Diagram

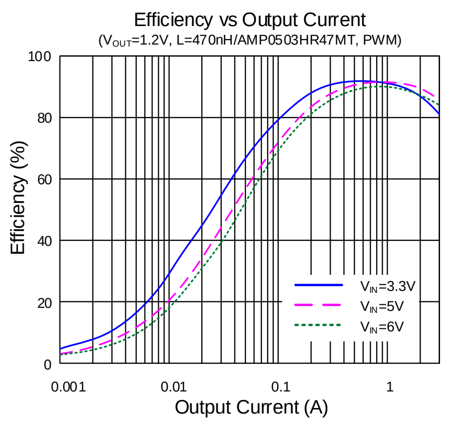


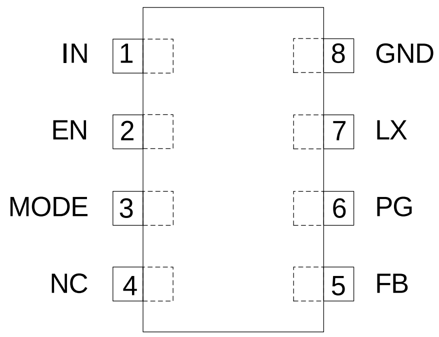
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SA25903BAT	SOT583 RoHS-Compliant and Halogen-Free	**HTW*xyz***

x = year code, y = week code, z = lot number code

Pinout (Top View)



(SOT583)

Pin Description

Name	SOT583	Pin Description
IN	1	Input pin. Decouple this pin to GND pin using at least a 10µF ceramic capacitor.
EN	2	Enable control. Pull the pin high to turn on the device and pull low to turn it off. Do not leave this pin floating.
MODE	3	Light load mode control pin. Under light load conditions, the device operates in forced PWM mode when the pin is pulled high and in PFM mode when this pin is pulled low. Do not leave this pin floating.
NC	4	Not connected.
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6×(1+R_{TOP}/R_{BOT}).
PG	6	Power-good indicator. This is an open-drain output. The pin is in high-impedance state when the output voltage is within 93% to 107% of the regulation point, driven low otherwise.
LX	7	Inductor pin. Connect this pin to the switching node of the inductor.
GND	8	Power Ground pin.

Block Diagram

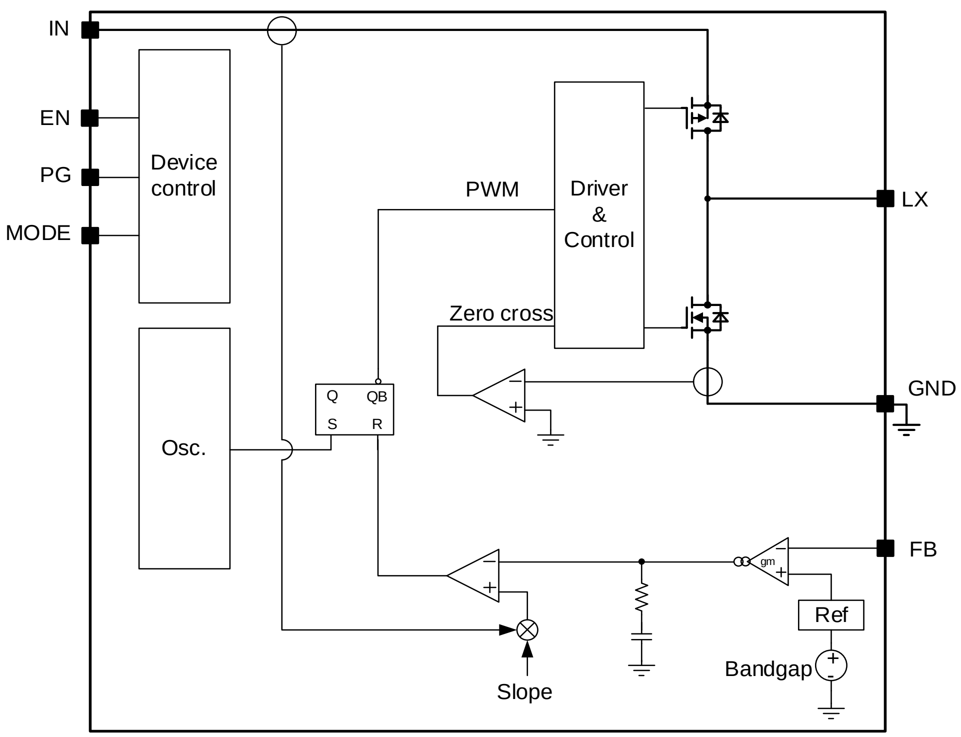


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	6.5	V
LX	-0.3	IN + 0.3	
EN, MODE, PG	-0.3	6.5	
FB	-0.3	6	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)		±2000	V
CDM (Charged Device Model)		±500	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	118.6	°C/W
θ_{JB} Junction-to-Board Thermal Resistance	53	
θ_{JC_top} Junction-to-Case Thermal Resistance	29	
Ψ_{JT} Junction-to-Top Characterization Parameter	3.8	
P_D Power Dissipation $T_A = 25°C$	1.06	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.8	6	V
Output Voltage	0.6	5.5	
Output Current	0	3	A
Junction Temperature	-40	150	°C

Electrical Characteristics

(V_{IN} =5V,-40°C≤T_J≤150°C. Typical values at T_J = 25°C, unless otherwise specified. (**Note 4**))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	UVLO Rising Threshold	$V_{IN,UVLO\_R}$		2.6	2.7	2.8	V
	UVLO Hysteresis	$V_{IN,UVLO\_H}$			100		mV
	Quiescent Current	I_Q	V_{FB} = 105% × V_{REF}, PFM		35	60	µA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		2.5	15	µA
Output	Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
	Soft-Start Time	t_{SS}		0.2	0.5	0.8	ms
	Output Discharge Resistance	R_{DIS}			200		Ω
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			65		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			25		mΩ
	Top FET Current Limit	$I_{LMT,TOP}$	L=0.47µH	4.5	5.9	7	A
	Bottom FET Current Limit	$I_{LIM,BOT}$	L=0.47µH	2.7	3.7	4.8	A
	Bottom FET Negative Current Limit	$I_{LMT,NEG}$	L=0.47µH	-2.2	-1.5	-0.8	A
Enable (EN)	EN Logic High Threshold	$V_{EN,H}$		1.2			V
	EN Logic Low Threshold	$V_{EN,L}$				0.4	V
MODE	Mode Logic High Voltage	$V_{MODE,H}$		1.2			V
	Mode Logic Low Voltage	$V_{MODE,L}$				0.4	V
Power-Good	Power Good Threshold	V_{PG}	V_{FB} rising, PG from low to high	90	93	96	$\%V_{REF}$
			V_{FB} falling, PG from high to low	86	90	94	$\%V_{REF}$
			V_{FB} falling, PG from low to high	104	107	110	$\%V_{REF}$
			V_{FB} rising, PG from high to low	107	110	113	$\%V_{REF}$
	PG Delay Time	t_{PG}		5	30	50	µs
	PG Output Low	$V_{PG,L}$	2mA sink current		17	50	mV
Switching Frequency	Switching Frequency	f_{SW}		1.92	2.2	2.5	MHz
	Minimum On Time	$t_{ON,MIN}$	(Note 5)		60		ns
	Minimum Off Time	$t_{OFF,MIN}$	(Note 5)		60		ns
	Maximum Duty Cycle	D_{MAX}	(Note 5)	100			%
OTP	Thermal Shutdown Temperature	T_{OTP}		150	165	185	°C
	Thermal Shutdown Hysteresis	T_{HYS}			20		°C
UVP	Output UVP Threshold	V_{UVP}	V_{FB} as percent of V_{REF}	35	50	65	$\%V_{REF}$

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in natural convection at TA = 25°C on a 1oz two-layer Silergy evaluation board.

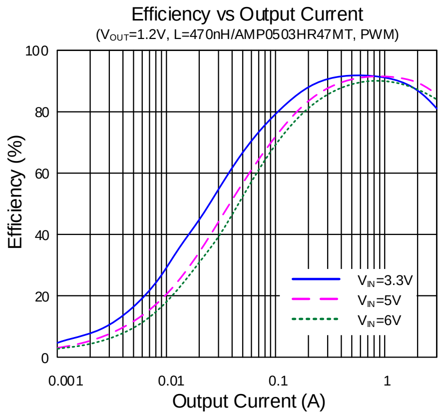
Note 3: The device is not guaranteed to function outside its operating conditions.

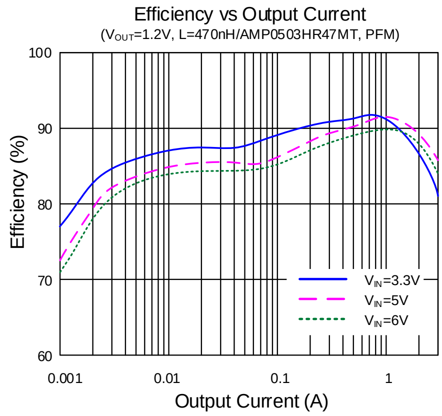
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that T_A ≅ T_J = 25℃. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

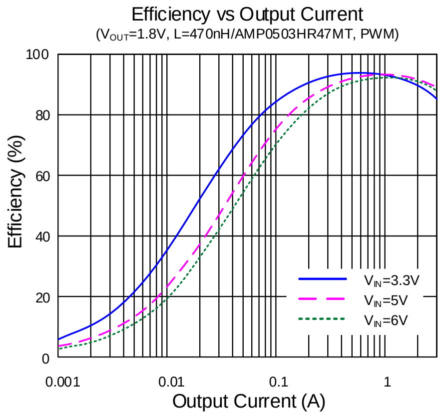
Note 5: Guaranteed by design or statistical correlation and not production tested.

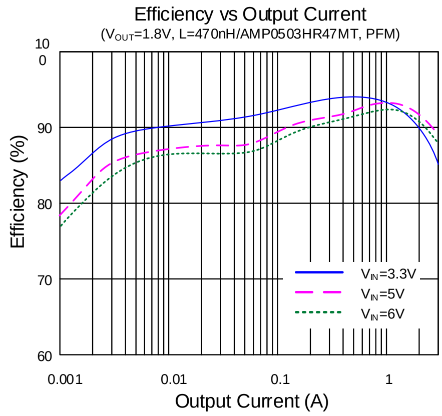
Typical Performance Characteristics

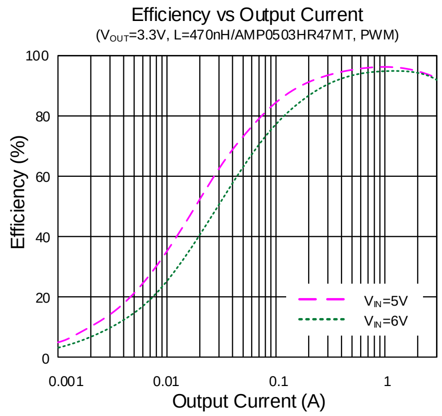
(T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 3A, L = 470nH, C_{OUT} = 20µF, unless otherwise specified)

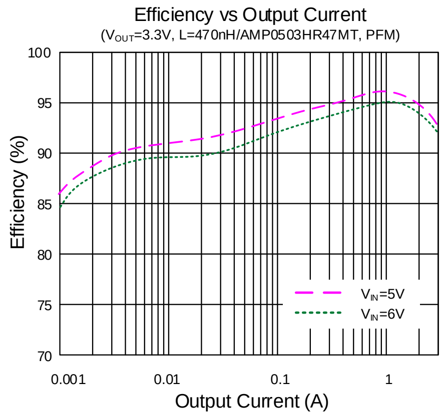






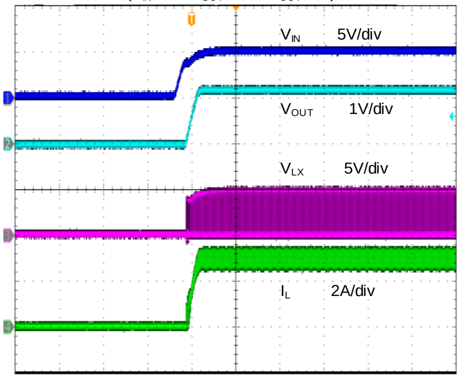






Startup from V_{IN}

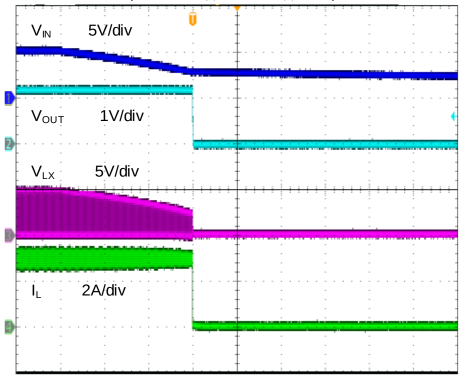
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from V_{IN}

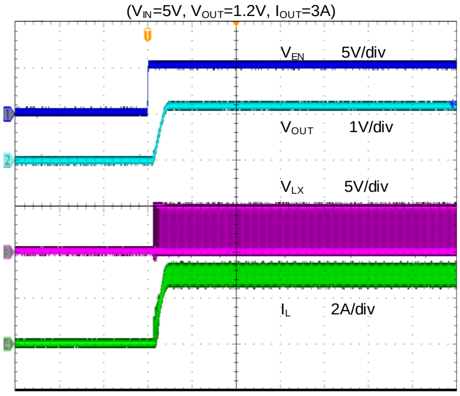
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A)



Time (2ms/div)

Startup from EN

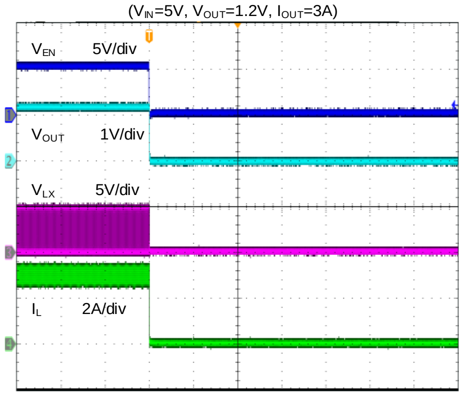
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from EN

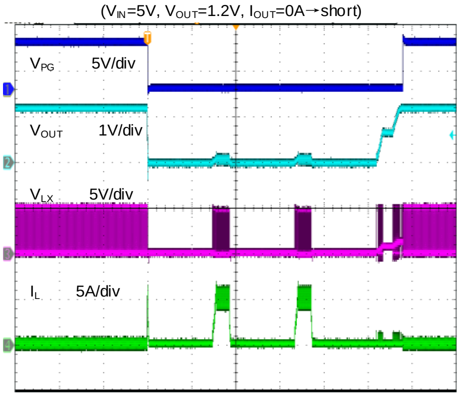
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A)



Time (2ms/div)

Short Circuit Protection

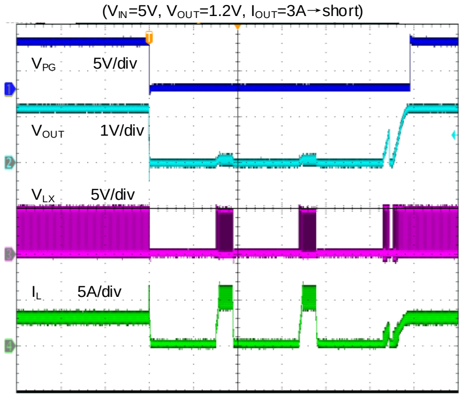
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A→short)



Time (2ms/div)

Short Circuit Protection

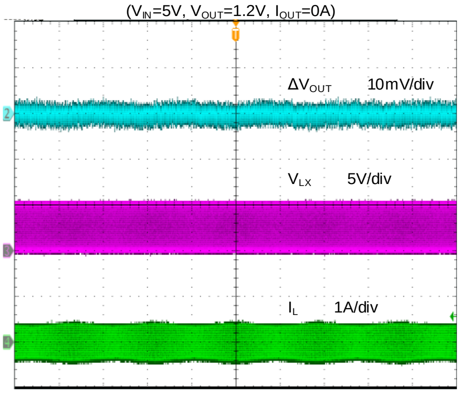
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A→short)



Time (2ms/div)

Output Ripple

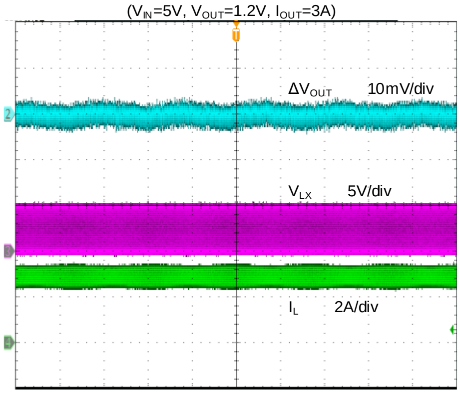
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A)



Time (200µs/div)

Output Ripple

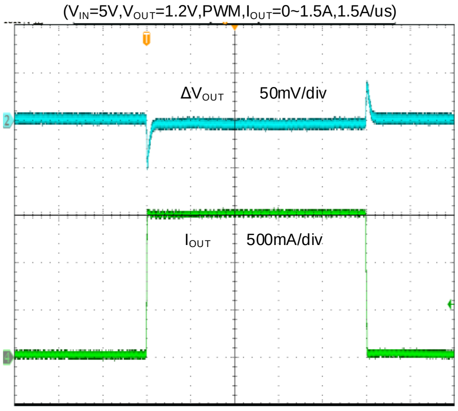
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=3A)



Time (200µs/div)

Load Transient

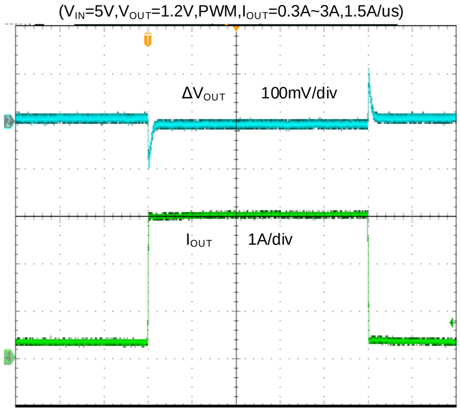
(V_{IN}=5V,V_{OUT}=1.2V,PWM,I_{OUT}=0~1.5A,1.5A/us)



Time (100µs/div)

Load Transient

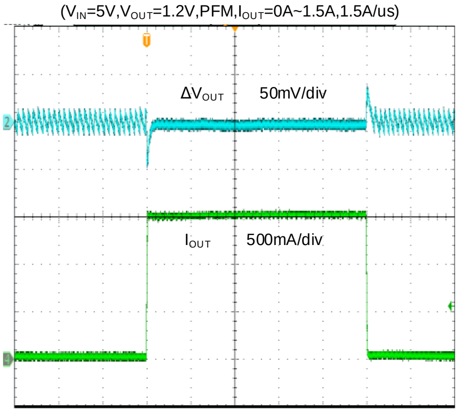
(V_{IN}=5V,V_{OUT}=1.2V,PWM,I_{OUT}=0.3A~3A,1.5A/us)



Time (100µs/div)

Load Transient

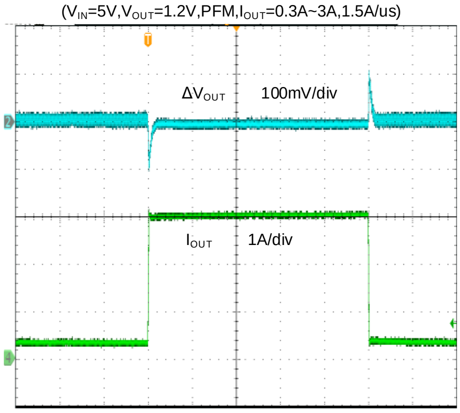
(V_{IN}=5V,V_{OUT}=1.2V,PFM,I_{OUT}=0A~1.5A,1.5A/us)



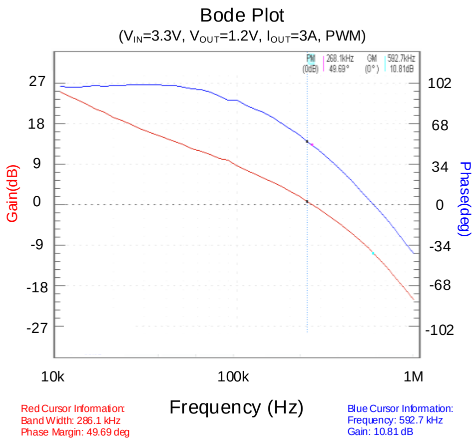
Time (100µs/div)

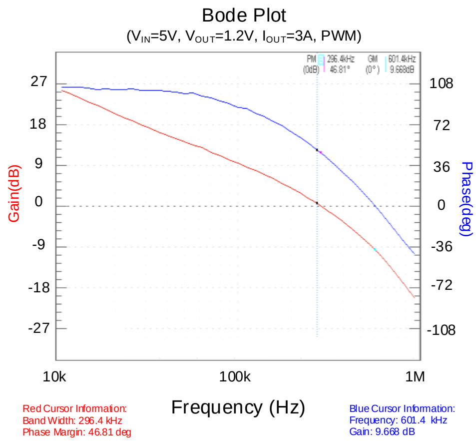
Load Transient

(V_{IN}=5V,V_{OUT}=1.2V,PFM,I_{OUT}=0.3A~3A,1.5A/us)



Time (100µs/div)


Bode Plot
(VIN=3.3V, VOUT=1.2V, IOUT=3A, PWM)
Gain(dB)
Phase(deg)
27
18
9
0
-9
-18
-27
102
68
34
0
-34
-68
-102
10k
100k
1M
Frequency (Hz)
Red Cursor Information:
Band Width: 286.1 kHz
Phase Margin: 49.69 deg
Blue Cursor Information:
Frequency: 592.7 kHz
Gain: 10.81 dB


Bode Plot
(VIN=5V, VOUT=1.2V, IOUT=3A, PWM)
Gain(dB)
Phase(deg)
27
18
9
0
-9
-18
-27
108
72
36
0
-36
-72
-108
10k
100k
1M
Frequency (Hz)
Red Cursor Information:
Band Width: 296.4 kHz
Phase Margin: 46.81 deg
Blue Cursor Information:
Frequency: 601.4 kHz
Gain: 9.668 dB

Functional Description

The SA25903 is a high-efficiency 2.2MHz synchronous step-down converter that operates over an input voltage range of 2.8V to 6V, and can deliver an output current of up to 3A. It integrates very low $R_{DS(ON)}$ main and synchronous MOSFETs to minimize conduction loss. The 2.2MHz constant switching frequency reduces the required external inductor and capacitor values.

Enable Control

The EN input is a high-voltage-capable input with logic-compatible threshold. When EN is driven higher than $V_{EN,H}$, normal device operation is enabled. When driven to lower than $V_{EN,L}$, the device shuts down, reducing the input current to less than 2.5µA.

Output Power-Good Indicator

The power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is in power-good range (see EC table thresholds), PG is in a high-impedance state, otherwise, it is pulled low. PG should be connected to V_{IN} or another voltage source through a resistor (e.g. 10kΩ~100kΩ).

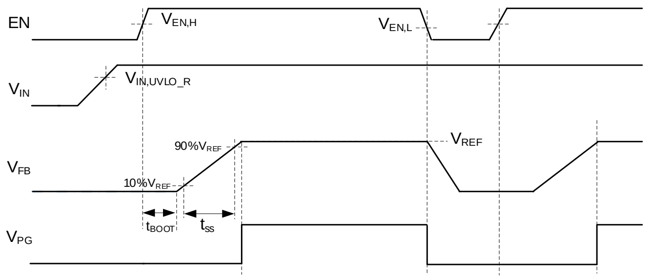


Figure 4. Power Good Logic

Adaptive Frequency Fold-Back at Min Toff Operation (Dropout)

The SA25903 provides an adaptive frequency decreasing function during large duty-cycle conditions when min T_{OFF} occurs. Different from traditional peak current control mode, it ensures the stability of the circuit in dropout conditions.

When VIN drops below the configured output voltage, the SA25903 enters dropout mode, where its high-side MOSFET is always ON.

MODE

The MODE pin controls light load operation. Connecting the MODE pin to GND enables power-save mode, allowing automatic transitions between PWM and PFM modes to improve efficiency under light load conditions. When this pin is pulled high, the converter operates in forced PWM mode.

Spread Spectrum Clocking

The spread spectrum function is used to optimize EMI performance. The operating frequency is varied ±8% around the set switching frequency. The modulation signal is a triangular waveform with a period of approximately 330µs. Consequently, F_{SW} ramps down 8% and returns to the center frequency in approximately 165µs, then ramps up 8% and returns to the center frequency in approximately 165µs.

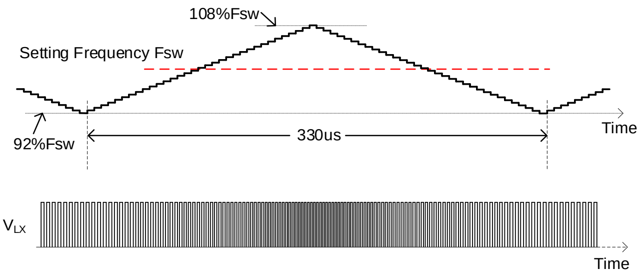


Figure 5. Spread Spectrum Clocking

Fault Protection Modes

The SA25903 integrates output short-circuit protection, output under-voltage protection, output over-current protection and thermal shutdown protection features.

Protection	Threshold	Noise Filter Time	Operation
Thermal Shutdown	Rising:165°C Falling:145°C	-	Shutdown when temperature>165°C Restart when temperature<145°C
Current Limit			Peak limit = valley limit; Valley foldback to 80% after 3 cycles.
Output UVP	V_{FB}<50%V_{REF}	10us	Hiccup time 3ms

Output Current Limit

The device features cycle-by-cycle current limit protection. When the current sense amplifier detects a voltage above the peak current limit, the peak current limit causes the power switch to turn off for the remainder of the cycle.

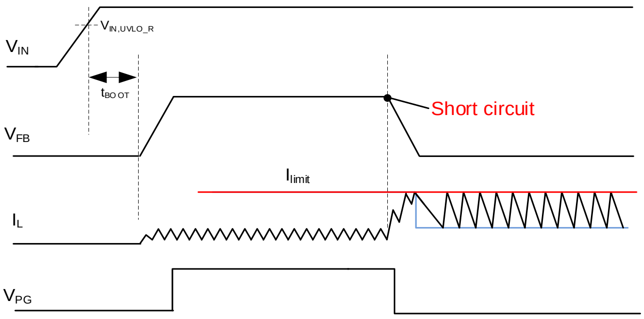


Figure 6. Cycle-by-Cycle Current Limit

Output Undervoltage Protection (UVP)

If V_{OUT} is less than approximately 50% of the target output voltage, for a duration exceeding the UVP delay time (typically 10µs), the output under voltage protection (UVP) is triggered, and the device enters hiccup protection mode, where the device is turned off for a duration of 3 ms before a soft-start sequence is initiated.

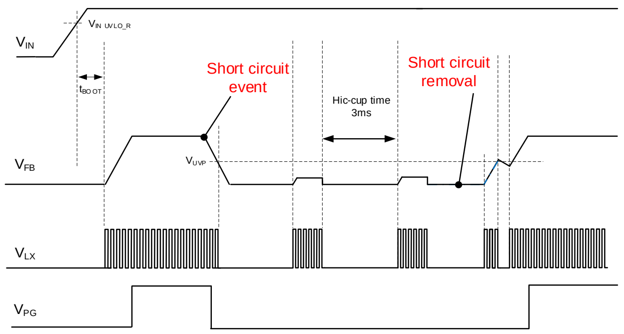


Figure 7. Undervoltage Protection

When the output fault conditions are removed during the hiccup on-time, the internal soft-start circuit voltage (V_{SS}) will be temporarily pulled low to prevent output overshoot if V_{FB} exceeds the UVP threshold. The V_{SS} will then rise monotonically to ramp the output to the desired voltage during a new soft-start cycle.

Overtemperature Protection (OTP)

The SA25903 includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The device will shut down when the junction temperature exceeds T_{OTP}. Once the junction temperature drops by approximately T_{HYS}, the device will resume normal operation after completing a soft-start cycle. For continuous operation, ensure adequate power dissipation to prevent the junction temperature from exceeding the OTP threshold.

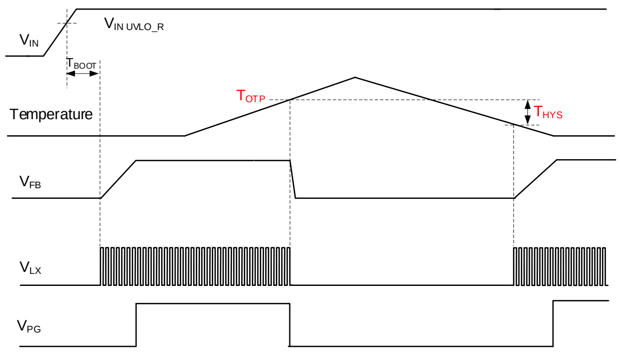


Figure 8. Over Temperature Protection

Output Discharge

In order to ensure that the output voltage decreases at a certain slope when the device is disabled, as well as keeping the output voltage close to 0 V when the device is turned off, the SA25903 features an output discharge function. The discharge function is enabled immediately when the device is disabled, in thermal shutdown, or in over-voltage protection.

Application Information

The following paragraphs describe the selection process for the input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistors R_{TOP} and R_{BOT}.

Feedback Resistor-Divider R_{TOP} and R_{BOT}

Choose R_{TOP} and R_{BOT} to program the target output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors. If R_{BOT} is selected, then R_{TOP} can be calculated as follows:

$$V_{OUT} = \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \times V_{REF}$$

Where V_{REF} is 0.6V typically.

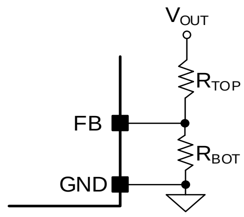


Figure 9. Output Voltage Programming

Output Inductor L

The following conditions must be met when selecting this inductor:

1) Choose the inductance to achieve desired ripple current. It is recommended to set the ripple current to approximately 40% of the maximum output current in the current application. The inductance is calculated as:

$$L = \frac{V_{OUT} \times \left(1 - V_{OUT} / V_{IN\_MAX}\right)}{f_S \times I_{OUT\_MAX} \times \frac{\Delta I_L}{I_{OUT\_MAX}}}$$

where f_S is the switching frequency and I_{OUT_MAX} is the maximum load current in the current application.

The SA25903 has a high tolerance for variations in ripple current amplitude. As a result, the final inductance selected can differ slightly from the calculated value without significantly impacting performance.

2) The saturation current rating of the inductor must be selected to exceed peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times \left(1 - V_{OUT} / V_{IN\_MAX}\right)}{2 \times f_S \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be sufficiently low to meet the desired efficiency requirements. It is advisable to select an inductor with a lower DCR to achieve optimal efficiency.

Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT\_MAX} \times \sqrt{D \times (1 - D)}$$

The capacitance of the input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times f_S \times Eff \times V_{IN}^2}$$

where ΔV_{IN} is the maximum allowed input voltage ripple.

To minimize noise, place an X5R or better grade ceramic capacitor close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and the VIN/GND pins. A 10µF low ESR ceramic capacitor is recommended for most applications.

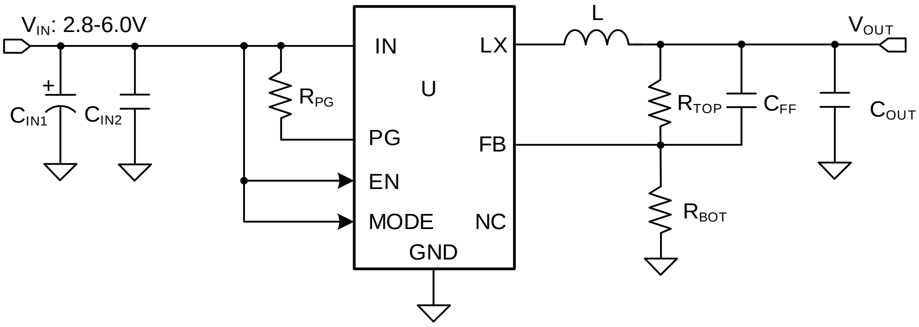
Output Capacitor C_{OUT}

The output capacitor is selected to meet the output current ripple noise requirements. Both steady-state ripple and transient requirements must be considered when selecting this capacitor. It is recommended to use X5R or higher grade ceramic capacitors. Depending on the input/output voltage conditions two or three 10µF low ESR capacitors, connected in parallel, are recommended, as detailed in the Recommended Component Values table.

Load-Transient Considerations

The SA25903 integrates compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_{TOP} may further enhance the load-transient responses. It is recommended for applications with significant load transient step requirements.

Application Schematic (V_{OUT} = 1.2V)



BOM List

Designator	Description	Part Number	Manufacturer
U	3A, Buck	SA25903BAT	Silergy
L	0.47µH	AMP0503HR47MT	SunLord
C_{IN1}	47µF/25V(electrolytic capacitor)		
C_{IN2}	10µF/10V, 0603, X7R	GRM188Z71A106KA73D	Murata
C_{OUT}	2 x 10µF/10V, 0603, X7R	GRM188Z71A106KA73D	Murata
C_{FF}	33pF/50V, 0603, C0G	GRM1885C1H330GA01D	Murata
R_{TOP}	51kΩ, 1%, 0603		
R_{BOT}	51kΩ, 1%, 0603		
R_{PG}	10kΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V_{OUT}(V)	R_{TOP}(kΩ)	R_{BOT}(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
0.6	0	NC	NC	0.47µH/ AMP0503HR47MT	3 x 10µF/10V, 0603, X7R
0.8	10	30	33	0.47µH/ AMP0503HR47MT	3 x 10µF/10V, 0603, X7R
0.9	15	30	33	0.47µH/ AMP0503HR47MT	3 x 10µF/10V, 0603, X7R
1.0	20	30	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R
1.1	20	24	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R
1.2	51	51	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R
1.5	30	20	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R
1.8	100	50	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R

V_{OUT}(V)	R_{TOP}(kΩ)	R_{BOT}(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
2.5	47.5	15	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R
3.3	100	22	33	0.47µH/ AMP0503HR47MT	2 x 10µF/10V, 0603, X7R

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND using a wide copper plane.

Output Capacitors: Connect the C_{OUT} negative terminal to the GND pin using wide copper trace instead of vias to achieve better accuracy and stability of the output voltage.

Feedback Network: Place the feedback components (R_{TOP}, R_{BOT}, and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near the LX pin or other high-frequency signals, as these are noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

Control Signals: It is not recommended to connect control signals directly to V_{IN}. A resistor in the range of 1kΩ to 1MΩ should be used if the lines are pulled high to V_{IN}.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance.

PCB Board: To achieve optimal thermal and noise performance, maximize the PCB copper area connected to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

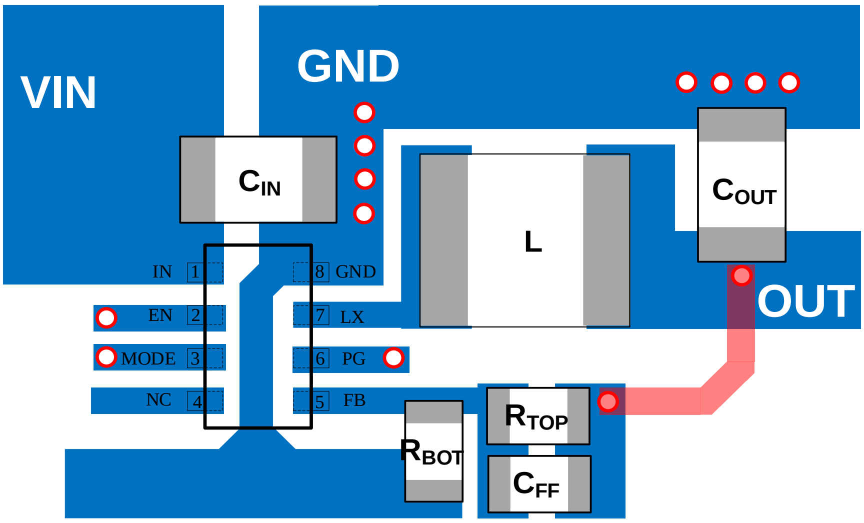
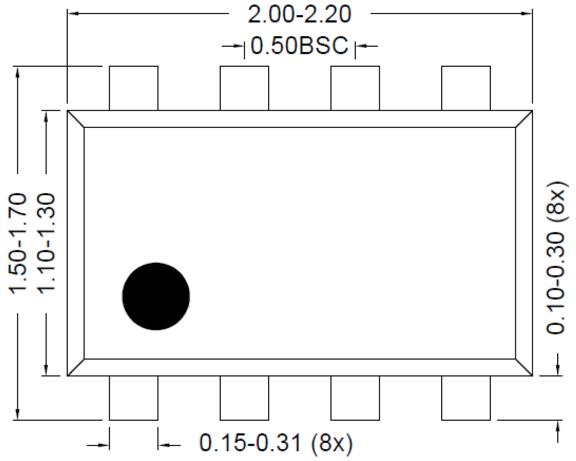
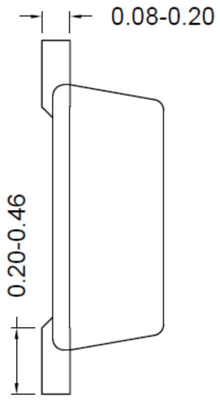


Figure 10. Suggested PCB Layout

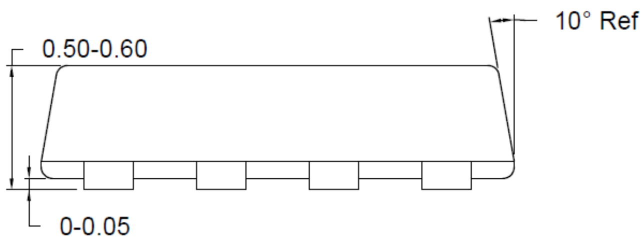
SOT583 Package Outline Drawing



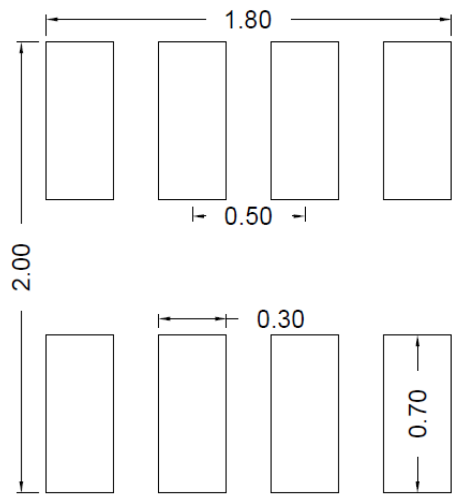
Top View



Side View



Front View



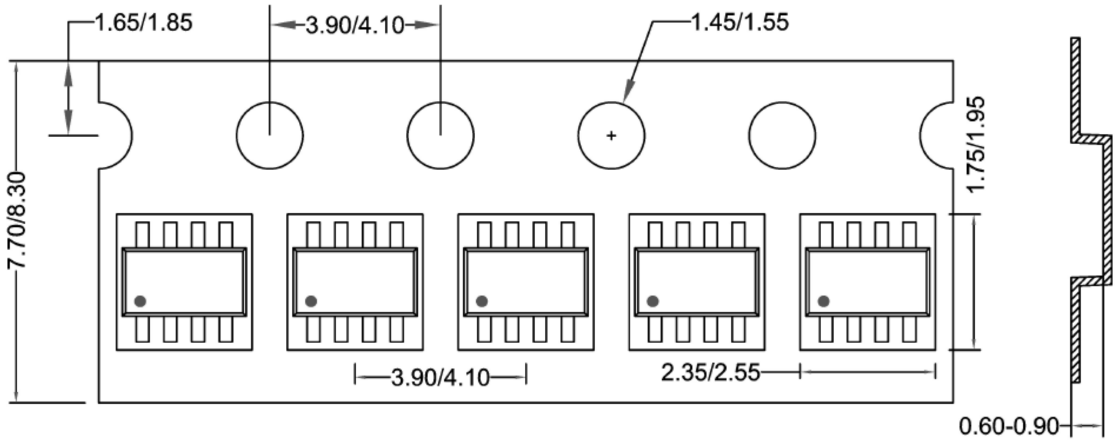
Recommended PCB Layout (Reference Only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Information

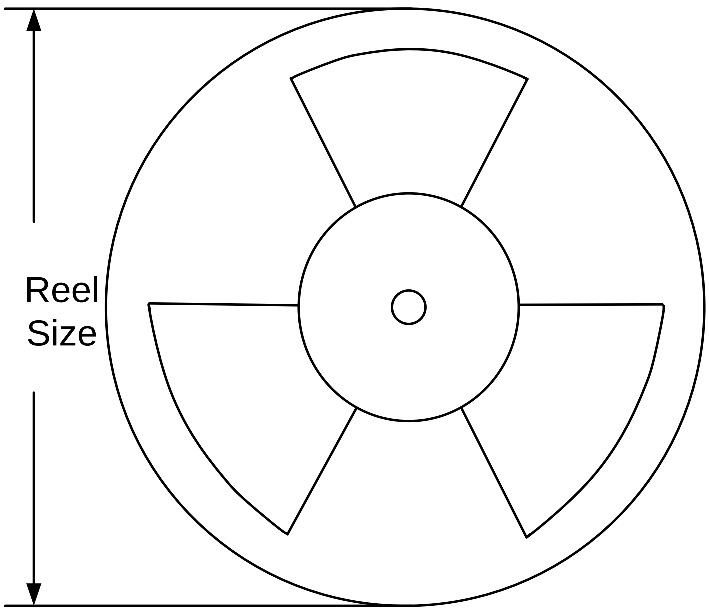
Tape Dimensions and Pin 1 Orientation

SOT583



Direction of feed

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
SOT583	8	4	7"	280	200	5000

All dimensions are nominal

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
May.20, 2025	Revision 1.0	Initial Release	-

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