SY86809A

2.95V~15V, 9A, 10mΩ, Programmable Current Limit Switch

General Description

The SY86809A is a programmable current limit switch with input voltage range selection and output voltage clamping. Extremely low $R_{DS(ON)}$ of the integrated protection N-channel FET helps to reduce power loss during the normal operation. Programmable soft-start time controls the slew rate of the output voltage during the start-up time. Independent enable control allows the complicated system sequencing control. It integrates the over-temperature protection shutdown and auto-recovery with hysteresis. This IC along with small QFN2×2.5-10 footprint provides small PCB area application.

Features

- Wide Input Voltage Range from 2.95V to 15V with Surge up to 30V
- Extremely Low Power Path Resistance $R_{DS(ON)}$
  - $R_{DS(ON)}$=10mΩ(typ) at 3.3/5/12 V_{IN} Condition
- 9A Output Current Capability/10.8A Peak Current
- Programmable Current Limit
- Programmable Soft-Start Time
- Selectable Clamping Output Voltage Threshold
- Independent ON/OFF Control Input
- Thermal Shutdown Protection & Auto Recovery
- Moisture Sensitivity Level (MSL): 1
- Compact package: QFN2×2.5-10

Applications

- SSD M.2 from Factor
- SSD Dual Input Power Application
- SSD Load Switch

Typical Application

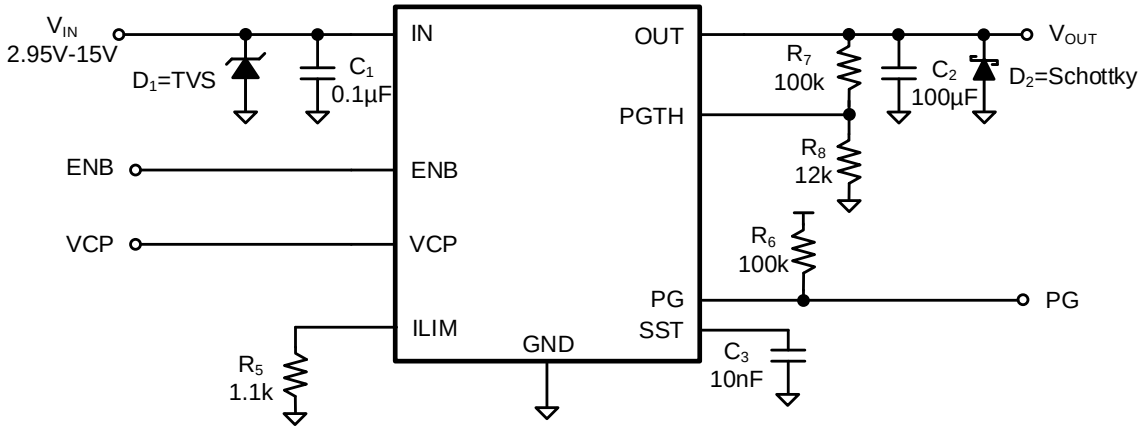


Figure1. Schematic Diagram

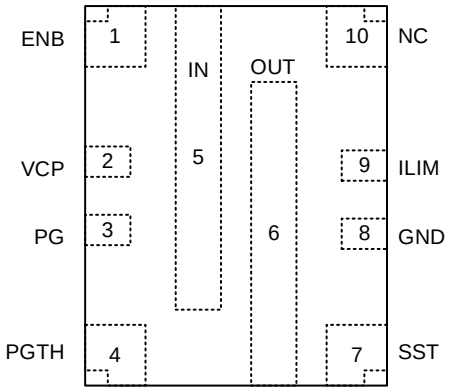
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY86809AAAQ	QFN2×2.5-10 RoHS Compliant and Halogen Free	**GQA*xyz***

Device code: GQA

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin Name	Pin Number	Pin Description
ENB	1	Enable pin, active low. Pull low to enable the SY86809A, pull high to disable the SY86809A. Don't leave it floating.
VCP	2	Output clamp voltage selection based on the input voltage. Pull the VCP pin to High by connecting a resistor ≤10kΩ to IN or pull the VCP pin to Low by connecting a resistor ≤10kΩ to ground, or float the VCP pin to select different output clamping thresholds.
PG	3	Power Good indication. Open drain output. Connect a pull-high resistor to OUT or other supply. High impedance when PGTH is higher than V_{PGTHR}.
PGTH	4	Positive input of PGOOD comparator. Once the voltage on this pin is higher than V_{PGTHR}, the PG pin is set to high impedance. Connect a resistor divider from OUT to GND to program the power good threshold.
IN	5	Power input pin. Decouple high frequency noise by connecting at least a 0.1μF MLCC to ground as close as possible to the IC. A TVS is recommended to add to absorb the voltage spike for hot plug application.
OUT	6	Output voltage pin. Connect a 1μF MLCC and 100μF Electrolytic capacitor to GND.
SST	7	Soft-start time program pin. Connect a capacitor to ground to program the soft start time. 0.6ms (typ.) time for NC condition.
GND	8	Power ground pin.
ILIM	9	Current limit program pin. Connect a resistor between this pin and GND to program input current limit.
NC	10	No connection.

VCP	VIN		Clamping Threshold		
			Min	Typ	Max
LOW	3.3V	Over 4V	3.6V	3.8V	4V
HIGH	5V	Over 6V	5.4V	5.7V	6V
Floating	12V	Over 14V	12.6V	13.3V	14V

Block Diagram

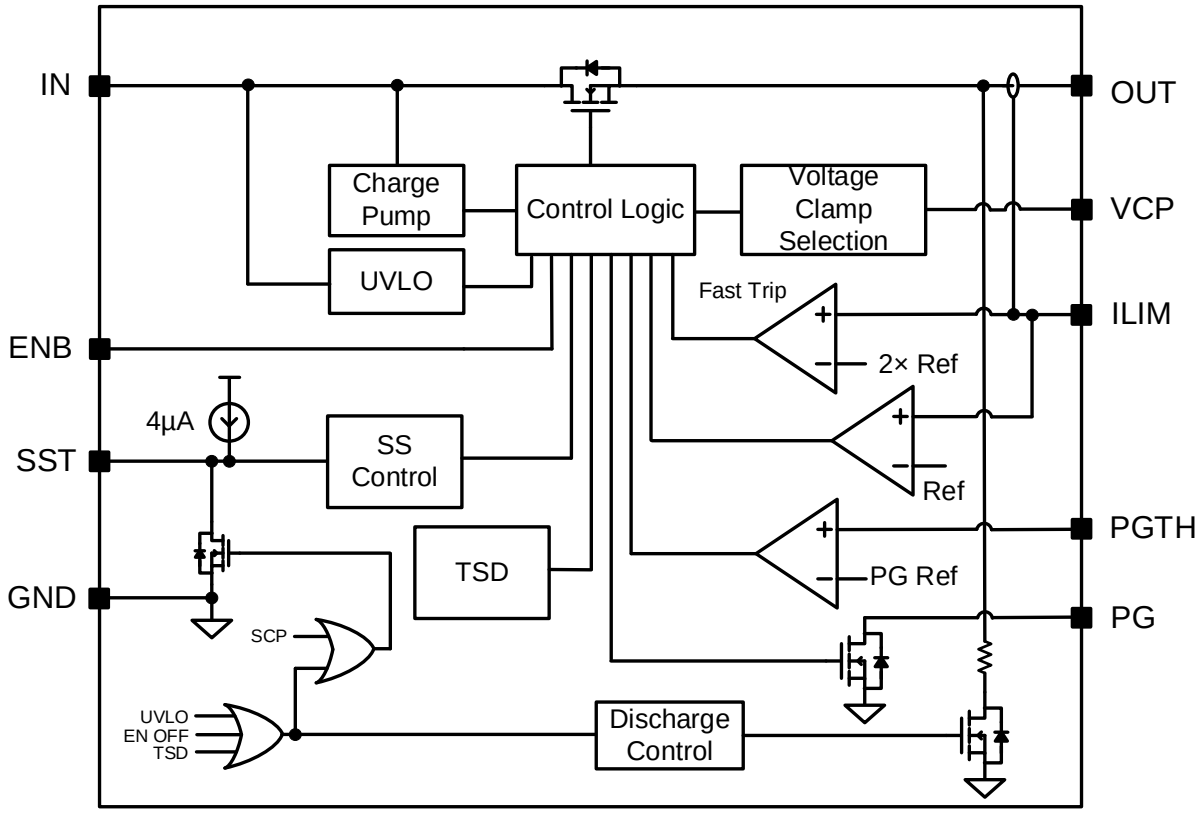


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, VCP, ENB, OUT, PG, PGTH	-0.3	30	V
SST, ILIM	-0.3	3.6	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	36.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance	23	
P_D Power Dissipation, @ T_A = 25°C	2.74	W

ESD Susceptibility

Parameter	Value	Unit
HBM (Human Body Mode)	±2000	V
CDM (Charged Device Mode)	±500	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	2.95	15	V
VCP, ENB, OUT, PG, PGTH	0	15	
SST, ILIM	0	3.3	
Resistance Range Recognized as VCP Floating	1		MΩ
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 5V, C_{IN}=C_{OUT}=1μF, SST=Floating, R_{LIM}=2.2kΩ, T_J = -40°C~125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.95		15	V
Input UVLO Threshold	V_{UVLO}	VCP=Low	2.7		2.9	V
		VCP=High	3.4		3.8	V
		VCP floating	8.1		9	V
UVLO Hysteresis	V_{HYS}	VCP=Low	0.05	0.1	0.15	V
		VCP=High	0.05	0.1	0.15	V
		VCP floating	0.1	0.19	0.29	V
Shutdown Current	I_{SD}	EN=disable		10	18	μA
Bias Current	I_{BIAS}	V_{IN}=3.3V, V_{EN}=0V, VCP=Low		115	150	μA
		V_{IN}=5V, V_{EN}=0V, VCP=High		115	150	
		V_{IN}=12V, V_{EN}=0V, VCP=Floating		120	155	
Clamping Output Voltage	V_{CLP}	VCP=Low	3.6	3.8	4.0	V
		VCP=High	5.4	5.7	6.0	V
		VCP floating	12.6	13.3	14	V
Over Voltage Clamp Response Time	t_{OVP}	VCP=High, V_{IN}=5V to 12V/100μs, C_{IN}=C_{OUT}=1μF, R_{LOAD}=100Ω (Note 6)		6		μs
VCP High Voltage Range	V_{SEL_HI}	V_{IN}=5V, V_O changes to 5V	2.2			V
VCP Low Voltage Range	V_{SEL_LO}	V_{IN}=5V, V_O changes to 3.8V			0.2	V
ENB High Voltage Range	V_{ENH}		1			V
ENB Low Voltage Range	V_{ENL}				0.4	V
ENB Deglitch Time	t_{DEG}	ENB high to V_{SST}↓, C_{SST}=open. (Note 6)		1		μs
ENB Turn ON Delay	t_{D_ON}	ENB low to V_{OUT}=10%×V_{IN}, C_{SST}=open, C_{OUT}=1μF, R_{OUT}=100Ω	100	185	290	μs
ENB Turn Off Delay	t_{D_OFF}	ENB high to V_{OUT}=90%×V_{IN}, C_{SST}=open, C_{OUT}=1μF, R_{OUT}=100Ω	5	10	15	μs
PGTH Threshold Voltage Rising	V_{PGTHR}		1.178	1.194	1.21	V
PGTH Threshold Voltage Falling	V_{PGTHF}		1.13	1.146	1.162	V
PGTH Input Leakage Current	I_{PGTH}		-100	0	100	nA
PG Low Voltage	V_{PGL}				0.2	V
PG Leakage Current	V_{PGLK}				1	μA
PG Delay Time Rising	t_{PGR}	V_{PGTH}>V_{PGTHR} to PG↑	10	18	26	μs
PG Delay Time Falling	t_{PGF}	V_{PGTH}>V_{PGTHF} to PG↓	10	18	26	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Resistance of Power Path	$R_{DS(ON)}$	V_{IN}=3V, I_{OUT}=200mA, from IN to OUT		10		mΩ
Soft-start Time Program Range	t_{SST}	C_{SST}=100nF (Note 4)		24		ms
Soft-start Time Accuracy		C_{SST}≥1nF	-30%		30%	t_{SST}
SST Current Source	I_{SST}	V_{SST}=0.8V, C_{SST}=open		4		μA
Current Limit Program Range	I_{LIM}	(Note 5)	1		9	A
Current Limit Accuracy		I_{LMT} = 4A	-10%		10%	I_{LIM}
Discharge Resistance	R_{DSG}	V_{IN}=5V, EN=0V, V_{OUT}=0.1V		30		Ω
Thermal Shutdown Temperature	T_{SD}	(Note 6)		150		°C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 6)		20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} and θ_{JC} are simulated in the natural convection at T_A = 25°C on Silergy’s test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note4: Recommended Soft-start Time Program Table

(V_{IN}=12V, T_J=25℃)

SST Cap (nF)	None	10	47	100
Rise Time (ms)	0.6	2.4	11.3	24

Recommended Formula for C_{SST} & Soft-start Time Calculation

$t_{SS} = t_{SS\_DLT}$, No external C_{SST}, or

$t_{SS} = \frac{0.8 \times V_{IN} \times C_{SST}}{AV_{SS} \times I_{SST}}$, $t_{SS} > t_{SS\_DLT}$

Where, t_{SS_DLT} is the internally fixed default soft-start time, about 0.6ms, which means there’s no any external C_{SST}; I_{SST} is the internal current source, about 4μA. t_{SS} is defined as the rise time of the output voltage equal to 10% ×V_{IN} to 90% ×V_{IN}. AV_{SS} is the Gain of V_{OUT}, V_{SST}, about 10V/V.

Note5: Recommended Current Limit Program Table

SY86809A’s current limit value can be programmed by ILIM as below table

Current Limit Resistance (kΩ)	11	5.5	3.7	2.75	2.2	1.83	1.38	1.22
Current Limit (A)	1.0	2.0	3.0	4.0	5.0	6.0	8.0	9.0

Recommended Formula for R_{LIM} & Current Limit Calculation

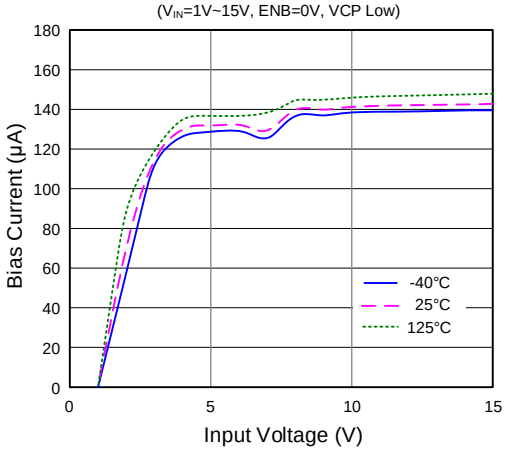
$R_{LIM} = \frac{11k}{I_{LIM}} (\Omega)$

Note6: Guaranteed by design, but not production test.

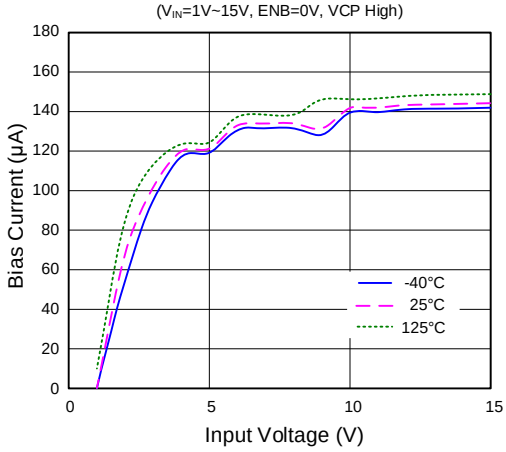
Typical Performance Characteristics

(T_J = 25ºC, unless otherwise specified.)

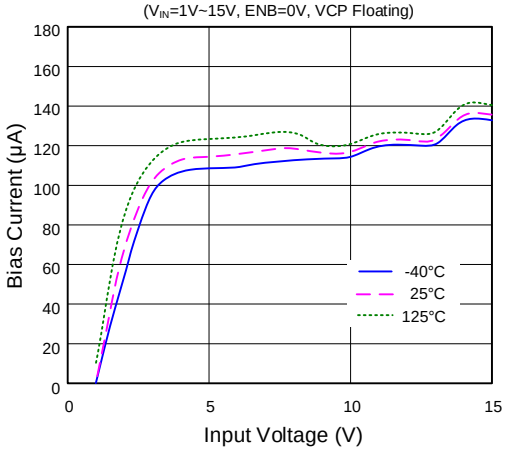
Bias Current vs. Input Voltage
(V_{IN}=1V~15V, ENB=0V, VCP Low)



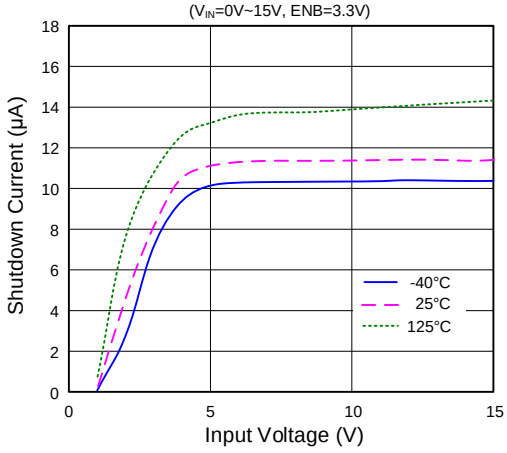
Bias Current vs. Input Voltage
(V_{IN}=1V~15V, ENB=0V, VCP High)



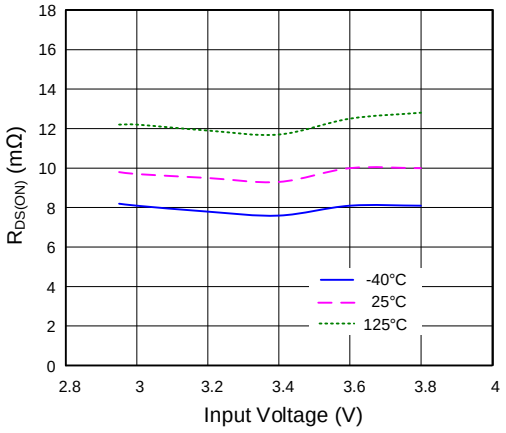
Bias Current vs. Input Voltage
(V_{IN}=1V~15V, ENB=0V, VCP Floating)



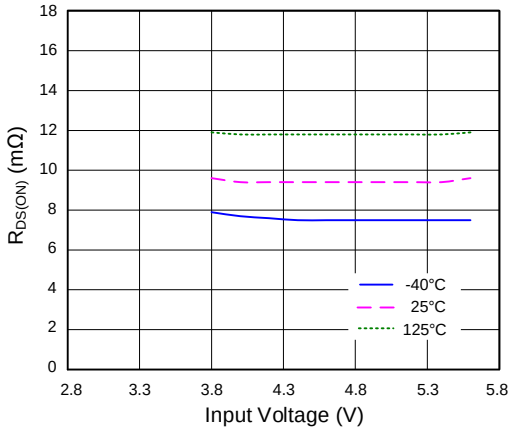
Shutdown Current vs. Input Voltage
(V_{IN}=0V~15V, ENB=3.3V)



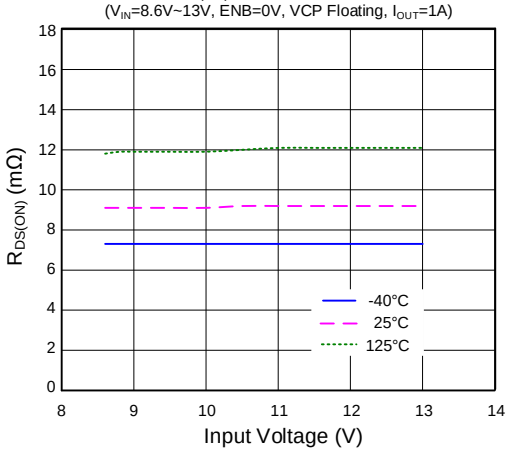
$R_{DS(ON)}$ vs. Input Voltage
(V_{IN}=2.95V~3.8V, ENB=0V, VCP Low, I_{OUT}=1A)



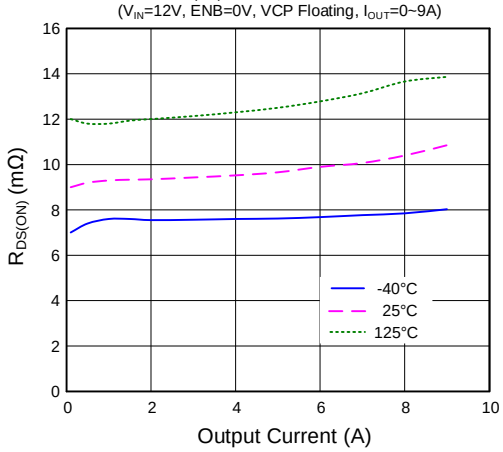
$R_{DS(ON)}$ vs. Input Voltage
(V_{IN}=3.8V~5.6V, ENB=0V, VCP High, I_{OUT}=1A)



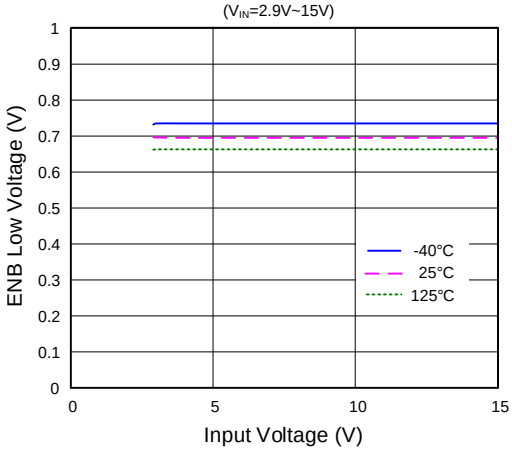
$R_{DS(ON)}$ vs. Input Voltage
(V_{IN}=8.6V~13V, ENB=0V, VCP Floating, I_{OUT}=1A)



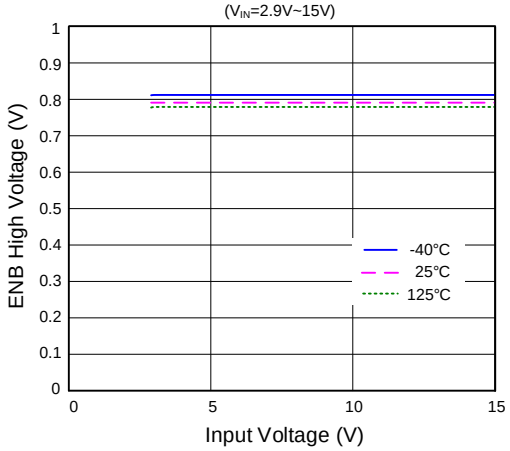
$R_{DS(ON)}$ vs. Output Current
(V_{IN}=12V, ENB=0V, VCP Floating, I_{OUT}=0~9A)



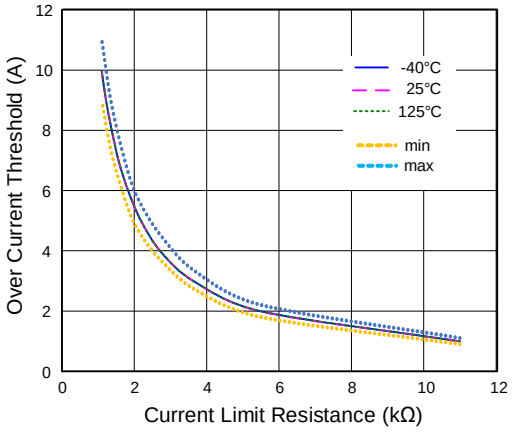
ENB Low Voltage vs. Input Voltage
(V_{IN}=2.9V~15V)



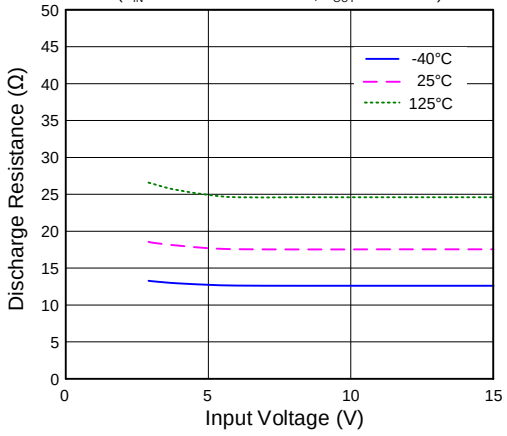
ENB High Voltage vs. Input Voltage
(V_{IN}=2.9V~15V)



Over Current Threshold vs. Current Limit Resistance
(V_{IN}=12V, ENB=0V, VCP Floating)

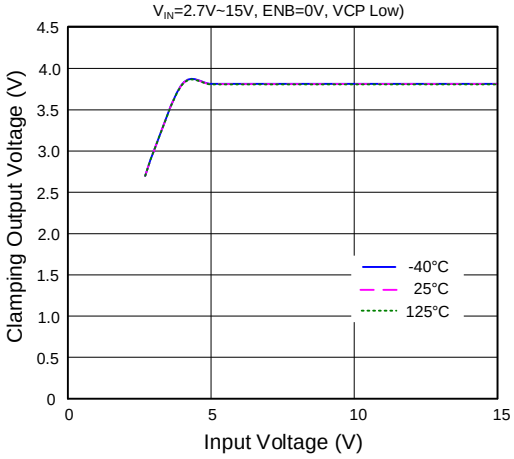


Discharge Resistance vs. Input Voltage
(V_{IN}=2.9V~15V，ENB=3.3V, V_{OUT} Force 0.1V)



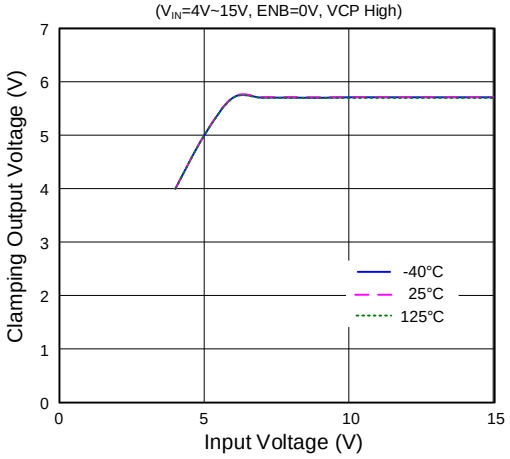
Clamping Output Voltage vs. Input Voltage

(V_{IN}=2.7V~15V, ENB=0V, VCP Low)



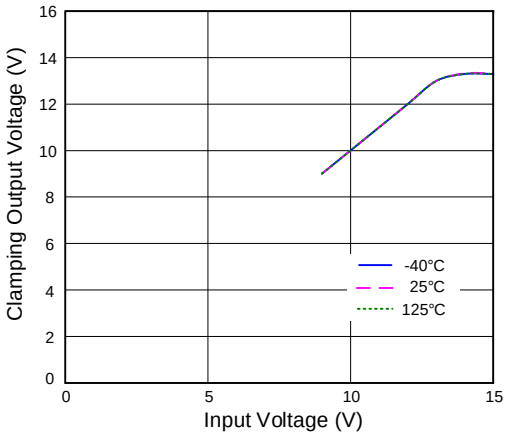
Clamping Output Voltage vs. Input Voltage

(V_{IN}=4V~15V, ENB=0V, VCP High)



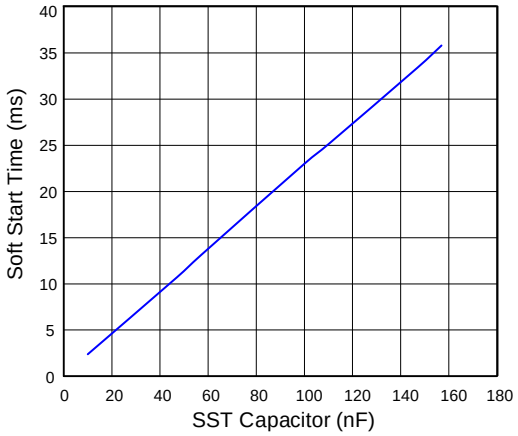
Clamping Output Voltage vs. Input Voltage

(V_{IN}=9V~15V, ENB=0V, VCP Floating)



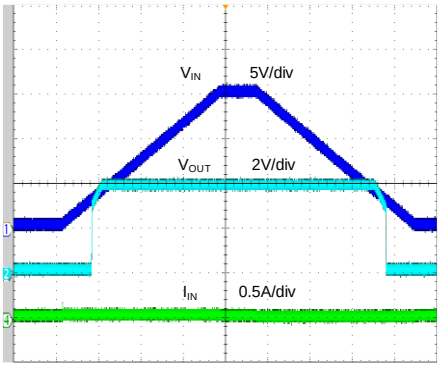
Soft Start Time vs. SST Capacitor

(V_{IN}=12V, ENB= 0V, VCP Floating, C_{IN}=0.1μF, C_{OUT}=100μF)



Clamping Output Voltage Test

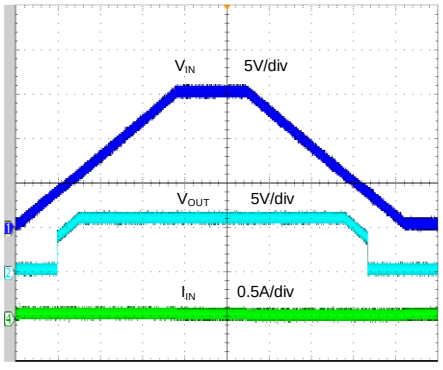
(V_{IN}=0V~15V~0V, ENB=0V, VCP=Low)



Time (400ms/div)

Clamping Output Voltage Test

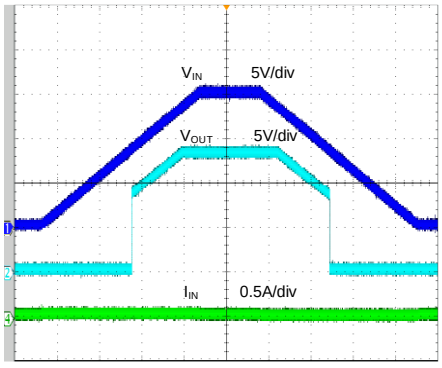
(V_{IN}=0V~15V~0V, ENB=0V, VCP=High)



Time (400ms/div)

Clamping Output Voltage Test

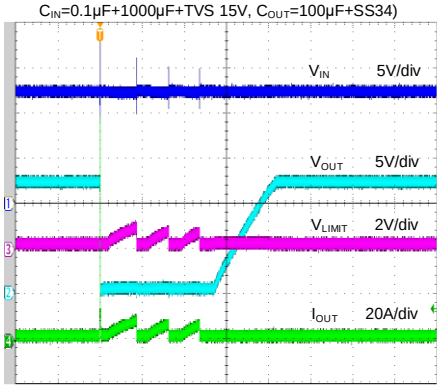
(V_{IN}=0V~15V~0V, ENB=0V, VCP=Floating)



Time (400ms/div)

First Startup then Short Test

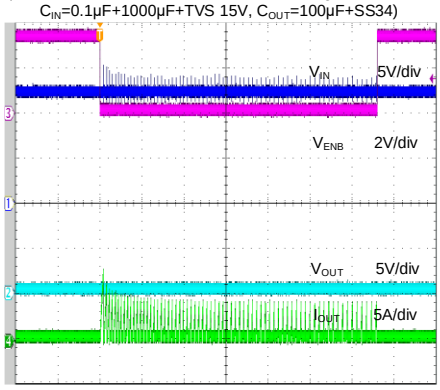
(V_{IN}=12V, ENB=0V, VCP=Floating, R_{LIMIT}=619Ω, C_{IN}=0.1μF+1000μF+TVS 15V, C_{OUT}=100μF+SS34)



Time (2ms/div)

First Short then Startup Test

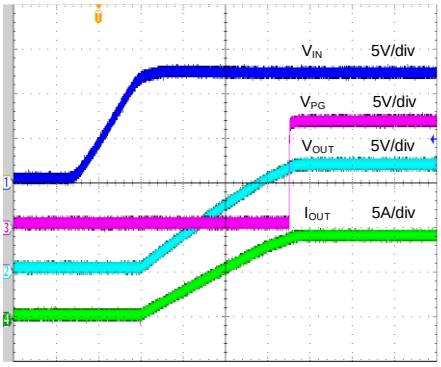
(V_{IN}=12V, ENB=3.3V~0V~3.3V, VCP=Floating, R_{LIMIT}=619Ω, C_{IN}=0.1μF+1000μF+TVS 15V, C_{OUT}=100μF+SS34)



Time (20ms/div)

IN ON

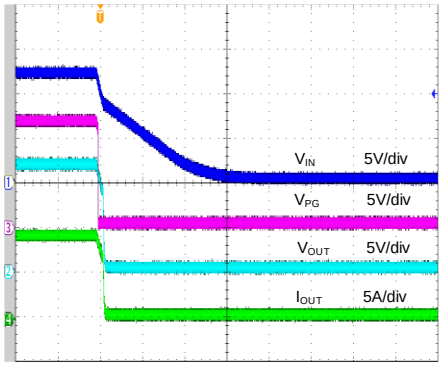
(V_{IN}=12V, ENB=0V, VCP=Floating, C_{IN}=0.1μF+1000μF, C_{SST}=10nF, C_{OUT}=100μF，R_{LIMIT}=619Ω, I_{OUT}=9A)



Time (800μs/div)

IN OFF

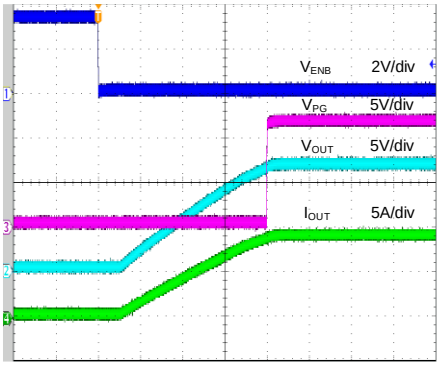
(V_{IN}=12V, ENB=0V, VCP=Floating, C_{IN}=0.1μF+1000μF, C_{SST}=10nF, C_{OUT}=100μF，R_{LIMIT}=619Ω, I_{OUT}=9A)



Time (10ms/div)

EN ON

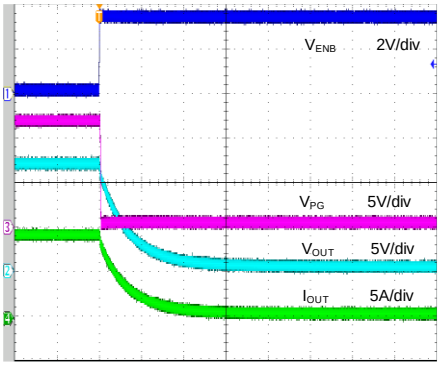
(V_{IN}=12V, ENB=3.3V~0V~3.3V, VCP=Floating, R_{LIMIT}=619Ω, C_{IN}=0.1μF+1000μF, C_{SST}=10nF, C_{OUT}=100μF，I_{OUT}=9A)



Time (800μs/div)

EN OFF

(V_{IN}=12V, ENB=3.3V~0V~3.3V, VCP=Floating, R_{LIMIT}=619Ω, C_{IN}=0.1μF+1000μF, C_{SST}=10nF, C_{OUT}=100μF，I_{OUT}=9A)



Time (200μs/div)

Operation

The SY86809A is an electronic fuse (eFuse) that incorporates a power delivery path designed to safeguard the power supply within system. It initiates its operation by monitoring the IN bus.

When V_{IN} > V_{UVLO} and V_{ENB} < V_{ENL}, the device is enabled, allowing current to flow from IN to OUT. And the internal power path is disabled when V_{IN} < V_{UVLO} or V_{ENB} > V_{ENH}.

Following a successful initialization, the device actively supervises its load current and input voltage, managing the internal FET to guarantee that the user-defined overcurrent protection limit (I_{ILIM}) is not exceed. It also clamps overvoltage spikes when the clamping output voltage threshold (V_{CLP}) is exceeded. Additionally, the device is equipped with fast severe overcurrent protection in the event of a short circuit, safeguarding the system from potentially damaging voltage and current levels.

The device is also equipped with an integrated thermal sensor that triggers a shutdown to safeguard the device if the junction temperature exceeds the recommended operating temperature range.

IN Pin

A 0.1μF or larger input ceramic capacitor is strongly recommended to be placed close to IN pin. An output short or heavy load transient condition will cause ringing on the IN pin. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage even for a short duration. Keep the area formed by the input capacitor, IN and GND as small as possible.

In hot plug application, a 0.1 μF or less input ceramic capacitor is recommended to reduce input inrush current. In addition, a TVS must be added to prevent transient voltage from exceeding the absolute maximum rating of the device in the application of long input cable. And the selected TVS clamp voltage should be lower than ABS voltage of the device.

Output Pin

A 100μF or larger output ceramic capacitor is recommended to be placed close to the IC to reduce voltage drop during load transient. A 100μF or larger high-value electrolytic capacitor is recommended to be placed on the output pin in large transient current application.

For long output cable application, an anti-parallel Schottky diode must be placed as close to the OUT pin as possible to absorb the negative ringing caused by the long cable with large parasitic inductance.

Under Voltage Lockout

The SY86809A has a fixed threshold inside the under-voltage lockout (UVLO) at the IN pin. When V_{IN} > V_{UVLO} and V_{ENB} < V_{ENL}, the device is enabled, and the output voltage soft starts with t_{SS}, allowing current to flow from IN to OUT. And the internal power path is disabled when V_{IN} < V_{UVLO} or V_{ENB} > V_{ENH}.

By setting different VCP pin states, the input UVLO threshold changes as follows:

Table 1 Input UVLO Threshold Selection

VCP	Input UVLO Threshold		
	Min	Typ	Max
LOW	2.7V		2.9V
HIGH	3.4V		3.8V
Floating	8.1V		9V

Soft-start Time Program

The device has a controlled output slew rate, providing soft start functionality. This limits the inrush current caused by the output capacitor(s) charging and enables these devices to be used in hot-swap applications. The slew rate can be decreased with an external capacitor added between the SST pin and the ground.

Recommended formula for t_{SST} calculation:

$$t_{SS} = \frac{0.8 \times V_{IN} \times C_{SST}}{AV_{SS} \times I_{SST}}, (C_{SST} \geq 1\text{nF}, 2.95\text{V} \leq V_{IN} \leq 15\text{V})$$

Where, t_{SS_DLT} is the internally fixed default soft-start time, about 0.6ms, which means there's no any external C_{SST}; I_{SST} is the internal current source, about 4μA. t_{SS} is defined as the rise time of the output voltage equal to 10% ×V_{IN} to 90% ×V_{IN}. AV_{SS} is the Gain of V_{OUT}, V_{SST}, about 10V/V.

Inrush current can be calculated based on the given output capacitance and slew rate:

$$I_{INRUSH}(mA) = C_{OUT}(\mu\text{F}) \times \frac{0.8 \times V_{IN}}{t_{SS}}$$

Power Good Indication

The SY86809A offers an active high digital output signal (PG), which functions as an indicator of a stable power supply and is active when the device is operating normally and ready to provide power. The PG pin is an open-drain type and require an external pull-up resistor to an appropriate power source. Once the PGTH pin voltage is above V_{PGTHR}, the PG signal is activated after a deglitch time (t_{PGR}). If the FET is turned off at any time or PGTH pin voltage falls below V_{PGTHF}, PG is de-asserted. The time required for the PG to clear its assertion is t_{PGF}.

The table summarizes the PG responses to various fault conditions.

As shown below Figure 3, the PG trip point can be adjusted using the external voltage divider network consisting of R_1, and R_2, which is connected between the OUT and GND pins of the device. The values required are calculated by solving the following equations:

$$V_{PG} = \frac{V_{PGTHR} \times (R_1 + R_2)}{R_2}$$

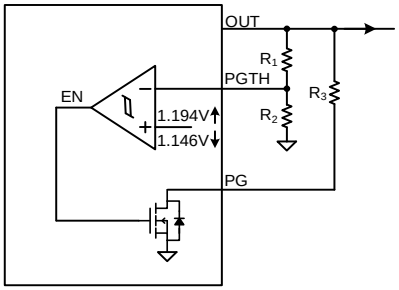


Figure3. PGTH thresholds set by R_1 and R_2

Table 2 PG Indication Summary

Event	Protection Response	PG pin	PG Delay
Over Temperature	Shutdown	H (if V_{PGTH}>V_{PGTHR})	t_{PGR}
		L (if V_{PGTH}<V_{PGTHF})	t_{PGF}
Under Voltage (UVP or UVLO)	Shutdown	L	
Over Voltage	Clamping	H (if V_{PGTH}>V_{PGTHR})	t_{PGR}
		L (if V_{PGTH}<V_{PGTHF})	t_{PGF}
Steady-State	None	H (if V_{PGTH}>V_{PGTHR})	t_{PGR}
		L (if V_{PGTH}<V_{PGTHF})	t_{PGF}
Persistent Over Current	Current Limit	H (if V_{PGTH}>V_{PGTHR})	t_{PGR}
		L (if V_{PGTH}<V_{PGTHF})	t_{PGF}
Output Short Circuit to GND	Fast trip followed by current limit	H (if V_{PGTH}>V_{PGTHR})	t_{PGR}
		L (if V_{PGTH}<V_{PGTHF})	t_{PGF}

Output Voltage Clamp Function

The SY86809A integrates output clamping function to ensure that the subsequent system is not affected by input overvoltage.

When the surge overvoltage occurs at the IN pin, the SY86809A quickly suppresses the climb of the output voltage around 6μs, ultimately limiting the output voltage to near the clamping threshold.

By setting different VCP pin states, the output clamp voltage threshold changes as follows:

Table 3 Output Clamp Voltage Selection

VCP	VIN		Clamping Threshold		
			Min	Typ	Max
LOW	3.3V	Over 4V	3.6V	3.8V	4V
HIGH	5V	Over 6V	5.4V	5.7V	6V
Floating	12V	Over 14V	12.6V	13.3V	14V

Analog Load Current Monitor

As shown in the figure, The SY86809A allows the system to accurately monitor the output load current by providing an analog current sense output on the ILIM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILIM}) across the R_{ILIM} to get a measure of the output load current.

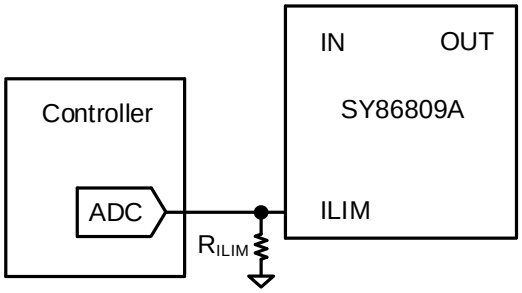


Figure4. Load Current Monitoring Schematic

Use the following formula to determine the output load current (I_{LOAD}):

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$$I_{LOAD}(A) = \frac{V_{ILIM}(\mu V)}{G_{ILIM}(\mu A/A) \times R_{ILIM}(\Omega)}$$

G_{ILIM} is the current sense ratio of I_{ILIM}: I_{LOAD}, about 90μA/A.

To achieve a higher detection accuracy for load current, the ILIM pin voltage must exceed 150mV due to the offset current present on the ILIM pin.

Current Limit Protection

At all times load current is monitored by sensing voltage across an internal sense resistor. During overload events, current is limited to the current limit (I_{ILIM}) programmed by R_{ILIM} resistor.

The value of R_{ILIM} for setting the overcurrent threshold can be determined by using the following formula.

$$R_{ILIM}(\Omega) = \frac{11k}{I_{ILIM}(A)}(\Omega)$$

The minimum recommended overcurrent threshold is 1A. Overcurrent threshold beyond 9A is not recommended.

For overload conditions, the internal current limit amplifier regulates the output current to $I_{ILIM.}$ The output voltage droops during the current regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold (T_{SD}), The internal FET is turned off. Once the chip temperature drops below T_{HYS}, the part will restart.

During start up stage, the SY86809A can limit the output current for overcurrent condition. And the current limit of device will be folded back at about 80%×I_{ILIM} to decrease power dissipation when V_{OUT} < V_{IN}-1V.

Short Circuit Protection

The device incorporates two distinct levels: a current limit (I_{ILIM}) and a fast-trip threshold (I_{FT}). Fast trip operation is shown in the following equation:

$$I_{FT}(A) = 2 \times I_{ILIM}$$

During a transient short circuit event, the current through the device increases very rapidly. As current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold I_{FT}. This comparator shuts down the pass device within 1μs, when the current through internal FET exceeds I_{FT} (I_{OUT} > I_{FT}), and terminates the rapid short-circuit peak current. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to I_{ILIM}. Then, device behaves similar to overload condition.

Thermal Shutdown Protection

An integrated thermal shutdown protection system monitors the junction temperature (T_J) at all times and forces a shutdown if the safe operating limit (T_{SD}) is exceeded, safeguarding the device.

The internal thermal shutdown protection turns off the MOSFET when internal die temperature T_J>150ºC (typical). Once the chip temperature drops below T_{HYS}, the part will restart.

Auto Output Discharge

The SY86809A features a built in output discharge capability that can fast eliminate residual charge on the larger output capacitors, preventing the bus from floating at an indeterminate voltage level. The internal discharge pulldown FET connected to the OUT pin is engaged when V_{ENB} > V_{ENH}, UVLO, or TSD.

PCB Layout Suggestion

For best performance of the SY86809A, the following guidelines must be strictly followed:

1) Use a ceramic decoupling capacitor with a 0.1μF or greater positioned between IN pin and GND pin for all applications.

2) Input and output capacitors should be placed closed to the IC. It is crucial to reduce the loop area that is created by the connection of the bypass capacitor to reduce noise coupling.

3) Keep all VBUS traces as short and wide as possible and use at least 2 ounce copper for all VBUS traces.

4) The IN and OUT pin serve as pathways for heat dissipation. It is advisable to connect these pins to the largest possible copper areas on both the top and bottom layers of the PCB by utilizing thermal vias. This vias positioned beneath the device also contribute to reducing the voltage gradient across the IN and OUT pads and ensures a consistent distribution of current throughout the device.

5) Protective components like TVS diodes, snubbers, capacitors, or diodes should be placed as close as possible to the device. It is essential to use short trace lengths when routing these protective components to minimize inductance. For instance, a Schottky diode can counteract negative voltage spikes caused by the switching of inductive loads. Additionally, a ceramic decoupling capacitor with a capacitance of at least 10μF is recommended to place between the OUT and GND pin. It is important to reduce the loop area created by the connections of the Schottky diode, the bypass capacitor, the OUT pin, and the device's GND pin.

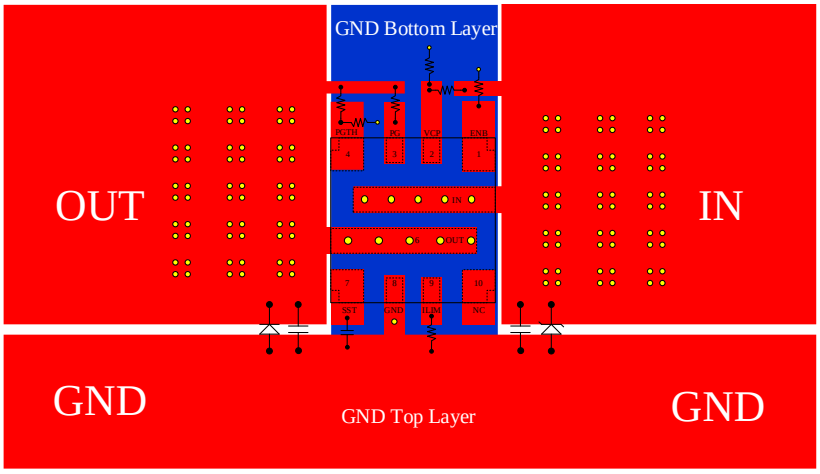
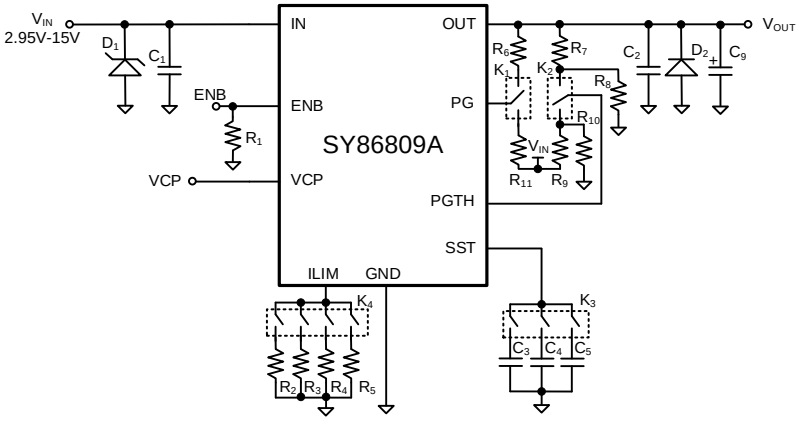


Figure 5. PCB Layout Suggestion

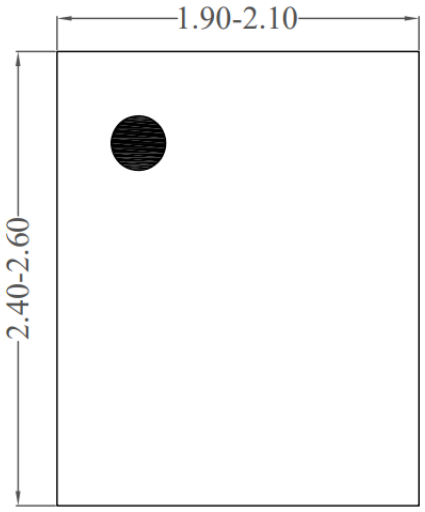
Schematic



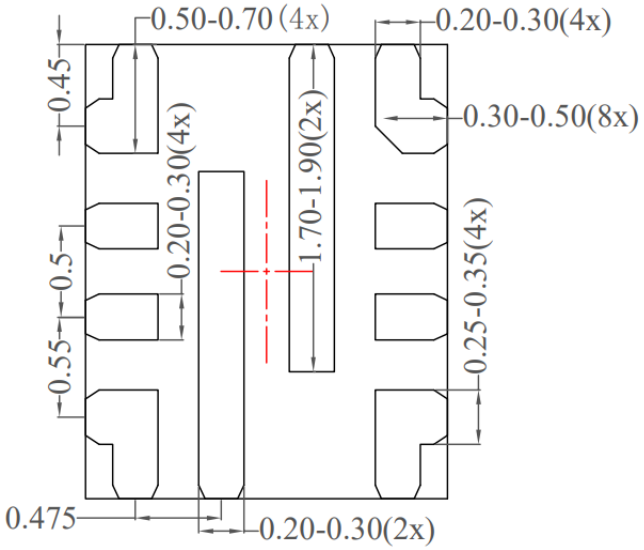
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1, C_5	100nF/50V, 0603	GRM188R71H104K	Murata
C_2	1μF/25V, 1206	GRM319R71E105K	Murata
C_3	10nF/50V, 0603	GRM188R71H103K	Murata
C_4	47nF/50V, 0603	GRM188R71H473K	Murata
C_9	100μF/25V		AISHI
D_1	SMAJ15CA	SMAJ15CA	Littelfuse
D_2	SS34	SS34	RoHS
R_9, R_{10}, R_{11}	Null		
R_1	10kΩ	RC0603FR-0710KL	YAGEO
R_6, R_7	100kΩ	RC0603FR-07100KL	YAGEO
R_8	12kΩ	RT0603BRD0712KL	YAGEO
R_2	11kΩ	RT0603BRD0711KL	YAGEO
R_3	3.32kΩ	RT0603BRE073K32L	YAGEO
R_4	2.2kΩ	RT0603BRD072K2L	YAGEO
R_5	1.1kΩ	RT0603BRD071K1L	YAGEO

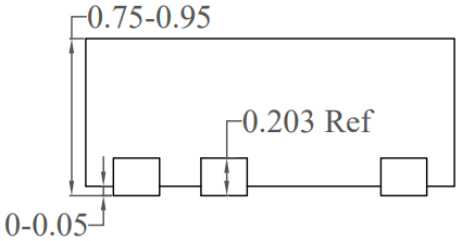
QFN2×2.5-10 Package Outline



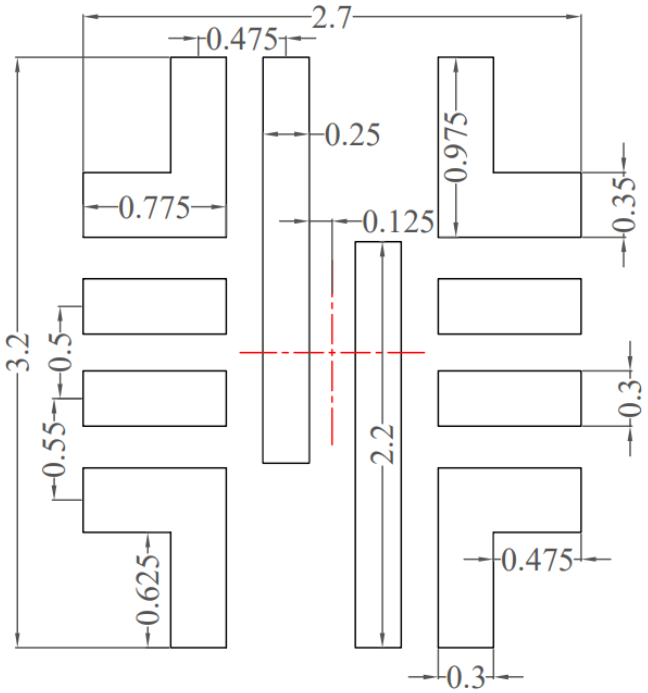
Top View



Bottom View



Side View

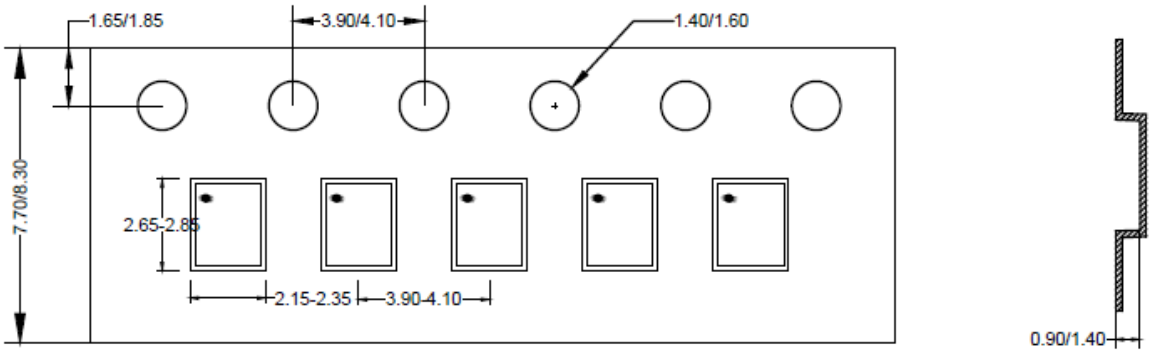


Recommended PCB Layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

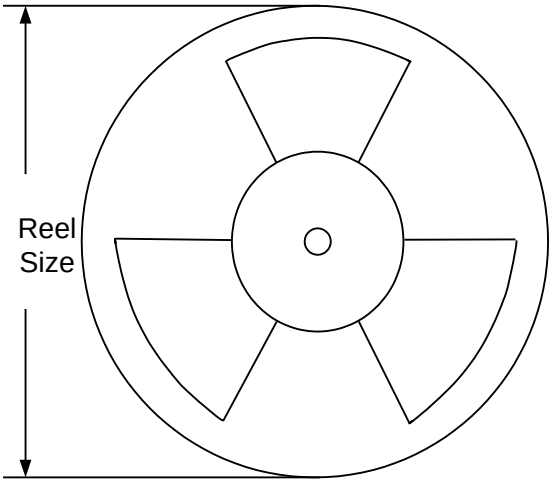
Tape and Reel Information

Tape Dimensions and Pin1 Orientation



Feed Direction ⟶

Reel Dimensions



Package Type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Qty per reel (pcs)
DFN2x2.5	8	4	7"	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 23, 2025	Revision 1.0	Initial Release

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