

General Description

The SA21340PDAD is an automotive grade, 300 mA high-current capacity linear regulator with ultra-low ground current and low dropout voltage. The device provides a fixed output voltage of 3.3V, also offers protective features, including over current limiting, output short-circuit protection, and over-temperature protection.

The SA21340PDAD is available in a compact DFN3×3-8 package.

Applications

- Industrial/Automotive Applications
- Portable/Battery-Powered Equipment
- Gateway Applications
- Remote Keyless Entry Systems
- Cellular Handsets
- SMPS Post-regulator/ DC-DC Modules
- Medical Imaging

Features

- Wide Input Voltage Range: 4V to 36V
- Fixed 3.3V Output Voltage
- Output Voltage Accuracy: $\pm 2\%$ over Temperature
- Low Dropout Voltage of 300mV at Full Load 300mA
- 300mA Maximum Load Current
- Ultra-low Quiescent Current
- Extremely Low Shutdown Current
- Stable with Tantalum or Ceramic Capacitors
- Excellent Load and Line Regulation
- Enable Control Input
- Over Current Limit Protection
- Output Short-Circuit Protection (Hiccup Mode)
- Over Temperature Protection with Auto Recovery
- RoHS Compliant and Halogen Free
- Moisture Sensitivity Level (MSL): 1
- Compact DFN3×3-8 Package
- Automotive AEC- Q100 Grade 1 Qualified

Typical Application

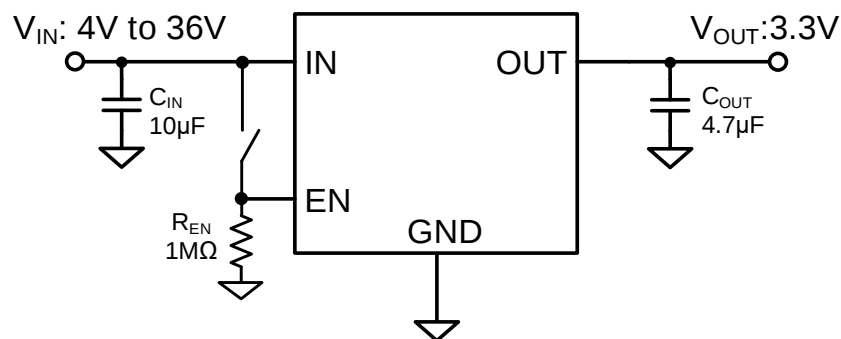


Figure1. Typical Application Schematic

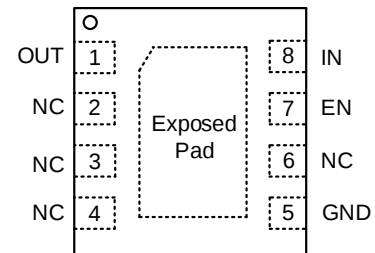
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA21340PDAD	DFN3×3-8 RoHS Compliant and Halogen Free	HLDxyz

Device Code: HLD

x=year code, y=week code, z=lot number code

Pinout (Top View)



Pin Description

Pin No.	Pin Name	Description
1	OUT	Output pin, decoupled with a recommended 4.7μF MLCC capacitor to GND.
2, 3, 4, 6	NC	No connection, leave it floating or connect to GND.
5	GND	Ground pin. Connect to the device thermal pad.
7	EN	Enable pin. Pull it high to enable the chip. Do not leave it floating.
8	IN	Input pin, decoupled with at least a 0.1μF MLCC capacitor to GND.
Exposed Pad		The exposed pad should be connected to the ground plane for better thermal performance.

Block Diagram

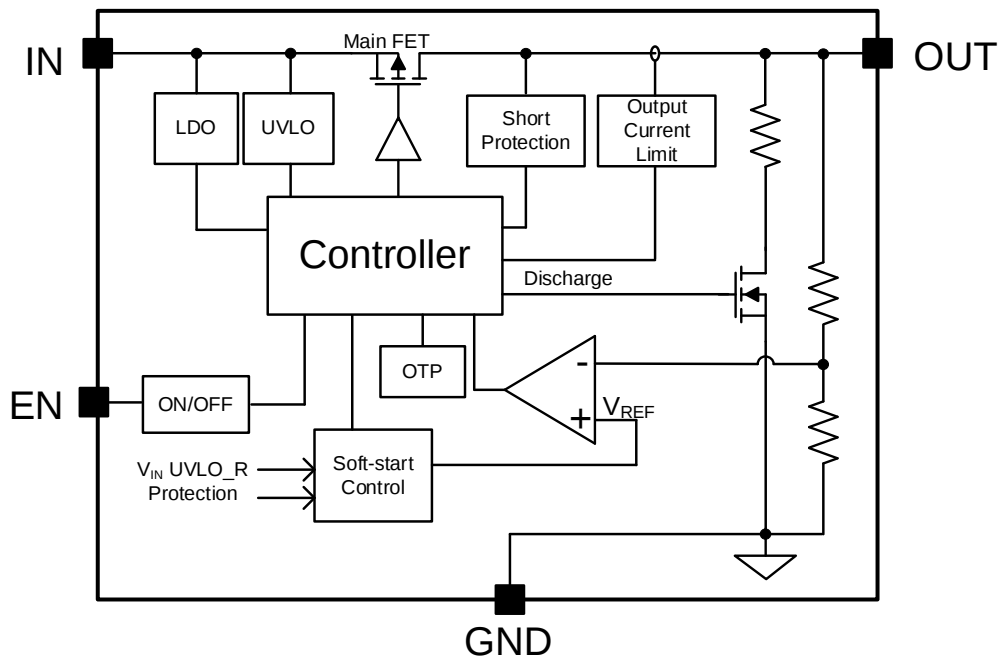


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
IN, EN to GND		-0.3	40	V
OUT to GND		-0.3	8	
Lead Temperature (Soldering, 10 sec.)			260	°C
Junction Temperature, Operating		-40	150	
Storage Temperature		-65	150	
V _{ESD} Electrostatic Discharge	Human-body model(HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
	Charged-device model(CDM), per JEDEC specification JESD22-C101		±500	V

Thermal Information

Parameter (Note 2)		Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	1s0p (Note 3)	233.5	°C/W
	2s2p (Note 4)	45.3	
$\theta_{JC(Top)}$ Junction-to-case(Top) Thermal Resistance		26.4	°C/W
$\theta_{JC(Bottom)}$ Junction-to-case(Bottom) Thermal Resistance		5.4	°C/W
θ_{JB} Junction-to-board Thermal Resistance (Note5)		20.8	°C/W
Ψ_{JB} Junction-to-board Characterization Parameter		13.24	°C/W
P _D Power Dissipation T _A =25°C	1s0p (Note 3)	0.53	W
	2s2p (Note 4)	2.75	W

Recommended Operating Conditions

Parameter (Note 6)		Min	Max	Unit
IN		4	36	V
OUT		0	8	
EN		0	36	
Output Current		0	300	mA
Input Capacitor C _{IN} (Note 7)		0.1		μF
Output Capacitor C _{OUT} (Note 7)		1	68	
Output Capacitor Equivalent Series Resistance (C _{OUT} ESR)		0.001	1	Ω
Operating Temperature	Ambient Temperature	-40	125	°C
	Junction Temperature	-40	150	°C

Electrical Characteristics

($V_{IN}=4V$ to $36V$, $T_A=-40^{\circ}C \sim 125^{\circ}C$, $T_A \leq T_J \leq 150^{\circ}C$, typical values are at $T_J=25^{\circ}C$, unless otherwise specified (Note8))

	Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage	V_{IN}		4		36	V
	Input Voltage UVLO Threshold	V_{UVLO}	V_{IN} rising	2.9	3.3	4	V
	UVLO Hysteresis	$V_{UVLO,HYS}$			200		mV
	Shutdown Current	I_{SHDN}	$V_{EN}=0V$, $T_J = -40^{\circ}C \sim 125^{\circ}C$			5	μA
	Quiescent Current	I_Q	$I_{OUT}=0mA$		15	22	μA
			$I_{OUT}=0.5mA$		16	23	μA
			$I_{OUT}=0.5mA$, $T_J=25^{\circ}C$			18	μA
Output	Output Voltage	V_{OUT}			3.3		V
	Output Accuracy	$V_{OUT,ACC}$		-2		+2	%
	Line Regulation	ΔV_{LNR}	$I_{OUT} = 5mA$		1	1.5	mV/V
	Load Regulation	ΔV_{LDR}	$V_{IN}=5V$, $5mA \leq I_{OUT} \leq 300mA$		27.5	55	mV/A
	Dropout Voltage	ΔV_{DROP}	$I_{OUT}=1mA$		1.5	3	mV
			$I_{OUT}=150mA$		150	300	mV
			$I_{OUT}=300mA$		300	600	mV
Enable (EN)	Enable Input Logic-High Voltage	$V_{EN,H}$		1.5			V
	Enable Input Logic-Low Voltage	$V_{EN,L}$				0.4	V
Short Protection	Output Short Protection Threshold	V_{SHORT}	Force V_{OUT} from 3.3V to 0V	0.264	0.528	0.99	V
	Output Short Off Time	$t_{SHORT,OFF}$			16		ms
Current Limit		I_{LIMIT}	Force $V_{OUT} = 3V$	600	900	1200	mA
Power Supply Rejection Ratio (Note 9)		PSRR	Frequency = 1kHz, $C_{OUT}=4.7\mu F$, $I_{OUT}=150mA$		53		dB
Soft-start Time		t_{SS}			1		ms
Thermal Shutdown Temperature		T_{SD}		155	170	185	$^{\circ}C$
Thermal Shutdown Hysteresis		T_{HYS}			20		$^{\circ}C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Based on JESD51-2A (Still-Air).

Note 3: Measured on a thermal conductivity test board based on JEDEC 51-3.

Note 4: Measured on a thermal conductivity test board with thermal vias based on JEDEC 51-5,7.

Note 5: Based on JEDEC 51-8.



SA21340PDAD

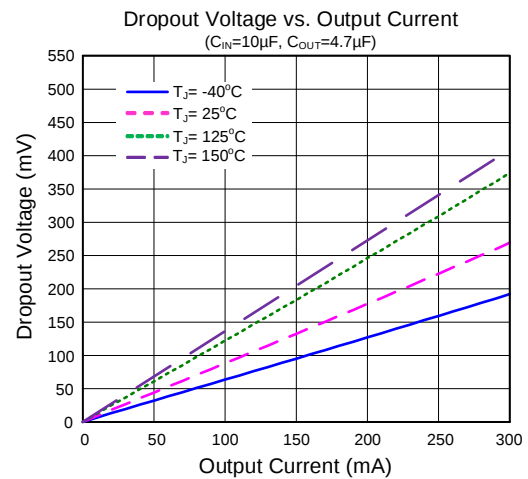
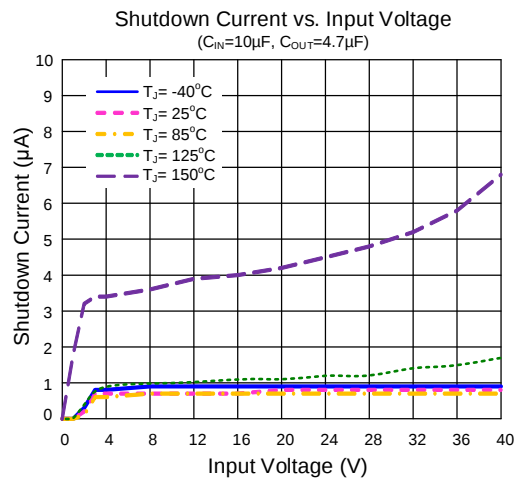
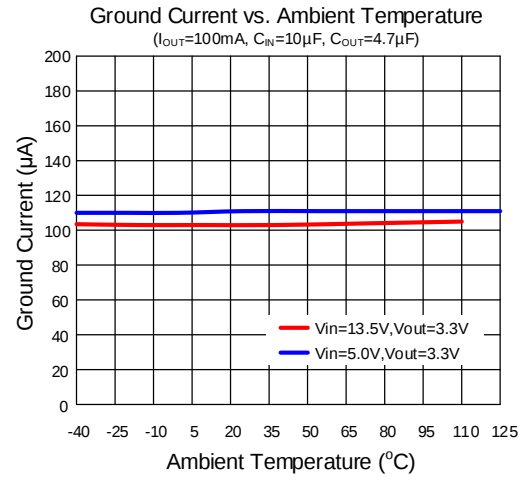
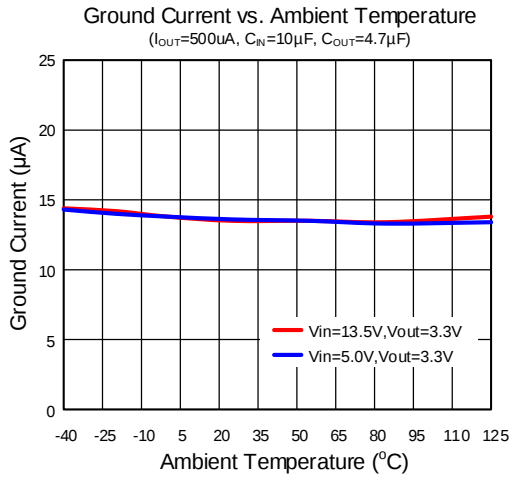
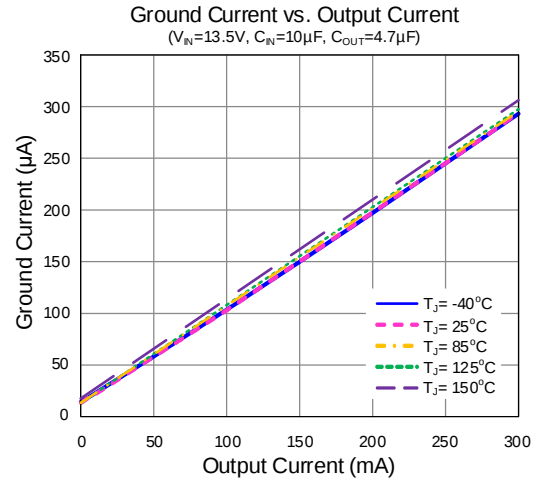
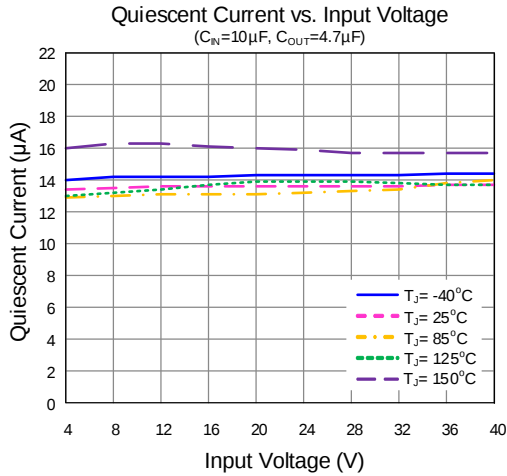
Note 6: The device is not guaranteed to function outside its operating conditions.

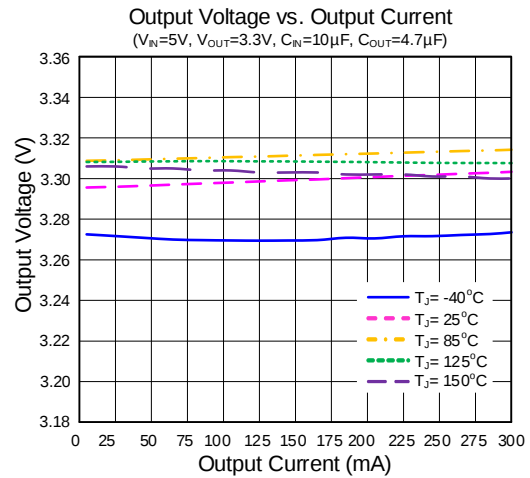
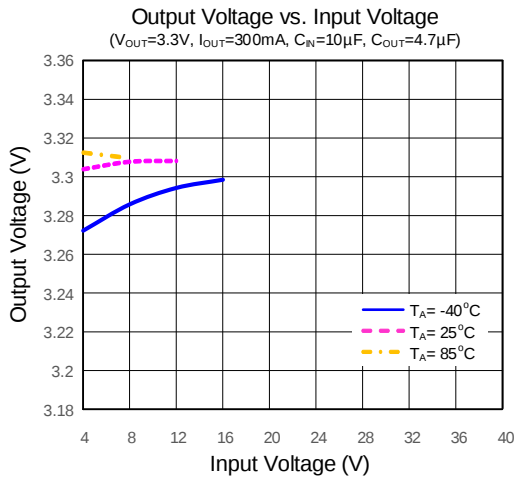
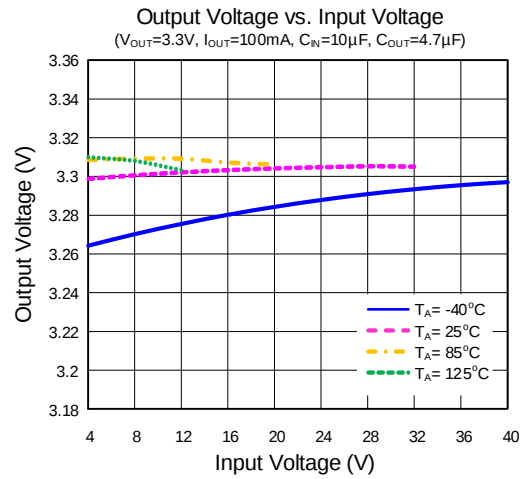
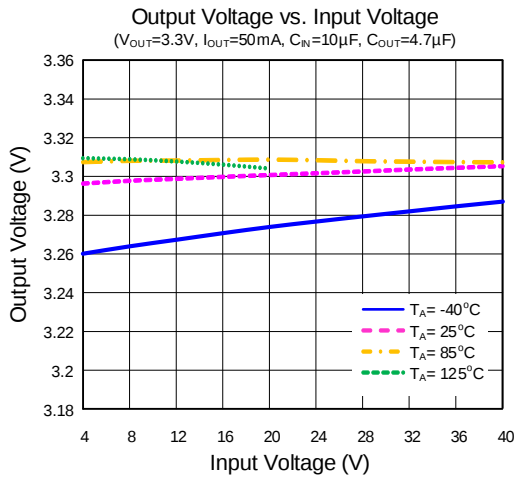
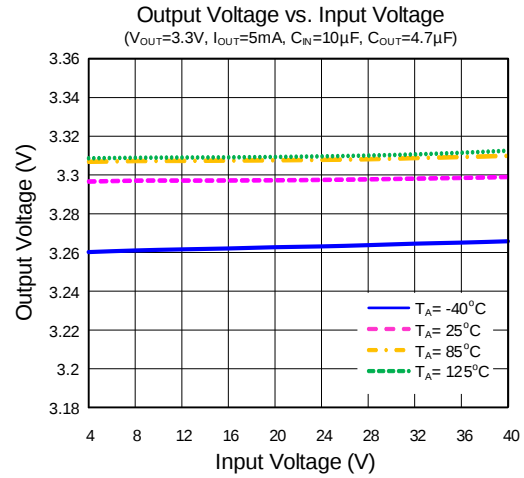
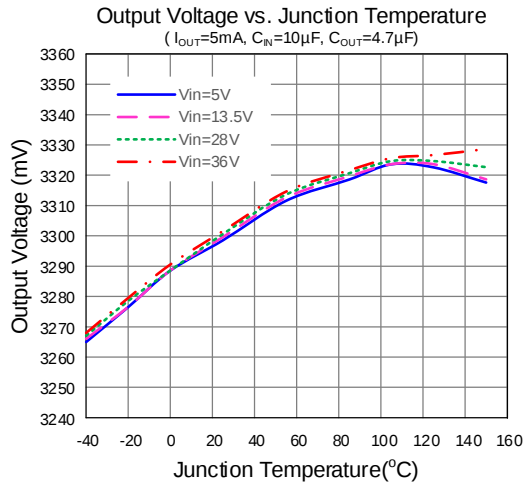
Note 7: Effective value, capacitance tolerance and temperature or DC bias characteristics should be taken into consideration.

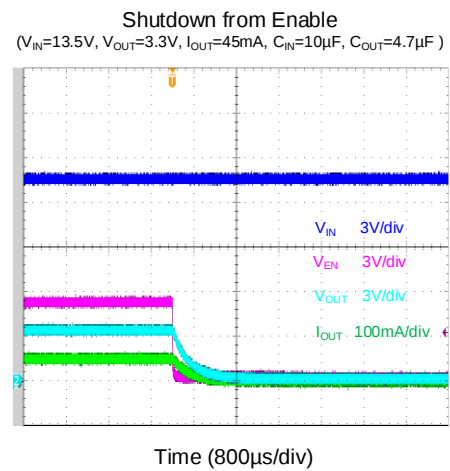
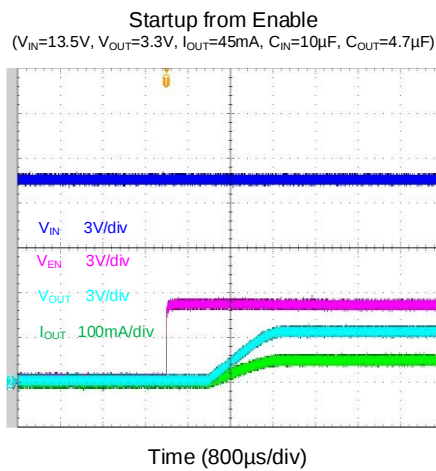
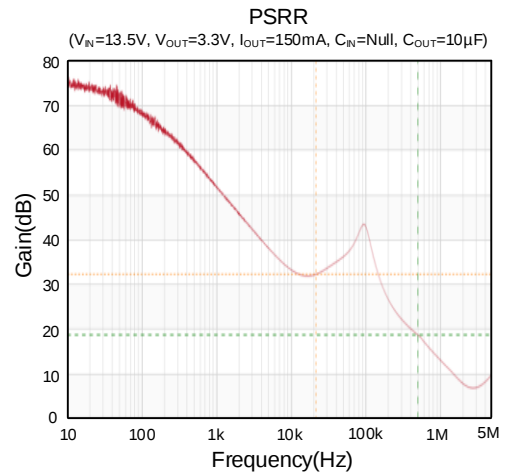
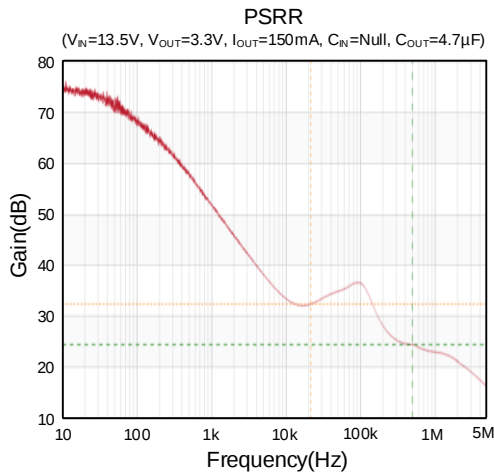
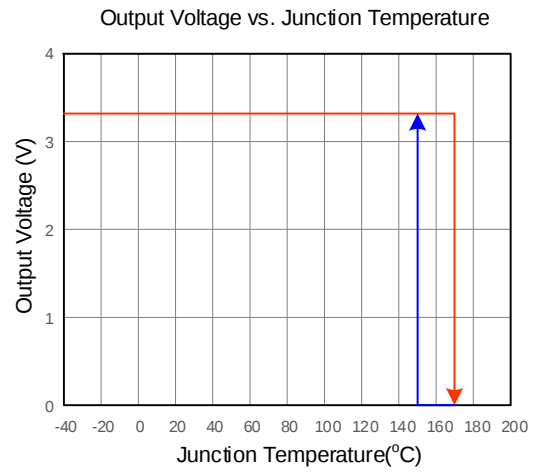
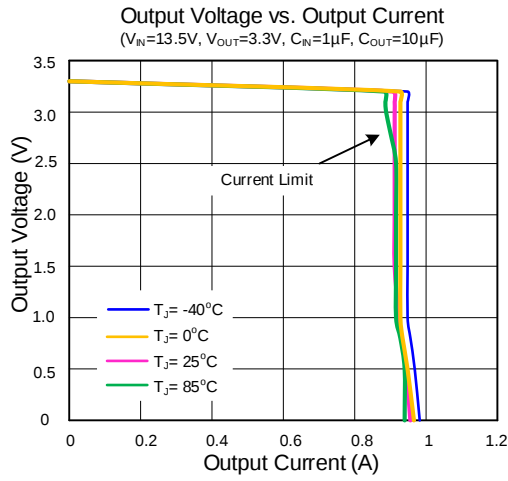
Note 8: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ\text{C}$. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 9: Guaranteed by design.

Typical Performance Characteristics

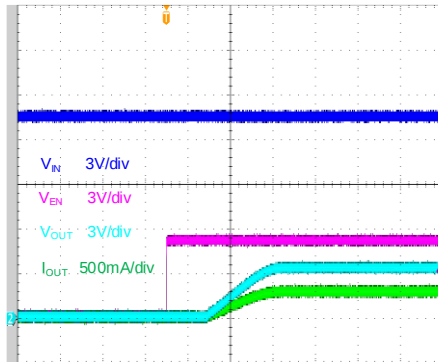






Startup from Enable

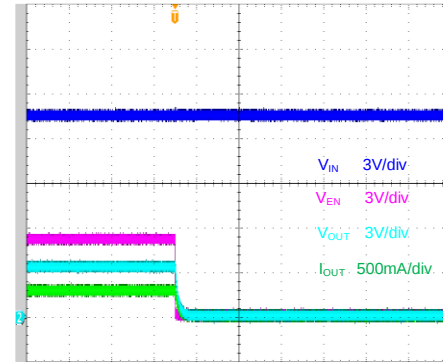
($V_{IN}=13.5V$, $V_{OUT}=3.3V$, $I_{OUT}=300mA$, $C_{IN}=10\mu F$, $C_{OUT}=4.7\mu F$)



Time (800μs/div)

Shutdown from Enable

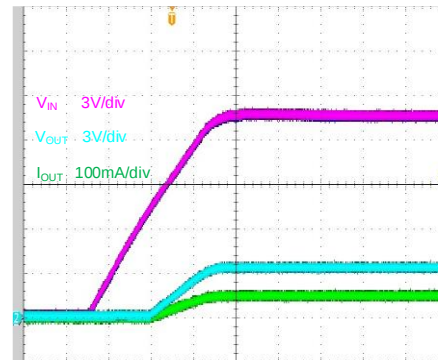
($V_{IN}=13.5V$, $V_{OUT}=3.3V$, $I_{OUT}=300mA$, $C_{IN}=10\mu F$, $C_{OUT}=4.7\mu F$)



Time (800μs/div)

Startup from VIN

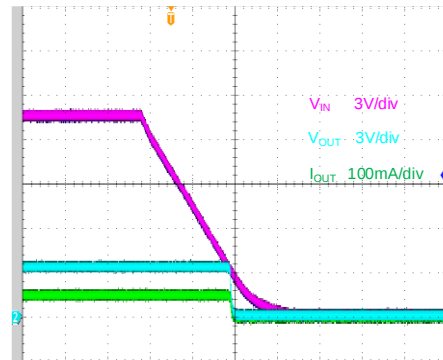
($V_{IN}=V_{EN}=13.5V$, $V_{OUT}=3.3V$, $I_{OUT}=45mA$, $C_{IN}=10\mu F$, $C_{OUT}=4.7\mu F$)



Time (800μs/div)

Shutdown from VIN

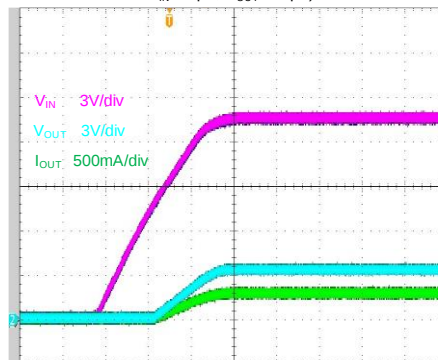
($V_{IN}=V_{EN}=13.5V$, $V_{OUT}=3.3V$, $I_{OUT}=45mA$, $C_{IN}=10\mu F$, $C_{OUT}=4.7\mu F$)



Time (10ms/div)

Startup from VIN

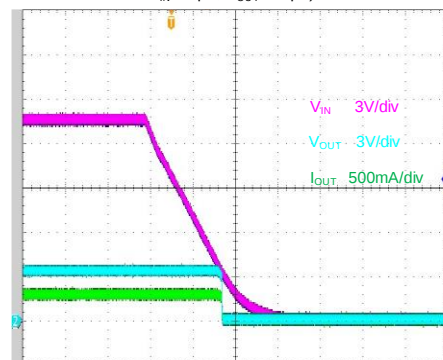
($V_{IN}=V_{EN}=13.5V$, $V_{OUT}=3.3V$, $I_{OUT}=300mA$, $C_{IN}=10\mu F$, $C_{OUT}=4.7\mu F$)



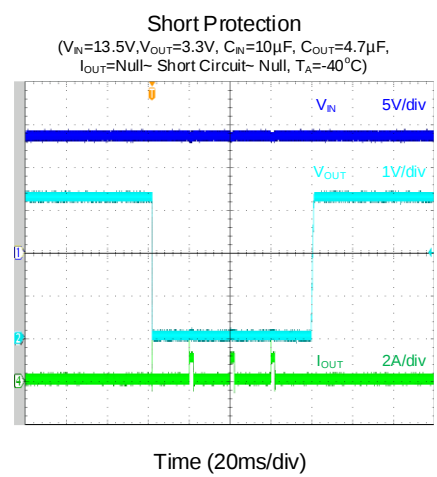
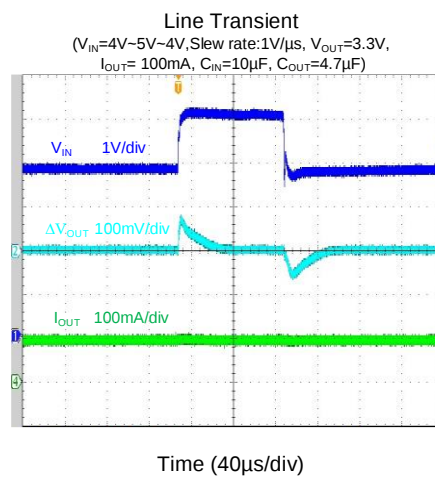
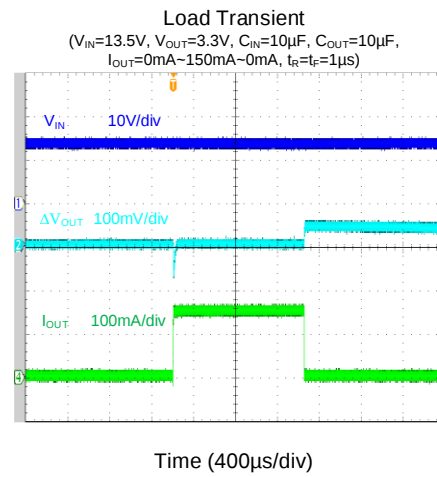
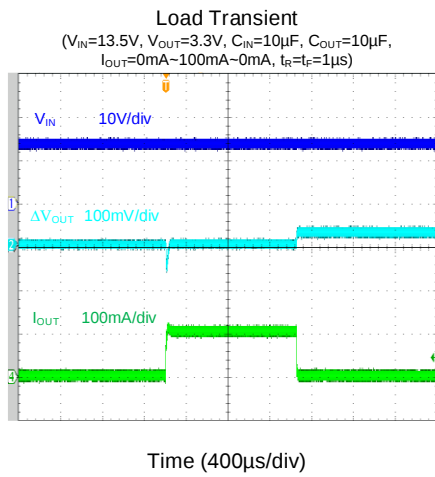
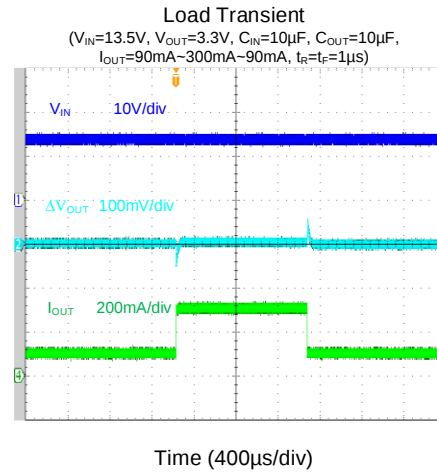
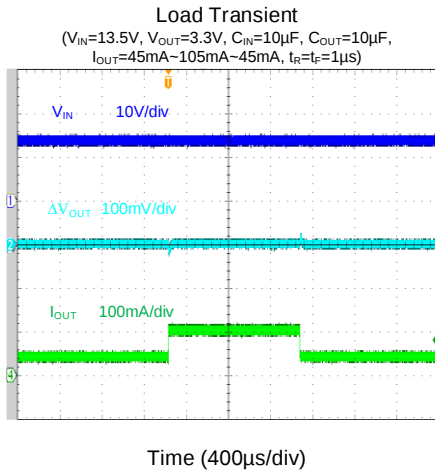
Time (800μs/div)

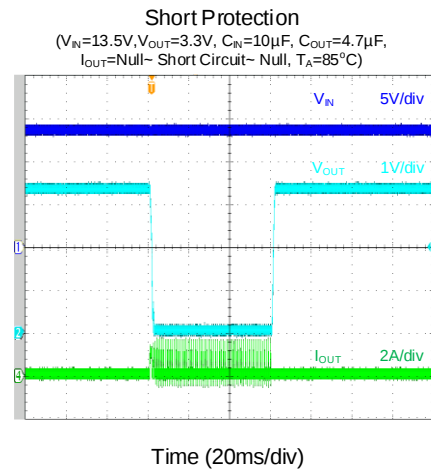
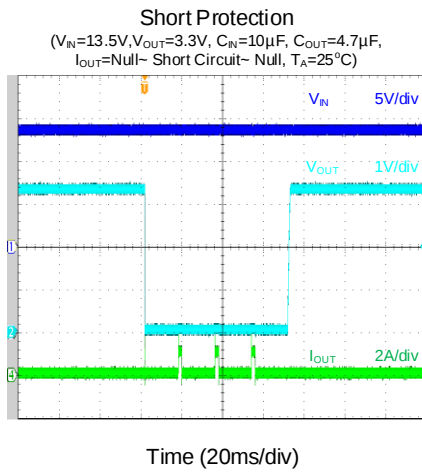
Shutdown from VIN

($V_{IN}=V_{EN}=13.5V$, $V_{OUT}=3.3V$, $I_{OUT}=300mA$, $C_{IN}=10\mu F$, $C_{OUT}=4.7\mu F$)



Time (10ms/div)





Detailed Description

General Features

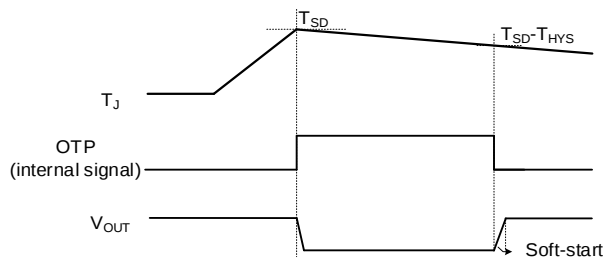
Input Under Voltage Lock-Out (UVLO)

To prevent operation before all internal circuitry is ready, the device remains in a shutdown state until V_{IN} exceeds the UVLO (rising) threshold.

Once this threshold is met and EN is active, the device initiates a soft-start ramp. If V_{IN} subsequently falls below $V_{IN, UVLO}$ minus the UVLO hysteresis, the device shuts down.

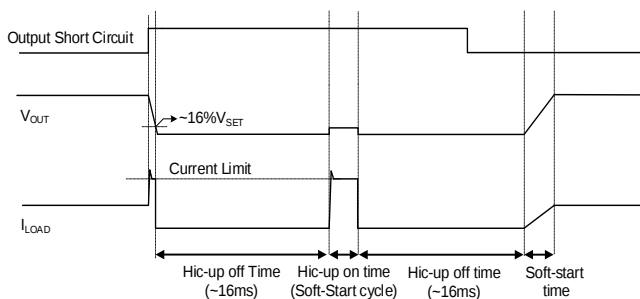
Over Temperature Protection (OTP)

The SA21340PDAD includes over-temperature protection (OTP) circuitry to prevent device damage due to excessive power dissipation. This will turn off the device when the junction temperature exceeds 170°C . Once the junction temperature cools down by approximately 20°C the device will resume normal operation.



Output Short-Circuit Protect

If V_{OUT} drops below approximately 16% of the OUT set point, the short-circuit protection mode will be initiated, and the device shuts down for approximately 16ms. The device then restart with a complete soft-start cycle. If the short circuit condition persists, another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the OTP threshold is reached.

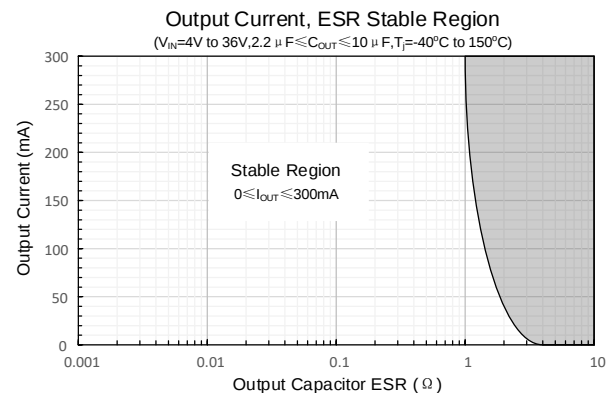
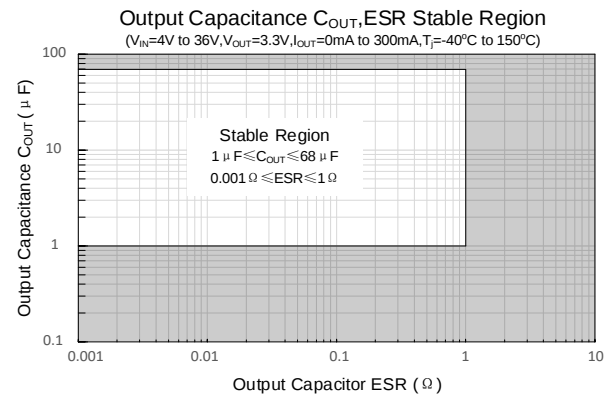


Input Capacitor C_{IN} and Output Capacitor C_{OUT}

For normal operation, a ceramic capacitor of at least

100 nF with an X7R grade or better is required to be placed close to the IN and GND pins. A larger value of the input ceramic capacitor can help improve noise immunity as well as improve power-supply rejection ratio (PSRR) and transient response. Care should be taken to minimize the loop area formed by C_{IN} and the IN/GND pins. A 10 μF low ESR ceramic capacitor is recommended for most applications.

For stable operation across the full temperature range, a 4.7 μF low-ESR ceramic capacitor is recommended. Use larger output-capacitor values such as 22 μF to reduce noise, improve load-transient response and enhance PSRR. Some ceramic dielectrics exhibit large capacitance and ESR variations with temperature.



Thermal Design Considerations

The SA21340PDAD can deliver a current of up to 300mA over the full operating temperature range. However, the maximum output current must be derated when operating at a higher ambient temperature. Across all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by the following thermal equation:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

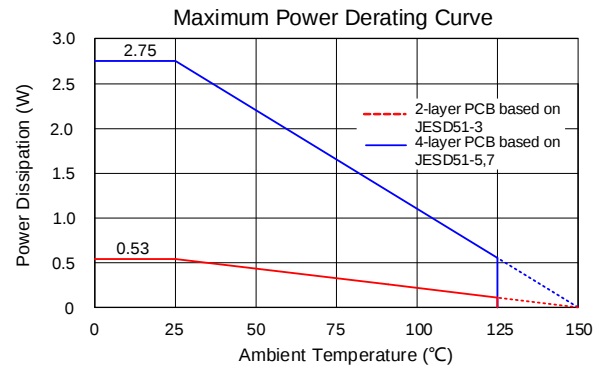
Where, $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 150°C, and the junction to ambient thermal resistance θ_{JA} is layout dependent. For the DFN3×3-8 package the thermal resistance θ_{JA} is 45.3°C/W when measured on a four-layer thermal test board with thermal vias based on JESD51-5, 7.

The maximum power dissipation at $T_A = 25^\circ\text{C}$ may be calculated by the following formula:

$$P_{D(MAX)} = (150^\circ\text{C} - 25^\circ\text{C}) / (45.3^\circ\text{C}/\text{W}) = 2.75\text{W}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . Use the derating curve in the figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

For optimal performance of the SA21340PDAD, the following guidelines must be strictly followed:

1. Place the input/output capacitors as close to the device as possible, minimizing the loop formed by these connections to improve transient performance.
2. Keep all power traces as short and wide as possible. The exposed pad should be connected to a large ground copper area and include multiple GND vias to the GND plane for efficient heat dissipation and noise reduction.
3. A 2-layer or 4-layer board is recommended for thermal performance and better current-handling capability.

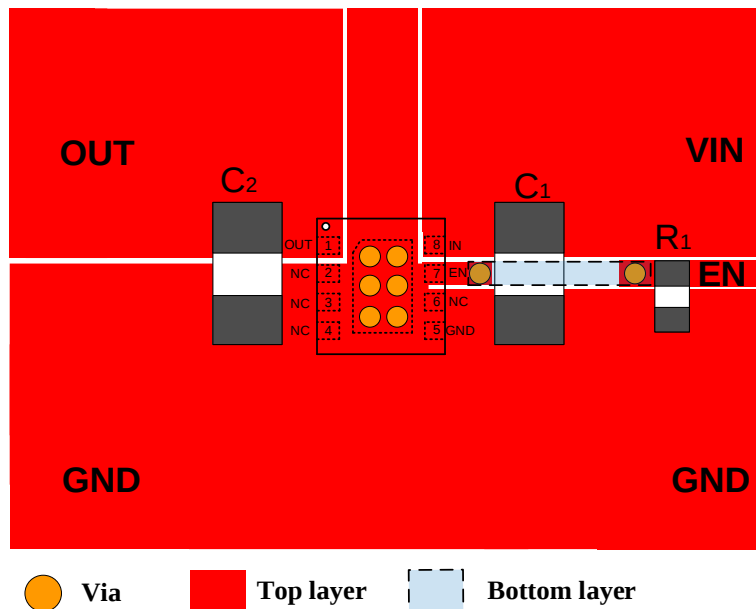
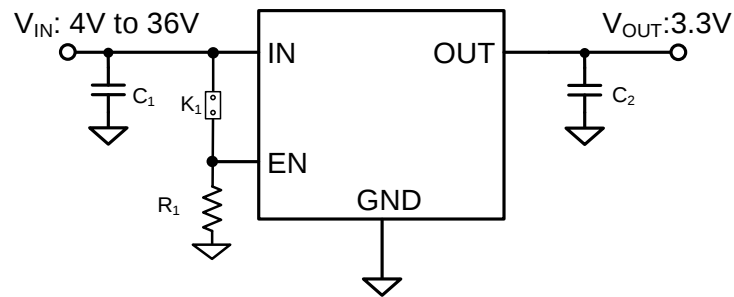


Figure3. PCB Layout Suggestion

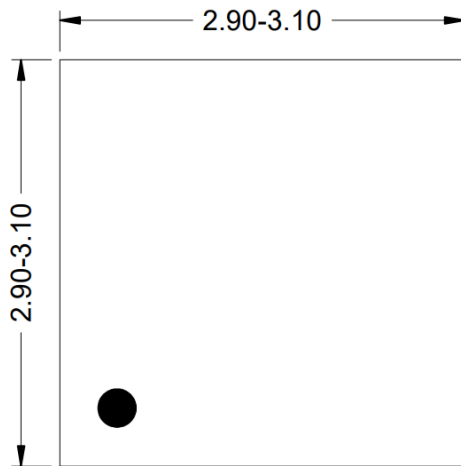
Schematic



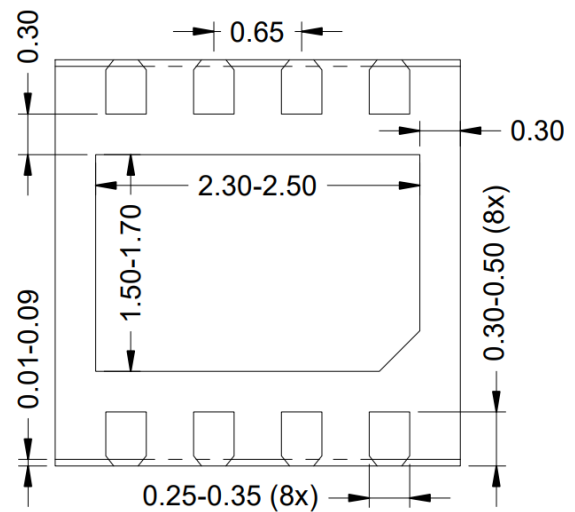
BOM List

Designator	Description	Part Number	Manufacturer
C ₁	10μF/50V/X7T,1206	GRM31CD71H106K	muRata
C ₂	4.7μF/50V/X7R,1206	GRM31CR71H475K	muRata
R ₁	1MΩ, 0603, 1%		

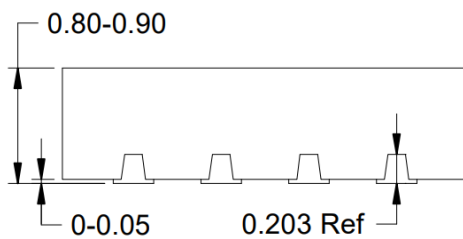
DFN3×3-8 Package Outline Drawing



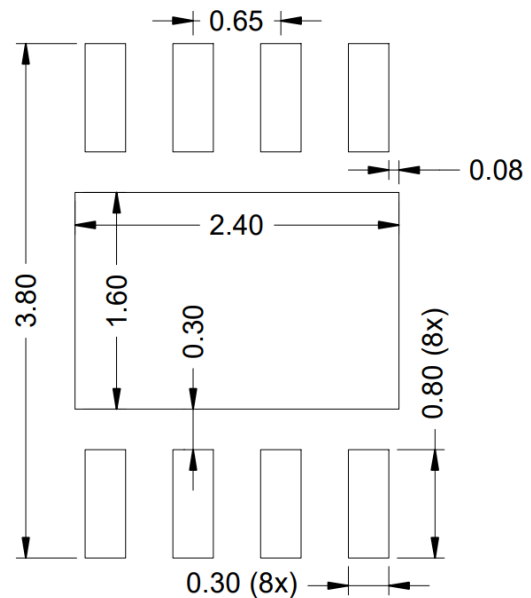
Top view



Bottom view



Front view

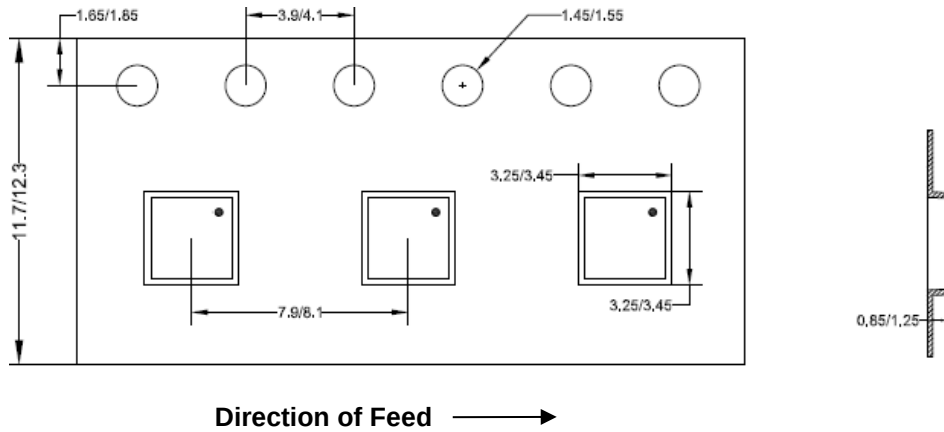


Recommended PCB layout
(Reference only)

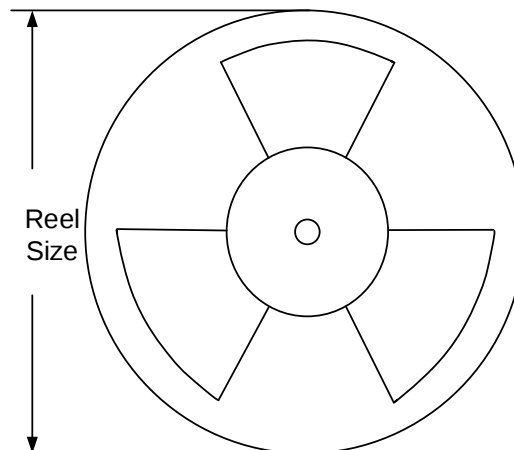
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Specification

Tape dimensions and pin 1 orientation



Reel dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN3×3	12	8	13"	400	400	5000



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.22, 2025	Revision 1.0	Initial Release

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