SA47301x

Automotive Power Management IC

General Description

The SA47301x is a multi-output power supply management device which integrates a multi-channel power supply for automotive applications. The pre-regulator can support a wide input voltage range of 3V to 40V, and up to 2.5A output current. Fully integrated switching regulators and linear regulators provide multiple output voltage rails, support low power mode and are available with various wake-up sources.

The SA47301x integrates safety functions, with two configurable fail-interrupt outputs which can meet ISO 26262 ASIL-D level.

The SA47301x is available in a compact QFN7×7-48 package.

Key Features

- 3V to 40V Input Voltage Range (6V to 40V if Boost Regulator is not used)
- Boost Regulator
  - Asynchronous Boost Regulator
  - 500kHz Fixed Switching Frequency
  - Maximum Duty Cycle of up to 95%
  - External Sense Resistor for Overcurrent Setting
- Buck Regulator
  - 5.8V Fixed Output Voltage
  - Integrated High Side Power MOSFET: 360mΩ (Typical)
  - Integrated Low Side Power MOSFET: 130mΩ (Typical)
  - Up to 2.5A Output Current
  - 2.2MHz or 400kHz Fixed Switching Frequency
- LDO1(MCU Supply, VUC)
  - Selectable Output Voltage (3.3V or 5.0V)
  - Maximum 600mA/850mA Output Current.
  - Output Voltage Accuracy ±2%
  - Output Current Limit Protection
- LDO2(Communication Supply, VCO)
  - Selectable Output Voltage (3.3V or 5.0V)
  - Maximum 300mA Output Current.
  - Output Voltage Accuracy ±2%
  - Output Current Limit Protection
- LDO3 (Tracker 1, VT1)
  - Output Voltage Derived from Voltage Reference (VR pin) or Fixed 5V
  - Maximum 150mA Output Current
  - ±10mV Voltage Tracking Accuracy to VR
- LDO4 (Tracker 2, VT2)
  - Output Voltage Derived from Voltage Reference (VR Pin) or Fixed 5V
  - Maximum 150mA Output Current
  - ±10mV Voltage Tracking Accuracy to VR
- LDO5 (Voltage Reference, VR)
  - Selectable Output Voltage (3.3V or 5.0V)
  - Maximum 200mA Output Current
  - Output Voltage Accuracy ±1%
- LDO6 (Standby LDO, VSTBY)
  - Selectable Output Voltage (3.3V or 5.0V)
  - Maximum 20mA Output Current
  - Output Voltage Accuracy ±4%
- Configurable Functional and Window Watchdog
- Provides Enable, Synchronization and a Voltage Monitor for an External Regulator.
- Independent Internal Voltage Monitoring Block
- Reset and Interrupt Output
- Two Safe State Outputs with Programmable Delay Time
- 16-bit SPI Communication Interface
- Input Overvoltage Protection
- Long Duration Timer (LDT)
- Error Signal Monitoring
- Multiple Wake-Up Sources
- Compact Package: QFN7×7-48, wettable flank
- Function Safety Meets ISO 26262 ASIL-D
- Automotive AEC- Q100 Grade 1 Certified
- MSL Rating: MSL3

Applications

- Electric Power Steering (EPS)
- Electrical Parking Brake (EPB)
- Transmission Control Unit (TCU)
- Active Suspension
- On-board Charger (OBC)
- Battery Management System (BMS)
- ADAS & Autonomous Driving
- Vehicle Control Unit (VCU)
- Zone Control Unit (ZCU)

Typical Applications

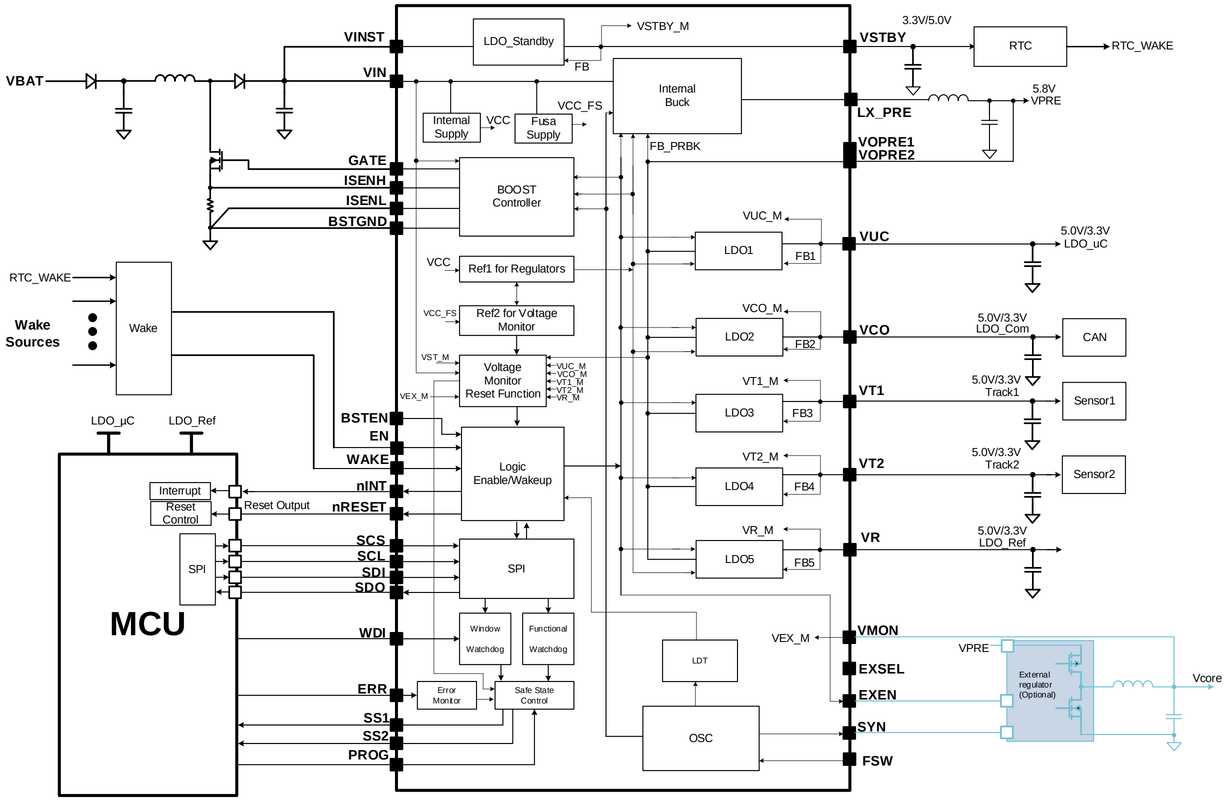


Figure 1. Application Schematic

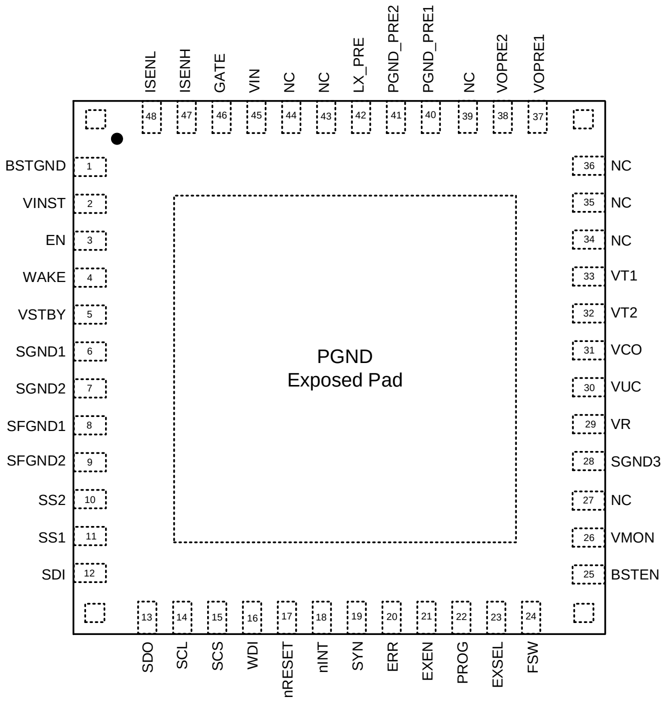
Ordering Information

Part Number	Top Mark	Package Type
SA47301QJQ	**GMP***xyz*	QFN7×7-48 RoHS-Compliant, Halogen-Free
SA47301BQJQ	**HLQ***xyz*	
SA47301CQJQ	**HLR***xyz*	
SA47301DQJQ	**HLT***xyz*	
SA47301EQJQ*	**HLW***xyz*	

**** = future product - specification subject to change; x = year code, y = week code, z = lot number code***

Part Number	Package Type	VSTBY	VUC	VR	VCO	VT1	VT2
SA47301QJQ	QFN7×7-48	5V	5V	5V	5V	5V	5V
SA47301BQJQ	QFN7×7-48	3.3V	3.3V	3.3V	5V	3.3V	3.3V
SA47301CQJQ	QFN7×7-48	3.3V	3.3V	3.3V	5V	5V	5V
SA47301DQJQ	QFN7×7-48	3.3V	3.3V	5V	5V	5V	5V
SA47301EQJQ	QFN7×7-48	3.3V	3.3V	3.3V	3.3V	3.3V	3.3V

Pinout (Top View)



(QFN7×7-48)

Pin Description

Pin Number	Pin Name	Pin Description
1	BSTGND	Boost Driver Ground: In order to avoid noise in sensitive ground, connect this pin to ground at the low side of the Boost current sense resistor. If Boost is not used, connect this pin to ground.
2	VINST	Voltage input pin of standby LDO: This pin is connected to the battery through the reverse protection diode and a filter capacitor placed between pin and ground. An EMC filter is recommended.

3	EN	Enable Input: The device will wake up when a rising edge signal appears on the EN pin. If the EN pin is not used, connect to ground.
4	WAKE	Wake Signal Input: The device will wake up when a logic high signal with defined length appears on the WAKE pin. If the WAKE pin is not used, connect to ground.
5	VSTBY	Standby LDO Output Pin: Connect a capacitor as close as possible to this pin.
6	SGND1	Signal Ground Pin 1: Connect this pin directly to ground.
7	SGND2	Signal Ground Pin 2: Connect this pin directly to ground.
8	SFGND1	Safety Signal Ground Pin 1: Connect this pin directly to ground. Connect this pin directly to the source of the safety NMOS if a safety switch is used.
9	SFGND2	Safety Signal Ground Pin 2: Connect this pin directly to ground. Connect this pin directly to the source of the safety NMOS if a safety switch is used.
10	SS2	Safe State Signal 2: The safe state output signal 2 signals a safe state. SS2 is delayed compared with SS1 and the delay can be adjusted via SPI command.
11	SS1	Safe State Signal 1: The safe state output signal 1 signals a safe state.
12	SDI	SPI Data Input: SPI signal input pin. Connect this pin to the MCU’s SPI port MOSI pin to receive commands during SPI communication.
13	SDO	SPI Data Output: SPI signal output pin. Connect this pin to the MCU’s SPI port MISO pin to receive commands during SPI communication.
14	SCL	SPI Clock: SPI clock input pin. Connect this pin to the MCU’s SPI clock for SPI communication.
15	SCS	SPI Chip Select: Connect this pin to the MCU’s SPI port “chip select” pin to address the device for SPI communication.
16	WDI	Watchdog Input, Trigger Signal: This is an input pin for trigger signal connected to MCU’s “Watchdog trigger signal output” pin. This pin is internally pulled down, leave floating if not used.
17	nRESET	Reset Output: This pin is an open drain structure that integrates a pull-up current source. A reset event will be detected when this pin is pulled low.
18	nINT	Interrupt signal: This pin uses a push-pull driver structure to signal interrupt events to the MCU. The MCU will read out the status registers by SPI. Connect this pin to a non-maskable interrupt (NMV) pin of the MCU.
19	SYN	Synchronization Output Signal: Connect this output to the synchronization input of an optional external regulator. The signal provides the switching frequency of the external regulator, in phase or shifted by 180° (selectable via SPI command). The external regulator will synchronize to the rising edge. Leave floating if not used.
20	ERR	Error Signal Input: Receive error signals from MCU safety managing unit. Connect the “error signal output” of the MCU to this pin.
21	EXEN	External Regulator Enable Pin: This pin connects to the enable input of the external regulator. Leave open if not used.
22	PROG	MCU Programming Support Pin:

		This pin can be pulled to ground to enable operation and can also be used for MCU debugging and programming purposes. Watchdog and ERR signals will be ignored if this pin is pulled high.
23	EXSEL	External Regulator Select Pin: If an external regulator is not used, connect this pin to ground directly or with a resistance less than 10 ohms. Leave open if the external regulator is used.
24	FSW	Switching Frequency Select Pin: Connect pin to ground directly for 400kHz switching frequency, or leave open for 2.2MHz switching frequency.
25	BSTEN	Boost Converter Enable Pin: Connect this pin to ground directly if the Boost pre-regulator is not used. Leave open if the Boost pre-regulator is used.
26	VMON	Monitor Pin for External Regulator Output Voltage: This pin is used to adjust the over and under voltage thresholds of the reset output signal nRESET by connecting an external resistor divider. Leave open if the external regulator is not used.
27	NC	Not connected
28	SGND3	Signal Ground, pin 3: Connect this pin directly to ground.
29	VR	Output Pin of LDO_REF: Connect a capacitor as close as possible to pin.
30	VUC	Output Pin of LDO_UC: Connect a capacitor as close as possible to pin.
31	VCO	Output Pin of LDO_COM: Connect a capacitor as close as possible to pin.
32	VT2	Output Pin of Tracker 2: Connect a capacitor as close as possible to pin.
33	VT1	Output Pin of Tracker 1: Connect a capacitor as close as possible to pin.
34	NC	Not connected
35	NC	Not connected
36	NC	Not connected
37	VOPRE1	Buck Pre-Regulator Feedback Pin. Decouple this pin to PGND_PRE1/2 with a 10uF MLCC capacitor. Always connect in parallel with pins VOPRE1 and VOPRE2.
38	VOPRE2	Power Input Pin of Post LDO Regulators. Decouple this pin to PGND_PRE1/2 with a 10uF MLCC capacitor. Always connect in parallel with pins VOPRE1 and VOPRE2.
39	NC	Not connected
40	PGND_PRE1	Power Ground Pin of Pre-Buck Regulator: Connect this pin straight to ground and Buck pre-regulator output capacitor negative terminal. Always connect in parallel with pin PGND_PRE2.
41	PGND_PRE2	Power Ground Pin of Pre-Buck Regulator: Connect this pin straight to ground and Buck pre-regulator output capacitor negative terminal. Always connect in parallel with pin PGND_PRE1.
42	LX_PRE	Switching Node Pin for Buck Pre-Regulator. Connect to the inductor of the Buck pre-regulator.
43,44	NC	Not connected
45	VIN	Voltage Input Pin of Buck Pre-Regulator: This pin is connected to the output of the Boost pre-regulator when the pre-regulator is used, otherwise it is connected to battery voltage with a reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
46	GATE	Gate of Low Side Switch of Boost pre-regulator: Connect to the gate of an external N-channel MOSFET. Leave open if the boost pre-regulator is not used.
47	ISENH	Boost Pre-Regulator Current Sense High Side Pin:

		This pin is connected to the high side of the current sense resistor. It is used to determine the maximum current threshold through the power MOSFET of the boost pre-regulator. Connect to ground if Boost pre-regulator is not used.
48	ISENL	Boost Pre-Regulator Current Sense Low Side Pin: This pin is connected to low side of the current sense resistor. It is used to determine the maximum current threshold through the power MOSFET of Boost pre-regulator. Connect to ground if Boost pre-regulator is not used.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN, VINST, GATE, ISENH, EN, WAKE, VT1, VT2, LX_PRE, SS1, SS2	-0.3	40	V
VOPRE1, VOPRE2	-0.3	7	
nRESET, SCS, SCL, SDI, SDO, nINT, WDI, ERR, VR, VCO, VUC, VMON, EXEN, SYNC, EXSEL, BSTEN, FSW, VSTBY, PROG	-0.3	6	
ISENL, BSTGND, PGND_PRE1, PGND_PRE2, SGND1, SGND2, SGND3, SFGND1, SFGND2	-0.3	0.3	
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	
ESD Susceptibility			
HBM (Human Body Model)	±2000		V
CDM (Charged Device Model)	±500		

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	25.5	°C/W
θ_{JC_TOP} Junction-to-Case(Top) Thermal Resistance	15	
θ_{JC_BOT} Junction-to-Case(Bottom) Thermal Resistance	5	
θ_{JB} Junction-to-Board Thermal Resistance	8.5	
P_D Power Dissipation $T_A = 25°C$	4.9	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN, VINST, GATE, ISENH, EN, WAKE, VT1, VT2, LX_PRE, SS1, SS2	-0.3	36	V
VOPRE1, VOPRE2	-0.3	6	
ISENL, nRESET, SCS, SCL, SDI, SDO, nINT, WDI, ERR, VR, VCO, VUC, VMON, EXEN, SYNC, EXSEL, BSTEN, FSW, VSTBY, PROG	-0.3	5.5	
Junction Temperature Range	-40	150	°C
Ambient Temperature Range	-40	125	

Electrical Characteristics

(V_{VIN} =6.0V to 40V, T_j = -40°C to +125°C, all voltages are measured with respect to ground, positive current flowing into pin, unless otherwise specified, **(Note 4)**)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
General Specifications	VIN Rising Voltage for Boost Start-Up Threshold	$V_{VIN\_POR\_Rising}$		4.3	4.5	4.7	V
	VIN Falling Voltage for Whole Chip Shutdown	$V_{VIN\_POR\_Falling}$		4.1	4.3	4.5	V
	VIN Start-up Voltage Threshold for Power Sequencing	$V_{VIN\_INIT\_Rising}$	Vin rising threshold to enter INIT state	5.6	5.8	6	V
	VIN Falling Threshold for Power Off State	$V_{VIN\_PD\_Falling}$	Vin falling threshold to enter power off state	4.9	5.1	5.3	V
	Quiescent Current (under no load and all selectable regulators, watchdog, LDT are turned off)	I_q	In INIT/NORMAL/WAKE state, $T_j \leq 85$℃, Boost is off, f_{sw} pin is floating, $10V \leq V_{IN} \leq 28V$			45	mA
			In STANDBY state, $T_j \leq 40$℃, Standby LDO is off, VIN =14V			60	μA
			In STANDBY state, $T_j \leq 85$℃, Standby LDO is off, $10V \leq V_{IN} \leq 28V$			80	μA
			In STANDBY state, $T_j \leq 85$℃, Standby LDO is on, $10V \leq V_{IN} \leq 28V$			100	μA
			In SLEEP state, $T_j \leq 85$℃			380	μA
			In FAILSAFE state, $T_j \leq 85$℃, $10V \leq V_{IN} \leq 28V$			250	μA
Boost Pre-Regulator	Boost Output Voltage	$V_{PRE\_REG,boost}$		7.00	7.50	8.00	V
	Boost Output Voltage Accuracy	-		-6.6		6.6	%
	Threshold External Sense Resistor for OC	$V_{ISENH-ISENL}$		190	210	230	mV
	High Side Sense Input Current	I_{ISENH}	V_{ISENH} =0V	-1		1	μA
	Input Under Voltage Threshold	$V_{PRE\_REG,boost,UV}$		8.0	8.3	8.6	V
	Input Under Voltage Threshold Accuracy	-		-3.6		3.6	%
	Input Under Voltage Threshold Hysteresis	$V_{PRE\_REG,boost,UV, hyst}$		80	-	300	mV
	Gate Driver Peak Sourcing Current	$I_{GATE,SRC}$		-	130	-	mA
	Gate Driver Peak Sinking Current	$I_{GATE,SNK}$		-	100	-	mA
	Gate Driver Output Voltage	V_{GATE}	V_{IN} >6V	4.5	5.0	5.5	V
	Maximum Duty Cycle	D_{MAX}		75	95		%
	Blanking Time	t_{Blank}		-	240	-	ns
	Boost Frequency Range	$f_{OSC,Boost}$		400	500	600	kHz
Buck Pre-Regulator	Output Voltage	$V_{PREREG,BUCK}$	PWM mode, $V_{IN} \geq 6.5$ V	5.65	5.80	5.95	V
	Output Voltage	$V_{PREREG,BUCK}$	PFM mode, $V_{IN} \geq 6.5$ V	5.60	5.80	6.00	V

	Power Stage High Side Switch On Resistance	$R_{ON, HS}$	V_{IN} ≥ 6 V	150	360	630	mΩ
	Power Stage Low Side Switch On Resistance	$R_{ON, LS}$	V_{IN} ≥ 6 V	65	130	195	mΩ
	Buck Peak Over Current Limit	$I_{PREREG, max}$		2.9	3.4	3.9	A
	LX_PRE Rise Time **(Note 5)**	$T_{R, LXPRE}$		2	6	14	ns
	LX_PRE Fall Time **(Note 5)**	$T_{F, LXPRE}$		2	9	18	ns
	Maximum Duty Cycle **(Note 5)**	$D_{BUCK, max}$				100	%
	Minimum Switch On Time **(Note 5)**	$t_{ON, min}$	I_{PREREG} ≥ 0.5 A	20	50	80	ns
	Soft Start Ramp	$t_{SS, BUCK}$	$V_{PREREG,BUCK}$ rising from 5% to 95% of $V_{PREREG,nominal}$; 2.2 MHz switching frequency, no load	70	190	380	µs
	SOFT Start Ramp	$t_{SS, BUCK}$	$V_{PREREG,BUCK}$ rising from 5% to 95% of $V_{PREREG,nominal}$; 400kHz switching frequency, no load	0.7	2	3.5	ms
	Over Temperature Warning Threshold	$T_{j,OT, WRN}$		130	140	150	°C
	Over Temperature Shutdown Threshold	$T_{j,OT, Shutdown}$		150	160	170	°C
	Over Temperature Sensor Hysteresis	$T_{j,OT, hyst}$		-	10	-	°C
	Buck Switching Frequency Range	$f_{OSC,Buck}$	FSW pin connected to GND	300	400	500	kHz
			FSW pin open	2000	2200	2500	kHz
LDO_UC Part (MCU Supply)	Output Voltage	V_{VUC}	0 mA ≤ I_{VUC}≤ 600 mA	4.9	5.0	5.1	V
		V_{VUC}	0 mA ≤ I_{VUC}≤ 600 mA	3.23	3.30	3.37	V
	Output Current Limitation	$I_{VUC, max}$	0x36[0]=0	650	-	1100	mA
			0x36[0]=1	850		1300	mA
	Dropout Voltage	$V_{dr, VUC}$	5.0V Output, 0 mA ≤ I_{VUC}≤ 600 mA	-	-	400	mV
			3.3V Output, 0 mA ≤ I_{VUC}≤ 600 mA	-	-	500	mV
	Load Regulation	ΔV_{VUC}	I_{VUC} = 100µA to 600 mA 5.0V Output	-	45	81	mV
			I_{VUC} = 100µA to 600 mA 3.3V Output	-	39	60	mV
	Power Supply Ripple Rejection **(Note 5)**	$PSRR_{VUC}$	V_{PREREG} = 5.8 V ; fripple = 100 kHz, $ESRC_{VUC}$ ≤ 100mΩ	26	-	-	dB
	Effective Output Capacitance **(Note 5)**	C_{VUC}		2.2	-	47	µF
	Output Capacitor, ESR **(Note 5)**	ESR C_{VUC}		0	-	200	mΩ
	Pulldown discharge resistance	R_{DIS_VUC}		10		40	Ω
	Over Temperature Warning Threshold	$T_{j,OT, WRN}$		130	140	150	°C
	Over Temperature Shutdown Threshold	$T_{j,OT, Shutdown}$		150	160	170	°C
	Over Temperature Sensor Hysteresis	$T_{j,OT, hyst}$		-	10	-	°C
LDO_COM (Communication Supply)	Output Voltage	V_{VCO}	0 mA ≤ I_{VCO}≤ 300 mA	4.9	5.0	5.1	V
	Output Current Limitation	$I_{VCO, max}$		350	-	500	mA
	Drop Voltage	$V_{dr, VCO}$	0 mA ≤ I_{VCO}≤ 300 mA	-	-	500	mV
	Load Regulation	ΔV_{VCO}	I_{VCO} = 100µA to 300 mA	-	40	70	mV

	Power Supply Ripple Rejection **(Note 5)**	PSRR$_{\text{VCO}}$	V$_{\text{PREREG}}$ = 5.8 V ; f$_{\text{ripple}}$ = 100 kHz, ESRC$_{\text{VCO}}$ ≤ 100mΩ	26	-	-	dB
	Effective Output Capacitance **(Note 5)**	C$_{\text{VCO}}$		1	-	47	µF
	Output Capacitor, ESR **(Note 5)**	ESR C$_{\text{VCO}}$		0	-	200	mΩ
	Pulldown discharge resistance	R$_{\text{DIS\_VCO}}$		10		40	Ω
	Over Temperature Warning Threshold	T$_{\text{j,OT, WRN}}$		130	140	150	°C
	Over Temperature Shutdown Threshold	T$_{\text{j,OT, Shutdown}}$		150	160	170	°C
	Over Temperature Sensor Hysteresis	T$_{\text{j,OT, hyst}}$		-	10	-	°C
Tracker 1/2 (Used for sensor supply)	Output Voltage Tracking Accuracy to Voltage Reference	ΔV$_{\text{Tx}}$	0 mA ≤ I$_{\text{VT1}}$≤ 150 mA	-10	-	10	mV
	Output Accuracy in 5V Mode		0 mA ≤ I$_{\text{VT1}}$≤ 150 mA	-1		1	%
	Output Current Limitation	I$_{\text{Tx, max}}$		170	-	360	mA
	Drop Voltage	V$_{\text{dr, Tx}}$	0 mA ≤ I$_{\text{VT1}}$≤ 150 mA	-	-	500	mV
	Power Supply Ripple Rejection **(Note 5)**	PSRR$_{\text{VTx}}$	V$_{\text{PREREG}}$ = 5.8 V ; f$_{\text{ripple}}$ = 100 kHz, ESRC$_{\text{VTx}}$ ≤ 100mΩ	26	-	-	dB
	Effective Output Capacitance **(Note 5)**	C$_{\text{VTx}}$		1	-	10	µF
	Output Capacitor, ESR **(Note 5)**	ESR C$_{\text{VTx}}$		0	-	200	mΩ
LDO_REF (Voltage Reference)	Output Voltage	V$_{\text{VR}}$	5.0V Output 0 mA ≤ I$_{\text{VR}}$≤ 150 mA	4.95	5.0	5.05	V
			3.3V Output 0 mA ≤ I$_{\text{VR}}$≤ 150 mA	3.267	3.3	3.333	V
	Output Current Limitation	I$_{\text{VR, max}}$		220	-	345	mA
	Drop Voltage	V$_{\text{dr, VR}}$	0 mA ≤ I$_{\text{VR}}$≤ 150 mA	-	-	400	mV
	Load Regulation	ΔV$_{\text{VR}}$	I$_{\text{VCO}}$ = 100µA to 150 mA	-	4.5	9	mV
	Power Supply Ripple Rejection **(Note 5)**	PSRR$_{\text{VR}}$	V$_{\text{PREREG}}$ = 5.8 V ; ESRC$_{\text{VR}}$ ≤ 100mΩ	26	-	-	dB
	Effective Output Capacitance **(Note 5)**	C$_{\text{QVR}}$		1	-	10	µF
	Output Capacitor, ESR **(Note 5)**	ESR C$_{\text{VR}}$		0	-	200	mΩ
Standby LDO	Output Voltage	V$_{\text{VSTBY}}$	5.0V Output 0 mA ≤ I$_{\text{VST}}$≤ 10 mA	4.8	5.0	5.2	V
			3.3V Output 0 mA ≤ I$_{\text{VST}}$≤ 10 mA	3.17	3.3	3.43	V
	Output Current Limitation	I$_{\text{VSTBY, max}}$		20	-	70	mA
	Drop Voltage	V$_{\text{dr, VSTBY}}$		-	-	400	mV
	Load Regulation	ΔV$_{\text{VSTBY, load}}$	5.0V Output I$_{\text{VST}}$ = 100 µA to 10 mA	-	25	40	mV
			3.3V Output I$_{\text{VST}}$ = 100 µA to 10 mA	-	20	40	mV
	Line Regulation	ΔV$_{\text{VSTBY, line}}$	5.0V Output	-	0.1	0.5	mV/V
	Line Regulation	ΔV$_{\text{VSTBY, line}}$	3.3V Output	-	0.1	0.5	mV/V
	Power Supply Ripple Rejection **(Note 5)**	PSRR$_{\text{VSTBY}}$	f$_{\text{ripple}}$ = 100 kHz ESRC$_{\text{VSTBY}}$ ≤ 100mΩ	40	-	-	dB
	Effective Output Capacitance **(Note 5)**	C$_{\text{VSTBY}}$		1	-	10	µF

	Output Capacitor, ESR **(Note 5)**	ESR C_{VSTBY}		0	-	200	mΩ
	Pulldown discharge resistance	R_{DIS_VSTBY}		10		40	Ω
nRESET Signals-Timing	Reset Cycle Time	t_{CYCLE}		9.4	10	10.65	µs
	Reset Delay Time, Default Value	t_{RD}		-	1000	-	t_{CYCLE}
	Reset Delay Time, Adjustable Range by SPI Command	t_{RD}		20	-	1500	t_{CYCLE}
	Reset Reaction Time **(Note 5)**	t_{RR}		8	-	20	µs
	Reset Reaction Time, Standby Regulator **(Note 5)**	$t_{RR,\ STBY}$	Exclude STANDBY state	8	-	40	µs
	LDO Short To Ground Detection Time	t_{StG}		2.7	3.0	3.3	ms
	Buck Regulator Short to Ground Detection Time	$t_{StG,BK}$	Buck 2.2 MHz switching frequency	2.7	3.0	3.3	ms
			Buck 400kHz switching frequency	5.4	6.0	6.6	ms
	VMON Short to Ground Detection Time	$t_{StG,VMON}$	Buck 2.2 MHz switching frequency	2.7	3.0	3.3	ms
			Buck 400kHz switching frequency	5.4	6.0	6.6	ms
	System Shutdown Time	t_{SDT}		9	-	20	ms
Reset Thresholds Standby Regulator, Pin VSTBY	Over Voltage Reset Threshold	$V_{OV,VST,high}$	5.0V Output	5.25	5.35	5.45	V
			3.3V Output	3.46	3.53	3.60	V
	Under Voltage Reset Threshold	$V_{UV,VST,low}$	5.0V Output	4.2	4.3	4.4	V
			3.3V Output	2.90	2.97	3.05	V
Reset Thresholds LDO_µC, Pin VUC	Over Voltage Reset Threshold	$V_{OV,VUC,high}$	5.0V Output	5.25	5.35	5.45	V
			3.3V Output	3.46	3.53	3.60	V
	Under Voltage reset threshold	$V_{UV,VUC,low}$	5.0V Output	4.2	4.3	4.4	V
			3.3V Output	2.90	2.97	3.05	V
Reset Thresholds V_PreReg, pins VOPREx	Over Voltage Reset Threshold	$V_{OV,FB,high}$		6.46	6.58	6.7	V
	Under Voltage Reset Threshold	$V_{UV,FB,low}$		5.0	5.1	5.2	V
Reset Thresholds LDO_COM, Pin VCO	Over Voltage Reset Threshold	$V_{OV,VCO,high}$	5.0V Output	5.4	5.5	5.6	V
			3.3V Output	3.46	3.53	3.60	V
	Under Voltage Reset Threshold	$V_{UV,VCO,low}$	5.0V Output	4.4	4.5	4.6	V
			3.3V Output	2.90	2.97	3.05	V
Reset Thresholds Voltage Reference, Pin VR	Over Voltage Reset Threshold	$V_{OV,VR,high}$	5.0V Output	5.25	5.35	5.45	V
			3.3V Output	3.46	3.53	3.60	V
	Under Voltage Reset Threshold	$V_{UV,VR,low}$	5.0V Output	4.2	4.3	4.4	V
			3.3V Output	2.90	2.97	3.05	V
Reset Thresholds Tracker1, Pin VT1	Over Voltage Reset Threshold	$V_{OV,VT1,high}$	5.0V Output	5.4	5.5	5.6	V
			3.3V Output	3.46	3.53	3.60	V
	Under Voltage Reset Threshold	$V_{UV,VT1,low}$	5.0V Output	4.4	4.5	4.6	V
			3.3V Output	2.90	2.97	3.05	V
Reset Thresholds	Over Voltage Reset Threshold	$V_{OV,VT2,high}$	5.0V Output	5.4	5.5	5.6	V
			3.3V Output	3.46	3.53	3.60	V

Tracker2, Pin VT2	Under Voltage Reset Threshold	$V_{UV,VT2,low}$	5.0V Output	4.4	4.5	4.6	V
			3.3V Output	2.90	2.97	3.05	V
Reset Thresholds External CORE (PIN VMON)	Over Voltage Reset Threshold	$V_{OV,VMON,,high}$		0.86	0.872	0.884	V
	Under Voltage Reset Threshold	$V_{UV,VMON, low}$		0.716	0.728	0.74	V
Input Voltage VIN/VINST Monitoring, Pin VIN/VINST	Input Over Voltage Reset Threshold	$V_{VIN,OV}$		40.2	42	44.2	V
Reset Output nRESET	Reset Output, pull-up Current	$I_{nRESET, pu}$	$V_{nRESET} \leq 2.0$ V	-220	-110	-15	µA
	Reset Output, Low Level	$V_{nRESET, low}$	V_{VUC} = 5.0 V, I_{nRESET} = 7 mA	-	-	0.7	V
	Reset Output, Low Level	$V_{nRESET, low}$	V_{VUC} = 5.0 V, I_{nRESET} = 3.5 mA	-	-	0.4	V
	Reset Output, Low Level	$V_{nRESET, low}$	V_{VUC} = 3.3 V, I_{nRESET} = 5.5 mA	-	-	0.7	V
	Reset Output, Low Level	$V_{nRESET, low}$	V_{VUC} = 3.3 V, I_{nRESET} = 3.0 mA	-	-	0.4	V
	Reset Output Fall Time	$t_{nRESET, fall}$	$C_{nRESET,load}$ = 50 pF	-	-	25	ns
Interrupt Output nINT	Interrupt Output, High Level	$V_{nINT, high}$	V_{VUC} = 5.0 V, I_{INT} = -9 mA	4.0	-	-	V
	Interrupt Output, Low Level	$V_{nINT, low}$	V_{VUC} = 5.0 V, I_{INT} = 7 mA	-	-	0.7	V
	Interrupt Output, High Level	$V_{nINT, high}$	V_{VUC} = 3.3 V, I_{INT} = -7 mA	2.3	-	-	V
	Interrupt Output, Low Level	$V_{nINT, low}$	V_{VUC} = 3.3 V, I_{INT} = 5 mA	-	-	0.7	V
	Interrupt Output Rise Time	$t_{nINT, rise}$	$C_{nINT,load}$ = 50 pF	-	-	25	ns
	Interrupt Output Fall Time	$t_{nINT, fall}$	$C_{nINT,load}$ = 50 pF	-	-	25	ns
	Minimum interrupt pulse width **(Note 5)**	t_{nINT}		70	100	130	µs
	Interrupt time out **(Note 5)**	t_{nINTTO}		260	300	340	µs
Enable Signal Input EN	Enable Upper Threshold	$V_{EN,hi}$	V_{EN} increasing	-	-	2	V
	Enable Lower Threshold	$V_{EN, lo}$	V_{EN} decreasing	0.8	-	-	V
	Enable Threshold Hysteresis	$V_{EN,hyst}$		-	400		mV
	Enable Signal, Rise Time **(Note 5)**	$t_{EN,rise}$		-	-	10	µs
	Enable Signal, Minimum High Time **(Note 5)**	$t_{EN,high}$		20	-	-	µs
	Enable High Input Current	$I_{EN,hi}$	V_{EN} = 16 V	-	8	11	µA
	Enable Low Input Current	$I_{EN,lo}$	V_{EN} = 0.5 V	-	0.1	2	µA
Wake Signal Input WAKE	Wake Upper Threshold	$V_{WAKE,hi}$	V_{WAKE} increasing			2	V
	Wake Lower Threshold	$V_{WAKE,lo}$	V_{WAKE} decreasing	0.8			V
	Wake Signal Hysteresis	$V_{WAKE,hyst}$			400		mV
	Wake Signal, Minimum Length **(Note 5)**	$t_{WAKE,min}$		40			µs
	Wake High Input Current	$I_{WAKE,hi}$			8	11	µA

	Wake Low Input Current	$I_{WAKE,lo}$			0.1	2	µA
State Machine Transition	INIT Timer	t_{INIT}		550	600	650	ms
	FAILSAFE Timer	$t_{FAILSAFE}$	Thermal shutdown	0.9	1	1.1	s
			Other conditions	18	20	22	ms
	Transition Delay Time Accuracy	-		-20		20	%
	LDO_UC Current Monitor Accuracy		10mA monitor current	-60		60	%
			30mA monitor current	-40		40	%
			60mA monitor current	-35		35	%
			100mA monitor current	-30		30	%
	State Transition Time	$t_{Transition}$	Does not include transition to SLEEP, transition to and from STANDBY			100	µs
	State Transition Time to INIT	$t_{TR,INIT}$	Does not include transition from STANDBY, FAILSAFE and POWERDOWN			150	µs
			From STANDBY and FAILSAFE			800	µs
	Startup Time from Power Down	t_{START}			0.4	2	ms
ERR Pin	ERR Pin High Voltage Level	$V_{ERR,High}$	V_{VUC}=5V	3.6			V
			V_{VUC}=3.3V	2			V
	ERR Pin Low Voltage Level	$V_{ERR,Low}$				0.8	V
	ERR Pin Hysteresis	$V_{ERR, Hys}$	V_{VUC}=5V		350		mV
			V_{VUC}=3.3V		160		mV
	ERR Pin Pull Down Current	$I_{ERR, PULL}$			150	330	µA
	Valid ERR Input Frequency Range	$f_{ERR, Valid}$	50% duty	10		45	kHz
	Invalid ERR Input Frequency Range	$f_{ERR, Invalid}$	Invalid high frequency range	96.2		500	kHz
			Invalid low frequency range			5	kHz
	Invalid ERR Pin Detection Time	$t_{TR,INIT}$	High frequency	5.2		11.1	µs
			Low frequency	50.1		99.9	µs
	ERR Time Out	t_{TO}	After SLEEP mode	9	10	11	ms
			After receiving re-enable command from SPI	50.1		110	µs
Safe State Pins, Pin SS1/SS2	SSx Pin Output High Level	$V_{SSx,High}$	V_{VUC}=5V, I_{SSx}<1mA	3.6	4.8	V_{VUC}	V
			V_{VUC}=5V, I_{SSx}<5mA	3	4.3	V_{VUC}	V
			V_{VUC}=3.3V, I_{SSx}<1mA	2.9	3.2	V_{VUC}	V
			V_{VUC}=3.3V, I_{SSx}<5mA	2	2.8	V_{VUC}	V
	SSx Pin Pull Down Resistor	$R_{SSx, pulldown}$		70	100	130	kΩ
	SSx Pin Output Low Level	$V_{SSx,Low}$				0.8	V
	SSx Internal Reaction Time	$t_{SSx, act}$			12	30	µs
	Programmable Recover Delay Time Range			0		10	ms
	Programmable Range of Delay Time Between SS1 and SS2			0		2500	ms
	The SSx Timer Accuracy			-10		10	%

Watchdog, Pin WDI	Watchdog Timer Accuracy			-6		+6	%
	Time Between Two Functional Watchdog Responses			20			us
	WDI Pin High Voltage Level	$V_{WDI,High}$	V_{VUC}=5V	3.6			V
			V_{VUC}=3.3V	2			V
	WDI Pin Low Voltage Level	$V_{WDI,Low}$				0.8	V
	WDI Pin Hysteresis	$V_{WDI, Hys}$	V_{VUC}=5V		350		mV
			V_{VUC}=3.3V		160		mV
	WDI Pin Pull Down Current	$I_{WDI, PULL}$			150	330	μA
PROG Pin	PROG Upper Threshold	$V_{PROG,hi}$	V_{PROG} increasing			2	V
	PROG Lower Threshold	$V_{PROG,lo}$	V_{PROG} decreasing	0.8			V
	PROG Signal Hysteresis	$V_{PROG,hyst}$			400		mV
SPI Interface, Pin SCS, SCL, SDO, SDI	SCS Pin High Voltage Level	$V_{SCS,High}$	V_{VUC}=5V	3.6			V
			V_{VUC}=3.3V	2			V
	SCS Pin Low Voltage Level	$V_{SCS,Low}$				0.8	V
	SCS Pin Hysteresis	$V_{SCS, Hys}$	V_{VUC}=5V		350		mV
			V_{VUC}=3.3V		160		mV
	SCS Pin Pull Up Current	$I_{SCS, PULL}$	V_{SCS}=0V	-220	-120		μA
	SCL Pin High Voltage Level	$V_{SCL,High}$	V_{VUC}=5V	3.6			V
			V_{VUC}=3.3V	2			V
	SCL Pin Low Voltage Level	$V_{SCL,Low}$				0.8	V
	SCL Pin Hysteresis	$V_{SCL, Hys}$	V_{VUC}=5V		350		mV
			V_{VUC}=3.3V		160		mV
	SCL Pin Pull Down Current	$I_{SCL, PULL}$	V_{SCL}= V_{VUC}		150	330	uA
	SDI Pin High Voltage Level	$V_{SDI,High}$	V_{VUC}=5V	3.6			V
			V_{VUC}=3.3V	2			V
	SDI Pin Low Voltage Level	$V_{SDI,Low}$				0.8	V
	SDI Pin Hysteresis	$V_{SDI, Hys}$	V_{VUC}=5V		350		mV
			V_{VUC}=3.3V		160		mV
	SDI Pin Pull Down Current	$I_{SDI, PULL}$	V_{SDI}= V_{VUC}		150	330	μA
	SDO Pin High Voltage Level	$V_{SDO,High}$	V_{VUC}=5V, I_{SDO}=-9mA	4			V
			V_{VUC}=3.3V, I_{SDO}=-7mA	2.3			V
	SDO Pin Low Voltage Level	$V_{SDO,Low}$	I_{SDO}=-7mA			0.7	V
	SDO Pin Voltage Rise Time	$t_{SDO, rise}$	C_{SDO}=50pF			25	ns
	SDO Pin Voltage Fall Time	$t_{SDO, fall}$	C_{SDO}=50pF			25	ns
	SDO Pin Leakage Current	$I_{SDO, Leakge}$	Tri-state	-10		10	μA
SPI Timing	CLK_SPI Operating Frequency	$f_{SPI, clk}$				10	MHz

	CLK_SPI Operating Frequency	$f_{SPI, clk}$	SLEEP state			1.5	MHz
	CLK Signal Duty Cycle	D_{SCL}		45	50	55	%
	CLK_SPI Operating Period	$t_{SPI, clk}$		100			ns
	CLK_SPI High Time	$t_{SPI, wsclkh}$		45			ns
	CLK_SPI Low Time	$t_{SPI, wsclkl}$		45			ns
	CLK_SPI Fall Time	$t_{SPI, clkf}$	tSPI_fact ≤ tSPI_clk ; 100 ns ≤ tSPI_fact ≤ 1 µs			0.1*tSPI_fact	ns
	CLK_SPI Rise Time	$t_{SPI, clkr}$	tSPI_fact ≤ tSPI_clk ; 100 ns ≤ tSPI_fact ≤ 1 µs			0.1*tSPI_fact	ns
	CLK_SPI Lead Time	$t_{SPI, lead}$		100			ns
	CLK_SPI Lag Time	$t_{SPI, lag}$		50			ns
	SPI Chip Select (SCS) Rise Time	$t_{SPI, scsr}$	tSPI_fact ≤ tSPI_lag ; 50 ns ≤ tSPI_fact ≤ 500 ns			0.2*tSPI_fact	ns
	SPI Chip Select (SCS) Fall Time	$t_{SPI, scsf}$	tSPI_fact ≤ tSPI_lead; 100 ns ≤ tSPI_fact ≤ 1 µs			0.2*tSPI_fact	ns
	SPI Data Input (SDI) Setup	$t_{SPI, su}$		10			ns
	SPI Data Input (SDI) Hold Time	$t_{SPI, hi}$		10			ns
	SPI Data Output (SDO) Valid After CLK_SPI	$t_{SPI, v}$	CSDO,load= 50 pF; tSPI_fact ≥ tSPI_clkf ; 10 ns ≤ tSPI_fact ≤ 100 ns			(0.1*tSPI_fact) +36	ns
	SPI Write Propagation Delay SDI to SDO	$t_{SPI, wpd}$				35	ns
	SPI Data Output (SDO) Access	$t_{SPI, a}$	CSDO,load = 50 pF			50	ns
	SPI Data Output (SDO) Disable Time	$t_{SPI, dis}$	CSDO,load = 50 pF			100	ns
	Sequential Transfer Delay	$t_{SPI, td}$		350			ns
	Sequential Transfer Delay	$t_{SPI, td}$	SLEEP state	2			us
	Frame Duration (SCS low)	$t_{SPI, fl}$				1.85	ms
Long Duration Timer (LDT)	LDT Internal Counter Timer	-	REG00[6] = 1		1		s
			REG00[6] = 0		1		ms
	LDT Internal Clock Accuracy	-	-20°C to +85°C	-5		5	%
	LDT Internal Counter	-			24		bit
External Regulator (VMON)	EXEN High Level	$V_{EXEN,High}$	In VUC 5.0V output mode, VQUC = 5.0 V, IEXEN = -9 mA	4			V
			In VUC 5.0V output mode, VQUC ≥ 4.7 V, IEXEN = -0.5 mA	4.6			V
			In VUC 3.3V output mode, VQUC = 3.3 V IEXEN = -7 mA	2.3			V
			In VUC 3.3V output mode, VQUC ≥ 3.1 V, IEXEN = -0.5 mA	3			V
	EXEN Low Level	$V_{EXEN,LOW}$	VQUC = 5.0 V IEXEN = 7 mA			0.7	V
			VQUC = 3.3 V IEXEN = 5.5 mA			0.7	V
	Enable Rise Time	$t_{EXEN,rise}$	CEXEN, load = 50 pF			25	ns

	Enable Fall Time	$t_{EXEN,fall}$	CEXEN, load = 50 pF			25	ns
	SYN Out High Level	$V_{SYN,High}$	In VUC 5.0V output mode, VQUC = 5.0 V, ISYN = -9 mA	4			V
			In VUC 5.0V output mode, VQUC ≥ 4.7 V, ISYN = -0.5 mA	4.6			V
			In VUC 3.3V output mode, VQUC = 3.3 V ISYN = -7 mA	2.3			V
			In VUC 3.3V output mode, VQUC ≥ 3.1 V, ISYN = -0.5 mA	3			V
	SYN Out Low Level	$V_{SYN,Low}$	In 5.0V output mode, VQUC = 5.0 V ISYN = 7 mA			0.7	V
			In 3.3V output mode, VQUC = 3.3 V ISYN = 5.5 mA			0.7	V
	Sync Out Signal Duty Cycle **(Note 5)**	D_{SYN}			50		%
	Sync Out Signal Rise Time	$t_{SYN,rise}$				25	ns
	Sync Out Signal Fall Time	$t_{SYN,rise}$				25	ns
	External Voltage Monitoring Input Pull-up Current		VMON = 0.8 V		100	130	nA

Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The exposed pad of the QFN7×7-48 packages is used for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

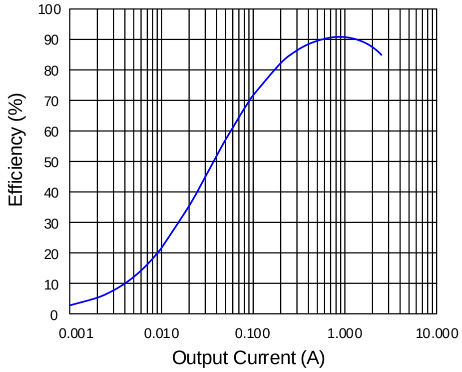
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = -40°C, 25°C and 125°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

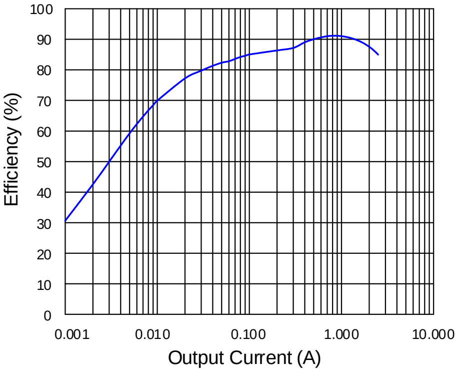
PreBuck Efficiency vs Output Current

(V_{IN}=12V, Prebuck=5.8V, L=4.7µH, Fre=2.2MHz, FCCM)



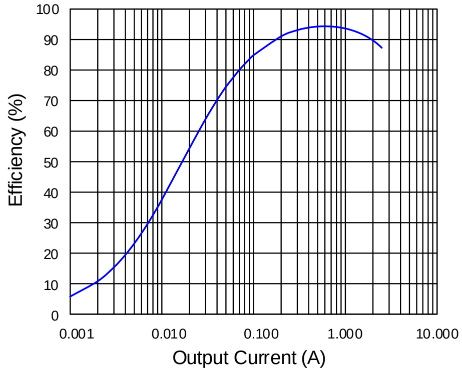
PreBuck Efficiency vs Output Current

(V_{IN}=12V, Prebuck=5.8V, L=4.7µH, Fre=2.2MHz, PFM)



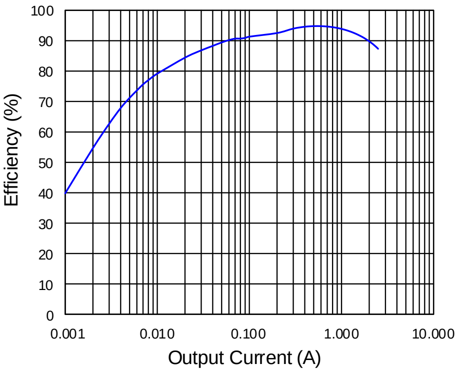
PreBuck Efficiency vs Output Current

(V_{IN}=12V, Prebuck=5.8V, L=22µH, Fre=400kHz, FCCM)



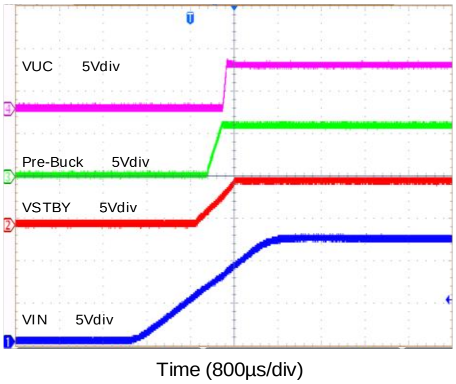
PreBuck Efficiency vs Output Current

(V_{IN}=12V, Prebuck=5.8V, L=22µH, Fre=400kHz, PFM)



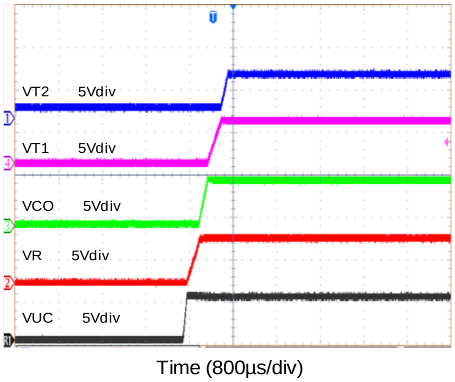
Power On Sequence

(V_{IN}=12V, $V_{prebuck}$=5.8V, V_{VSTBY}=5V, V_{VUC}=5V, V_{VR}=5V, V_{VCO}=5V, V_{VT1}=V_{VT2}=5V, EXSEL connect to GND)



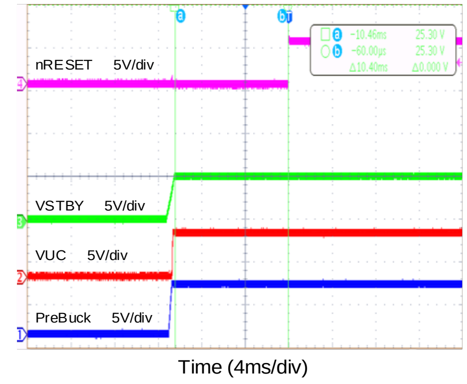
Power On Sequence

(V_{IN}=12V, $V_{prebuck}$=5.8V, V_{VSTBY}=5V, V_{VUC}=5V, V_{VR}=5V, V_{VCO}=5V, V_{VT1}=V_{VT2}=5V, EXSEL connect to GND)

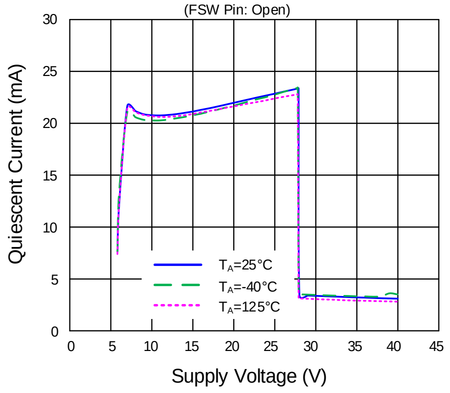


Power On Sequence

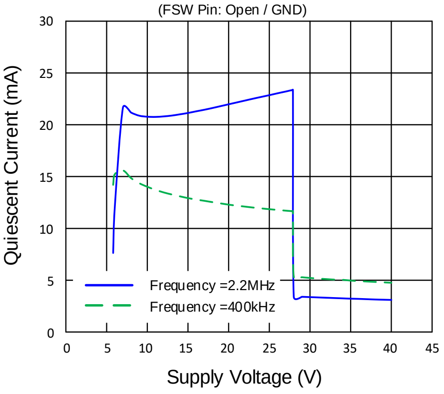
(V_{IN}=12V, $V_{prebuck}$=5.8V, V_{VST}=5V, V_{VUC}=5V, V_{VR}=5V, V_{VCO}=5V,
V_{VT1}=V_{VT2}=5V, EXSEL connect to GND)



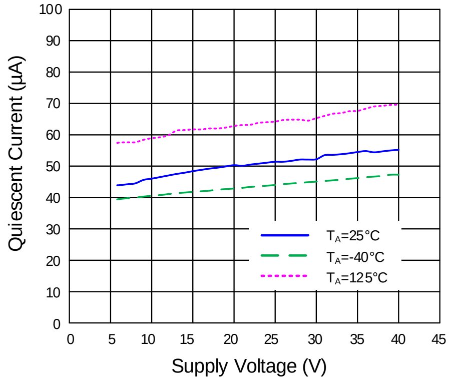
INIT, NORMAL and WAKE
Current Consumption vs Supply Voltage
(FSW Pin: Open)



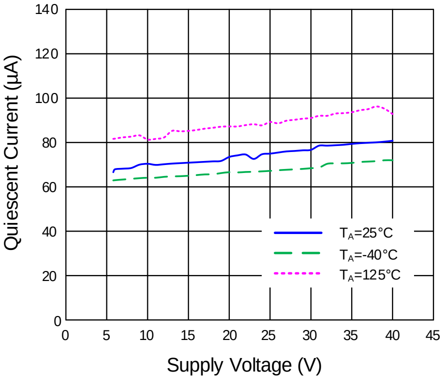
INIT, NORMAL and WAKE
Current Consumption vs Supply Voltage
(FSW Pin: Open / GND)



STANDBY Current Consumption vs Supply Voltage
(VSTBY Disabled)

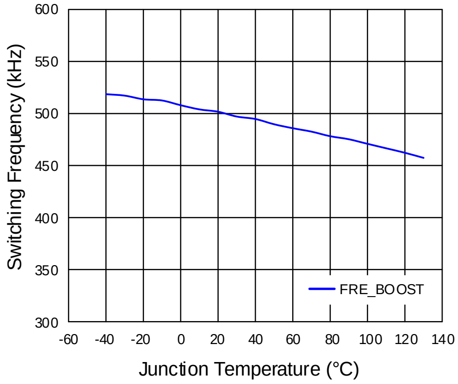


STANDBY Current Consumption vs Supply Voltage
(VSTBY Enabled)



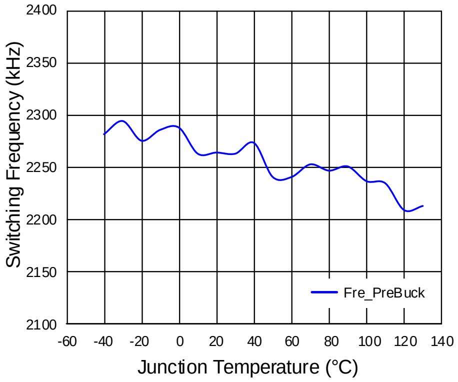
Boost Switching Frequency vs Junction Temperature

(V_{BAT}=6V, V_{IN}=7.5V)



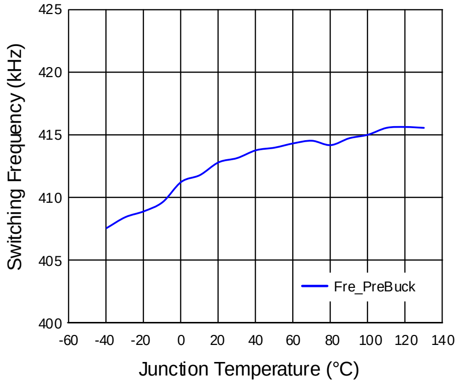
VOPRE Buck Switching Frequency vs Junction Temperature

(FSW Pin: Open)



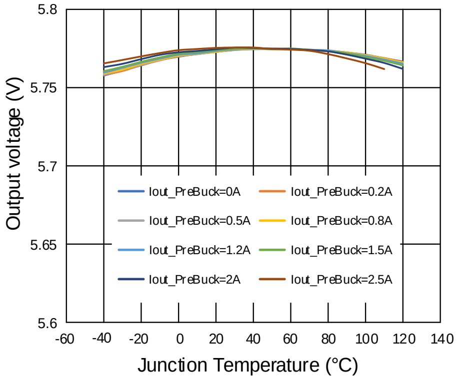
VOPRE Buck Switching Frequency vs Junction Temperature

(FSW Pin: GND)



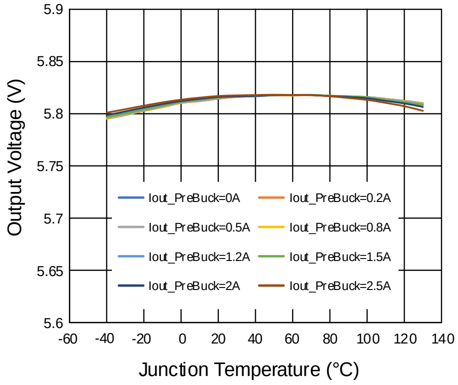
VOPRE Buck Output Voltage vs Junction Temperature

(V_{IN}=12V, FSW Pin Open, Fre=2.2MHz)



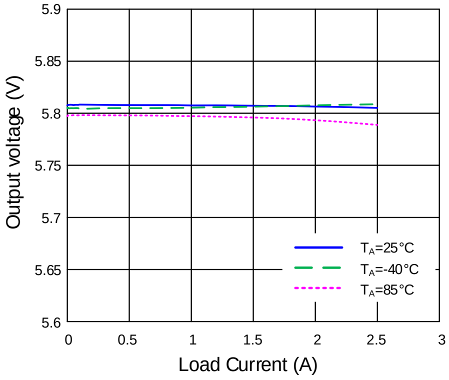
VOPRE Buck Output Voltage vs Junction Temperature

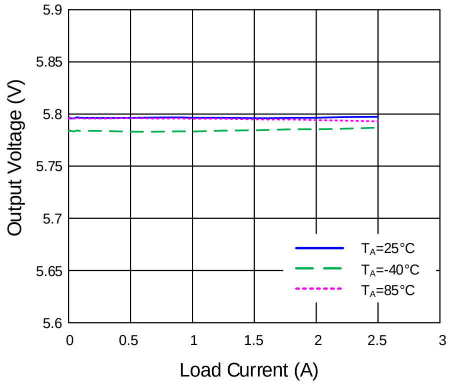
(V_{IN}=12V, FSW Pin GND, Fre=400kHz）



VOPRE Buck Output Voltage vs Load Current

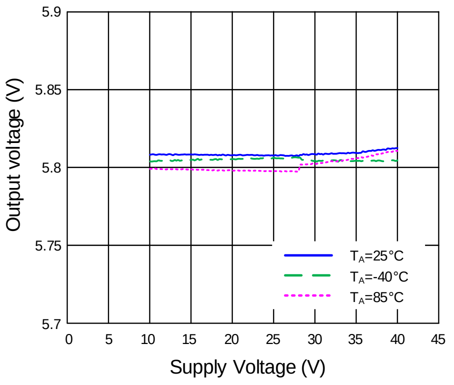
(V_{IN}=12V, FSW Pin Open, Fre=2.2MHz)





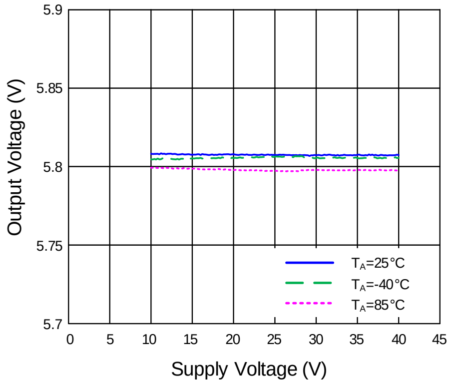
VOPRE Buck Output Voltage vs Load Current

(V_{IN}=12V, FSW Pin GND, Fre=400kHz)



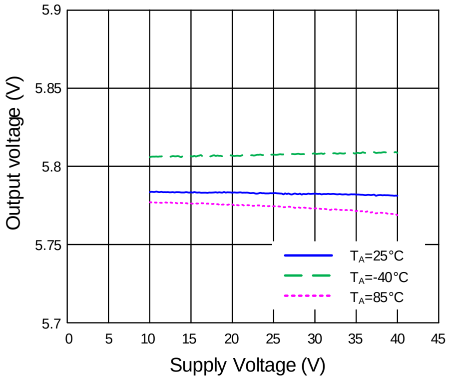
VOPRE Buck Output Voltage vs Supply Voltage

(FSW Pin Open, Fre=2.2MHz, Iout_Prebuck=0.01A)



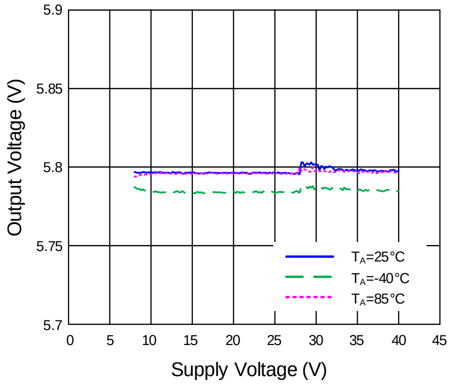
VOPRE Buck Output Voltage vs Supply Voltage

(FSW Pin Open, Fre=2.2MHz, Iout_Prebuck=0.25A)



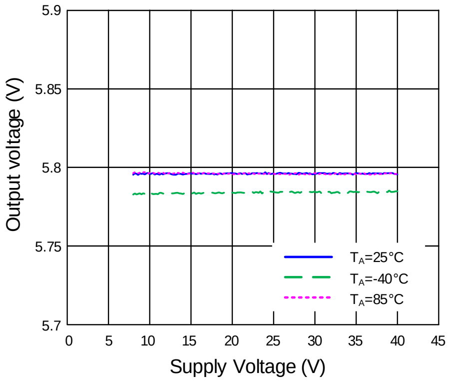
VOPRE Buck Output Voltage vs Supply Voltage

(FSW Pin Open, Fre=2.2MHz, Iout_Prebuck=1.25A)



VOPRE Buck Output Voltage vs Supply Voltage

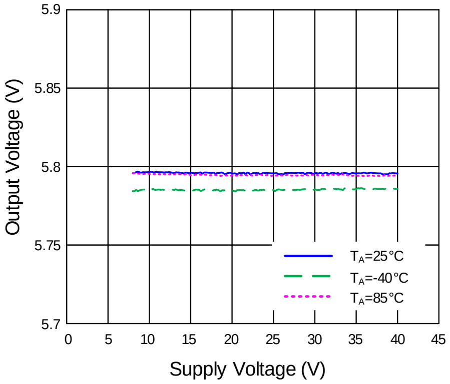
(FSW Pin GND, Fre=400kHz, Iout_Prebuck=0.01A)



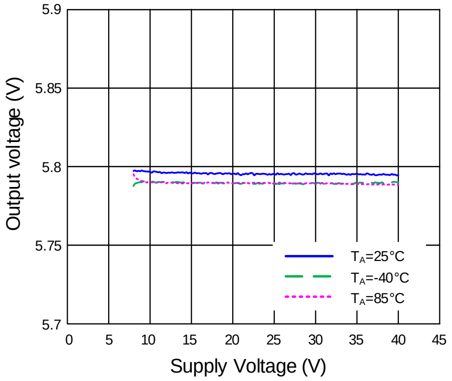
VOPRE Buck Output Voltage vs Supply Voltage

(FSW Pin GND, Fre=400kHz, Iout_Prebuck=0.25A)

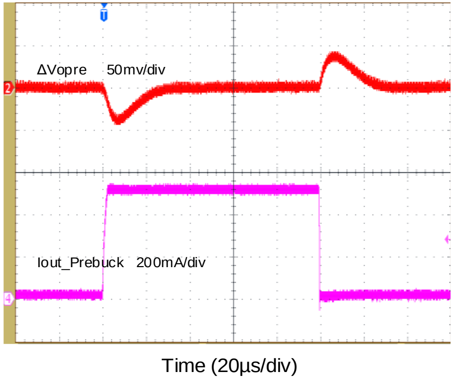
VOPRE Buck Output Voltage vs Supply Voltage
(FSW Pin GND, Fre=400kHz, Iout_Prebuck=1.25A)



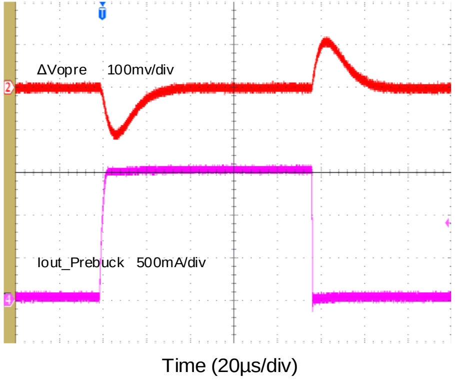
VOPRE Buck Output Voltage vs Supply Voltage
(FSW Pin GND, Fre=400kHz, Iout_Prebuck=2.5A)



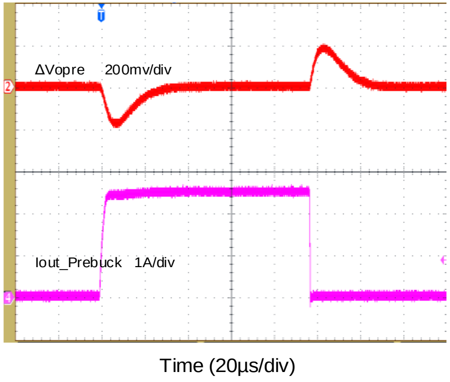
VOPRE Buck Dynamic Load Response
(2mA to 500mA)
(FSW-Pin: Open; Vopre=5.8V; Cvopre=50µF)



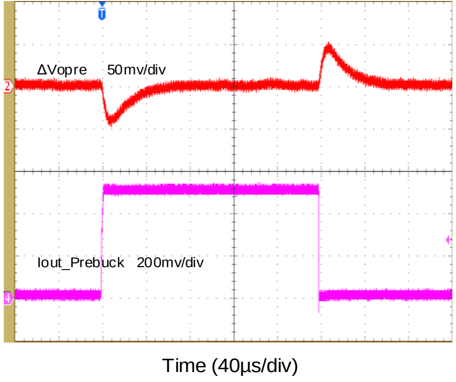
VOPRE Buck Dynamic Load Response
(2mA to 1500mA)
(FSW-Pin: Open; Vopre=5.8V; Cvopre=50µF)



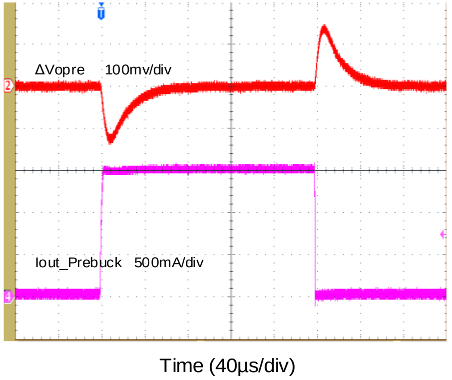
VOPRE Buck Dynamic Load Response
(2mA to 2500mA)
(FSW-Pin: Open; Vopre=5.8V; Cvopre=50µF)



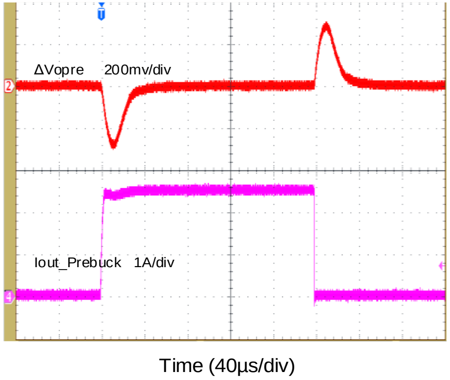
VOPRE Buck Dynamic Load Response
(2mA to 500mA)
(FSW-Pin: GND; Vopre=5.8V; Cvopre=100µF)



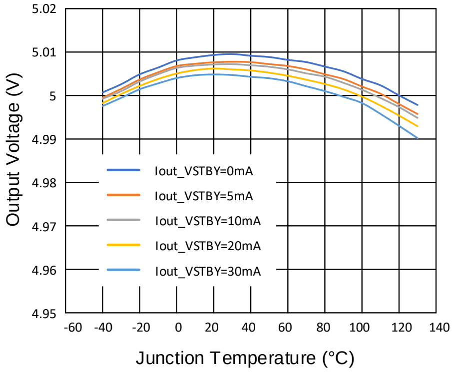
VOPRE Buck Dynamic Load Response
(2mA to 1500mA)
(FSW-Pin: GND; Vopre=5.8V; Cvopre=100µF)



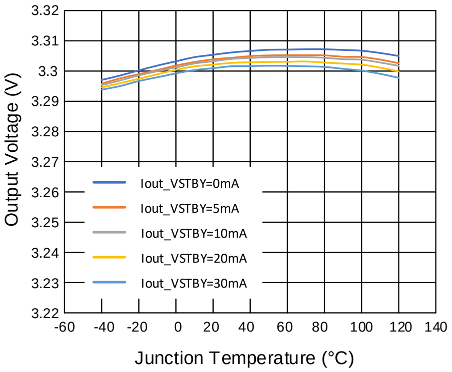
VOPRE Buck Dynamic Load Response
(2mA to 2500mA)
(FSW-Pin: GND; Vopre=5.8V; Cvopre=100µF)



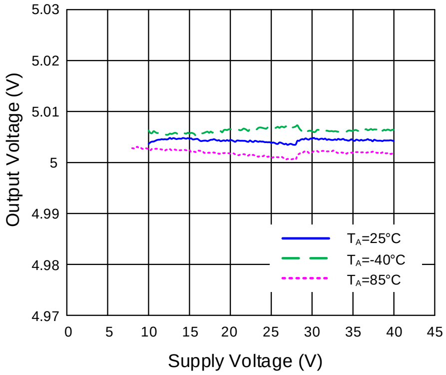
VSTBY Output Voltage vs Junction Temperature
(V_{IN}=12V，VSTBY=5V)



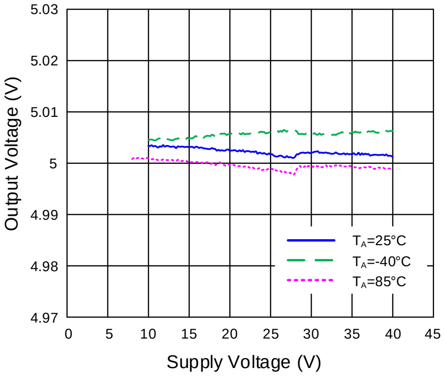
VSTBY Output Voltage vs Junction Temperature
(V_{IN}=12V，VSTBY=3.3V)



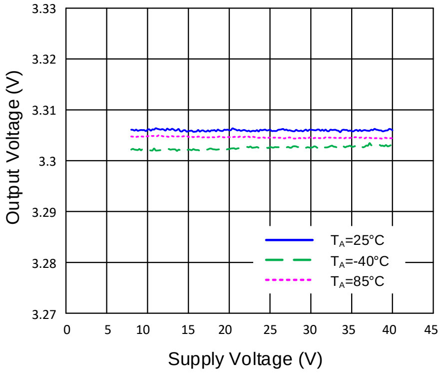
VSTBY Output Voltage vs Supply Voltage
(VSTBY=5V，Iout_VSTBY=0.01A)



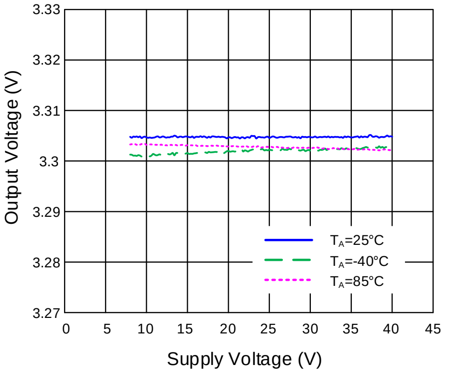
VSTBY Output Voltage vs Supply Voltage
(VSTBY=5V，Iout_VSTBY=0.02A)



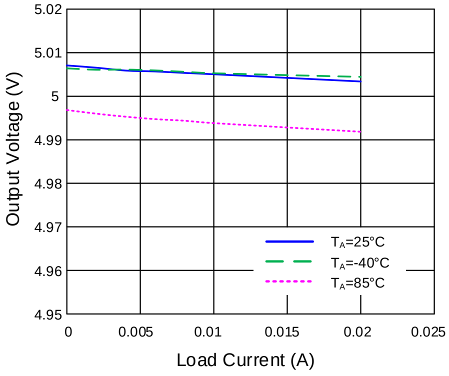
VSTBY Output Voltage vs Supply Voltage
(VSTBY=3.3V，Iout_VSTBY=0.01A)



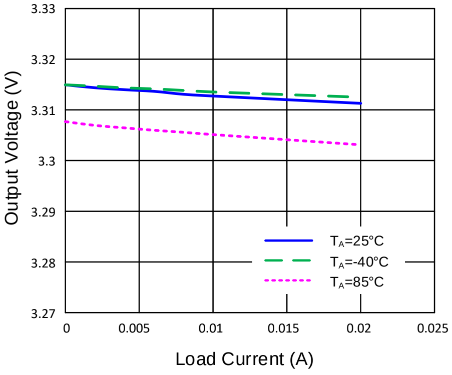
VSTBY Output Voltage vs Supply Voltage
(VSTBY=3.3V，Iout_VSTBY=0.02A)



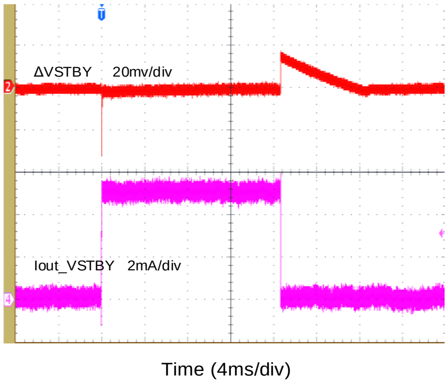
VSTBY Output Voltage vs Load Current
(VIN=12V，VSTBY=5V)



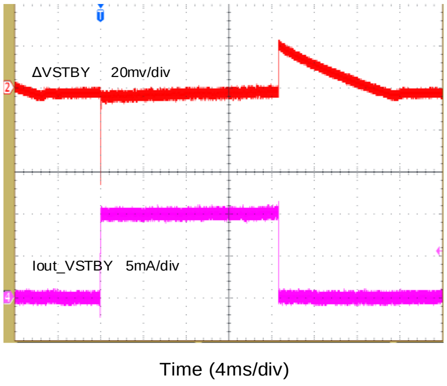
VSTBY Output Voltage vs Load Current
(VIN=12V，VSTBY=3.3V)



VSTBY Dynamic Load Response(0mA to 5mA)
(FSW-Pin: Open; VSTBY=5V; Cvstby=4.7µF)

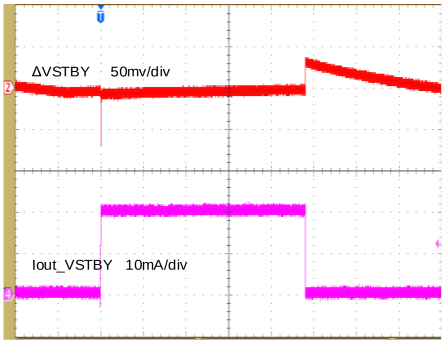


VSTBY Dynamic Load Response(0mA to 10mA)
(FSW-Pin: Open; VSTBY=5V; Cvstby=4.7µF)



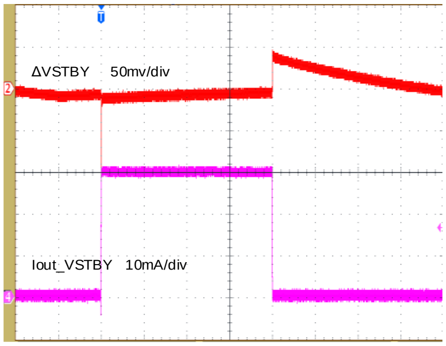
VSTBY Dynamic Load Response(0mA to 20mA)

(FSW-Pin: Open; VSTBY=5V; Cvstby=4.7µF)



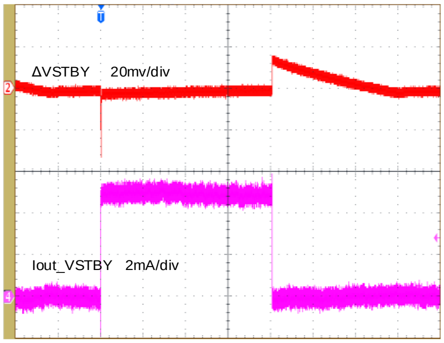
VSTBY Dynamic Load Response(0mA to 30mA)

(FSW-Pin: Open; VSTBY=5V; Cvstby=4.7µF)



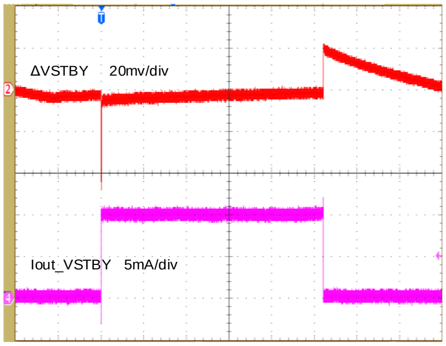
VSTBY Dynamic Load Response(0mA to 5mA)

(FSW-Pin: Open; VSTBY=3.3V; Cvstby=4.7µF)



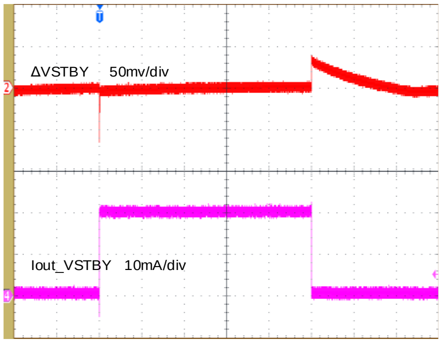
VSTBY Dynamic Load Response(0mA to 10mA)

(FSW-Pin: Open; VSTBY=3.3V; Cvstby=4.7µF)



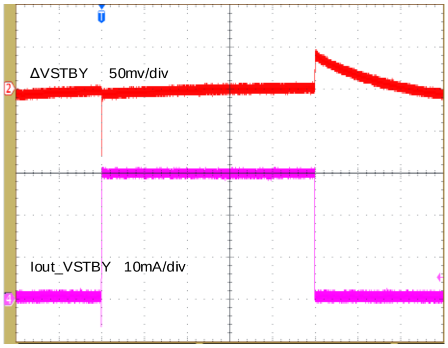
VSTBY Dynamic Load Response(0mA to 20mA)

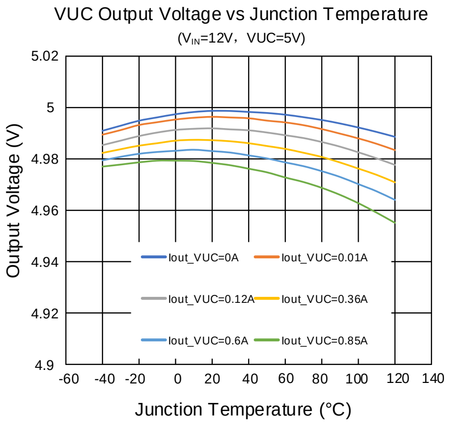
(FSW-Pin: Open; VSTBY=3.3V; Cvstby=4.7µF)

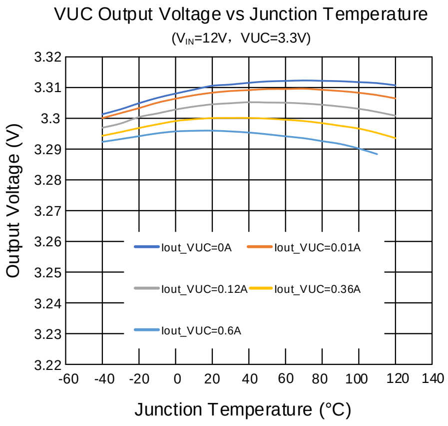


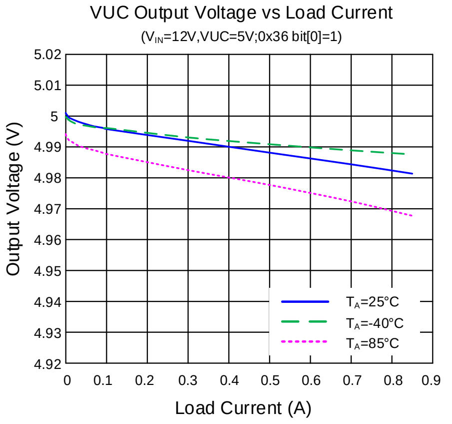
VSTBY Dynamic Load Response(0mA to 30mA)

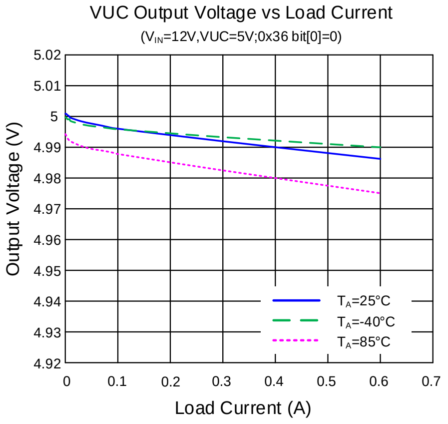
(FSW-Pin: Open; VSTBY=3.3V; Cvstby=4.7µF)

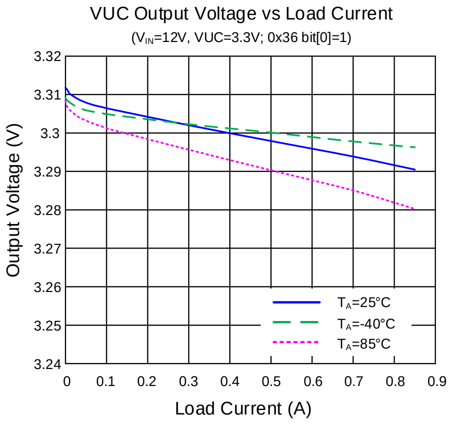


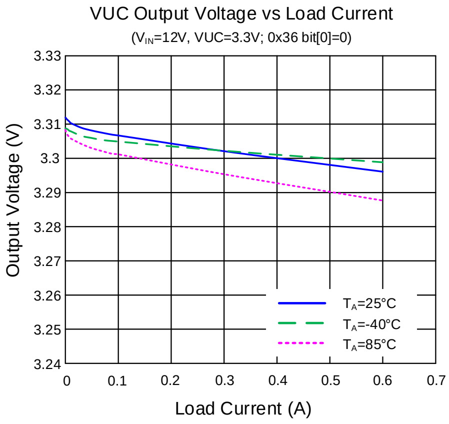

VUC Output Voltage vs Junction Temperature
(V_{IN}=12V，VUC=5V)
Output Voltage (V)
5.02
5
4.98
4.96
4.94
4.92
4.9
-60
-40
-20
0
20
40
60
80
100
120
140
Junction Temperature (°C)
Iout_VUC=0A
Iout_VUC=0.01A
Iout_VUC=0.12A
Iout_VUC=0.36A
Iout_VUC=0.6A
Iout_VUC=0.85A


VUC Output Voltage vs Junction Temperature
(V_{IN}=12V，VUC=3.3V)
Output Voltage (V)
3.32
3.31
3.3
3.29
3.28
3.27
3.26
3.25
3.24
3.23
3.22
-60
-40
-20
0
20
40
60
80
100
120
140
Junction Temperature (°C)
Iout_VUC=0A
Iout_VUC=0.01A
Iout_VUC=0.12A
Iout_VUC=0.36A
Iout_VUC=0.6A

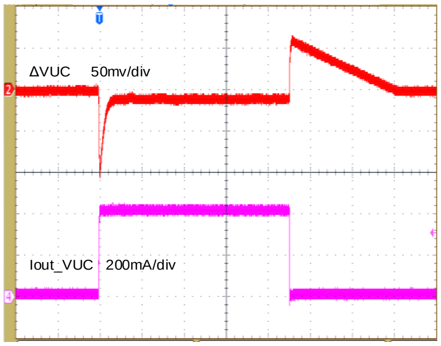

VUC Output Voltage vs Load Current
(V_{IN}=12V,VUC=5V;0x36 bit[0]=1)
Output Voltage (V)
5.02
5.01
5
4.99
4.98
4.97
4.96
4.95
4.94
4.93
4.92
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
Load Current (A)
T_A=25°C
T_A=-40°C
T_A=85°C


VUC Output Voltage vs Load Current
(V_{IN}=12V,VUC=5V;0x36 bit[0]=0)
Output Voltage (V)
5.02
5.01
5
4.99
4.98
4.97
4.96
4.95
4.94
4.93
4.92
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
Load Current (A)
T_A=25°C
T_A=-40°C
T_A=85°C


VUC Output Voltage vs Load Current
(V_{IN}=12V, VUC=3.3V; 0x36 bit[0]=1)
Output Voltage (V)
3.32
3.31
3.3
3.29
3.28
3.27
3.26
3.25
3.24
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
Load Current (A)
T_A=25°C
T_A=-40°C
T_A=85°C

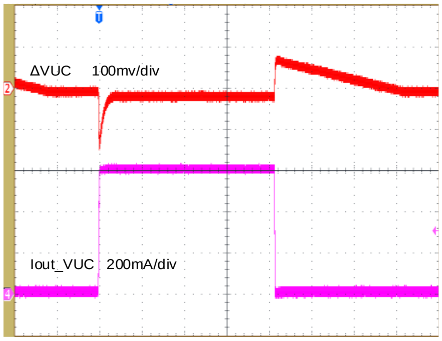

VUC Output Voltage vs Load Current
(V_{IN}=12V, VUC=3.3V; 0x36 bit[0]=0)
Output Voltage (V)
3.33
3.32
3.31
3.3
3.29
3.28
3.27
3.26
3.25
3.24
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
Load Current (A)
T_A=25°C
T_A=-40°C
T_A=85°C

VUC Dynamic Load Response(1mA to 400mA)
(FSW-Pin: Open; VUC=5V; Cvuc=11µF; 0x36 bit[0]=1)



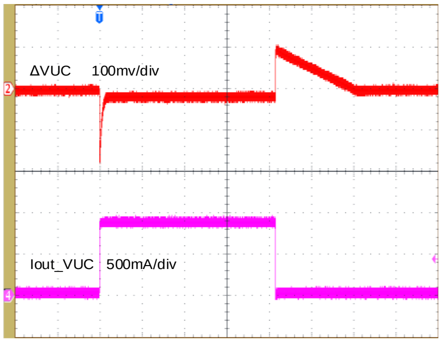
Time (100µs/div)

VUC Dynamic Load Response(1mA to 600mA)
(FSW-Pin: Open; VUC=5V; Cvuc=11µF; 0x36 bit[0]=1)



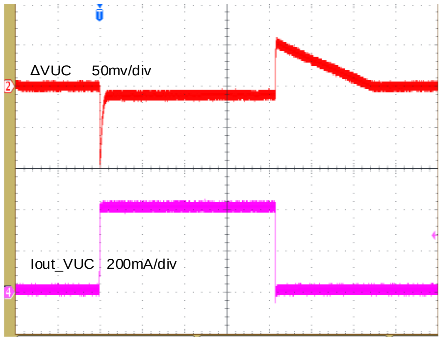
Time (100µs/div)

VUC Dynamic Load Response(1mA to 850mA)
(FSW-Pin: Open; VUC=5V; Cvuc=11µF; 0x36 bit[0]=1)



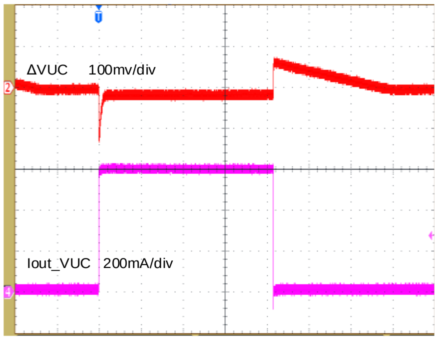
Time (200µs/div)

VUC Dynamic Load Response(1mA to 400mA)
(FSW-Pin: Open; VUC=3.3V; Cvuc=11µF; 0x36 bit[0]=1)



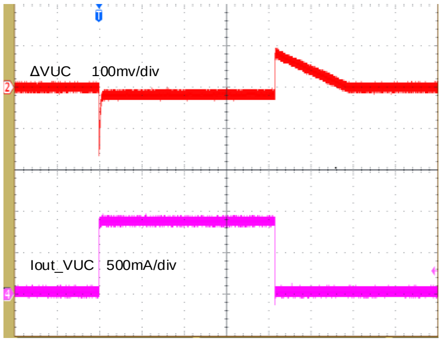
Time (200µs/div)

VUC Dynamic Load Response(1mA to 600mA)
(FSW-Pin: Open; VUC=3.3V; Cvuc=11µF; 0x36 bit[0]=1)



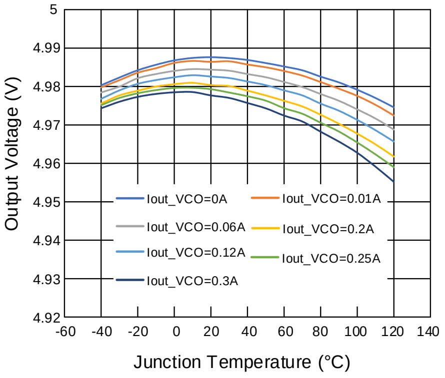
Time (200µs/div)

VUC Dynamic Load Response(1mA to 850mA)
(FSW-Pin: Open; VUC=3.3V; Cvuc=11µF; 0x36 bit[0]=1)

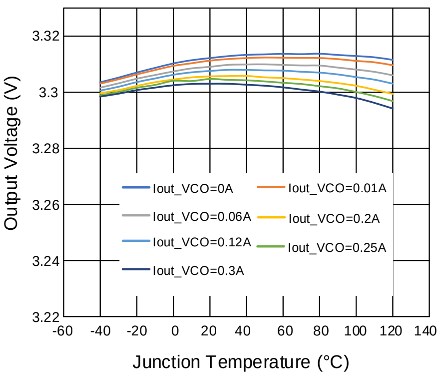


Time (400µs/div)

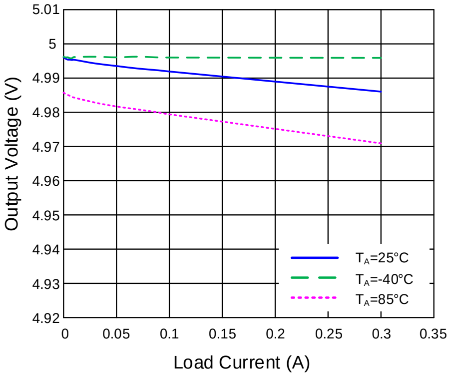
VCO Output Voltage vs Junction Temperature
(V_{IN}=12V，VCO=5V)



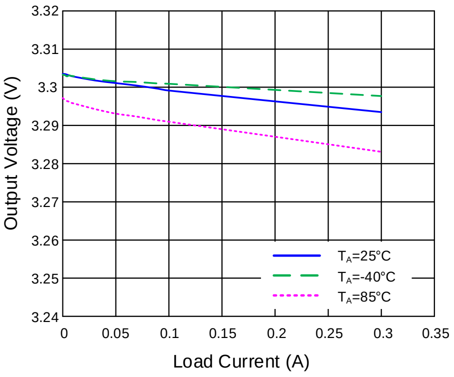
VCO Output Voltage vs Junction Temperature
(V_{IN}=12V，VCO=3.3V)



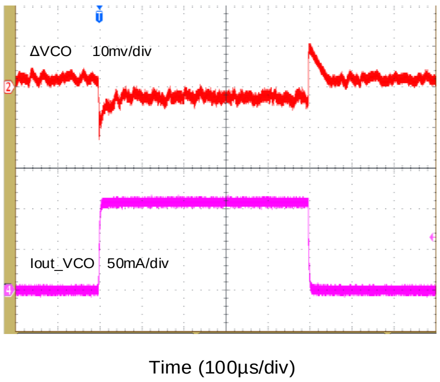
VCO Output Voltage vs Load Current
(V_{IN}=12V,VCO=5V)



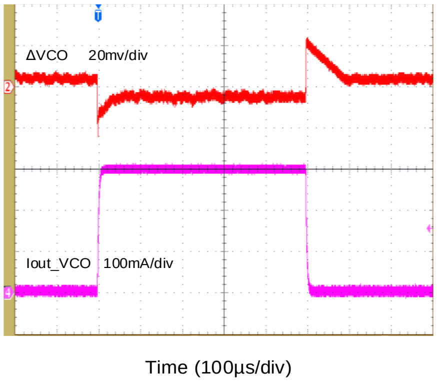
VCO Output Voltage vs Load Current
(V_{IN}=12V,VCO=3.3V)



VCO Dynamic Load Response(1mA to 100mA)
(FSW-Pin: Open; VCO=5V; C_{VCO}=11µF)

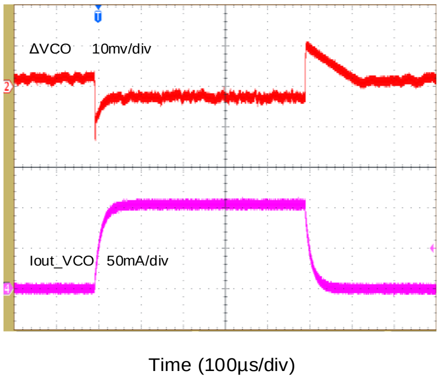


VCO Dynamic Load Response(1mA to 300mA)
(FSW-Pin: Open; VCO=5V; C_{VCO}=11µF)



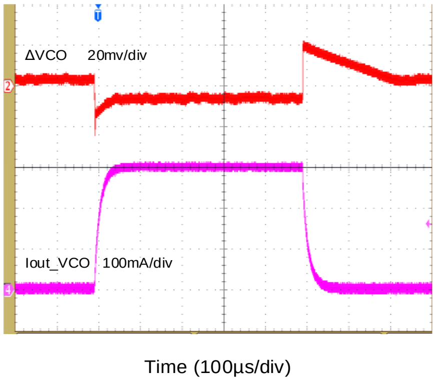
VCO Dynamic Load Response(1mA to 100mA)

(FSW-Pin: Open; VCO=3.3V; C_{VCO}=11µF)



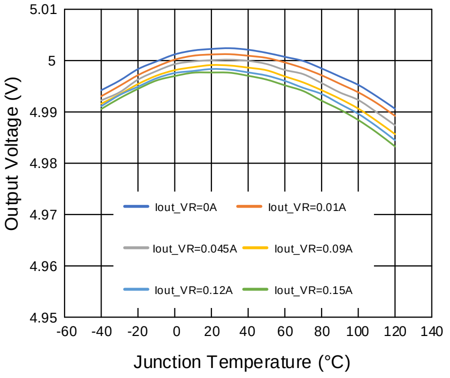
VCO Dynamic Load Response(1mA to 300mA)

(FSW-Pin: Open; VCO=3.3V; C_{VCO}=11µF)



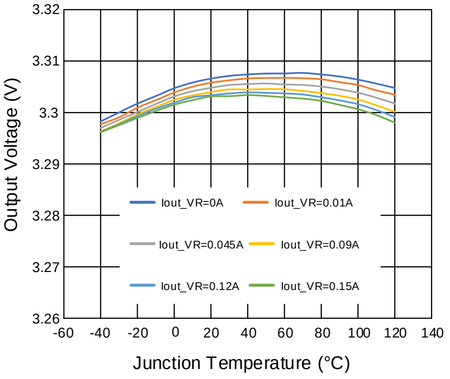
VR Output Voltage vs Junction Temperature

(V_{IN}=12V, VR=5V)



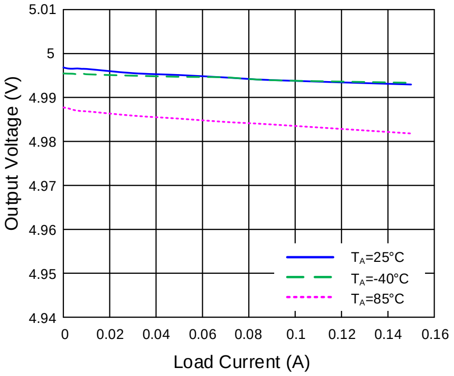
VR Output Voltage vs Junction Temperature

(V_{IN}=12V, VR=3.3V)



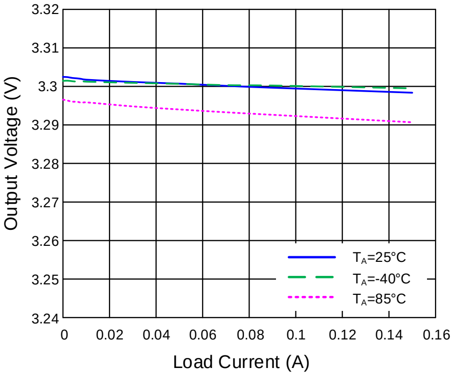
VR Output Voltage vs Load Current

(V_{IN}=12V,VR=5V)



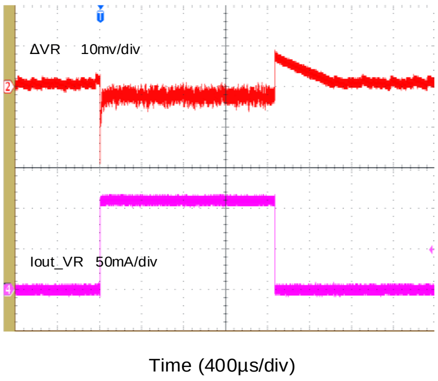
VR Output Voltage vs Load Current

(V_{IN}=12V,VR=3.3V)



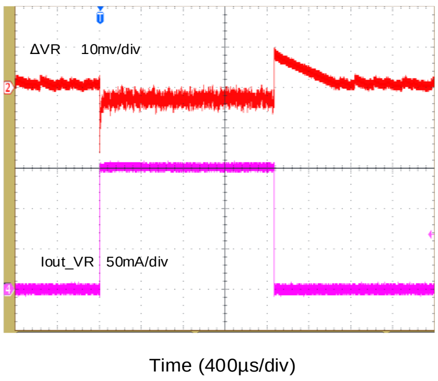
VR Dynamic Load Response(1mA to 100mA)

(VR=5V; Cvr=4.7µF)



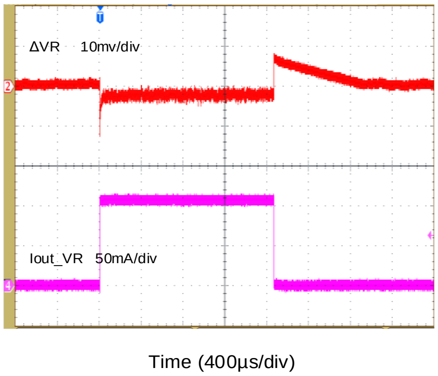
VR Dynamic Load Response(1mA to 150mA)

(VR=5V; Cvr=4.7µF)



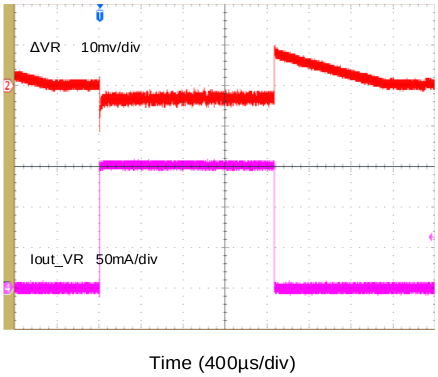
VR Dynamic Load Response(1mA to 100mA)

(VR=3.3V; Cvr=4.7µF)



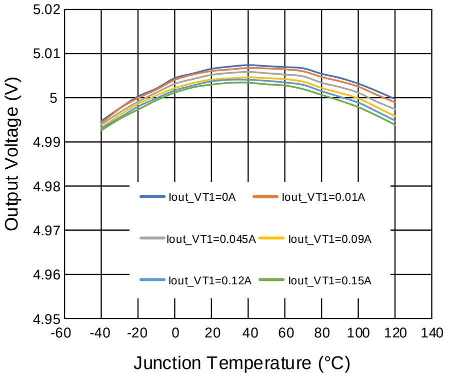
VR Dynamic Load Response(1mA to 150mA)

(VR=3.3V; Cvr=4.7µF)



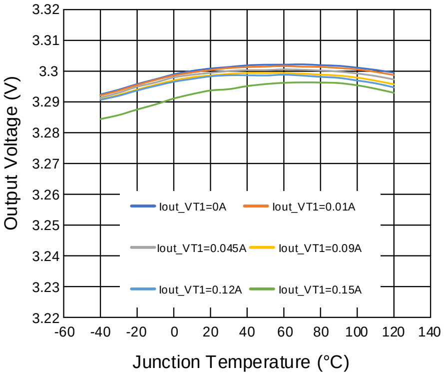
VT1 Output Voltage vs Junction Temperature

(V_{IN}=12V，VT1=5V)



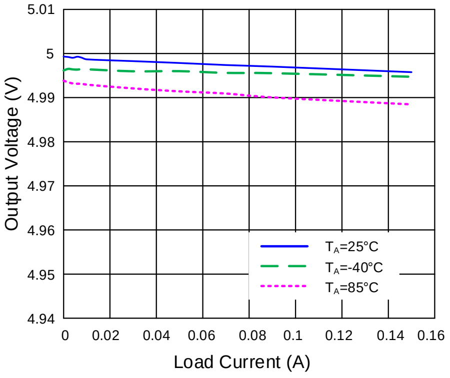
VT1 Output Voltage vs Junction Temperature

(V_{IN}=12V，VT1=3.3V)



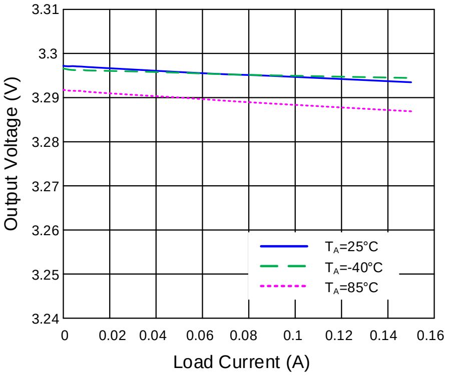
VT1 Output Voltage vs Load Current

(V_{IN}=12V,VT1=5V)



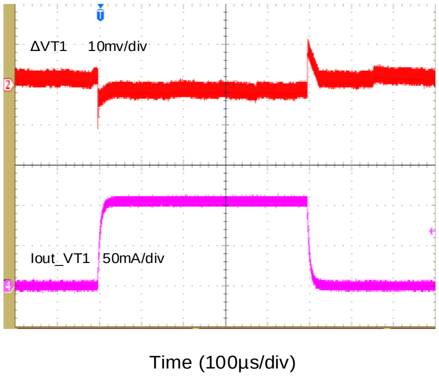
VT1 Output Voltage vs Load Current

(V_{IN}=12V,VT1=3.3V)



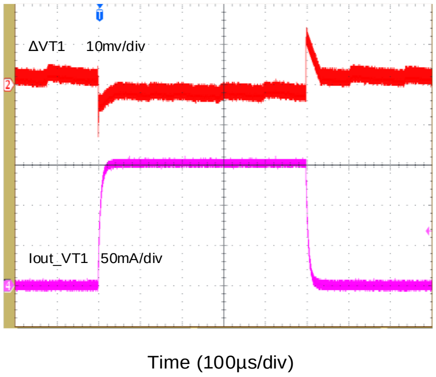
VT1 Dynamic Load Response(1mA to 100mA)

(VT1=5V; Cvt1=4.7µF)



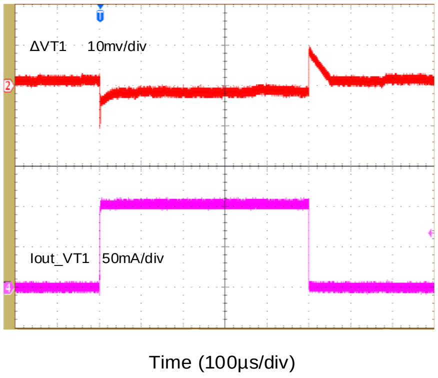
VT1 Dynamic Load Response(1mA to 150mA)

(VT1=5V; Cvt1=4.7µF)



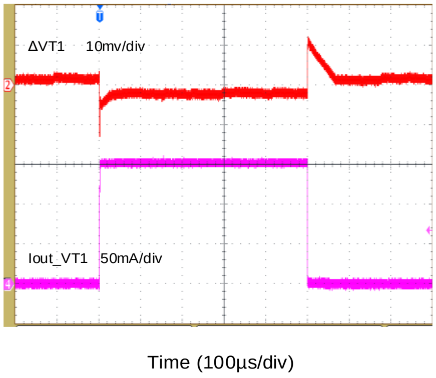
VT1 Dynamic Load Response(1mA to 100mA)

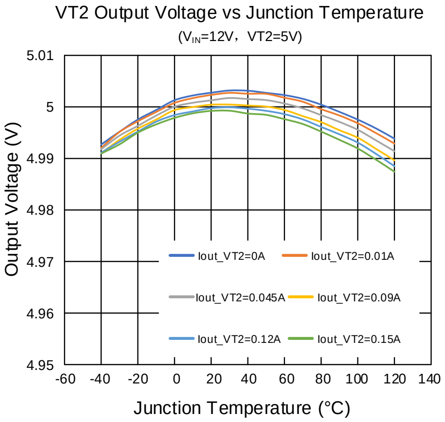
(VT1=3.3V; Cvt1=4.7µF)



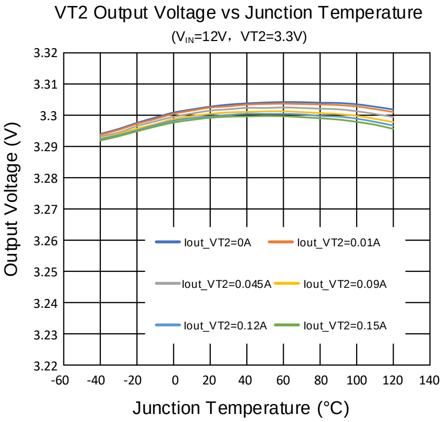
VT1 Dynamic Load Response(1mA to 150mA)

(VT1=3.3V; Cvt1=4.7µF)

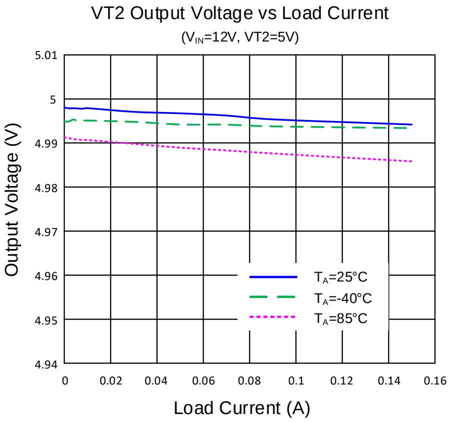



VT2 Output Voltage vs Junction Temperature

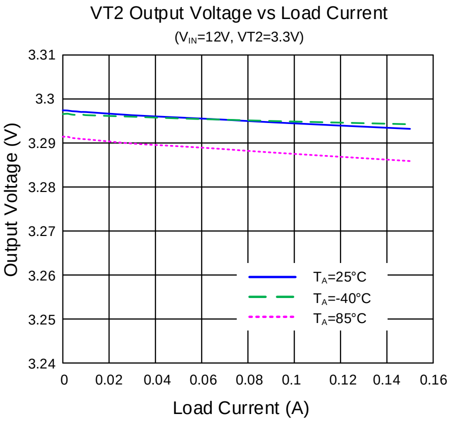
(V_{IN}=12V，VT2=5V)


VT2 Output Voltage vs Junction Temperature

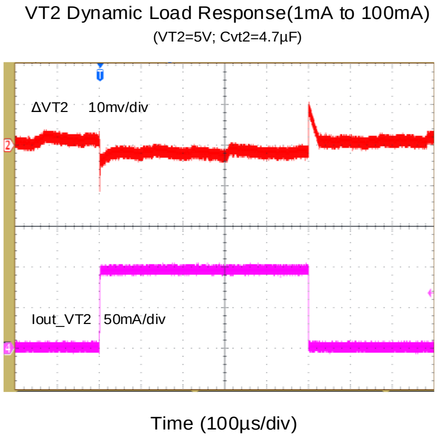
(V_{IN}=12V，VT2=3.3V)


VT2 Output Voltage vs Load Current

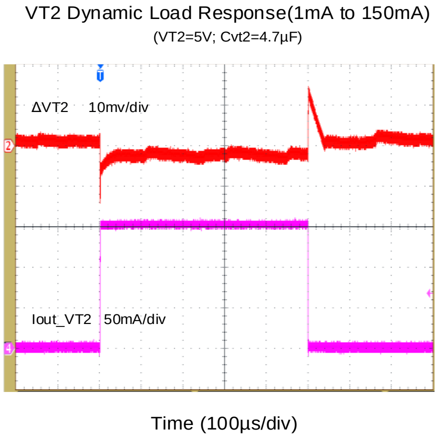
(V_{IN}=12V, VT2=5V)


VT2 Output Voltage vs Load Current

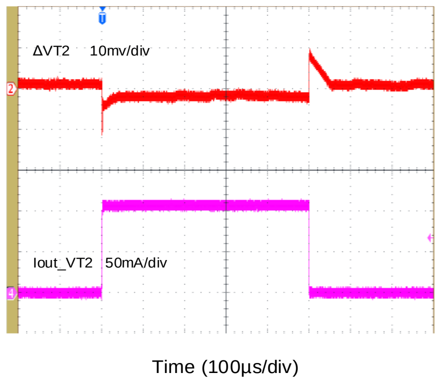
(V_{IN}=12V, VT2=3.3V)

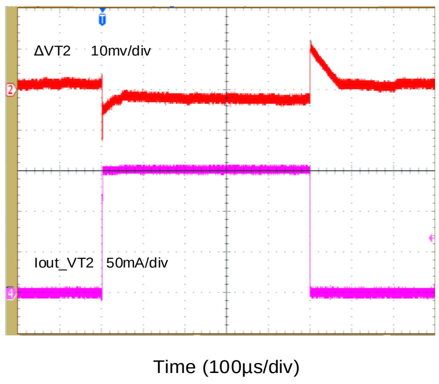

VT2 Dynamic Load Response(1mA to 100mA)

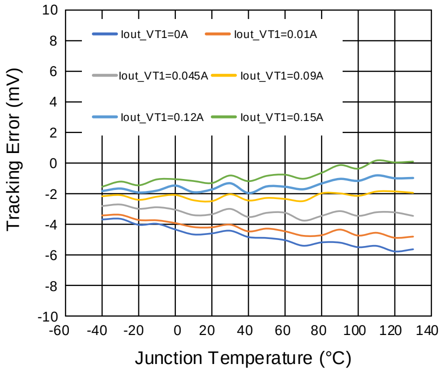
(VT2=5V; Cvt2=4.7μF)

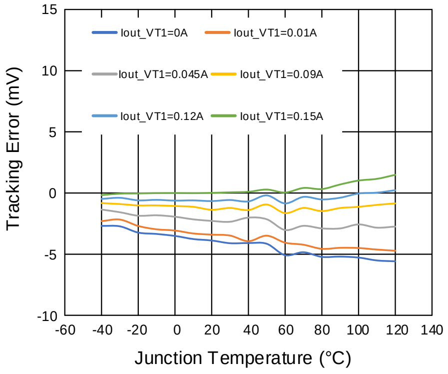

VT2 Dynamic Load Response(1mA to 150mA)

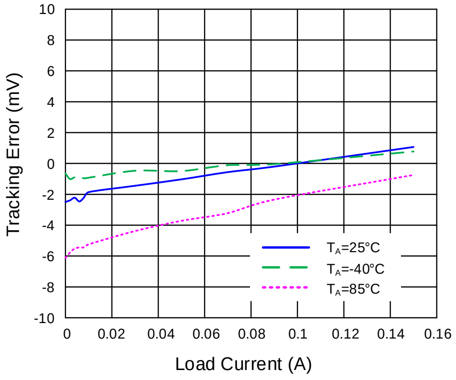
(VT2=5V; Cvt2=4.7μF)

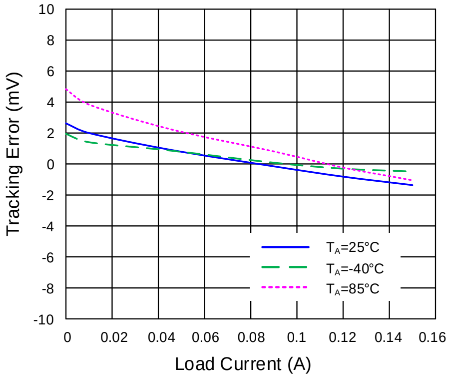

VT2 Dynamic Load Response(1mA to 100mA)
(VT2=3.3V; Cvt2=4.7µF)

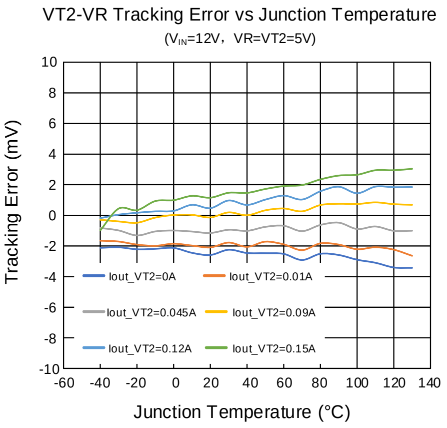

VT2 Dynamic Load Response(1mA to 150mA)
(VT2=3.3V; Cvt2=4.7µF)


VT1-VR Tracking Error vs Junction Temperature
(V_{IN}=12V，VR=VT1=5V)


VT1-VR Tracking Error vs Junction Temperature
(V_{IN}=12V，VR=VT1=3.3V)

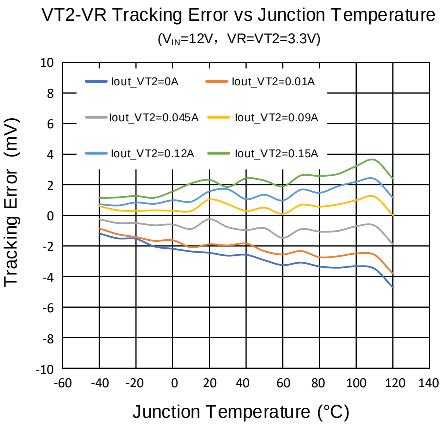

VT1-VR Tracking Error vs Load Current
(V_{IN}=12V,VR=VT1=5V)


VT1-VR Tracking Error vs Load Current
(V_{IN}=12V,VR=VT1=3.3V)



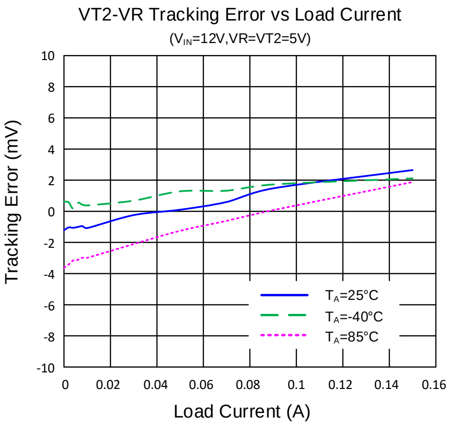
VT2-VR Tracking Error vs Junction Temperature

(V_{IN}=12V，VR=VT2=5V)



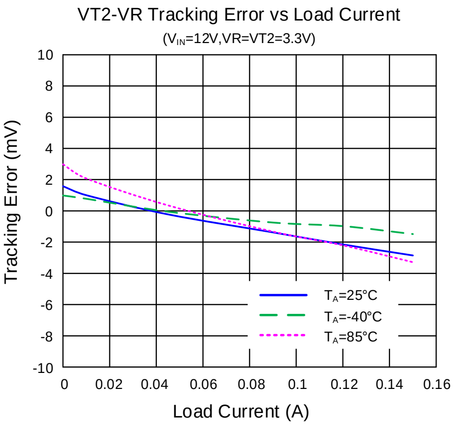
VT2-VR Tracking Error vs Junction Temperature

(V_{IN}=12V，VR=VT2=3.3V)



VT2-VR Tracking Error vs Load Current

(V_{IN}=12V,VR=VT2=5V)



VT2-VR Tracking Error vs Load Current

(V_{IN}=12V,VR=VT2=3.3V)

Function Description

1 Wake Function

The SA47301x has different states of operation. The following figure simply shows the state flow diagram. For detailed information please refer to the State Machine section in this document.

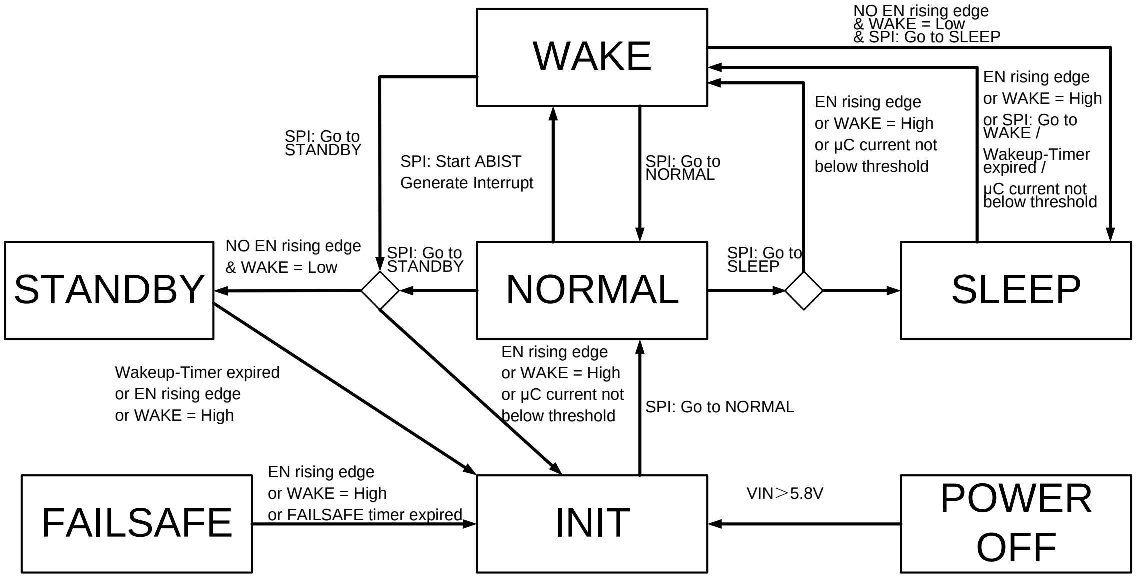


Figure 2. Flow Diagram State

The SA47301x powers on when VIN is connected to a voltage supply, and switches into INIT state from Power Off State automatically, where the device will be configured. After successful configuration, the device transitions to NORMAL state using an SPI command. From NORMAL or WAKE states, the device can be sent to SLEEP or STANDBY states to achieve lower power consumption using SPI commands. The wake-up signals are external triggers used to exit the low power or the FAILSAFE states.

A valid Wakeup signal can be generated using the WAKE or EN input pins. A voltage of the WAKE pin is higher than $V_{WAKE,hi}$ applied for at least $t_{WAKE,min}$ represents a valid wake-up signal. A rising edge at pin EN within a rise time $t_{EN,rise}$ represents a valid wake-up signal.

1) Enable (pin EN - edge triggered)

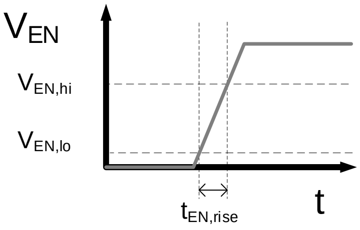


Figure 3. Valid Enable Signal

2) Wake (WAKE pin - level triggered)

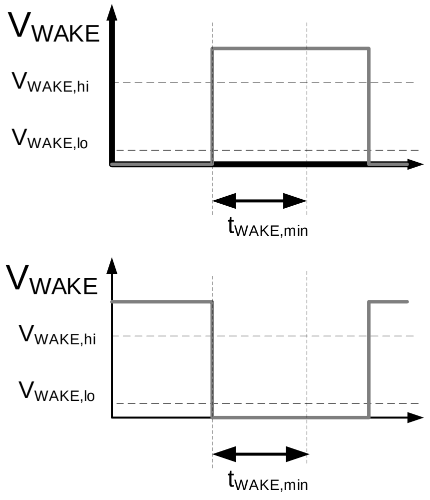


Figure 4. Valid Wake Signal

The device will transition from STANDBY to INIT, from SLEEP to WAKE, or from FAILSAFE to INIT when a valid wake-up signal is detected.

The device will initiate a transition to the WAKE state and generate an interrupt when a valid wake-up signal is detected during the transition phase from NORMAL or WAKE to SLEEP state.

The device will initiate a transition to INIT state and generate a Reset (nRESET pin pulled low) when a valid wake-up signal is detected during the transition phase from NORMAL or WAKE to STANDBY.

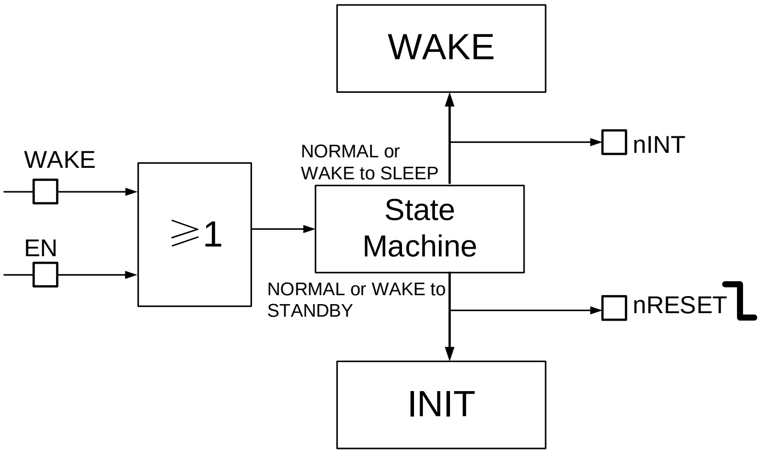


Figure 5. States Transitions

2 Pre-Regulators

2.1 Introduction

The pre-regulator starts operating after the VIN voltage rises above $V_{VIN\_POR\_Rising}$ level. It is designed to supply a stable voltage to the post regulators. It consists of two independent regulators: a boost controller and a fully integrated buck converter. The boost is used to maintain a minimum input voltage for the buck converter which is connected at its output.

A simplified diagram is shown below:

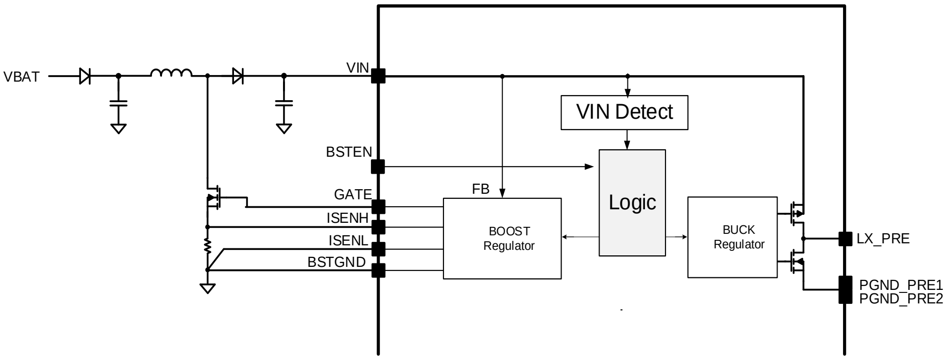


Figure 6. Pre-regulator Stage Block Diagram

If the boost converter is needed, the BSTEN pin should be left open. Connecting the BSTEN pin to ground will disable the boost converter. The boost converter only operates during low input voltage conditions when VIN voltage drops below the threshold $V_{PRE\_REG,boost,UV}$, to maintain a high enough VIN/VINST voltage for the step-down regulator.

When the VIN voltage rises above the pre-regulator boost output voltage $V_{PRE\_REG,boost}$ due to the increase voltage of VBAT, boost will stop operation. It will start switching again when the VIN voltage drops below the threshold $V_{PRE\_REG,boost,UV}$.

2.2 Pre-Regulator: Boost Regulator

The boost controller can be enabled by the BSTEN pin. The following figure shows the boost controller block diagram. If the boost is not used, the BSTEN pin should be connected to ground, and the external power elements (MOSFET, diode) are not needed.

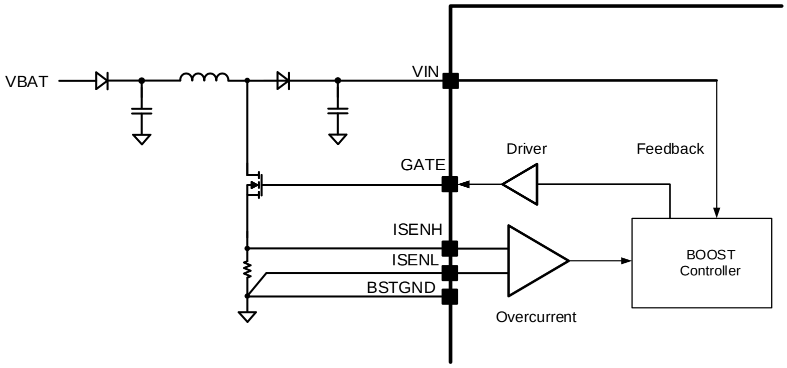


Figure 7. Boost Regulator

The boost output voltage VIN/VINST is regulated below the nominal supply voltage to ensure that it only operates during low input voltage conditions. When enabled, the boost regulator provides a higher output voltage than the nominal output voltage of the buck regulator. This regulator will only turn on when VIN/VINST voltage drops below the threshold $V_{PRE\_REG,boost,UV}$, and will turn off when VIN/VINST voltage is higher than the $V_{PRE\_REG,boost,UV}$.

The switching frequency of the boost regulator is internally fixed at 500kHz.

2.3 Pre-Regulator: Buck Regulator

The buck regulator uses a fixed frequency peak current control architecture. Both high side and low side power MOSFETs are integrated. Under light load conditions, the regulator operates in Forced Continues Current Mode (FCCM) in NORMAL, WAKE and INIT modes. In SLEEP mode, the pre buck regulator operates in Pulse Frequency Modulation (PFM) to minimize power consumption under light load conditions. The synchronization function is not available in PFM mode. The SA47301x cannot be synchronized to an external frequency source.

The frequency of the pre buck regulator can be set to 2.2MHz by leaving the FSW pin float, or 400kHz by connecting the FSW pin to ground. The switching frequency can be fine-tuned using an SPI command. A spread spectrum function is available for the internal clock of the converter and it can be enabled or disabled using SPI commands.

A synchronization signal which has the same frequency as the buck regulator is enabled at the SYN pin, and can be used for synchronizing external regulators, if the EXSEL pin is left open. The synchronization signal is the same phase or 180-degree shift compared with the pre buck regulator switching clock signal. The phase can be programmed using an SPI command.

A low ESR 47μF output capacitor is recommended for the high frequency setting, and the recommended capacitance value for the low frequency setting is 100μF.

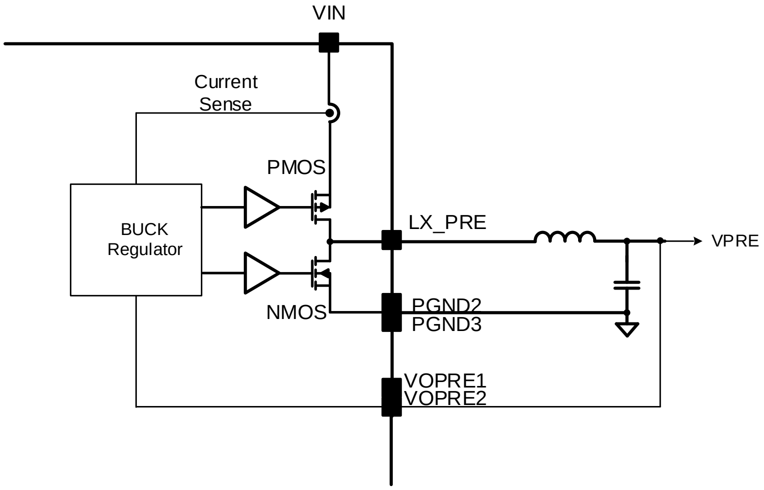


Figure 8. Buck Regulator

3 Post Regulators

3.1 Introduction

There are five LDOs supplied by the buck regulator, as well as control signals for an external post regulator for the MCU core supply, if needed.

The bandgap1 will provide the voltage reference to the MCU power supply (VUC), the communication power supply (VCO) and the reference power supply (VR). VR will provide the voltage reference to trackers VT1 and VT2. If VR is 3.3V and VT1 and VT2 require 5V output, the bandgap1 will also provide a voltage reference to VT1 and VT2.

An external regulator can be added when the pin EXSEL is left open. The EXSEL pin must be connected to ground if the external regulator is not used. The external buck regulator turns on with a high logic level signal, and turns off with a low logic level signal at the EXEN pin. The input of the external regulator is provided by either pre-regulator output or the battery.

The outputs of the post regulators and optional external regulator are monitored using the internal monitoring block.

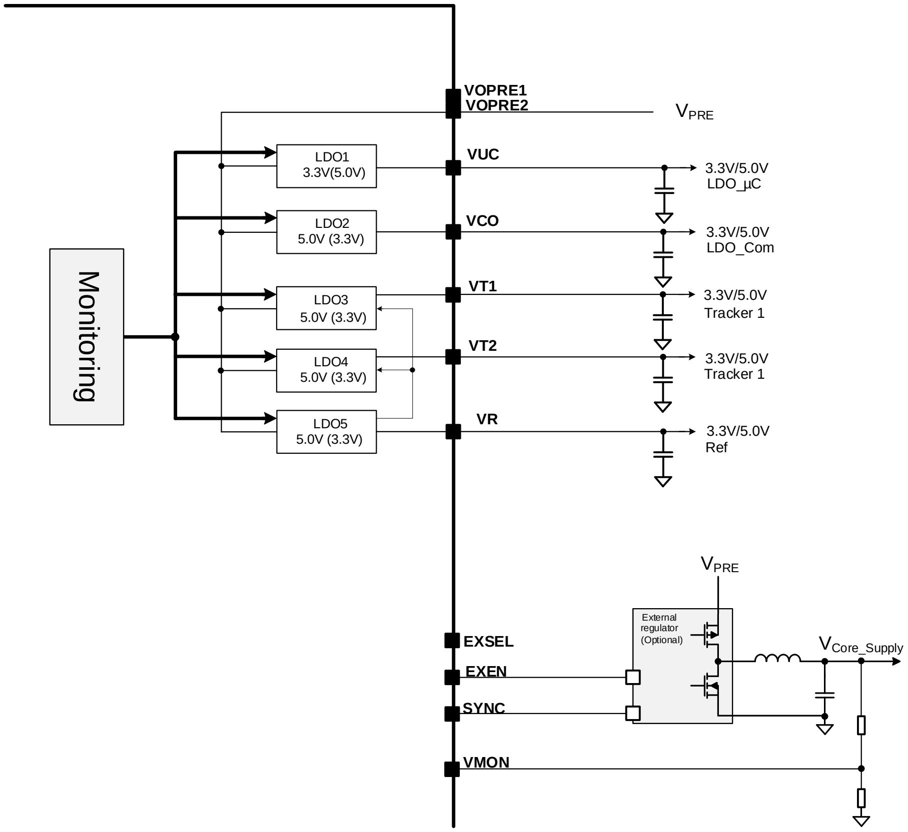


Figure 9. Post Regulators

3.2 VUC Regulator

The LDO_UC is supplied from the output of the pre-regulator. The output voltage V_{VUC} (at pin VUC) with a set value of 3.3V or 5.0V is regulated by the internal error amplifier with a reference voltage derived from band gap 1. To ensure stable operation, a low ESR MLCC capacitor with a sufficient voltage rating is recommended as the output capacitor.

Internal protection circuits are used to prevent the LDO and the external components from damage.

1) The output overvoltage (OV), undervoltage (UV) and Short to Ground (StG) are monitored by the voltage monitoring block. If overvoltage is detected at the VUC pin, the LDO_UC will be turned off and the OV event will be stored in the status register. The nRESET pin will be pulled low and the operation state will switch to FAILSAFE state. If an undervoltage event is detected, the LDO_UC will not turn off. The UV event will be stored in the status register. The nRESET pin will be pulled low and the operation will switch to INIT state. If the under-voltage condition lasts for longer than t_{StG}, the Short to Ground event will be triggered. The LDO_UC will be turned off. The StG event will be stored in the status register and the operation state will switch to FAILSAFE state.

2) An integrated current limit circuit protects the LDO_UC from overload or StG conditions. If the current flow through the LDO_UC is higher than the internal current limit threshold, the current will be regulated at the threshold level and the output voltage will drop.

3) A dedicated temperature sensor is integrated to sense the junction temperature of LDO_UC's power MOSFET. If the junction temperature exceeds the pre-warning threshold, the nINT pin will be pulled low and the event will be stored in the status register. If the junction temperature exceeds the thermal shutdown threshold, the operation state will switch to the FAILSAFE state, the LDO_UC will turn off for at least one second, and the event will be stored in the status register.

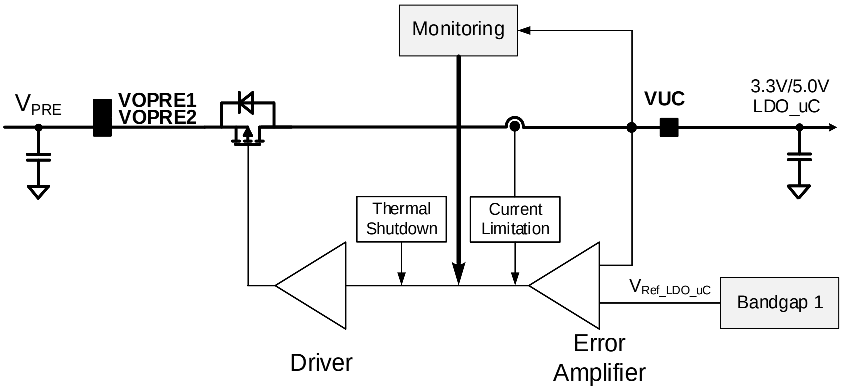


Figure 10. LDO_UC for MCU Supply

3.3 VCO Regulator

The LDO_COM is supplied by the output of the buck pre-regulator. The output voltage V_{VCO} (at pin VCO) set to 3.3V or 5.0V is regulated by the internal error amplifier with a reference voltage derived from band gap 1. To ensure stable operation, a low ESR MLCC capacitor with a sufficient voltage rating is recommended as the output capacitor. The LDO_COM turns off in STNDBY and FAILSAFE states. In INIT, NORMAL, WAKE and SLEEP states, the LDO_COM is on or off, as determined by the register configuration.

Internal protection circuits are used to prevent the LDO and the external components from damage.

1) The output overvoltage (OV), undervoltage (UV) and short to ground (StG) are monitored by the voltage monitoring block. If an overvoltage event is detected at the VCO pin, the LDO_COM will turn off and an OV event will be stored in the status register. The nINT pin will be pulled low. If undervoltage event is detected, the LDO_COM will not turn off. The nINT pin will be pulled low and a UV event will be stored in the status register. If the undervoltage condition lasts for longer than t_{StG}, the short to ground event will be triggered. The LDO_COM will be turned off. The nINT pin will be pulled low and the StG event will be stored in the status register.
2) An integrated current limit circuit protects the LDO_COM from over-load or short to ground conditions. If the current flow through the LDO_COM is higher than the internal current limit threshold, the current will be regulated at the threshold level and the output voltage will drop.
3) A dedicated temperature sensor is integrated to sense the junction temperature of the LDO_COM power MOSFET. If the junction temperature exceeds the pre-warning threshold, the nINT pin will be pulled low and the event will be stored in the status register. If the junction temperature exceeds the thermal shutdown threshold, the LDO_COM will turn off, the event will be stored in the status register, and nINT will be pulled low. LDO_COM can be enabled again using an SPI command.

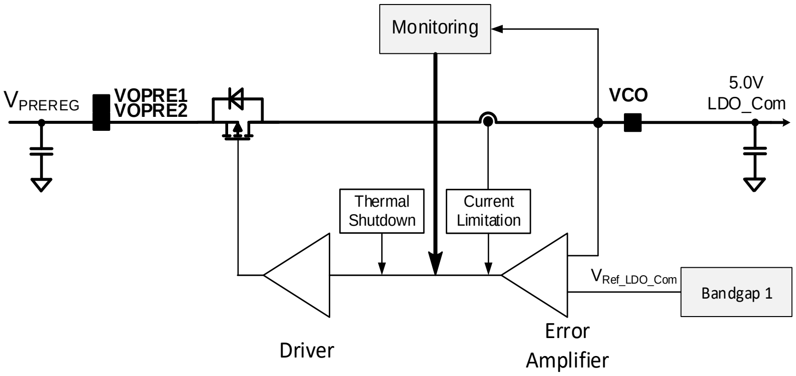


Figure 11. LDO_COM for Communications Supply

3.4 VR Regulator

The LDO_REF is supplied by the output of the buck pre-regulator. The output voltage V_{VR} (at pin VR) set to 3.3V or 5.0V is regulated by the internal error amplifier with a reference voltage derived from band gap 1. To ensure stable operation, a low ESR MLCC capacitor with a sufficient voltage rating is recommended as the output capacitor. The LDO_REF turns off in STNDBY and FAILSAFE states. In INIT, NORMAL, WAKE and SLEEP states, the LDO_REF is on or off, as determined by the register configuration.

Internal protection circuits are used to prevent the LDO and the external components from damage.

1) The output overvoltage (OV), undervoltage (UV) and Short to Ground (StG) are monitored by the voltage monitoring block. If overvoltage event is detected at the VR pin, the LDO_REF will turn off and the OV event will be stored in the status register. The nINT pin will be pulled low if bit 0x36[1] is set (high). The nRESET pin will be pulled low and the operation state will switch to FAILSAFE if bit 0x36[1] is 0. If an undervoltage event is detected, the LDO_REF will not turn off. The nINT pin will be pulled low and the UV event will be stored in the status register. If the under voltage condition lasts for longer than t_{StG}, a short to ground event will be triggered. The LDO_REF will be turned off. The nINT pin will be pulled low and the StG event will be stored in the status register.
2) An integrated current limit circuit protects the LDO_REF from over-load or short to ground conditions. If the current flow through the LDO_REF is higher than the internal current limit threshold, the current will be regulated at the threshold level and the output voltage will drop.
3) An overload at LDO_REF (overcurrent detected for more than 3ms) will be indicated by pulling nINT low, and it will be stored in the SPI status register.

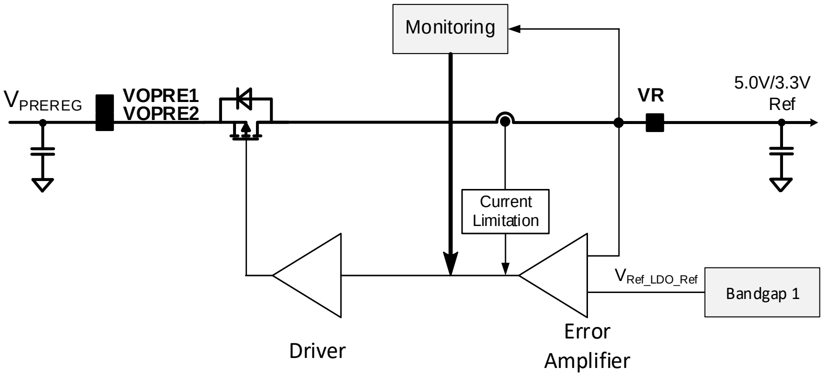


Figure 12. Precise LDO_REF as A Voltage Reference

3.5 VT1 and VT2 LDOs

LDO Tracker1 and Tracker2 are supplied by the output of the pre-regulator. The output voltage for V_{VT1} and V_{VT2} (at pins VT1 and VT2) is set to 5.0 V and it is regulated by the internal error amplifier with a reference voltage derived from LDO_REF (if LDO_REF is 5V) or band gap 1 (if LDO_REF is 3.3V). To ensure stable operation, a low ESR MLCC capacitor with sufficient voltage rating is recommended as the output capacitor. Tracker1 and Tracker2 rails are turned off in STNDBY and FAILSAFE states. In INIT, NORMAL, WAKE and SLEEP states, Tracker1 and Tracker2 are on or off determined by the register configuration.

The following internal protection circuits are used to prevent the LDOs and the external components from damage.

1) The output overvoltage (OV), undervoltage (UV) and Short to Ground (StG) are monitored by the voltage monitoring block. If an overvoltage event is detected on the VT1 or VT2 pins, the corresponding tracker will be turned off and the OV event will be stored in the status register. The nINT pin will pull low. If an undervoltage is detected, the corresponding tracker will not turn off. The nINT pin will be pulled low and the UV event will be stored in the status register. If the under voltage condition lasts for longer than t_{StG}, the short to ground event will be triggered. The corresponding tracker will turn off. The nINT pin is pulled low and the StG event will be stored in the status register.

2) An integrated current limit circuit protects Tracker1 and Tracker2 from overload or short to ground conditions. If the current flow through the corresponding tracker is higher than the internal current limit threshold, the current will be regulated at the threshold level and the output voltage will drop.

3) A reverse block power MOSFET is integrated in trackers to protect the device in the case of a short to battery case. In this situation, an overvoltage will be detected, and the corresponding tracker will be turned off. The OV event will be stored in the status register.

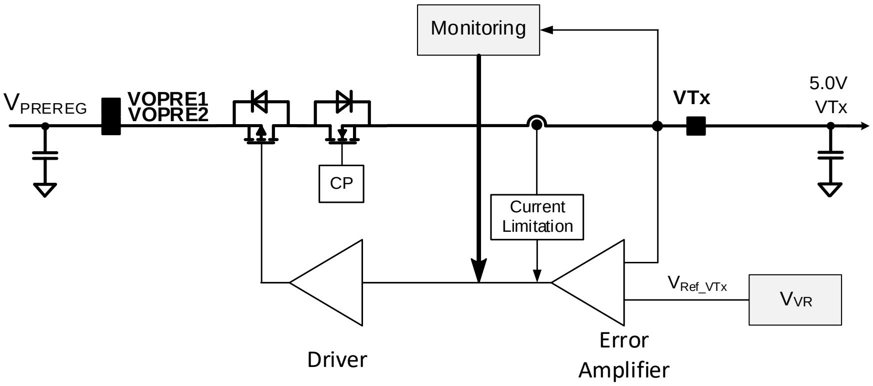


Figure 13. Tracker 1 & 2 for Sensor Supply

3.6 External Buck Regulator

An external buck regulator can be added to provide core supply or other supply, if needed in the system. The input of the external regulator could be connected to the output of pre regulator or directly to the battery.

The EXSEL pin should be left open if the external regulator is used. SA47301x only checks the configuration of the EXSEL pin during the POR state. The configuration status will not be updated after the operation state moves to INIT state.

The EXEN pin should be connected to the enable input pin of the external buck regulator to control the on/off of the regulator. The output of the EXEN pin is controlled by the state machine. A synchronization signal of 50% duty cycle is offered at pin SYN with the same phase or shifted by 180 degree and with the same frequency as the buck regulator clock. The phase can be configured using an SPI command. The synchronization signal at pin SYN can be switched on by SPI command, with the default configuration being off.

During the power up process, when EXEN is pulled high, the VMON voltage needs to rise to 0.8V within the $t_{stg,VMON}$ time; otherwise, it will be determined that VMON is short-circuited to ground, triggering the corresponding fault response.

Internal protection circuits are used to monitor the output of the external buck regulator. The output of the external buck regulator should be connected to the VMON pin using a properly calculated resistor divider.

1) The output overvoltage (OV), undervoltage (UV) and short to ground (StG) are monitored by voltage monitoring block.

   If an overvoltage event is detected on the VMON pin, the external buck regulator will be turned off by pulling the EXEN pin low and the OV event will be stored in the status register. The nRESET pin will be pulled low and the operation state will switch to FAILSAFE state. If an undervoltage event is detected, the external buck regulator will not be turned off. The nRESET pin will be pulled low and the UV event will be stored in the status register. The operation state will switch to INIT state. If the under voltage condition lasts for longer than $t_{StG,VMON}$, the short to ground event will be triggered. The external buck regulator will be turned off by pulling the EXEN pin low. The nRESET pin will be pulled low and the StG event will be stored in the status register. The operation state will switch to FAILSAFE state.

2) The external buck should include load current limit to protect from short to ground or overload conditions.

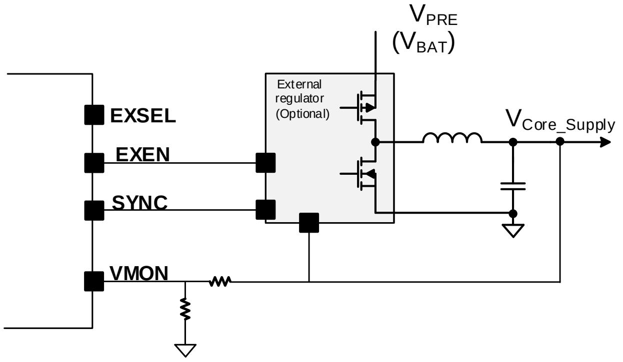


Figure 14. External Buck Regulator

4 VSTBY Regulator

The standby regulator LDO_STBY is supplied by pin VINST, which can be connected directly to the battery voltage (protected by reverse polarity diode) or to the output of the boost pre regulator (pin VIN). The regulator is independent from the buck pre-regulator stage and the other post regulators. The LDO_STBY offers a precise 3.3 V (or 5.0 V, equal to LDO_UC) output voltage for standby supply. The output voltage VSTBY (at pin VSTBY) is controlled by the error amplifier with a reference voltage derived from band gap 1 for regulators. LDO_STBY can be switched ON or OFF using an SPI command in all states. It will keep its state with its previous configuration when leaving STANDBY state. The status of LDO_STBY (ON or OFF) during STANDBY state has to be configured in previous states.

The following internal protection circuits are used to prevent the LDOs and the external components from damage.

1) Output overvoltage (OV), undervoltage (UV) and Short to Ground (StG) events are monitored by the voltage monitoring block. If an overvoltage event is detected on the VSTBY pin, the LDO_STBY will be turned off and the OV event will be stored in the status register. The nRESET pin will be pulled low and the operation state will switch to FAILSAFE. If an undervoltage event is detected, the LDO_STBY will not turn off. The UV event will be stored in the status register. The nRESET pin will be pulled low and the operation state will switch to INIT. If the under voltage condition lasts for longer than t_{StG}, the short to ground event will be triggered. The LDO_STBY will be turned off. The StG event will be stored in the status register. The operation state will switch to FAILSAFE.
2) An integrated current limit circuit protects the LDO_STBY from overload or short to ground conditions. If the current flow through the LDO_STBY is higher than the internal current limit threshold, the current will be regulated at the threshold level and the output voltage will drop.
3) An overload at LDO_STBY (overcurrent detected for more than 3ms) will be indicated by an interrupt, except if the device is in STANDBY state, and the event will be stored in SPI status register.

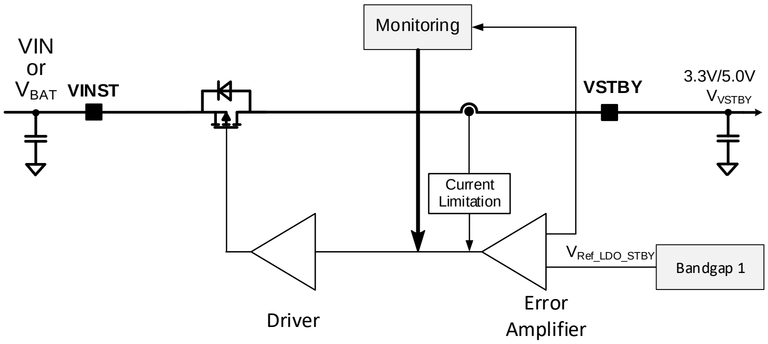


Figure 15. LDO for Standby Supply

5 Power Sequencing

The SA47301x uses internally fixed power sequencing to guarantee a proper power-up sequence for the system. After the VIN rises above $V_{VIN\_INIT\_Rising}$ threshold, the LDO_STBY and the pre regulators begin to operate.

If any of the power rails related to the MCU (LDO_STBY, pre regulators, LDO_UC and external regulator) fail to power up, the power sequence will stop and the operation will switch to FAILSAFE state. The nRESET pin will be driven low.

If any of power rails not related to the MCU (LDO_REF, LDO_COM, tracker1 and tracker2) fail to power up, the power sequence will stop, but pin nRESET will be set to high after the power on reset delay time t_{rd}. The MCU should check the status of the outputs by reading the SPI status register.

If any of the power rails not related to the MCU (LDO_REF, LDO_COM, tracker1 and tracker2) are disabled by the MCU using SPI commands during the power sequencing, the sequence will be stopped and the requested configuration will be executed.

5.1 Power Sequencing from POR to INIT State

If VIN is above $V_{VIN\_INIT\_Rising}$ rising threshold when ramping up and no undervoltage or overvoltage events are detected on the internal power supplies, the POR is released and the power sequencing from POR to INIT state starts.

1) When POR is released the standby regulator and the pre regulator start to operate.
2) When the output voltage of the buck regulator is above the UV threshold, the LDO_UC starts to operate.
3) When the output voltage of LDO_UC is above the UV threshold, the external buck regulator will start operating if enabled. If the external buck regulator is disabled, the LDO_REF starts to operate.
4) If the external regulator is enabled and the monitored voltage is above the UV threshold, the LDO_REF starts to operate.
5) When the output voltage of LDO_REF is above the UV threshold, the LDO_COM starts to operate.
6) When the output voltage of LDO_COM is above the UV threshold, Tracker1 starts to operate.
7) When the output voltage of Tracker1 is above the UV threshold, Tracker2 starts to operate.
8) When the output voltages of LDO_STBY, LDO_UC and external buck regulator all exceed their UV threshold, the nRESET pin is pulled high after a reset delay time t_{RD} which is programmable by SPI command.
9) The LDOs are using a current limited soft-start, with the soft-start time related to the output capacitance.

Once the nRESET pin is high, the MCU can change the regulators configuration, which will change the power sequencing accordingly.

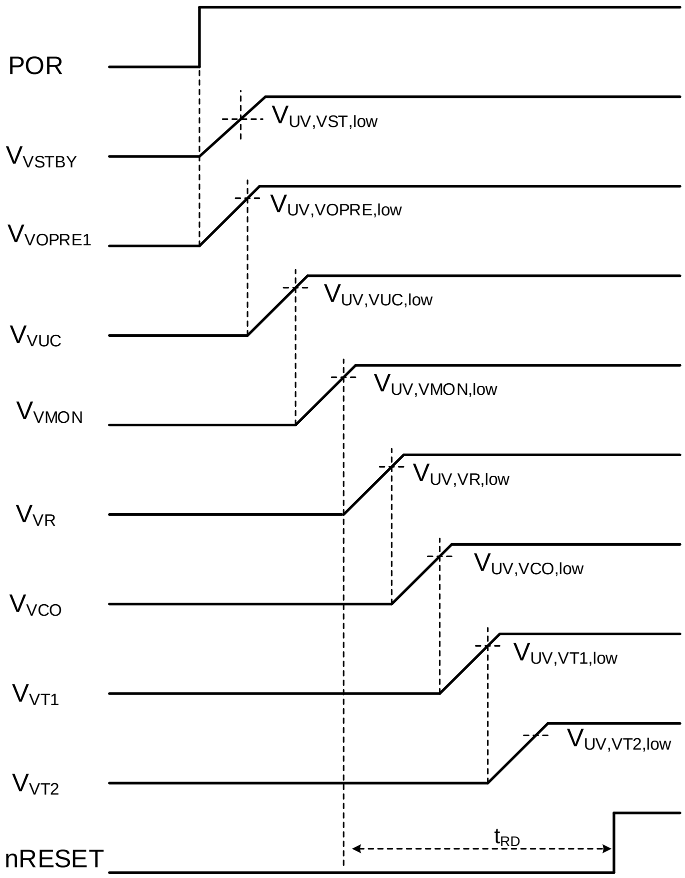


Figure 16. Power Sequencing POR to INIT State

5.2 Power Sequencing from STANDBY to INIT State

In STANDBY state, with the input voltage present, all other regulators (Pre-regulators and post regulators) are OFF except for LDO_STBY, assuming LDO_STBY is active.

1) After a valid wake-up signal or an expired wake-up timer the pre regulator starts to operate.
2) When the output voltage of the buck regulator is above the UV threshold, the LDO_UC starts to operate.
3) When the output voltage of LDO_UC is above the UV threshold, the external buck regulator will start working if it is enabled. If the external buck regulator is disabled, the LDO_REF starts to operate.
4) If the external regulator is enabled and the monitored voltage is above the UV threshold, the LDO_REF starts to operate.
5) When the output voltage of LDO_REF is above the UV threshold, the LDO_COM starts to operate.
6) When the output voltage of LDO_COM is above the UV threshold, Tracker1 starts to operate.
7) When the output voltage of Tracker1 is above the UV threshold, Tracker2 starts to operate.
8) When the output voltages of LDO_STBY, LDO_UC and external buck regulator all exceed their UV threshold, the nRESET pin is pulled high after a reset delay time t_{RD}, which is programmable using an SPI command.

Once the nRESET pin is high, the MCU can change the regulators configuration, which might change the power sequencing accordingly.

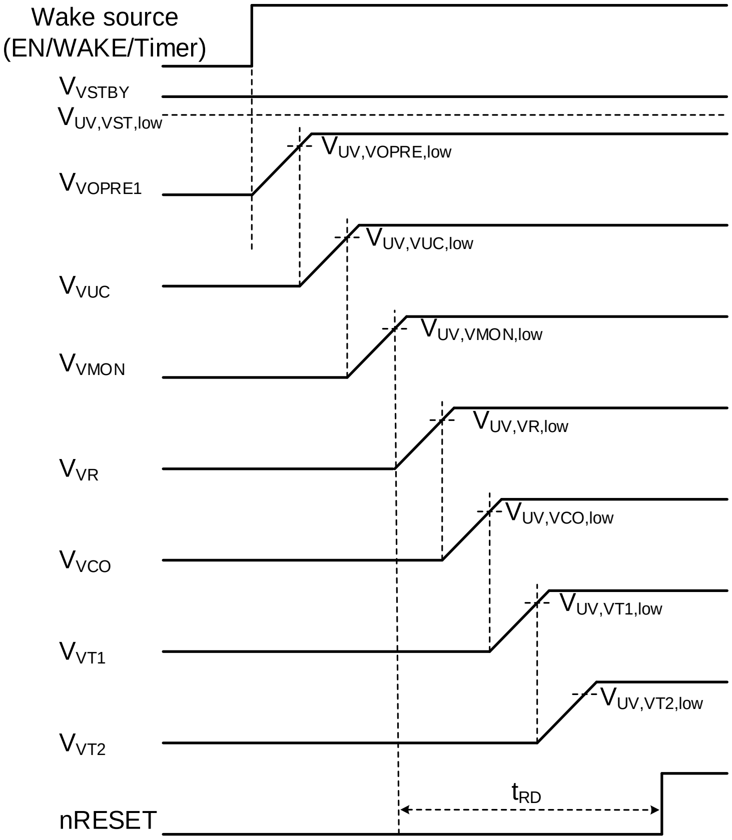


Figure 17. Power Sequencing from STANDBY to INIT State

5.3 Power Sequencing from SLEEP to WAKE State

In SLEEP state, if the input voltage is present, pre-regulators and LDO_UC are ON, and LDO_STBY is ON or OFF depending on the previous configuration. The other post regulators are switched ON or OFF depending on the configuration before the state transition request to move into SLEEP, and cannot be changed while in SLEEP state.

Assuming all selectable regulators are switched off in SLEEP state, and were switched on in previous the NORMAL state the following statements are true:

1) After a valid wake-up signal or an expired wake-up timer the LDO_REF starts to operate.
2) When the output voltage of LDO_REF is above the UV threshold, the LDO_COM starts to operate.
3) When the output voltage of LDO_COM is above the UV threshold, Tracker1 starts to operate.
4) When the output voltage of Tracker1 is above the UV threshold, Tracker2 starts to operate.
5) The reset output nRESET is high during SLEEP state and will be kept high when transitioning to WAKE state.

If a selectable regulator is switched off in the previous NORMAL state, it will not be enabled during the transition from SLEEP to WAKE, the power sequencing will follow up with the next LDO. If a selectable regulator is enabled during SLEEP state and was enabled in the previous NORMAL state, it will stay enabled.

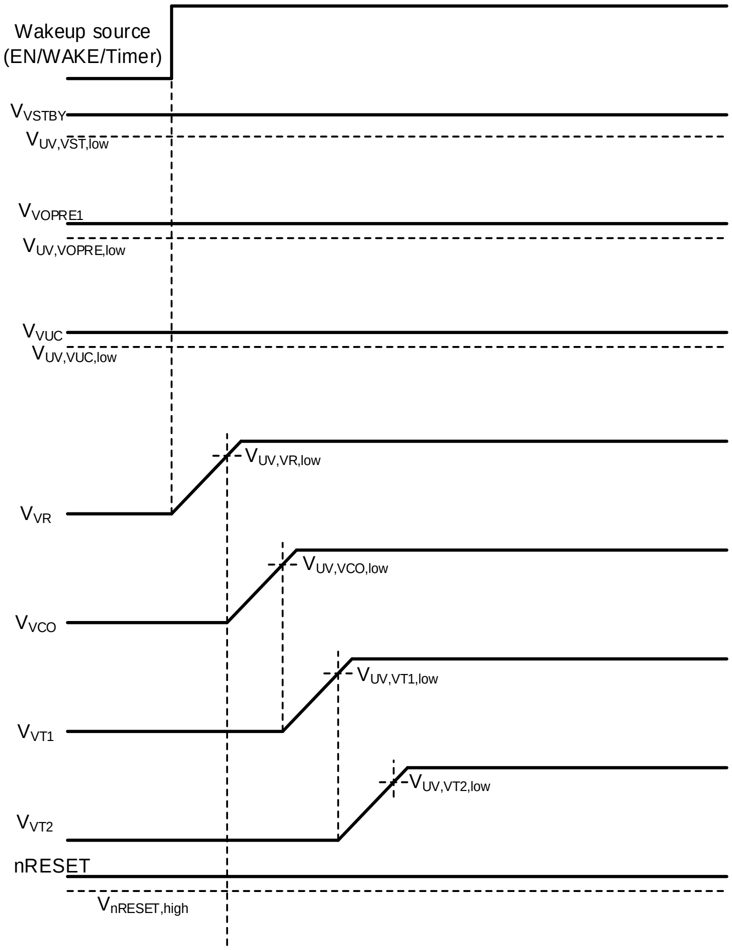


Figure 18. Power Sequencing SLEEP to WAKE State

6 Internal Supplies

To operate all power, monitor and logic functions, SA47301x integrates internal voltage supplies and circuits to supply bias currents. The internal supplies are monitored to guarantee normal operation. No external components are needed for the internal supplies and the voltage and current of internal supplies cannot be measured at the device pins.

7 Monitoring Function

7.1 Introduction

An independent monitoring block is integrated in SA47301x. The output voltage of all power rails including pre regulator, post regulator, external buck regulator and LDO_STBY are monitored. There are two comparators for each power rail: the over-voltage and under-voltage comparators. The reference of these comparators comes from bandgap 2, independent from bandgap 1 which provides the reference to the regulators.

There is a dedicated temperature sensor for the monitoring block. If the power stage temperature exceeds the temperature shutdown threshold, the device will transition to the FAILSAFE state, the regulators will be switched off for at least one second and the event will be stored in the SPI status register.

1) The thresholds of the over and undervoltage comparators are fixed for each power rail.
2) If the output voltage exceeds the over-voltage threshold and lasts for longer than t_{RR}, the OV event is triggered and the corresponding regulator will be turned off. Turning off other regulators is dependent on the device configuration. If the overvoltage lasts less than t_{RR}, it will be ignored and will not be detected.

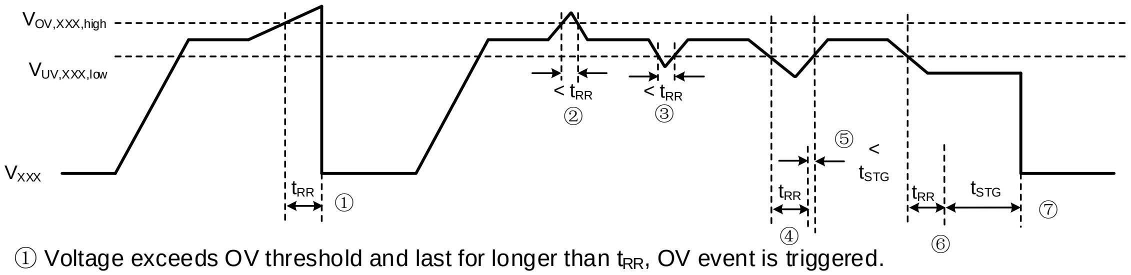
3) If the output voltage falls below the under-voltage threshold and lasts for longer than t_{RR}, the UV event is triggered but the corresponding regulator will not turn off. If the under voltage lasts less than t_{RR}, it will be ignored and will not be detected.

4) If output voltage falls below the under-voltage threshold and lasts for longer than t_{StG}, the StG event is triggered and the corresponding regulator will be turned off. Turning off other regulators is dependent on the device configuration. If the under voltage lasts less than t_{StG}, it will be treated as an UV event.

5) Overvoltage and undervoltage detection is performed only when a regulator is in use and switched on.

6) The OV and UV of internal supplies are monitored internally. The nRESET pin will be pulled low if OV or UV events for any of the internal supplies occur.

7) If overvoltage or a short to ground is detected at the external buck regulator, the EXEN pin will be pulled low to disable the regulator.



① Voltage exceeds OV threshold and last for longer than t_{RR}, OV event is triggered.
② Voltage exceeds OV threshold but last for shorter than t_{RR}, OV event is not triggered.
③ Voltage falls below UV threshold but last for shorter than t_{RR}, UV event is not triggered.
④ Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered.
⑤ After UV event is triggered, voltage still lower than UV threshold but last for shorter than t_{StG}, StG event is not triggered.
⑥ Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered.
⑦ After UV event is triggered, voltage still lower than UV threshold and last for longer than t_{StG}, StG event is triggered.

Figure 19. Timing Diagram of OV, UV, StG

All over and undervoltage events are stored in the SPI status register. The events are indicated by asserting the corresponding flag bits and interrupt or asserting the reset output, as shown in the table below:

Table 1. Indication of Over and Under Voltage

Regulator	Typical OV Threshold (V)	Typical UV Threshold(V)	OV Indication Pin	UV Indication Pin	StG Indication Pin
LDO_STBY	5.35 (3.53)	4.3 (2.97)	nRESET	nRESET	nRESET
Pre-Buck	6.58	5.1	nRESET	nINT	nRESET
LDO_UC	5.35 (3.53)	4.3 (2.97)	nRESET	nRESET	nRESET
External Post Buck	0.872	0.728	nRESET	nRESET	nRESET
LDO_REF	5.35 (3.53)	4.3 (2.97)	nRESET (0x36[1]=0) nINT (0x36[1]=1)	nINT	nINT
LDO_COM	5.5	4.5	nINT	nINT	nINT
Tracker1	5.5	4.5	nINT	nINT	nINT
Tracker2	5.5	4.5	nINT	nINT	nINT
VIN	42	5.1	nRESET (Except STANDBY MODE)	nRESET	NA
Internal Supplies	-	-	nRESET	nRESET	NA

7.2 Shutdown Function

The pre buck regulator detects short to ground events during the power sequence in INIT state. If a short to ground event of the pre regulator is detected, the operation state will switch to FAILSAFE.

When different events occur, each regulator behaves as follows:

Table 2. Behavior of Each Regulator When OV or STG Events Occur

Regulator	OV	Short to Ground
LDO_STBY	All regulators shut down	All regulators shut down
Pre-Buck	All regulators shut down	All regulators shut down
LDO_UC	All regulators shut down	All regulators shut down
External Post Buck	All regulators shut down	All regulators shut down
LDO_REF	All regulators shut down (Reg36[1]=0) Only LDO_REF shut down (Reg36[1]=1)	Related regulator shut down
LDO_COM	Only LDO_COM shut down	Only LDO_COM shut down
Tracker1	Only Tracker1 shut down	Only Tracker1 shut down
Tracker2	Only Tracker2 shut down	Only Tracker2 shut down

7.3 Reset and Interrupt Function

When the output voltages of LDO_STBY, LDO_UC and the external buck are all higher than the UV threshold, the nRESET pin will be pulled high after a reset delay time t_{RD}, which can be adjusted by SPI command.

A Soft Reset is defined as a condition when the nRESET pin is pulled low, but the pre and post regulators output voltages are not switched off. A Hard Reset is definied as a condtion when the nRESET pin is pulled low and the post regulator output voltages are switched off. In the case of a Hard Reset, power sequencing will be enabled after a delay of t_{SDT} (applicable to the second consecutive initialization timeout).

The nRESET pin is also used to indicate OV and UV events of internal supplies. The fault of the internal supplies will switch the operation state to FAILSAFE.

The detection of bandgaps changes, over load and temperature events will also trigger interrupt events.

8 Wake-Up Timer

The wake-up timer is an internal timer used to wake up the SA47301x from SLEEP or STANDBY states. Two registers need to be configured by SPI prior to using this feature: the value of the wake-up timer register and the time-base. The wake-up timer value may be set using SPI for the INIT, NORMAL and WAKE states. The value is stored in the 24 bit wide wake-up timer register (WKTIMCFG0, WKTIMCFG1, WKTIMCFG2). There are two choices (a 1 kHz or 1 Hz clock) for the time-base, which can be selected via SPI. For the selected time-base of 1 kHz, the timer resolution is 1ms and a wake-up time between 0 ms to 16,800 s can be configured. For the chosen time-base of 1 Hz, the timer resolution is 1s and a wake-up time between 0 s to 190 days can be configured.

When entering STANDBY or SLEEP states, the counter is loaded with the value of the wake-up timer register and starts decrementing. When the timer value reaches zero, the timer will wake up the device from either SLEEP or STANDBY state. When leaving SLEEP state, an interrupt will be generated.

If a wake-up event is not triggered by the wake-up timer, the timer stops and the MCU can read the remaining timer value by SPI to evaluate sleep time.

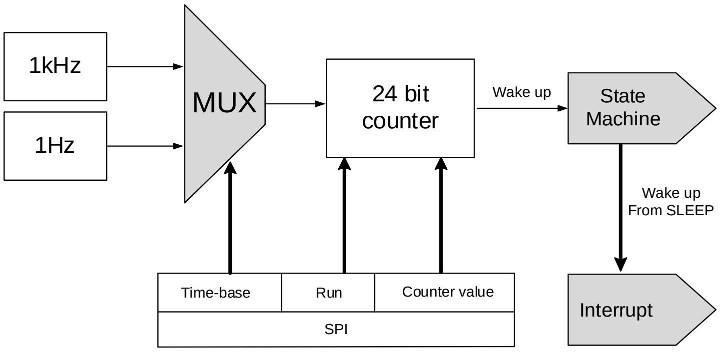


Figure 20. Wake-Up Timer

9 State Machine

The SA47301x has different states of operation. The transition between different states of operation is controlled by a state machine. This chapter describes the different states of operation and the transition between states.

The SA47301x will turn on when connected to a bus supply (Power-On-Reset POR) and moves into INIT state from Power Off state automatically, where the device is configured. After successful configuration, the device can move to NORMAL state using an SPI command. The device can switch from NORMAL to WAKE, SLEEP and STANDBY states using SPI commands, and can switch from WAKE to NORMAL, SLEEP and STANDBY states also using SPI commands. If the device operates in STANDBY state, it can only switch to INIT state using wake-up signals, and it could only switch to WAKE from SLEEP state via SPI commands or wake-up signals.

The following figure shows the state machine flow diagram:

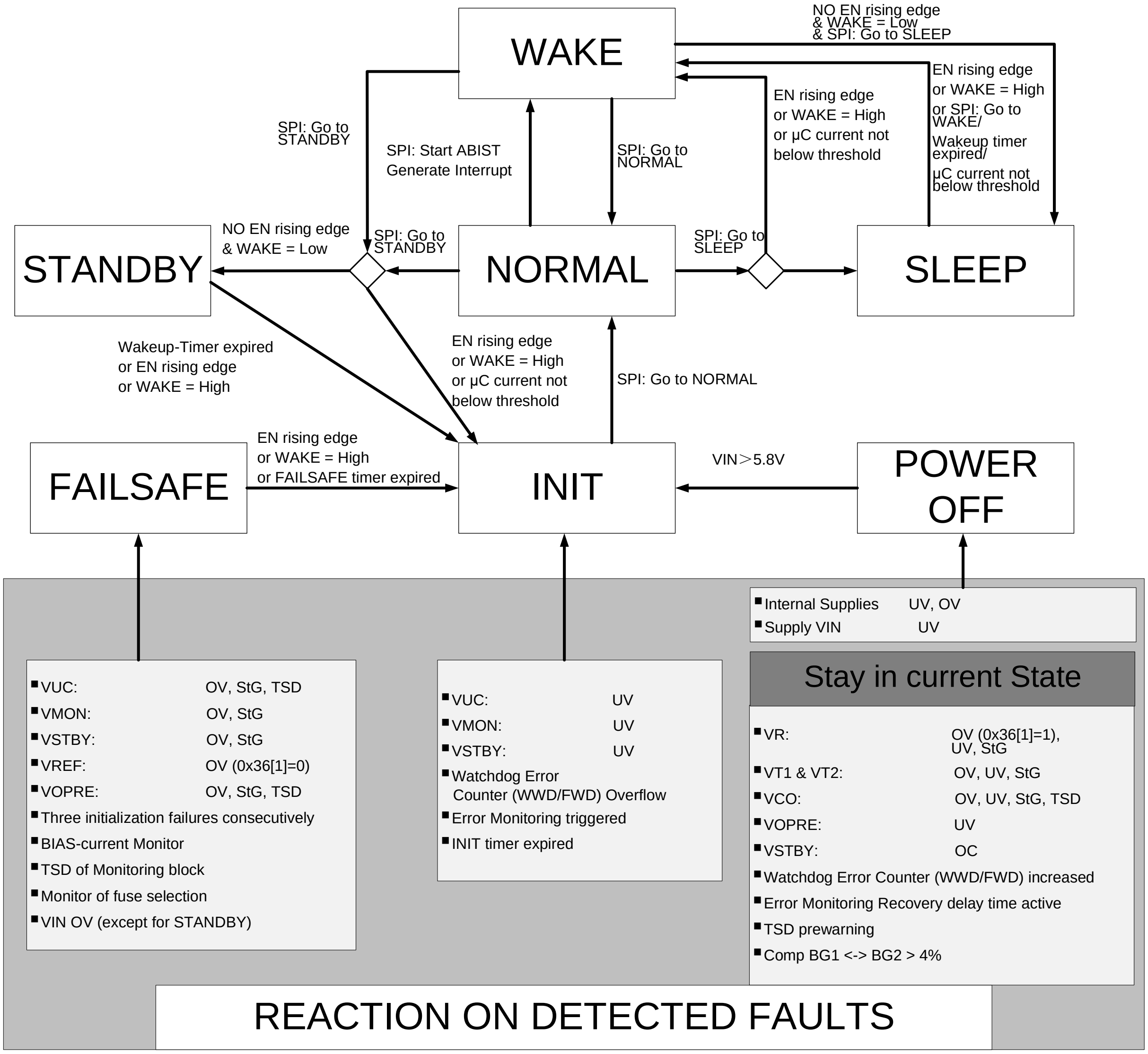


Figure 21. Flow Diagram State Machine

9.1 Description of States

Description:

- LOW:= Signal is low
- HIGH:= Signal is high
- OV:= Over-voltage
- UV:= Under-voltage
- StG:= Short to ground
- TSD:= Thermal shut-down
- OC:= Over-current
- ABIST:= Analog built-in self-test
- Comp BG1 <-> BG2 > 4%: The difference between bandgaps 1 and 2 is more than 4%

9.1.1 POWERDOWN State

When VIN voltage is lower than the undervoltage threshold, or the internal supplies are lower than their undervoltage thresholds, or higher than overvoltage thresholds, the SA47301x transitions to the POWERDOWN state. In this state, the status of each block is shown in the table below:

Table 3. POWERDOWN State

Functional Block	Status	Control Details
LDO_STBY	OFF	LDO_STBY is off.
LDO_UC	OFF	LDO_UC is off.
Pre-regulator	OFF	The Pre-regulator is off.
External Buck Regulator	OFF	The external buck regulator is off.
LDO_REF	OFF	LDO_REF is off.
LDO_COM	OFF	LDO_COM is off.
Tracker1	OFF	Tracker1 is off.
Tracker2	OFF	Tracker2 is off.
Wakeup Timer	OFF	The Wakeup Timer is off.
Window Watchdog	OFF	The Window Watchdog is off.
Functional Watchdog	OFF	The Functional Watchdog is off.
Error Monitoring	OFF	The Error Monitoring is off.
nRESET	LOW	The nRESET output is low.
SS1&2	LOW	Both safe state signals are LOW and the application is in safe state.

9.1.2 INIT State

If no valid communication from MCU within the INIT timer window is detected, the initialization timeout will be triggered. The INIT timer starts with the rising edge of nRESET and can be stopped when the following three conditions are met:

1) Valid SPI communication received from MCU.
2) Watchdog(s) serviced once according to default configuration or according to reconfiguration.
3) ERR monitoring serviced properly (minimum 3 periods provided) or configured to be OFF.

In INIT state, the status of each block is shown in the table below:

Table 4. INIT State

Functional Block	Status	Control Details
LDO_STBY	SELECTABLE*	1) Switched ON by default when entering from POWERDOWN state. 2) Switched ON or OFF depending on its configuration when entering from other states. 3) Switched ON or OFF by SPI command in INIT state.
LDO_UC	ON	1) Switched ON per default by entering the INIT state and cannot be configured by SPI command.
Pre-regulator	ON	1) Boost is on if BSTEN pin is left floating and VIN is lower than Boost UV threshold. BSTEN pin status is only checked at POR. 2) Buck is switched on per default by entering the INIT state and cannot be configured by SPI command
External Buck Regulator	Adjusted	1) External buck regulator is switched ON if the EXSEL pin is left floating and cannot be configured by SPI command. 2) The EXSEL pin status is only checked at POR.
LDO_REF	ON*	1) Switched ON by default when entering the INIT state. 2) Switched ON or OFF by SPI command in INIT state.
LDO_COM	ON*	1) Switched ON by default when entering the INIT state. 2) Switched ON or OFF by SPI command in INIT state.
Tracker1	ON*	1) Switched ON by default when entering the INIT state. 2) Switched ON or OFF by SPI command in current state.
Tracker2	ON*	1) Switched ON by default when entering the INIT state.

		2) Switched ON or OFF by SPI command in INIT state.
Wakeup Timer	OFF	1) Switched OFF in INIT state, although enabled by SPI command.
Window Watchdog	ON*	1) Switched ON by default in SPI triggered mode when entering the INIT state. 2) Switched ON or OFF by SPI command in INIT state.
Functional Watchdog	OFF*	1) Switched OFF by default when entering the INIT state. 2) Switched ON or OFF by SPI command in INIT state.
Error Monitoring	ON*	1) Switched ON by default when entering the INIT state. 2) Switched ON or OFF by SPI command in current state.
nRESET	ACTIVE	The nRESET output goes HIGH as soon as V_{VST}, V_{VUC} and V_{VMON} are above their UV threshold, delayed by the reset delay time t_{RD}.
SS1&2	LOW	Both safe state signals are LOW and the application is in safe state.

9.1.3 NORMAL State

The SA47301x supply MCU and other devices in NORMAL mode. Safety and monitoring functions (like reset block and safe state control) are active. The MCU may configure several post regulators and the wake-up timer via SPI commands for this state.

In NORMAL state, the status of each block is shown in the table below:

Table 5. NORMAL State

Functional Block	Status	Control Details
LDO_STBY	SELECTABLE	1) Switched ON or OFF depending on previous state when entering the NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
LDO_UC	ON	1) Switched ON when entering the NORMAL state 2) Cannot be changed by SPI command in NORMAL state.
Pre-regulator	ON	1) Boost is on if BSTEN pin is left floating and VIN is lower than Boost UV threshold. BSTEN pin status is only checked at POR. 2) Buck is switched on per default by entering the INIT state and cannot be configured by SPI command
External Buck Regulator	Adjusted	1) External buck regulator is switched ON if the EXSEL pin is left floating and cannot be configured by SPI command. 2) The EXSEL pin status is only checked at POR.
LDO_REF	SELECTABLE	1) Switched ON or OFF depending on its configuration when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
LDO_COM	SELECTABLE	1) Switched ON or OFF depending on its configuration when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
Tracker1	SELECTABLE	1) Switched ON or OFF depending on its configuration when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
Tracker2	SELECTABLE	1) Switched ON or OFF depending on its configuration when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
Wakeup Timer	OFF	1) Switched OFF in NORMAL state, although enabled by SPI command.
Window Watchdog	SELECTABLE	1) Switched ON or OFF depending on its previous state when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.

Functional Watchdog	SELECTABLE	1) Switched ON or OFF depending on its previous state when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
Error Monitoring	SELECTABLE	1) Switched ON or OFF depending on its previous state when entering NORMAL state. 2) Switched ON or OFF by SPI command in NORMAL state.
nRESET	High	The nRESET output is HIGH in NORMAL state.
SS1&2	High	Both safe state signals are HIGH.

9.1.4 STANDBY State

The STANDBY state is a low power state which the MCU can configure to reduce the current consumption to a minimum when the subsystem is not used for a prolonged period, while keeping it in a safe state.

In STANDBY state, the status of each block is shown in the table below:

Table 6. STANDBY State

Functional Block	Status	Control Details
LDO_STBY	SELECTED	1) Switched ON or OFF depending on its configuration in previous state when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
LDO_UC	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Pre-regulator	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
External Buck Regulator	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
LDO_REF	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
LDO_COM	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Tracker1	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Tracker2	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Wakeup Timer	SELECTED	1) Switched ON or OFF depending on its configuration in previous state when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Window Watchdog	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Functional Watchdog	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
Error Monitoring	OFF	1) Switched OFF when entering the STANDBY state. 2) Cannot be changed in STANDBY state.
nRESET	LOW	The nRESET output is LOW in STANDBY state.
SS1&2	LOW	Both safe state signals are LOW, the application is in a safe state.

9.1.5 SLEEP State

SLEEP is a low power state which the MCU may configure to reduce the current consumption when the subsytem is not used (e.g., MCU is in STOP mode), while keeping it in a safe state. The MCU may configure the status of regulators and safety functions using SPI commands before entering SLEEP.

In SLEEP state, the status of each part is shown in the table below.

Table 7. SLEEP State

Functional Block	Status	Control Details
LDO_STBY	SELECTED	1) Switched ON or OFF depending on its configuration in previous state when entering the SLEEP state. 2) Cannot be changed in SLEEP state.
LDO_UC	ON	1) Switched ON when entering the SLEEP state 2) Cannot be changed by SPI command in SLEEP state. Note: In SLEEP state the device is monitoring the output current of LDO_UC, so that if the current exceeds a certain threshold, an interrupt will be generated and the device will move to WAKE state.
Pre-regulator	ON	1) Boost is on if BSTEN pin is left floating and VIN is lower than Boost UV threshold. BSTEN pin status is only checked at POR. 2) Buck is switched on per default by entering the SLEEP state and cannot be configured by SPI command
External Buck Regulator	Adjusted	1) External buck regulator is switched ON if the EXSEL pin is left floating and cannot be configured by SPI command. 2) The EXSEL pin status is only checked at POR.
LDO_REF	SELECTED	1) Switched ON or OFF depending on the configuration by the state transition request to move into SLEEP. 2) Cannot be changed in SLEEP state.
LDO_COM	SELECTED	1) Switched ON or OFF depending on the configuration by the state transition request to move into SLEEP. 2) Cannot be changed in SLEEP state.
Tracker1	SELECTED	1) Switched ON or OFF depending on the configuration by the state transition request to move into SLEEP. 2) Cannot be changed in SLEEP state.
Tracker2	SELECTED	1) Switched ON or OFF depending on the configuration by the state transition request to move into SLEEP. 2) Cannot be changed in SLEEP state.
Wakeup Timer	SELECTED	1) Switched ON or OFF depending on its configuration in previous state. 2) Cannot be changed in SLEEP state.
Window Watchdog	SELECTED	1) Switched ON or OFF depending on its configuration in previous state for SLEEP state. 2) Cannot be changed in SLEEP state.
Functional Watchdog	SELECTED	1) Switched ON or OFF depending on its configuration in previous state for SLEEP state. 2) Cannot be changed in SLEEP state.
Error Monitoring	SELECTED	1) Switched ON or OFF depending on its configuration in previous state for SLEEP state. 2) Cannot be changed in SLEEP state.
nRESET	High	The nRESET output is High in SLEEP state.
SS1&2	Low	Both safe state signals are Low and the application is in safe state.

9.1.6 WAKE State

The WAKE state falls between the NORMAL and SLEEP states and is an intermediate state. This function is consistent with NORMAL state, but is designed to ensure that the subsystem being in safe state by keeping the safe state outputs low. It is used to service the watchdogs and error monitoring (minimum 3 periods) according to the selected configuration, and prepares the system for a correct and safe re-entry to NORMAL state. It can also switch device to SLEEP and STANDBY.

An interrupt is generated when the device enters WAKE state and whether the supervision functions (watchdogs and ERR monitoring) is activated depends on the previous configuration in NORMAL state. After entering the WAKE state, the configuration of the regulators resumes to the same state as the previous NORMAL state, keeping the subsystem is in a safe state.

In WAKE state, the status of each part is shown in the table below:

Table 8. WAKE State

Functional Block	Status	Control Details
LDO_STBY	SELECTABLE	1) Switched ON or OFF depending on previous NORMAL state configuration when entering the WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
LDO_UC	ON	1) Switched ON when entering the WAKE state. 2) Not configurable by SPI command.
Pre-regulator	Adjusted	1) Boost is on if BSTEN pin is left floating and VIN is lower than Boost UV threshold. BSTEN pin status is only checked at POR. 2) Buck is switched on per default by entering the SLEEP state and cannot be configured by SPI command
External Buck Regulator	Adjusted	1) External buck regulator is switched ON if the EXSEL pin is left floating and cannot be configured by SPI command. 2) The EXSEL pin status is only checked at POR.
LDO_REF	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
LDO_COM	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
Tracker1	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
Tracker2	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
Wakeup Timer	OFF	1) Switched OFF when entering WAKE state, although enabled by SPI command.
Window Watchdog	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
Functional Watchdog	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
Error Monitoring	SELECTABLE	1) Switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE state. 2) Switched ON or OFF by SPI command in WAKE state.
nRESET	High	The nRESET output is HIGH in WAKE state.
SS1&2	Low	Both safe state signals are LOW and the application is in a safe state.

9.1.7 FAILSAFE-State

In FAILSAFE-state, all regulators are switched off. The status of each part is shown in the table below:

Table 9. FAILSAFE

Functional Block	Status	Control Details
LDO_STBY	OFF	LDO_STBY is off.
LDO_UC	OFF	LDO_UC is off.
Pre-regulator	OFF	Pre regulator is off.
External Buck Regulator	OFF	The external buck regulator is off.
LDO_REF	OFF	LDO_REF is off.
LDO_COM	OFF	LDO_COM is off.

Tracker1	OFF	Tracker1 is off.
Tracker2	OFF	Tracker2 is off.
Wakeup Timer	OFF	Wakeup Timer is off.
Window Watchdog	OFF	Window Watchdog is off.
Functional Watchdog	OFF	Functional Watchdog is off.
Error Monitoring	OFF	Error Monitoring is off.
nRESET	LOW	The nRESET output is low.
SS1&2	LOW	Both safe state signals are LOW and the application is in safe state.

9.2 Transition between States

State transitions requested via SPI commands are initiated by a valid rising edge of the chip select (SCS).

9.3 POWERDOWN State to INIT State

When the VIN voltage increases above the POR threshold and no undervoltage or overvoltage on internal supplies are detected, the device switches from POWERDOWN to INIT state.

9.3.1 INIT State to NORMAL State

In the INIT state, if the following four conditions are met, the device will switch from INIT to NORMAL state using the SPI command, “Go to NORMAL”:

1) Watchdog needs to be serviced at least once within the INIT timer window.
2) ERR monitor needs to be serviced for minimum 3 periods or disabled within the INIT timer.
3) If functional watchdog is activated, a valid FWD triggering needs to be provided.
4) A delay of 60µs after the provided services must be considered to ensure proper release of internal validation signals.

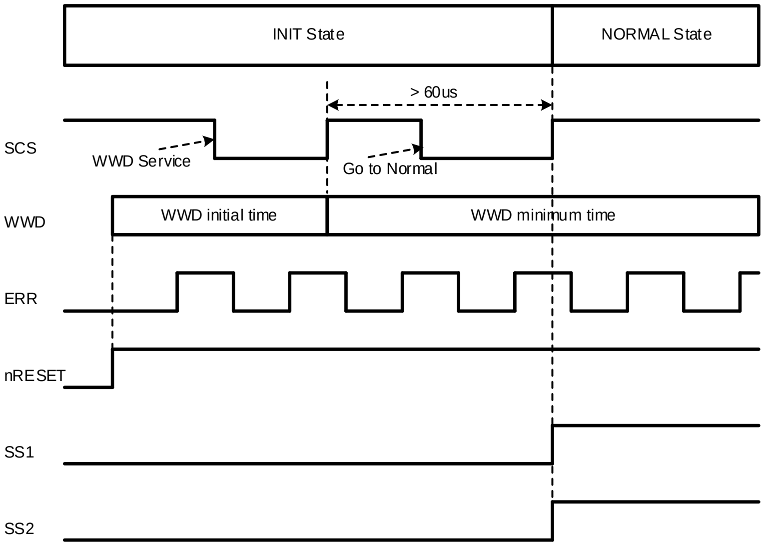


Figure 22. Transition from INIT to NORMAL State

Note:

1) A valid SPI command, “Go to NORMAL” (valid with chip select high at pin SCS) will move the device from INIT to NORMAL state.

2) nRESET pin stays HIGH as the post regulators are already active in INIT state.

3) With the positive edge of chip select high (at pin SCS) the safe state signals SS1 and SS2 are pulled HIGH after internal delay $t_{SS1,act}$ (typ:12us, max: 30us).

9.3.2 NORMAL State to SLEEP State

In NORMAL state, using the following configurations, the device will switch from NORMAL to SLEEP state using the SPI command "go to SLEEP".

1) Selection of LDO_UC current monitor or absolute transition timer by SPI command (Reg02[4]).

2) Transition delay timer $t_{tr,del}$ needs to be configured or default is used by SPI command (Reg00[3:0]).

3) Optionally LDO_UC current threshold needs to be defined, or default is used by SPI command (Reg02[3:2]).

During the transition to SLEEP state, when the following two situations occur, the device will move to WAKE state and the nINT pin will be pulled low to indicate an interrupt.

1) A valid EN (edge) or WAKE (level) signal is detected in transition state.

2) The LDO_UC current monitor is activated and the current consumption of the MCU is not below the selected LDO_UC current threshold before the transition delay timer $t_{tr,del}$ has expired. Transition delay time can be programmed by SPI command (Reg00[3:0]).

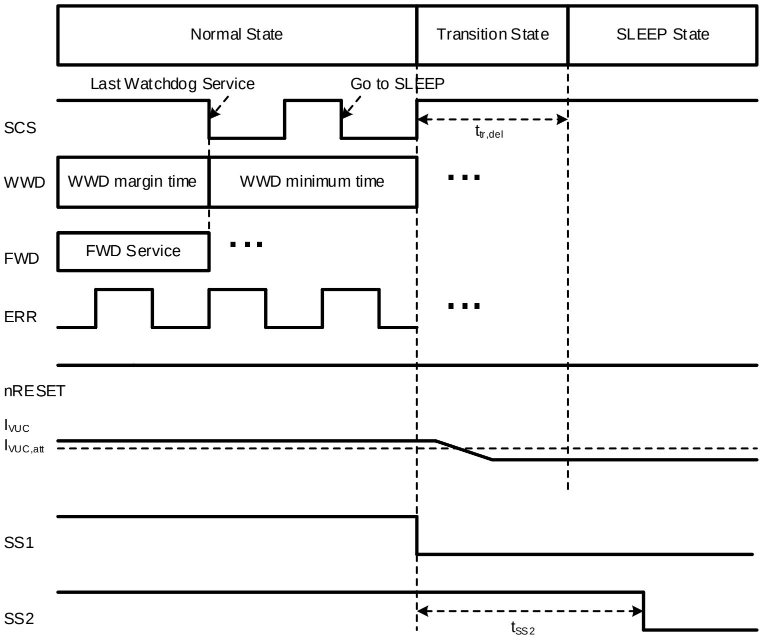


Figure 23. Transition from NORMAL to SLEEP State

Notes:

1) If the watchdog(s) is enabled in NORMAL state, it is recommended to service the watchdog(s) before issuing the SPI command "go to SLEEP", so that the positive edge of the SCS signal is in between the "WWD minimum time" of the window watchdog. This action can avoid interference between a missing watchdog trigger and the transition command "go to SLEEP".

2) After the SPI command "go to SLEEP", the positive edge of chip select (pin SCS) initiates the transition. With the positive edge of SCS high, the safe state SS1 output is pulled low, the device leaves NORMAL state and enters the transition state (to SLEEP state). After an adjustable delay time Δt_{SS2} between SS1 and SS2, the safe state SS2 output is pulled low.

3) If the monitoring of the window and functional watchdogs are both enabled by SPI command in NORMAL state, the monitoring will stop after transition state, due to watchdog functionality being disabled in SLEEP state by default. If watchdog functionality in SLEEP state is enabled, the watchdogs will operate based on individual configuration in NORMAL before entering SLEEP state.

4) If the error monitoring is enabled in NORMAL state, the monitoring will be stopped with the positive edge at pin SCS, as error monitoring function is disabled in SLEEP state by default. If error monitoring in SLEEP state is enabled, the error monitoring function will be ON or OFF based on its configuration in NORMAL state before entering SLEEP state.

5) nRESET pin stays HIGH as the MCU related regulators are not switched off.

6) If the LDO_UC current monitor is disabled and the absolute transition timer is selected in NORMAL state, the time of state transition depends on the transition delay time $t_{tr,del,}$ which can be programmed by SPI command between 100us and 1.6ms (default: 900us, 100us per step). Before the end of this transition time, it should be ensured that the LDO_UC current consumption has fallen below the LDO_UC monitoring threshold $I_{VUC, att}$ to keep the device in SLEEP state.

7) If the LDO_UC current monitor is enabled, the transition is made when the LDO_UC current falls below the LDO_UC current monitoring threshold $I_{VUC, att}$ within the configured maximum transition time $t_{tr,del}$ (1.6ms). The transition time is dependent on how long it takes for the LDO_UC current to fall below the current monitoring threshold $I_{VUC, att}$.

9.3.3 SLEEP State to WAKE State

In SLEEP state, when any of the following events occur, the device will enter WAKE state.

1) SPI command "Go to WAKE".

2) Valid Wakeup signal (rising edge on EN or high level on WAKE).

3) Current of LDO_UC exceeding the configured threshold.

4) Wake-up timer expired, if enabled.

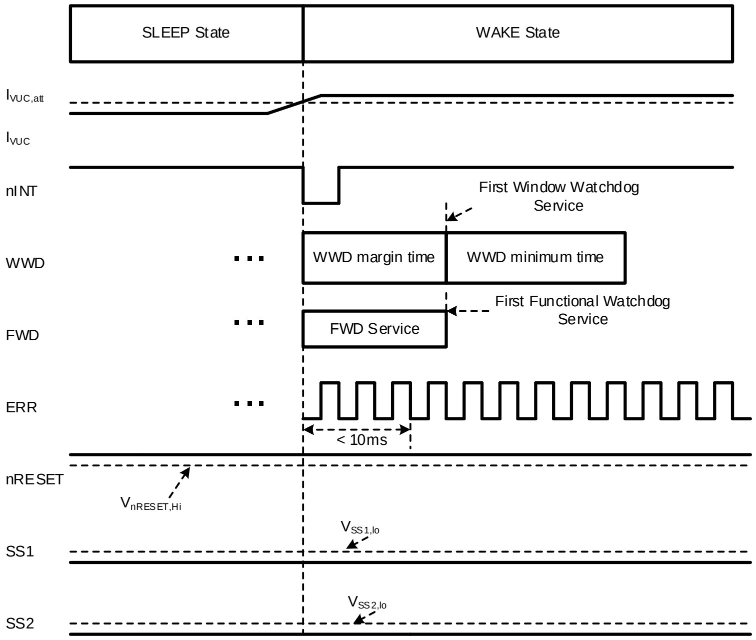


Figure 24. Transition from SLEEP to WAKE State

Notes:

1) State transition from SLEEP to WAKE requires no transition time. The nINT pin is pulled low to indicate that the state transition from SLEEP to WAKE has occurred. The event that caused the state transition from SLEEP state is stored in the status register.

2) All three monitoring functions (window watchdog, functional watchdog and error monitoring) will recover to the condition active or inactive (switched off) as they were in the NORMAL state prior to entering the SLEEP state.

3) The configuration of the post regulators will recover to the condition active or inactive (switched off) as they were in the NORMAL state prior to entering SLEEP state.

4) If the window watchdog is active in the previous NORMAL state and inactive in SLEEP state, the window watchdog will start the first WWD margin timer on the falling edge of pin nINT when entering the WAKE state. The WWD margin time can be programmed by SPI command and requires service. If the window watchdog is active in SLEEP state, continuous service is mandatory.

5) If the functional watchdog is active in the previous NORMAL state and inactive in SLEEP state, with the negative edge of interrupt signal (at pin nINT) the functional watchdog will start the heartbeat timer and require service. If the functional watchdog is active in SLEEP state continuous service will be mandatory.

6) If ERR pin monitoring is active in the previous NORMAL state and inactive in WAKE state, with the negative edge of interrupt signal (at pin nINT), error monitoring will become active again. At least 3 periods of valid ERR signal are required within 10ms after nINT pin is pulled low. If error monitoring has been active in SLEEP state, continuous toggling is mandatory.

7) nRESET pin stays HIGH as the post regulators are active in SLEEP state and in WAKE state.

8) The safe signals SS1 and SS2 will stay LOW in SLEEP and in WAKE state.

9.3.4 WAKE State to SLEEP State

In the WAKE state, if the the device is configured as shown below, the device will switch from WAKE state to SLEEP state using the SPI command “Go to SLEEP”.

1) Selection of LDO_UC current monitor or absolute transition timer by SPI command (Reg02[4]).

2) Transition delay timer $t_{tr,del}$ needs to be configured or default is used by SPI command (Reg00[3:0].

3) Optionally, the LDO_UC current threshold needs to be defined or default is used by SPI command (Reg02[3:2]).

During the transition to SLEEP state, when the following two situations occur, the device will switch to WAKE state and pin INT will be pulled low to indicate this interrupt.

1) A valid EN (edge) or WAKE (level) signal is detected in the transition state.

2) The LDO_UC current monitor is activated and the current consumption of the MCU is not below the selected LDO_UC current threshold before the transition delay timer $t_{tr,del}$ has expired. Transition delay time can be programmed by SPI command (Reg00[3:0]).

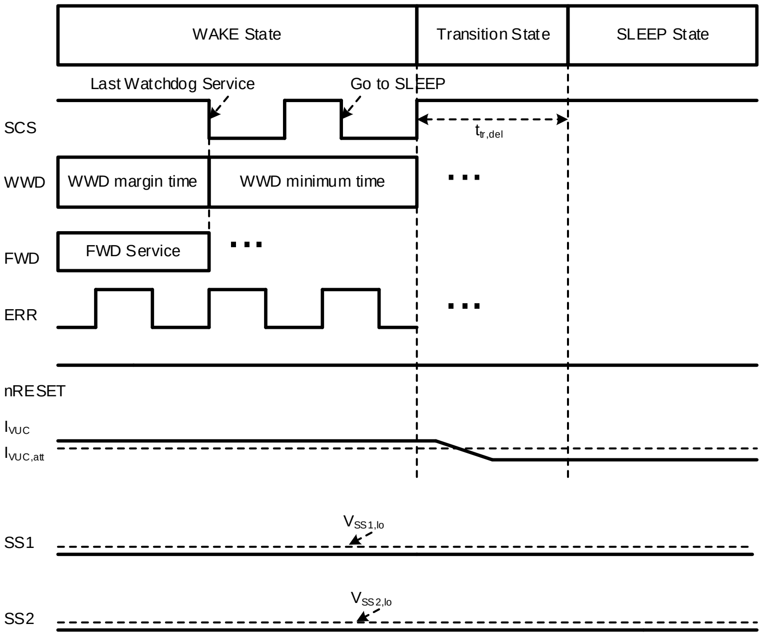


Figure 25. Transition from WAKE to SLEEP State

Notes:

1) If the watchdog(s) is enabled in WAKE state, it is recommended to serve watchdog(s) before issuing the SPI command "Go to SLEEP", so that the positive edge of SCS signal is within the WWD minimum time of the window watchdog. This action can avoid interference between a missing watchdog trigger and the transition command "Go to SLEEP".
2) After the SPI command "Go to SLEEP", the positive edge of chip select (pin SCS) initiates the transition. With the positive edge of SCS high, the device leaves WAKE state and enters the transition state (to SLEEP state).
3) If monitoring of the window and functional watchdogs is enabled by the SPI command in WAKE state, the monitoring will be stopped after transition state because watchdog functionality is disabled in SLEEP state by default. If watchdog functionality in SLEEP state is enabled, the watchdogs will work based on individual configuration in WAKE state before entering SLEEP state.
4) If the error monitoring is enabled in WAKE state, the monitoring will be stopped with the positive edge at pin SCS, due to the error monitoring function being disabled in SLEEP state by default. If error monitoring in SLEEP state is enabled, the error monitoring function will be ON or OFF based on its configuration in WAKE state before entering SLEEP state.
5) nRESET pin stays HIGH as the MCU related regulators are not switched off.
6) If the LDO_UC current monitor is disabled and the absolute transition timer is selected in WAKE state, the transition time depends on the transition delay time $t_{tr,del}$ which can be programmed via an SPI command from 100us to 1.6ms (default: 900us, 100us per step). Before the end of this transition time, it should be ensured that the LDO_UC current consumption has fallen below the LDO_UC monitoring threshold $I_{VUC,\ att}$ to keep the device in SLEEP state.
7) If the LDO_UC current monitor is enabled, the transition is done when the LDO_UC current falls below the LDO_UC current monitoring threshold $I_{VUC,\ att}$ within the configured maximum transition time $t_{tr,del}$ (1.6ms). The transition time is dependent on how long it takes for the LDO_UC current to fall below the LDO_UC current monitoring threshold $I_{VUC,att}$.
8) Safe state signals SS1 and SS2 stay LOW all the time.

9.3.5 NORMAL State to STANDBY State

In the NORMAL state, if the device is configured as shown below, the device will switch from NORMAL state to STANDBY state using the SPI command "Go to STANDBY".

1) Selection of LDO_UC current monitor or absolute transition timer via an SPI command (Reg02[4]).
2) Transition delay timer $t_{tr,del}$ needs to be configured via an SPI command (Reg00[3:0] or the default is used.
3) Optionally, LDO_UC current threshold needs to be defined, using an SPI command (Reg02[3:2]), or the default is used.

During the transition to STANDBY state, when the following two situations occur, the device will move into the INIT state and the nRESET pin will be pulled low to indicate the event.

1) A valid EN (edge) or WAKE (level) signal is detected during the transition.
2) The LDO_UC current monitor is activated and the current consumption of the MCU is not below the selected LDO_UC current threshold before the transition delay timer $t_{tr,del}$ has expired. The transition delay time can be programmed using an SPI command (Reg00[3:0]).

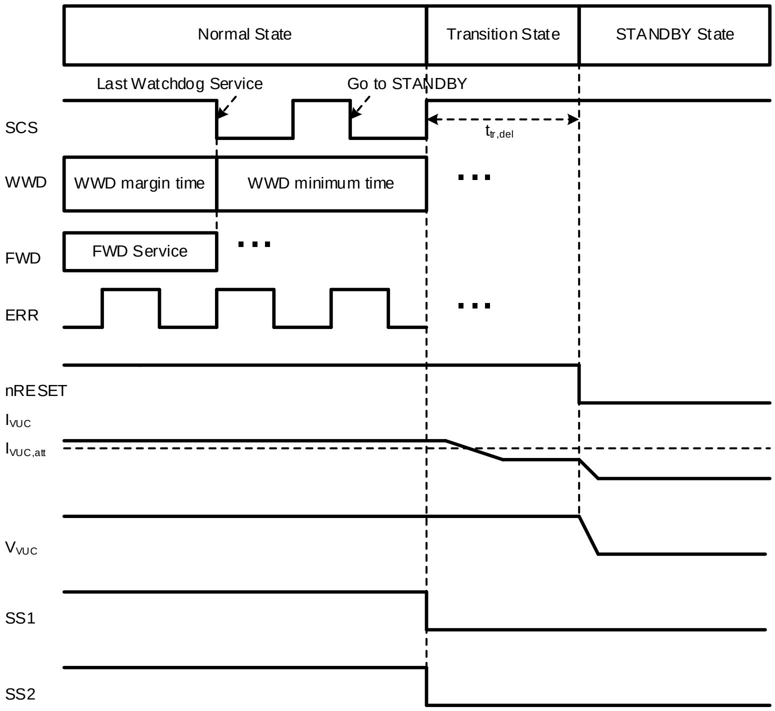


Figure 26. Transition from NORMAL to STANDBY State

Note:

1) If the watchdog(s) is enabled in NORMAL state, it is recommended to service the watchdog(s) before issuing the SPI command “Go to STANDBY”, so that the positive edge of SCS signal is within the WWD minimum time of the window watchdog. This action can avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”.
2) After the SPI command “Go to STANDBY”, the positive edge of chip select (pin SCS) initiates the transition. SS1 and SS2 are pulled low and the device leaves NORMAL state and enters the transition state (to STANDBY state) with the rising edge at SCS pin.
3) If monitoring of the window watchdog and the functional watchdog is enabled by SPI command in NORMAL state, the monitoring will be stopped after transition state because watchdog functionality is disabled in STANDBY state.
4) If error monitoring is enabled in NORMAL state, monitoring will be stopped with the positive edge at pin SCS due to error monitoring function being disabled in STANDBY state.
5) nRESET pin is pulled low after transition time.

6) All the pre and post regulator rails except LDO_STBY are turned off when the transition is complete. LDO_STBY may be ON or OFF in STANDBY state depending on its configuration in NORMAL state.

7) If the LDO_UC current monitor is disabled and the absolute transition timer is selected in NORMAL state, the time of transition state is dependent on the transition delay time $t_{tr,del,}$ which can be programmed using an SPI command from 100us to 1.6ms (default: 900us, 100us per step).

8) If the LDO_UC current monitor is enabled, the transition is done when the LDO_UC current falls below the LDO_UC current monitoring threshold $I_{VUC, att}$ within the configured maximum transition time $t_{tr,del}$ (1.6ms). The transition time is dependent on how long it takes for the LDO_UC current to fall below the LDO_UC current monitoring threshold $I_{VUC,att}$.

9) When the channel is turned off, the three channels (VSTBY, VUC, and VCO) have built-in discharge resistors inside the chip to rapidly discharge their outputs. Other output power supply channels do not have internal discharge resistors.

9.3.6 STANDBY State to INIT State

In STANDBY state, when a valid EN (edge) or WAKE (level) signal is detected, the device will switch from STANDBY state to INIT state. If the wake-up timer is enabled, the device will also switch from STANDBY state to INIT state when the wake-up timer expires.

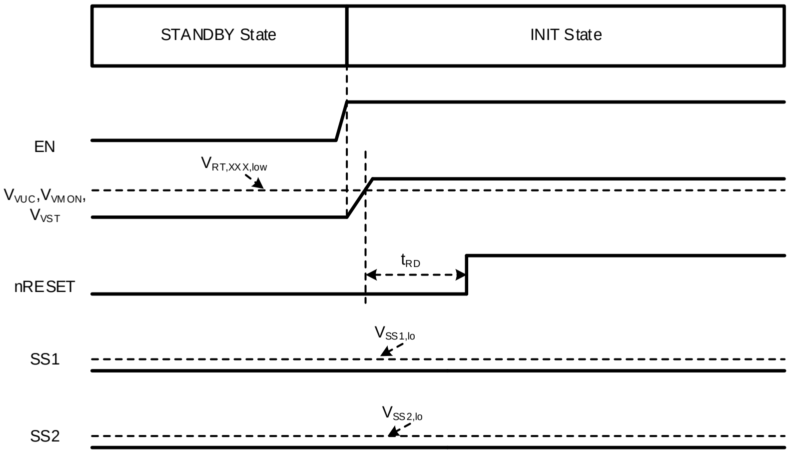


Figure 27. Transition from STANDBY to INIT State

Notes:

1) The pre regulator and all post regulators are switched on according to the power sequencing. LDO_STBY is kept ON or OFF according to its configuration.

2) When the output voltage of LDO_STBY (if enabled), LDO_UC and external buck are greater than the UV threshold, the power-on reset delay timer starts. After the power-on reset time t_{RD}, the nRESET pin will be pulled high.

3) SS1 and SS2 outputs will stay LOW in STANDBY state and in INIT state.

4) When the chip is wake up immediately after entering standby state, and when there is a large capacitor in the VOPRE, if the VOPRE voltage does not discharge below the under-voltage threshold before the chip restarts, the subsequent-stage VUC will start immediately. At this time, the soft-start reference inside VOPRE rises slowly from 0V. Since the VUC draw current from the load during startup, pulling down the VOPRE voltage, a false VOPRE undervoltage (UV) alarm will occur once during the startup process. The VOPRE output voltage will be properly established when the internal soft-start reference of VOPRE reaches a certain voltage level.

9.3.7 WAKE State to NORMAL State

The watchdogs need to be serviced at least once, and ERR monitoring needs to be serviced at least 3 periods in the active WAKE state, if they are restarted/reinitialized in WAKE state. After receiving the SPI command “Go to NORMAL” the device can switch from WAKE to NORMAL state.

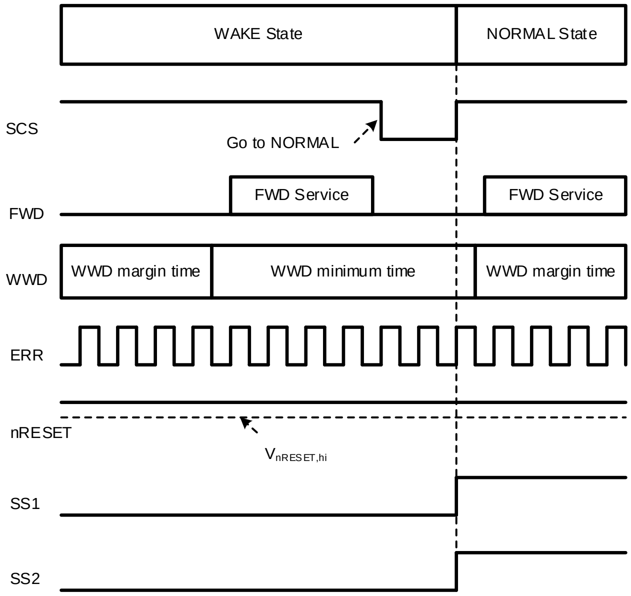


Figure 28. Transition from WAKE State to NORMAL State

Notes:

1) EN pin’s positive edge and WAKE pin’s high level are ignored during the WAKE state. A valid EN or WAKE signal will not trigger a transition from WAKE to NORMAL state.
2) A continuous service signal will be required for the watchdogs (if active in WAKE state), which is not synchronized to the transition from WAKE state to NORMAL state.
3) A continuous toggling signal will be required for error monitoring (if active in WAKE state), which is not synchronized to the transition from WAKE to NORMAL state. The device will start transition to the NORMAL state after at least 3 periods of the toggling signal are detected.
4) Reset pin nRESET stays HIGH as the post regulators are active in WAKE state and in NORMAL state.
5) On the positive edge of the SCS pin, the safe state signals SS1 and SS2 are pulled to HIGH at same time.

9.3.8 WAKE State to STANDBY State

In the WAKE state, the device will switch from WAKE state to STANDBY state by SPI command “Go to STANDBY”. The following steps are suggested for correct operation:

1) Selection of LDO_UC current monitor or absolute transition timer using an SPI command (Reg02[4]).
2) Transition delay timer $t_{tr,del}$ needs to be configured (or the default is used) using an SPI command (Reg00[3:0].
3) Optionally, LDO_UC current threshold needs to be defined (or the default value is used) by SPI command (Reg02[3:2]).

During the transition to STANDBY state, when the following two situations occur, the device will move into the INIT state and pin nRESET will be pulled low to indicate this event:

1) A valid EN (edge) or WAKE (level) signal is detected in transition state.

2) The LDO_UC current monitor is activated and the current consumption of the MCU is not below the selected LDO_UC current threshold before the transition delay timer $t_{tr,del}$ has expired. The transition delay time can be programmed using an SPI command (Reg00[3:0]).

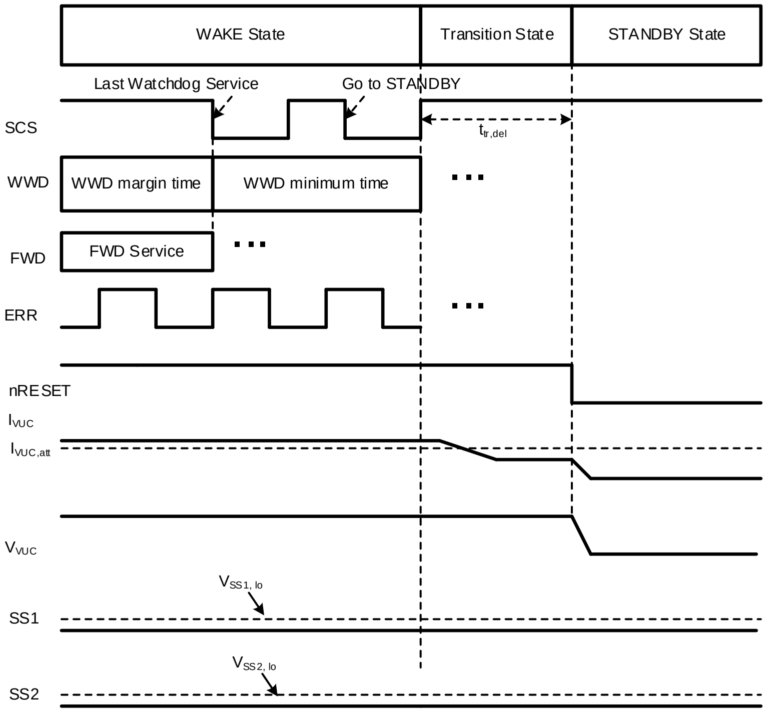


Figure 29. Transition from WAKE State to STANDBY State

Notes:

1) If the watchdog(s) is enabled in WAKE state, it is recommended to service the watchdog(s) before issuing the SPI command "Go to STANDBY", so that the positive edge of SCS signal is well within the WWD minimum time of the window watchdog. This action can avoid interference between a missing watchdog trigger and the transition command "Go to STANDBY".

2) After the SPI command "Go to STANDBY", the positive edge of pin SCS initiates the transition. SS1 and SS2 are pulled low, the device leaves WAKE state and enters the transition state (to STANDBY state) on the rising edge of SCS pin.

3) If the monitoring of window watchdog and the functional watchdog are both enabled via an SPI command in NORMAL state, the monitoring will be stopped after transition state, because watchdog functionality is disabled in STANDBY state.

4) If the error monitoring is enabled in WAKE state, the monitoring will be stopped on the positive edge of the SCS pin, because error monitoring function is disabled in STANDBY state.

5) nRESET pin is pulled low after the transition is complete.

6) All the pre and post regulator except LDO_STBY are turned off when transition is complete. LDO_STBY may be ON or OFF in STANDBY state, depending on its configuration in NORMAL state.

7) If the LDO_UC current monitor is disabled and the absolute transition timer is selected in WAKE state, the time of transition state depends on the transition delay time $t_{tr,del}$, which can be programmed by SPI command between 100us and 1.6ms (default: 900us, 100us per step).

8) If the LDO_UC current monitor is enabled, the transition is done when the LDO_UC current falls below the LDO_UC current monitoring threshold $I_{VUC, att}$ within the configured maximum transition time $t_{tr,del}$ (1.6ms). The transition time depends on how long it takes for the LDO_UC current to fall below the LDO_UC current monitoring threshold $I_{VUC, att}$.

9.3.9 FAILSAFE-State to INIT State

In FAILSAFE state, if the failsafe timer has expired and the VIN voltage is higher than UV threshold, the device will switch to INIT state if any of the following events occur:

1) Automatically switch to INIT state after the FAILSAFE timer has expired if the FAILSAFE state is not entered three times in a row with the same failure.
2) Valid EN (edge) or WAKE (level) signal.

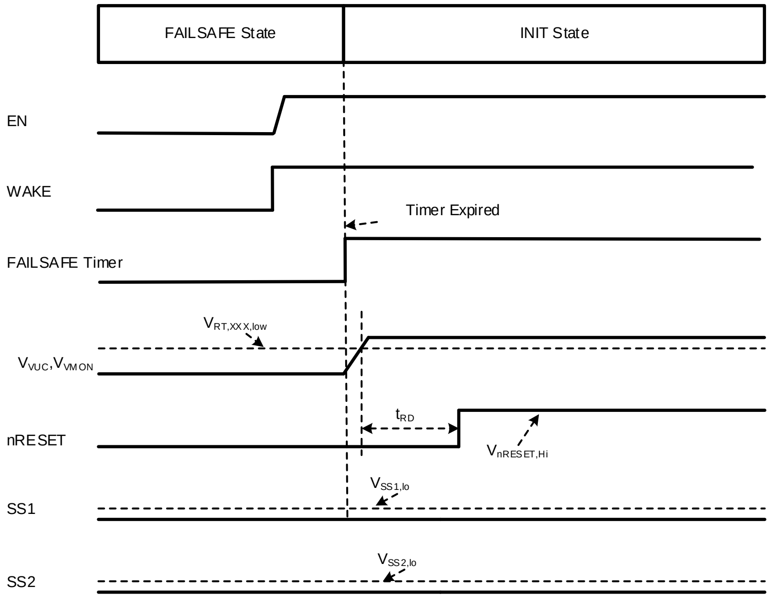


Figure 30. Transition from FAILSAFE-state to INIT State

Notes:

1) The device does not transition from FAILSAFE state to INIT state before the minimum FAILSAFE time $t_{FAILSAFE,min}$, which is 1s for thermal shutdown and 20ms for all other failures.
2) After switching to INIT state the output voltage of the regulators will start ramping up according to the power-up sequence.
3) The power on reset delay timer starts as soon as the last of the MCU related regulators V_{VUC}, V_{VMON} or V_{VST} (according to the previous configuration) crosses its undervoltage reset threshold $V_{RT,xxx,low}$ on the way up.
4) The device needs to be configured and initiated. All register values will be reset, except the configuration of the LDO_Stby (RSYSPCFG0) and the reset delay time (DEVCFG1).
5) The safe signals SS1 and SS2 are kept LOW in both FAILSAFE and INIT states.

9.4 Device Response to Detected Faults

There are four possible state transitions after a fault happens.

1) Stay in Current State: If the fault will not affect the MCU and has no risk to the device, the operation state of the device will not be changed. These faults are indicated by an interrupt.
2) Move to INIT State: The device will switch to INIT state when medium severity faults happen. The nRESET signal will be pulled low to reset the MCU.
3) Move to FAILSAFE State: The device will move to FAILSAFE state if critical faults happen.
4) Move to POWERDOWN State: Most critical errors, with high risk of damaging the device itself and the microcontroller.

In this document, the errors that will cause the device transition to move to the INIT state, FAILSAFE state and POWERDOWN state are referred to as “error triggered state transitions”.

When errors that cause device state transitions occur simultaneously, the device will preferentially enter the POWERDOWN or FAILSAFE states, which take precedence over INIT state.

Table 10. Reaction On Detected Faults

Failures	The Action of the Device
LDO_UC: OTW LDO_REF: OV when Reg36[1] = 1, UV, StG, OC. Tracker 1/2: OV, UV, StG. LDO_COM: OV, UV, StG, OTW, TSD Pre Buck: UV, OTW LDO_STBY: OC Watchdog (WWD/FWD) error counter increased Error Monitoring Recovery delay time active Comp BG1 <-> BG2 > 4%	Stay in current state and generate an interrupt
LDO_UC: UV External Buck: UV LDO_STBY: UV Watchdog (WWD/FWD) error counter overflow Error monitor triggered INIT timer expired	Move to INIT state and nRESET will be pulled low
LDO_UC: OV, StG, TSD External buck: OV, StG LDO_STBY: OV, StG LDO_REF: OV when Reg36[1] = 0 Pre buck: OV, StG, TSD Three initialization failures consecutively BIAS-current Monitor Monitoring block: TSD Monitor of fuse selection VIN: OV (except for STANDBY)	Move to FAILSAFE state
Internal supplies: OV, UV VIN: UV	Move to POWERDOWN state

9.4.1 Stay in Current State

When any of the following events occur, these errors will be indicated by an interrupt and the state of the device will not be changed:

1) Detection of overvoltage at LDO_REF V_{VR} when Reg36[1] = 1.
2) Detection of undervoltage, short to ground or overload detection at the LDO_REF V_{VR}.
3) Detection of over voltage, under voltage or a short to ground at trackers 1 or 2 (V_{VT1} or V_{VT2}).

4) Detection of over voltage, under voltage, a short to ground or thermal shutdown at LDO_COM (V_{VCO}).

5) Detection of under voltage at pre regulator Buck (V_{VOPRE}).

6) Detection of overload at standby LDO (V_{VST}).

7) The window/functional watchdog status counter increases, but actual value still stays below the threshold.

8) The recovery delay time of Error monitoring is active and ERR signal stops toggling.

9) Detection of thermal shutdown warning (Step down pre regulator or/and LDO_µC or/and LDO_COM).

10) Bandgap monitoring: More than 4% deviation occurs between both bandgaps.

Due to microcontroller supplies being switched off in STANDBY and FAILSAFE state, the interrupt on the nINT pin may not be visible. The event is stored in the status flags (IF, SYSSF, MONSF0, MONSF1, MONSF2, OTWRNSF, OTFAIL)

9.4.2 Transition into INIT State

The following failures will bring the device from any state to INIT state:

1) Detection of under voltage at LDO_µC (V_{VUC}).

2) Detection of under voltage at external Buck (V_{VMON}).

3) Detection of under voltage at Standby LDO (V_{VST}).

4) The window/functional watchdog status counter over threshold.

5) Detection of stop of error signal (immediate reaction mode) or stop of error signal detected for more than recovery delay time (recovery mode).

6) The INIT timer expires one or two consecutive times (configuration in INIT state failed).

- **Transition into INIT State Due to UV Fault**

When the voltage of pin VUC, VST or VMON is lower than undervoltage threshold $V_{RT,XXX,low}$ in INIT state, NORMAL state, SLEEP state or WAKE state, the device will switch from current state to INIT state, the nRESET pin is pulled to LOW and all the outputs are enabled (outputs that are disabled in the previous state will also be switched ON again), except for the Standby LDO, which will keep its configuration (ON or OFF). If the time of undervoltage is shorter than the short to ground detection time t_{StG}, the reset delay timer t_{RD} is started as soon as all µC related voltages V_{VUC}, V_{VST} and V_{VMON} are back in the valid range and the nRESET pin will be pulled HIGH after reset delay time.

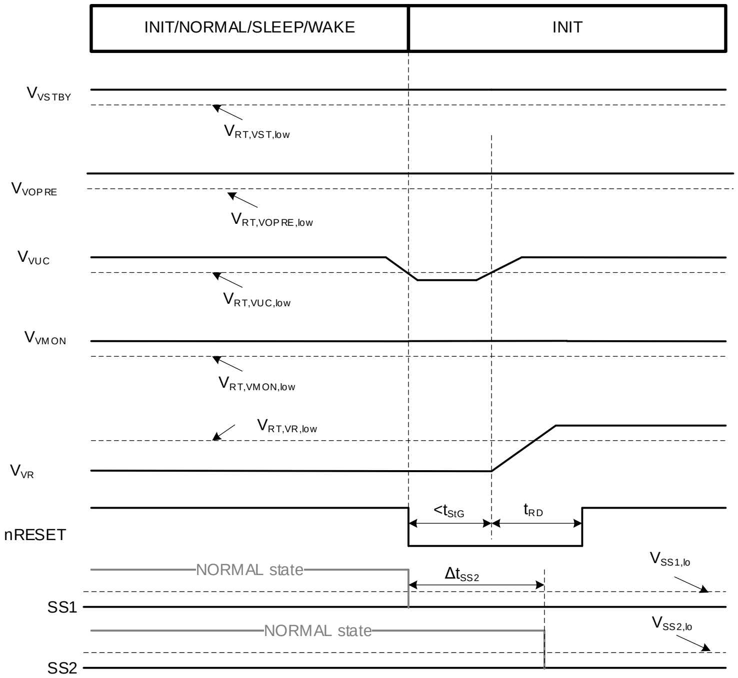


Figure 31. Transition into INIT State Because Of UV Fault

Figure 31 shows one example, with the LDO_REF disabled in current state. When VUC undervoltage is detected, the device moves to INIT state, the power sequence is started when entering INIT state, and the LDO_REF will be re-activated when LDO_UC voltage is higher than the UV threshold.

If the time of undervoltage is longer than the short to ground detection time t_{StG} in INIT state, the device will move into FAILSAFE state.

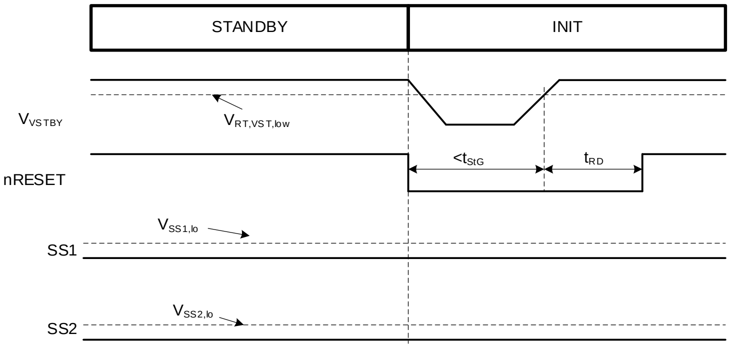


Figure 32. Transition from STANDBY State Into INIT State Because Of VST UV Fault

IN STANDBY state, if the configuration of Standby LDO is ON, when the voltage of pin VST is lower than undervoltage threshold $V_{RT,VST,low}$, the device will switch from STANDBY state to INIT state, the nRESET pin is pulled LOW, and all the outputs are re-activated (outputs that are OFF in the STANDBY state will also be switched ON again), except for the Standby LDO will keep its configuration (ON or OFF). If the time of undervoltage is shorter than the short to ground detection time t_{StG}, the reset delay timer t_{RD} is started as soon as all µC related voltages V_{VUC}, V_{VST} or V_{VMON} are back in the valid range and the nRESET pin will be pulled HIGH after reset time delay. If the time of undervoltage is longer than the short to ground detection time t_{StG} in INIT state, the device will move into FAILSAFE state.

The safe state signals SS1 and SS2 are LOW in STANDBY state and will be LOW in INIT state.

- **Transition into INIT State Due to WD Overflow or ERR Monitor**

If the watchdogs and error monitoring function are in use in INIT state or NORMAL state or SLEEP state or WAKE state, a window watchdog error counter overflow, a functional watchdog error counter overflow or an error indication (immediate or recovery delay time mode) can also cause the device to switch from current state to the INIT state. In this case, the nRESET pin is pulled Low, the reset delay timer t_{RD} starts from the falling edge of nRESET.

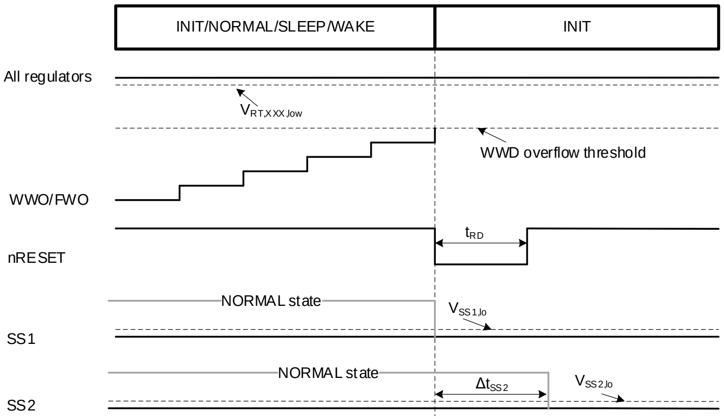


Figure 33. Transition into INIT State Because Of WWD/FWD Error Counter Overflow

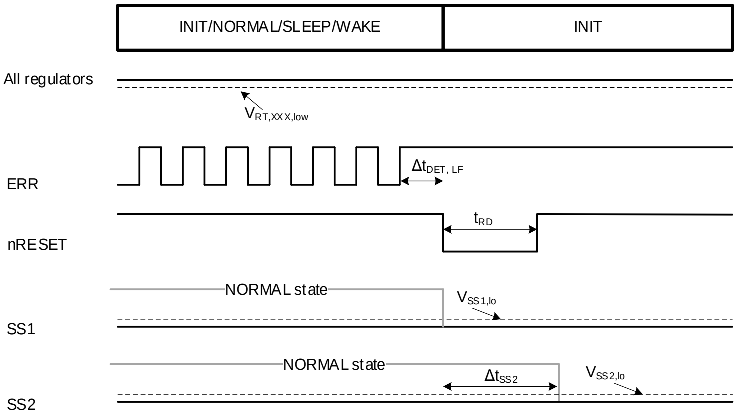


Figure 34. Transition into INIT State Because Of ERR Monitoring Failure (Immediate Mode)

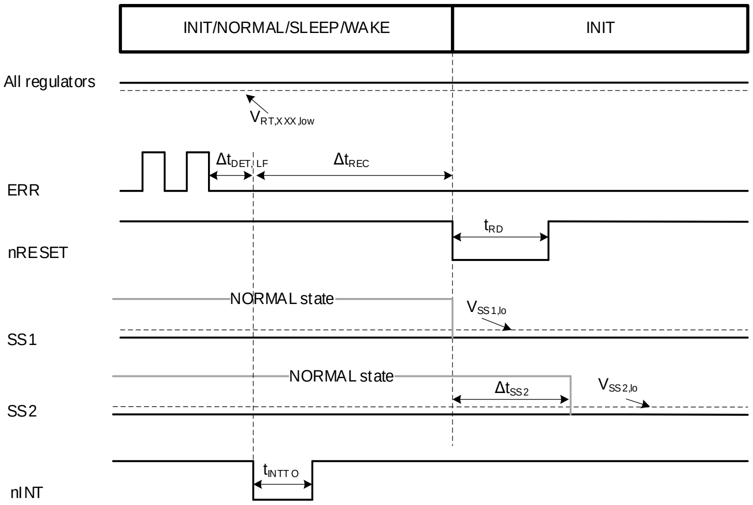


Figure 35. Transition into INIT State Because Of ERR Monitoring Failure (Recovery Mode)

If the current state is NORMAL state, SS1 will be pulled to LOW immediately at the same time with the nRESET pin, and SS2 will be pulled LOW after the selected Δt_{SS2}.

Note: In case of an UV event on VUC, a delayed SS2 signal will follow V_{VUC} as it is supplied from VUC.

In case the device is sent back to NORMAL state before the configured Δt_{SS2} has expired, the SS2 pin will be kept HIGH without being set to LOW.

- **Transition into INIT State Due to First INIT Timer Expired**

During the INIT state, the device needs to communicate effectively with MCU within the INIT timer period to configure WD and ERR monitor properly, otherwise an initialization timeout will occur. If the INIT timer expires, a so-called “Soft Reset” will be issued. The nRESET pin is pulled LOW for the reset delay time t_{RD} in case all MCU related voltages are in the valid range. The power sequence is started after entering the INIT state: the disabled outputs are re-activated, the other ones are kept enabled, except for the Standby LDO, which will keep its configuration (ON or OFF).

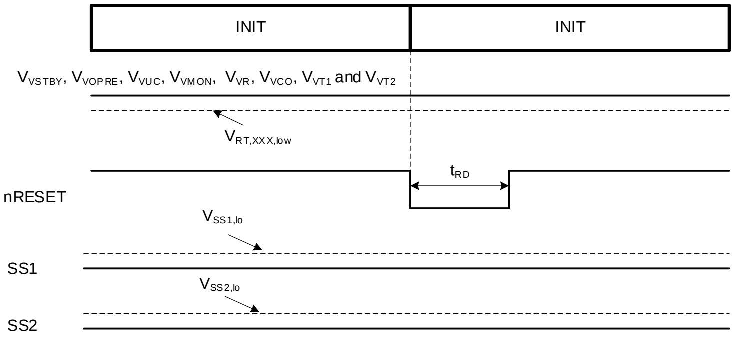


Figure 36. Transition from INIT to INIT State - First Movement

- **Transition into INIT State Due to Second INIT Timer Expired**

If the device transition from INIT to INIT state (or stays in INIT state) for the second time, a “hard reset” is triggered- the nRESET pin is pulled LOW and all outputs are disabled for the time t_{SDT} and restarted according to the power sequencing (Please refer to Chapter “Power Sequencing”), except for the Standby LDO, which will restore its configuration (ON or OFF). The nRESET pin will be released according to the power sequencing using a reset delay time, t_{RD}.

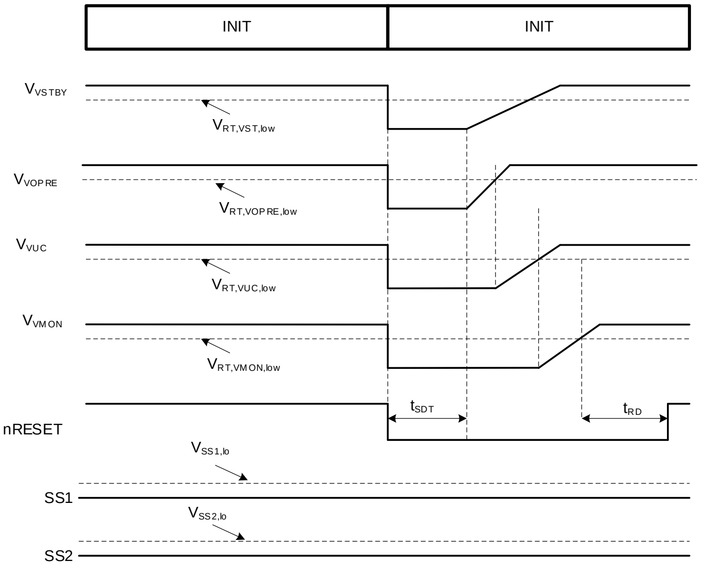


Figure 37. Transition from INIT to INIT State - Second Movement

If the initialization fails for three consecutive times, the device will enter the FAILSAFE state. For details, please refer to the transition from INIT to FAILSAFE state.

9.4.3 Transition into FAILSAFE State

The device will enter the FAILSAFE state when any of the following events occurs:

1) Detection of overvoltage, a short to ground or thermal shutdown at LDO_µC.
2) Detection of overvoltage or a short to ground at External Buck(V_{VMON}).
3) Detection of overvoltage or a short to ground at Standby LDO (V_{VST}).
4) Detection of overvoltage at LDO_REF when Reg36[1]=0 (V_{QVR}).
5) Detection of overvoltage, short to ground or thermal shutdown at pre regulator buck (V_{VOPRE}).
6) Three consecutive initialization failures (e.g., configuration in INIT state failed).
7) A BIAS current monitor failure.
8) An over temperature shutdown due triggered by the monitoring block.
9) A fuse selection monitor failure.
10) An over voltage at the supply pins (VIN) will trigger the overvoltage protection and move the device into FAILSAFE-state (except for STANDBY state).

The above events are called “**Move to Failsafe Faults**”.

- **Move to FAILSAFE State Due to STG Fault**

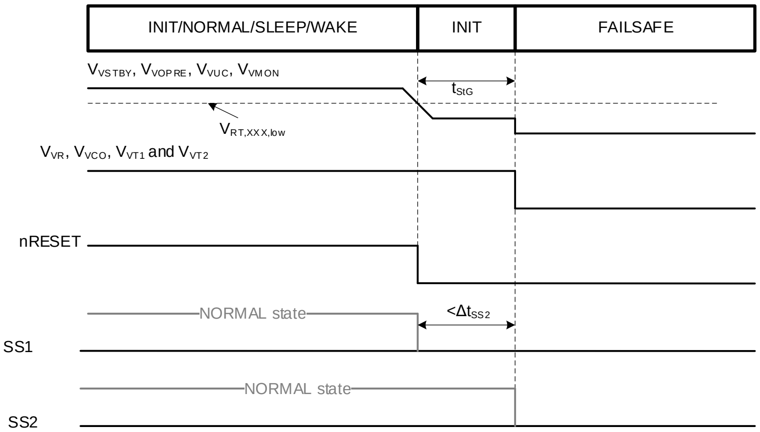


Figure 38. Transition into FAILSAFE State Because of StG Fault

When undervoltage at the MCU related voltages V_{VUC}, V_{VST} or V_{VMON} as shown in the figure is detected, the device will switch from the current state to the INIT state, the nRESET pin will be pulled LOW as soon as an undervoltage at V_{VUC}, V_{VST} or V_{VMON} is detected. The safe state signal SS1 will be pulled LOW at the same time with the falling edge of the nRESET pin. When the time of undervoltage at the MCU related voltages is longer than the short to ground detection time t_{StG}, a short to ground event is detected. As soon as the short to GND is detected, the device moves from INIT state to FAILSAFE state and all regulators will be switched off, regardless if they are in undervoltage condition or not. The safe state signal SS2 will be pulled LOW at the same time with the transition from INIT to FAILSAFE state, even if the delay time Δt_{SS2} has not expired yet, because LDO_µC is switched off (LDO_µC is switched on in INIT state, but switched off in FAILSAFE state).

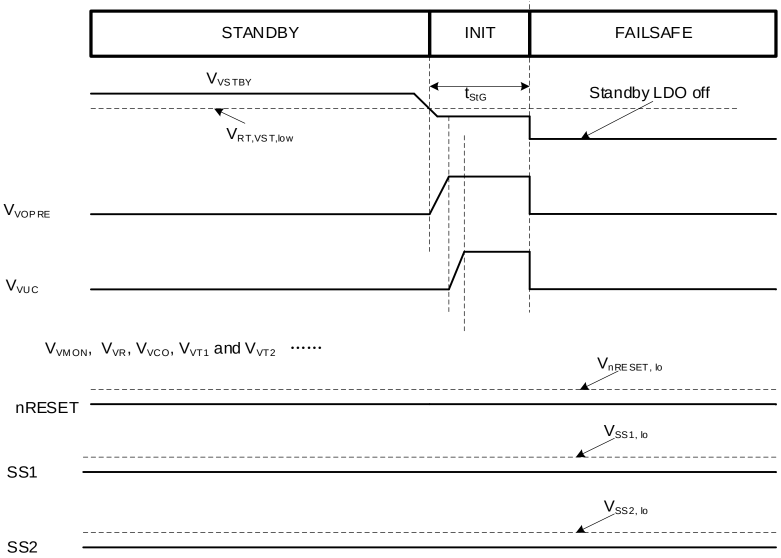


Figure 39. Transition from STANDBY State to FAILSAFE State Because of Standby LDO StG

When undervoltage at Standby LDO V_{VST} in STANDBY state as shown in the figure is detected, the device will switch from the STANDBY state to the INIT state, and the power sequence is started after entering the INIT state: all outputs are re-activated except the Standby LDO. When the time of undervoltage at V_{VST} is longer than the short to ground detection time t_{StG}, the device will move from INIT state to FAILSAFE state and all regulators will be switched off.

- **Move to FAILSAFE State Due to OV Fault**

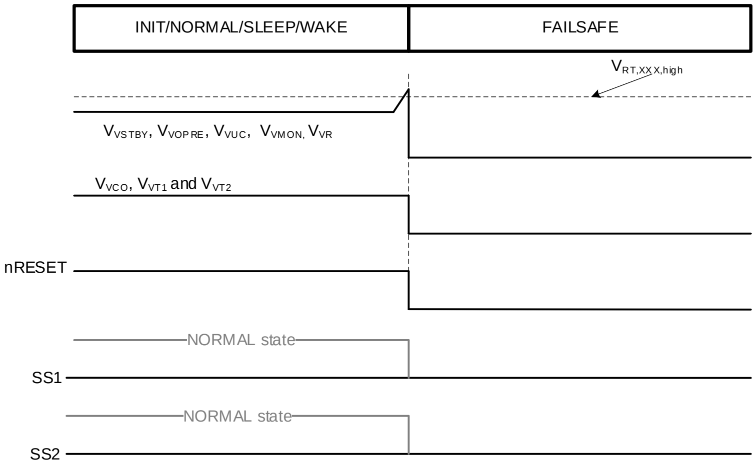


Figure 40. Move to FAILSAFE State Because of OV Fault (Reg36[1]=0)

When overvoltage at V_{VOPRE} or MCU related voltages V_{VUC}, V_{VST}, V_{VMON} or V_{QVR} (Reg36[1]=0) as shown in the figure is detected, the device will initiate the transition from current state to FAILSAFE state. The nRESET pin will be pulled LOW as soon as the overvoltage event is detected (at one or more of the regulators mentioned above - whichever is the first). All regulators will be switched off when the device turns from current state into FAILSAFE state, regardless if they are in overvoltage condition or not. The safe state signals will be pulled LOW immediately with the nRESET pin going low, because the LDO_µC is switched off.

In the STANDBY state, when Standby LDO is ON and overvoltage at Standby LDO V_{VST} is detected, the device will switch from STANDBY state to FAILSAFE state.

- **Transition into FAILSAFE state due to thermal shutdown**

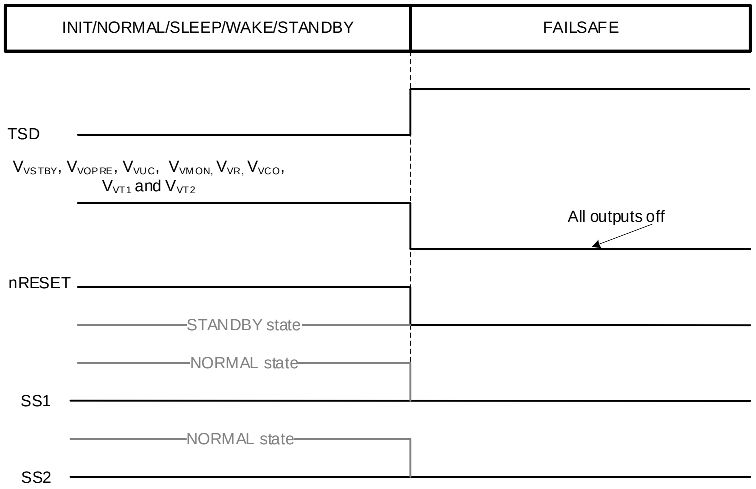


Figure 41.Transition Into to FAILSAFE State Due to Thermal Shutdown

In any state, when a thermal shutdown (TSD) is detected, the device will enter FAILSAFE state. The nRESET pin will be pulled to LOW as soon as the thermal shutdown will be detected. In this case, all regulators will be switched off regardless if they are in overtemperature condition or not. Out of NORMAL state the safe state signals SS1 and SS2 will be pulled LOW immediately at the same time with the nRESET pin going to low, because the LDO_µC is switched off. Out of any other state, the safe state signals SS1 and SS2 are LOW and will stay low.

The device will stay in FAILSAFE state after a thermal shutdown (TSD) for at least for 1 s.

9.4.4 Transition into POWERDOWN State

The following failures/events will bring the device always with highest priority to POWERDOWN state:

1) V_{VS} below $V_{PD,lo,min}$ when decreasing.

2) Detection of over or undervoltage on internal supplies.

10 Analog Built in Self-Test (ABIST) Function

To test certain monitoring functions with the assistance of the external MCU, the SA47301x offers a built-in self-test block.

10.1 Introduction of ABIST

The SA47301x provides error injection to test each comparator by artificially generating undervoltage and overvoltage (or current) conditions to activate a secondary safe shutdown path and generate an interrupt. If an ABIST operation is requested by the MCU, an ABIST global error status will be provided after the ABIST has been performed, whether the ABIST operation is successfully executed/judged by MCU.

The test of the monitoring and safety relevant output functions is run on three different areas in the system:

1) Comparator only: A “comparator only” test can be used to validate the functionality of a comparator and its corresponding deglitching logic. This test is carried out by generating the failure condition for a shorter duration than the deglitching time, neither the secondary safety shutdown path nor the interrupt are triggered by the failure. Only the chosen comparator(s) are tested during this test. If more than one comparator is selected, the test is performed with a fixed sequence of the comparators to be tested. An interrupt indicates that the test has been completed.

2) Comparator and corresponding deglitching logic: The comparator’s operation, including its corresponding deglitching logic and the role to the respective safety measure can be tested. Either the secondary safety shutdown path or the generation of an interrupt is used as a safety measure. This test takes longer to finish than the deglitching time.

3) Safe state or interrupt related comparator: In the third area, while the device provides information about the status for the first and the second ABIST, further microcontroller cooperation is needed. Whether the secondary safety shutdown path has been activated successfully (SS1/SS2 are set low) or an interrupt event has been detected, should be checked by the MCU.

10.1.1 How to Run the ABIST

During ABIST, the MCU needs to service the watchdog(s) and error monitoring depending on the configuration .If the MCU fails to execute, it will result in an assertion of the corresponding interrupt, reset, or safe state output event, which interferes with proper analysis of the ABIST results.

If the deglitching logic is chosen, during a performed ABIST, flag registers (SYSFAIL, INITERR, IF) and status registers (MONSF1, MONSF2, MONSF3) are triggered and updated by out-of-range conditions caused by the ABIST functionality. If the deglitching logic is not chosen, during a performed ABIST, only flag registers (SYSFAIL, IF) will be updated.

If a fault event ("move to INIT" failures) is part of the logic which is affected by the ABIST control, the assertion of nRESET will be blocked when the ABIST is performed by internal hardware and the state machine will not change its state. The device will transition from NORMAL to WAKE state if an ABIST contributing to the secondary safety shutdown path is started in NORMAL state and the deglitching logic is chosen. In addition, any out-of-range detection caused by ABIST itself does not affect the output voltage, and all voltages will be kept enabled.

Testing for a single function is performed as follows:

1) **Enable the comparator that needs to be tested:** configurable LDO's (LDO_REF, LDO_COM, tracker 1/2) need to be enabled if their comparators are selected to be tested. On the other hand, the ABIST test on a comparator which is not used by the system is not required to be performed.

2) **Select comparator for ABIST operation:** Select the comparator to perform the ABIST test by setting the corresponding registers (ABIST_SELECT0, ABIST_SELECT1, and ABIST_SELECT2). For this selection it is necessary to differentiate by the contribution to the different safety measure.

3) **Configure the register ABIST_CTRL0 according to the tested function:** the configuration consists of the tested safety measure (safe state related comparators or interrupt related comparators), the tested area/coverage by the ABIST (corresponding deglitching logic is chosen or not) and the configuration of a sequence or single comparator to be tested.

4) **Start ABIST operation:** The MCU shall set the global ABIST start bit to start the ABIST.

5) **The MCU reads the status of the global ABIST start bit:** If this bit is still set, the ABIST function is not completed. If the bit is cleared and an interrupt event is generated, the selected ABIST operation is completed.

6) **The MCU reads the status of the Select Registers:** Once a successful ABIST operation is performed on the particular comparator, each bit which has been set to select the test of a dedicated comparator (ABIST_SELECT0, ABIST_SELECT1 and ABIST_SELECT2) will be cleared. If the ABIST operation on the particular comparator failed, each bit which has been set to select the test of a dedicated comparator will be kept unchanged. Then, the ABIST status information can show a failing ABIST operation and the MCU can determine which comparator failed during the test.

Safety measures are divided into two categories:

1) Secondary Safety Shutdown Path: LDO_UC OV, LDO_UC UV, external buck OV, external buck UV, LDO_STBY OV, LDO_STBY UV, LDO_REF OV when Reg36[1] =0, Pre buck OV, Bias current low/high, VIN OV, internal supply OV (internal supply comparator must be tested only by "comparator only" test).

2) Interrupt: LDO_REF OV when Reg36[1] =1, LDO_REF UV, Tracker 1/2 OV, Tracker 1/2 UV, LDO_COM OV, LDO_COM UV, Pre buck UV, BG OV, BG UV.

10.1.2 Testing the Comparator Logic Only

During the ABIST operation the comparators are triggered by the ABIST controller for a time shorter than the internal deglitching time t_{rr} (reset reaction time). An out-of-range condition will be signaled by the properly operating comparator when the failure condition is applied.

According to the expected value, the provided information of each comparator will be checked. ABIST controller considers it as a passing test if the comparator output value matches the expected value, and any of the provided output values do not match the expected value, it will be considered as a failing test. The register ABIST_CTRL0 is used to store the general result of the ABIST and the registers ABIST_SELECT0, ABIST_SELECT1 and ABIST_SELECT2 are used to store the detailed result for each selected comparator. After the test is finished, if the previously selected bits are reset, the test is considered as pass. The still set bits indicates the failing comparator(s) that makes the overall STATUS to signal a failure.

Table 11. Accordingly the Maximum Selection When Comparator Logic Only

	Secondary Safety Shutdown Path (SS1/2) Related			**Interrupt (nINT) Related**		
	ABIST_ SELECT0	ABIST_ SELECT1	ABIST_ SELECT2	ABIST_ SELECT0	ABIST_ SELECT1	ABIST_ SELECT2
	$2F_H$ when Reg36[1] =0 $0F_H$ when Reg36[1] =1	$0E_H$	$C9_H$	$D0_H$ when Reg36[1] =0 $F0_H$ when Reg36[1] =1	$F1_H$	30_H
ABIST_CTRL0	01_H			09_H		

This type of ABIST can be performed in the INIT, NORMAL and WAKE states. The secondary safety shutdown path SS1/2 will not react if the ABIST is successful and only an interrupt is generated due to the finished ABIST (IF.ABIST set and IF.MON not set, considering cleared interrupt flags prior to the ABIST and no real failure events during the ABIST).

10.1.3 Testing the Comparator Logic and the Corresponding Deglitching Logic

During the ABIST operation the comparators are triggered by the ABIST controller for a time longer than the internal deglitching time trr (reset reaction time). An out-of-range condition will be signaled by the properly operating comparator when the failure condition is applied. The deglitching logic will forward the failure trigger after a trr delay and makes the device react to the recognized failure event. This reaction consists of storage of the respective monitoring failure flags as well triggering of the respective output function, which is either the interrupt INT or the secondary safety shutdown path SS1/2. The reaction of the safe state outputs SS1/2 can only be observed in case the test is started in NORMAL state.

In addition, according to the expected value, the provided information of each comparator will be checked. ABIST controller considers it as a passing test if the comparator output value matches the expected value, and if any of the provided output values do not match the expected value, it will be considered as a failing test. The register ABIST_CTRL0 is used to store the general result of the ABIST and the registers ABIST_SELECT0, ABIST_SELECT1 and ABIST_SELECT2 are used to store the detailed result for each selected comparator. After the test is finished, if the previously selected bits are reset, it can be considered as pass. The still set bit indicates the failing comparator(s), that makes the overall STATUS to be failed.

In addition to the results read from the ABIST controller related registers, the microcontroller must also read the results provided by the failure/interrupt flags (SYSFAIL, INITERR and IF) and monitoring status flags (MONSF1, MONSF2 or MONSF3), and check against the expected results based on the configuration set before the start of the ABIST.

INTOV located in register ABIST_SELECT2 cannot be tested in this way, testing of the comparator logic only is possible.

Table 12. Accordingly the Maximum Selection When Deglitching Logic Is Chosen

	Secondary Safety Shutdown Path (SS1/2) Related			Interrupt (nINT) related		
	ABIST_SELECT0	ABIST_SELECT1	ABIST_SELECT2	ABIST_SELECT0	ABIST_SELECT1	ABIST_SELECT2
	2F$_H$ when Reg36[1] =0 0F$_H$ when Reg36[1] =1	0E	C1	D0$_H$ when Reg36[1] =0 F0$_H$ when Reg36[1] =1	F1	30
ABIST_CTRL0	03$_H$			0B$_H$		

The analysis based on the largest possible selection will include what is shown in the table:

Table 13. Monitor Status When Deglitching Logic Is Chosen

	Secondary Safety Shutdown Path (SS1/2) Related	Interrupt (INT) Related
IF	40$_H$	48$_H$
INTTERR	04$_H$	00$_H$
SYSFAIL	04$_H$	00$_H$
MONSF1	2F$_H$ when Reg36[1] =0 0F$_H$ when Reg36[1] =1	D0$_H$ when Reg36[1] =0 F0$_H$ when Reg36[1] =1
MONSF2	0E$_H$	F1$_H$
MONSF3	C1$_H$	30$_H$

This type of ABIST can be performed in the INIT, NORMAL and WAKE states. If this test is run in NORMAL state on comparators contributing to the secondary safety shutdown path, the device will switch low the safe state outputs SS1/2 and the State Machine will move to WAKE state, without triggering a reset nRESET.

It must be considered that only the first comparator in the sequence will be covered when testing the complete monitoring chain until the respective output (SS1/2 or nINT) are triggered. The contribution to activation of the secondary safety shutdown path cannot be tested when this test is run in INIT or WAKE states. The system is in a safe state already and the secondary safety shutdown path is already activated. Both the proper behavior of the secondary shutdown path and the interrupt signal needs to be checked by the MCU.

10.1.4 Testing the Complete Monitoring Chain (Comparators, Deglitching and Output)

The SA47301x classifies the testing of the complete monitoring chain from the comparator till the respective output function into two categories according to the level of failure:

1) The secondary safety shutdown path called SS1/2 for severe microcontroller related failure events.

   The SA47301x should test the functionality of the secondary safety shutdown path in NORMAL state. To ensure that the SA47301x is in the NORMAL state, the MCU should check that the secondary shutdown path has been de-activated successfully (SS1/2 high).

   To test whether each comparator activates the secondary safety shutdown path, a single comparator should be selected in the NORMAL state. The configuration process is shown below:

   - **Comparator selection:** A single (x) bit has to be set for a corresponding comparator in registers ABIST_SELECT0 (00x0xxxx$_B$ when Reg36[1] =0 or 0000xxxx$_B$ when Reg36[1] =1), ABIST_SELECT1 (0000xxx0$_B$) or ABIST_SELECT2 (xx00000x$_B$).
   - **ABIST control selection:** A single comparator ABIST operation on the full path of the secondary safety shutdown path needs to be started (register ABIST_CTRL0: 00000111$_B$, safe state related comparators/Single comparator test/Comparator and corresponding deglitching logic).
   - **Analysis of test results:** The device will autonomously enter the WAKE state and generate an interrupt event when the requested ABIST operation is completed and the secondary safety shutdown path is activated (SS1/2 low; if SS2 delay is enabled, this delay will be applied when the ABIST operation is performed). The interrupt event indicates the completion of the ABIST and will be stored in register IF.ABIST. In addition, the respective

monitoring failure flag for the selected comparator will be set (either INITERR.VMONF for “Move to INIT State” failures or SYSFAIL.VMONF for “Move to FAILSAFE State” failures) which has to be checked and cleared by the MCU. Also, the status of the requested ABIST operation (ABIST_CTRL0.STATUS), the respective monitoring status flag (MONSF1, MONSF2 or MONSF3) to be set according to the previous selection and ABIST_SELECT0, ABIST_SELECT1 and ABIST_SELECT2 bits need to be checked by the MCU that they are not set .

2) The interrupt function nINT for peripheral related failure events in terms of voltage and current monitoring. The test of the generation of an interrupt event can be done in the INIT, NORMAL and WAKE states. It is recommended to have the application in safe state (INIT or WAKE state). The test configuration steps are shown below:

- **Comparator selection:** A single bit (‘x’) has to be set for a corresponding comparator in registers ABIST_SELECT0 (xx0x0000$_B$ when Reg36[1] =0 or xxxx0000$_B$ when Reg36[1] =1), ABIST_SELECT1 (xxxx000x$_B$) or ABIST_SELECT2 (00xx0000$_B$).
- **ABIST control selection:** A single comparator ABIST operation on the full path of the interrupt needs to be started (register ABIST_CTRL0: 00001111B, interrupt related comparators/ Single comparator test/ Comparator and corresponding deglitching logic).
- **Analysis of test results:** The artificial failure, triggered by the ABIST controller, on the selected comparator will generate an interrupt (INT) event. It is the responsibility of the MCU to check the generation of this interrupt event on the triggered failure. As this is a test of the generation of an interrupt based on a failure event, there is no dedicated ABIST completion event, nor the ABIST bit in the interrupt flags will be set. Accordingly, it is recommended to store the information about the started ABIST in the firmware. After the interrupt has been generated the interrupt flag register shall be checked for the monitoring bit (IF.MON) set and the ABIST completion bit (IF.ABIST) not set. The MCU also needs to read and check the status of the requested ABIST operation (ABIST_CTRL0.STATUS), the respective monitoring status flag (MONSF1, MONSF2 or MONSF3) to be set according to the previous selection and ABIST_SELECT0, ABIST_SELECT1 and ABIST_SELECT2 bits to be cleared.

10.1.5 Abort Conditions for ABIST Operation

If a severe monitoring failure event that contributes to the secondary safety shutdown path is detected on a unselected comparator or a severe failure event not related to the voltage or bias current monitoring function occurs during the an ABIST operation on the comparators only (ABIST_CTRL0.PATH not set), the device will react as it is supposed to do in normal operation. Accordingly, the monitoring, reset and safe state control are reacting, bringing the device into safe state and trigger the State Machine to move into FAILSAFE or INIT state. In this situation, the ABIST is aborted.

When an ABIST operation is performed on the full path (ABIST_CTRL0.PATH set), the comparators for voltage and bias current monitoring are blind for the duration of the ABIST operation. Therefore, it is recommended to do the test in safe state unless it is needed to start the test in NORMAL state. If the severe failure events unrelated to the voltage and bias current monitoring occurs, the device will be triggered to react in the same way as in usual condition, bringing the device into safe state and trigger the State Machine to move into FAILSAFE or INIT state. In this situation, the ABIST is aborted.

The SA47301x stores the ABIST abort event in the register SYSFAIL.ABISTERR. The artificial failure events that have been generated until the abort of the ABIST due to the detected real failure, will be stored as well in the monitoring registers.

10.2 Logic Built in Self-Test

Any tests related to digital logic in the SA47301x are performed by MCU, and there is no dedicated built-in self-test function for digital logic. FWD/WWD and ERR monitoring blocks can be tested by the MCU.

In order to verify correct functionality of these blocks and to check their contribution to nRESET or nINT and finally SS1/2 outputs, the MCU shall generate an error condition on the particular block and check for the occurrence of the expected system behavior.

1) **WWD/FWD**: For the watchdog function, this basically means stopping triggering the WD(s) and/or generating false trigger events. Interrupt will be generated and even assert the reset. The secondary safety shutdown path will be

activated, the MCU will be reset and the device will move into INIT state. This test can only be performed after the device enters the NORMAL state for verifying the activation of the secondary shutdown path.

2) **Error monitoring**: For the error monitoring block, the MCU needs to stop generating the signal connected to the ERR pin for observing the required system behavior. Whether to use error recovery mechanism depends on MCU.

11 MCU Program and Debug Mode Support

The MCU may be not enabled to offer correct watchdog or error monitor signal when it is under programming or debugging mode. To avoid the periodical resetting to the MCU in the program or debug mode, the PROG pin and PROG bit (0x3C[7]) can be used.

The SA47301x enters the MCU program mode if:

1) PROG pin is pull high or

2) PROG bit (0x3C[7]) is written to 1 using the SPI interface

If the device is in MCU program mode, then

1) The initialization timer is stopped

2) The nRESET pin will not be pulled low if the window watchdog counter overflow happens.

3) The nRESET pin will not be pulled low if the functional watchdog counter overflow happens

4) The nRESET pin will not be pulled low if the error monitor fault happens

Only the four above mentioned functions are disabled when device is in MCU program mode. All other functions including the state machine, the interrupt and the safe state control are not affected. Invalid watchdog service or invalid ERR signal will still generate interrupts. The device will still switch to INIT state if a watchdog counter overflow happens or if an error monitor fault is detected. The SS1/SS2 pin will be pulled low but the nRESET pin will stay high. This mode can be used for fault injection tests for the watchdog and error monitor functions. The MCU shall offer correct watchdog and error monitor signals or disable the related functions before exiting the MCU program mode.

12 Interrupt Generation

The device integrates a dedicated interrupt generation block that handles requests from independent sources to generate interrupts. The different interrupt sources are shown below:

1) State machine:

   - A requested state transition has not been performed successfully, e.g., a valid ENA (edge) or WAK (level) signal is detected in the transition state to SLEEP state or unable to enter SLEEP state due to LDO_µC current consumption above the selected threshold level and so on.
   - A requested state transition from SLEEP has been performed successfully, i.e., the device successfully entered WAKE state. The MCU may only send (additional) SPI commands after an interrupt event has been generated by the system. The interrupt event is to inform the MCU that a state transition has been successfully executed and the system is able to perform SPI communication at full SPI speed.

2) Watchdog, if the Watchdog doesn’t receive the correct service and is not configured in a way to allow service errors to occur, an interrupt request will be generated. i.e. an error counter threshold value of more than 2 is configured. In this case an interrupt is generated only if the error counter threshold is not exceeded due to this error.

3) Error pin monitoring, if the error pin monitoring block detects an error and is configured in a way to allow occurrence of this error for a certain amount of time (recovery delay action enabled), an interrupt request will be generated. If the error pin monitoring detects an error and the recovery delay has not expired, an interrupt is requested.

4) Monitoring Block, an interrupt request is generated based on the defined system reaction described in Chapter “Reaction on detected faults”.

5) Overtemperature warnings and overtemperature shutdown of LDO_REF, thermal warning of pre regulator buck.

6) Overcurrent conditions of LDO_REF or standby LDO.

7) SPI block in case an SPI error has occurred.

8) Double bit error in the protected configuration.

9) ABIST Done.

The interrupt signal generated by SA47301x is used to inform the host MCU that a non-severe system condition has occurred. In this case, the MCU performs the proper action based on the interrupt source. The interrupt output (pin nINT) is high by default. All internal interrupt sources are enabled by default and cannot be disabled.

After an internal interrupt condition occurs, an interrupt is signaled by pulling pin nINT low for at least t_{INT} (interrupt min. pulse width). After the t_{INT} time has elapsed, pin INT will be driven high if all IF register flag(s) has/have been cleared via SPI operation or t_{INTTO} has expired.

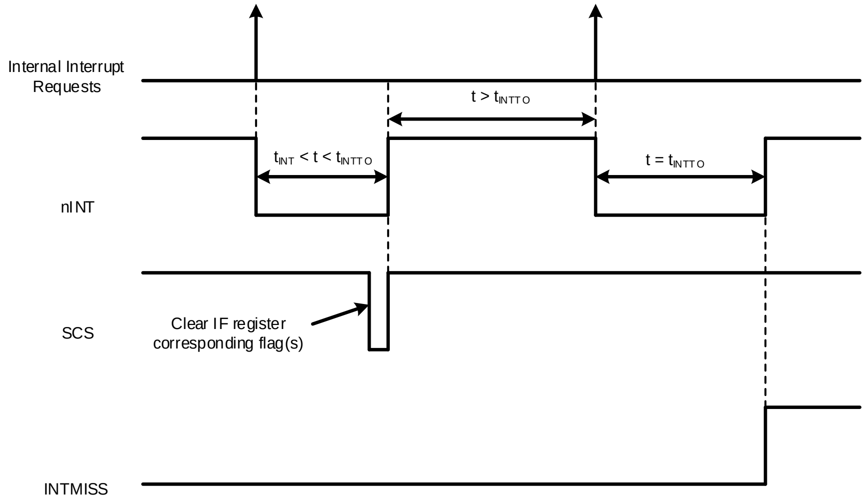


Figure 42. Interrupt Timing

Case1: If an interrupt signal is generated by pulling nINT low and the MCU has not cleared all interrupt status flags within t_{INTTO}, the nINT will remain low until t_{INTTO} expires, but no additional interrupts will be generated. Information about a pending interrupt event can be derived via the INTMISS status flag. This status flag is cleared each time the interrupt line is driven low.

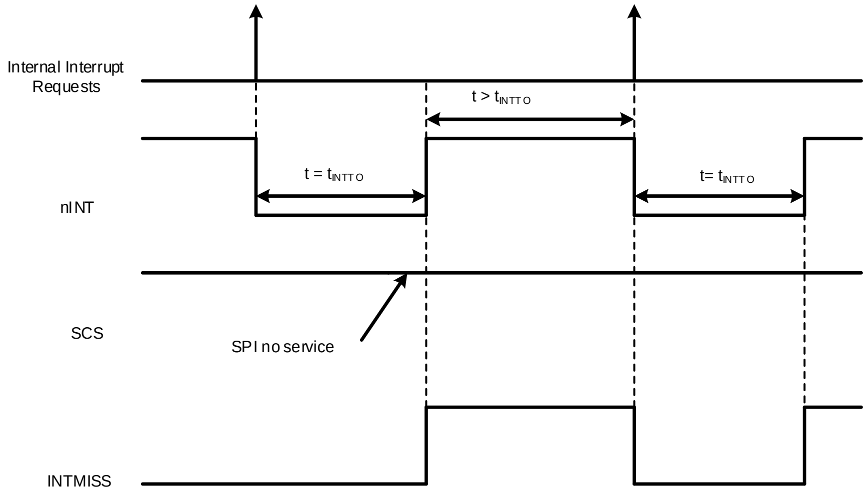


Figure 43. SPI No Service

Case2: If an interrupt is signaled by pulling nINT low and an additional bit is set in the IF register interrupt flag after the interrupt bits have been read by the MCU and this outdated information is used to clear the interrupt flags, the interrupt line will stay low until t_{INTTO} expires, but no additional interrupt will be generated. Information about a pending interrupt event can be derived via a status flag.

Case3: After releasing the interrupt line to high, the interrupt line will stay high for at least t_{INTTO} regardless of any additional internal interrupt conditions occurring. If a new interrupt event occurs during the delay timeout (t_{INTTO}), this will be signaled by generating a new pulse after the delay timeout t_{INTTO}.

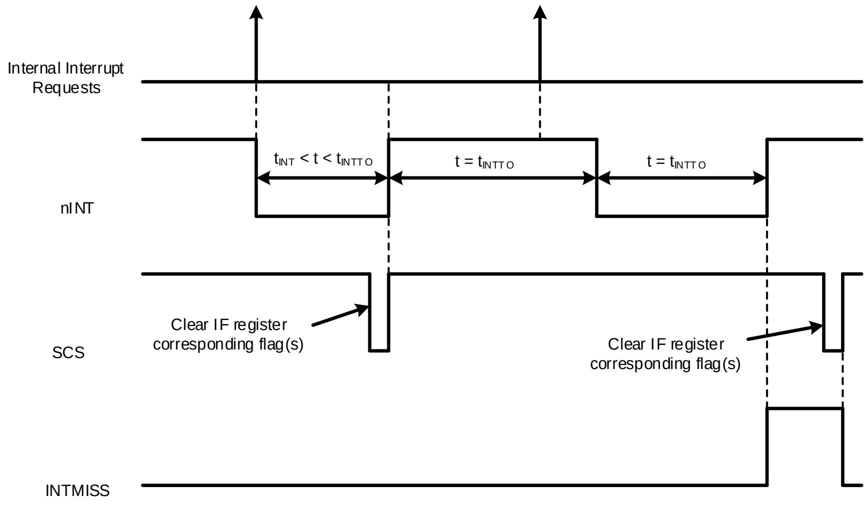


Figure 44. Interrupt Timing without Service in Time

All interrupt sources can only be cleared by a “write-1-to-clear” (w1c) SPI operation, i.e., writing a logic one to the corresponding bit(s) in the interrupt register will clear the event.

When interrupt events occur, the status flags and interrupt flag will be set to “1”. The interrupt flag provides information about different groups of interrupt events, while status flags provide detailed information about which particular event(s) generated the interrupt. To service an interrupt, one would only need to write the interrupt flag register (IF). The status flag registers are only meant to provide detailed information. However, all status flags can be cleared as well.

13 Window Watchdog and Functional Watchdog

13.1 Introduction

The SA47301x integrates two independent types of watchdogs:

1) An independent window watchdog (WWD) with selectable input trigger signal (pin WDI toggling or SPI command to WWDSCMD register).

2) An independent functional watchdog (FWD) operating in question-and-answer mode.

WWD and FWD have independent monitoring mechanisms, including independent timers and independent error counters, which allows both watchdog types to be used in parallel.

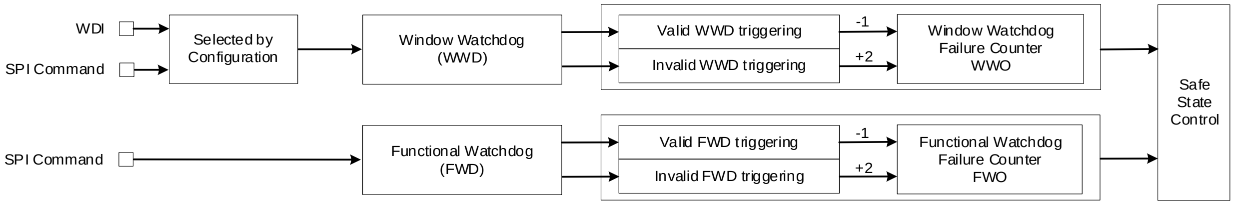


Figure 45. Window Watchdog and Functional Watchdog

The window watchdog and function watchdog are asynchronous, they are independent of each other and can be activated or deactivated separately. The results of the watchdogs (“Valid triggering” or “Invalid triggering”) are monitored independently by the related watchdog error counters:

1) The status of the window watchdog is WWO which is stored in status register “Register 0x29”;

2) The status of the functional watchdog is FWO, which is stored in status register “Register 0x2A”.

When the value of the error counter (WWO or FWO) is equal or higher than the programed threshold, the device will enter safe state. For better understanding, please refer to chapter safe state control for more details.

13.2 Window Watchdog

13.2.1 Principle of Operation and Configuration

The SA47301x integrates a window watchdog for monitoring the MCU firmware, which has to provide periodical triggering within the $T_{WWD,MARGIN}$. Depending on the configuration of the WWDTSEL bit “Register 0x06[1]”, a trigger can be configured as a falling edge on the WDI pin or be written to the register WWDSCMD “Register 0x17” using an SPI command. For the convenience of elaboration, in the watchdog function, define falling edge at the WDI pin and writing to the register WWDSCMD “Register 0x17” using an SPI command (Read Reg0x17[7] first and write the inverted value to Reg0x17[0]) as “Trigger”.

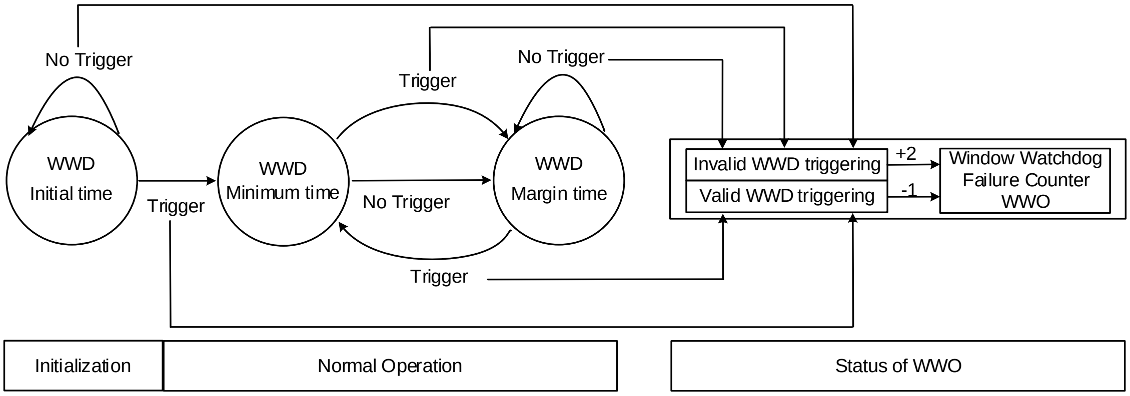


Figure 46. Watchdog State Diagram

“Trigger” within the $T_{WWD,INIT}$ and $T_{WWD,MARGIN}$ are considered as “Valid WWD Triggering”, in case of a “Valid WWD Triggering”, the timing of $T_{WWD,INIT}$ or $T_{WWD,MARGIN}$ was terminated and the timing of $T_{WWD,MIN}$ is started. "Trigger" within WWD initial timer $T_{WWD,MIN}$ or "No Trigger" within WWD margin timer $T_{WWD,MARGIN}$ is considered as "Invalid WWD Triggering". In case of a “Invalid WWD Triggering”, the watchdog output indicates an “Invalid WWD triggering” to the WWD failure counter and a new $T_{WWD,MARGIN}$ timer is started. "No Trigger" within $T_{WWD,INIT}$ is also considered as "Invalid WWD Triggering"; in this case, the watchdog opens again a WWD initial time.

If the microcontroller does not operate as expected, i.e., the microcontroller does not have the ability to trigger the watchdog with the correct timing, then the SA47301x will notify the microcontroller.

In INIT, NORMAL and WAKE state, the following parameters of the window watchdog can be configured using SPI commands:

1) Watchdog trigger selection: External pin WDI toggling or triggering via SPI command (register WWDSCMD). The default configuration is triggering via SPI.

2) The length of $T_{WD,MARGIN}$ and $T_{WD,MIN}$ configuration: Programed according to the application needs by SPI (Combination of cycle time WDCYC, WDCYCDIV and number of cycles for margin time and minimum time).

3) Window watchdog error counter overflow threshold (register 0x06 [7:4]).

13.2.2 Initialization

In the INIT state, when pin nRESET changes from low to high, the window watchdog is activated by default and the timing of $T_{WWD,INIT}$ (typ: 600ms) is started. During the $T_{WWD,INIT}$, the window watchdog expects a “Valid WWD Triggering” through SPI command by default, i.e., the device will ignore any signal to the watchdog trigger pin WDI. The SPI command is used as the default trigger mode to avoid the false triggering at the WDI pin during startup and initialization. During $T_{WWD,INIT}$, the microcontroller can change the configuration of the window watchdog such as the trigger selection, the timing of $T_{WWD,MIN}$ and $T_{WWD,MARGIN}$ and so on. If the microcontroller has reconfigured the watchdog via SPI commands, the window watchdog will restart with the new configuration, and the timing of $T_{WWD,MARGIN}$ will be started accordingly, expecting a valid trigger via the selected trigger input.

If a “Valid WWD Trigger” is not received when the system INIT timer expires, a so-called “Soft Reset” will be generated because of the first initialization failure. After the “Soft-Reset”, a new $T_{WWD,INIT}$ timer will be started by the window watchdog. Initialization failure is not indicated by interrupt and nRESET will be pulled low to indicate this event, and repetition of $T_{WWD,INIT}$ is limited. If the window watchdog is not correctly triggered during the second $T_{WWD,INIT}$, a "Hard-Reset" will occur because of the second initialization failure, which means that pin nRESET goes to low , all regulators except LDO_STBY will be turned off and the power sequence will be restarted after a delay of t_{SDT}. If there is no valid trigger after the third consecutive $T_{WWD,INIT}$, the state machine will start the transition to the "FAILSAFE" state.

13.2.3 Normal Operation

The window watchdog enters normal watchdog operation when any of the following events are met:

1) A “valid WWD trigger” is received during initial time. This event will terminate the timing of $T_{WWD,INIT}$ and start the timing of $T_{WWD,MIN}$.
2) Window watchdog is re-enabled after initial time. This event will start the timing of $T_{WWD,MARGIN}$ immediately.

In normal operation, the watchdog operates to cycle between the $T_{WWD,MARGIN}$ timer and $T_{WWD,MIN}$ timer.

Minimum time to margin time: If no trigger during minimum time, the time of $T_{WWD,MIN}$ is fixed and the timing of $T_{WWD,MARGIN}$ will automatically start when minimum time expires. An invalid WWD trigger within the $T_{WWD,MIN}$ will immediately terminate the timing of minimum time and start the timing of margin time. The window watchdog failure counter will be incremented by two when an invalid WWD trigger is detected and an interrupt will be generated to indicate this event.

Margin time to minimum time: After $T_{WWD,MIN}$ has ended or WWD is re-enabled by SPI command, the window watchdog starts the timing of $T_{WWD,MARGIN}$. A valid WWD triggering is expected within the $T_{WWD,MARGIN}$. If a valid trigger signal is received within the $T_{WWD,MARGIN}$, the watchdog terminates timing $T_{WWD,MARGIN}$ and starts the timing of $T_{WWD,MIN}$. The window watchdog failure counter will be decremented by one in case it is greater than zero when a valid WWD trigger is detected and no interrupt is generated to indicate this valid WWD triggering.

Margin time to margin time: The window watchdog will be incremented by two when no WWD trigger is received during margin time. A new $T_{WWD,MARGIN}$ timer cycle will be started after the current margin time expires and an interrupt will be generated to indicate the event.

13.2.4 Window Watchdog Trigger Signal at Pin WDI

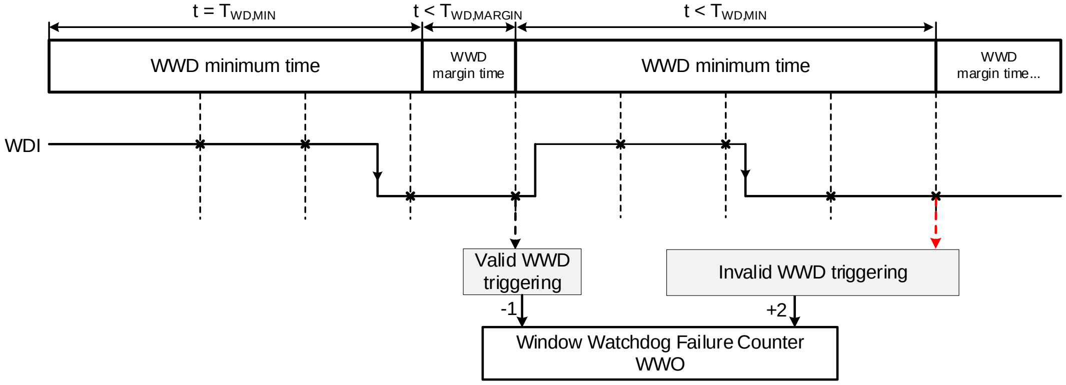
The watchdog input pin WDI integrates a pull-down current source I_{WDI}. The watchdog input WDI can transition to high within the $T_{WWD,MIN}$ or during the following $T_{WWD,MARGIN}$.

Watchdog input WDI is sampled periodically using T_{SAM} (Typ:200µs) period. The falling edge from the high level($V_{WDI,high}$)to the low level ($V_{WDI,low}$) is considered as a valid trigger. To improve immunity against noise or glitches on the WDI input, a valid trigger signal requires at least two high samples, followed by two low samples, which are considered valid when measured as low signal at the second consecutive sampling point. Figure 47 shows several critical cases.

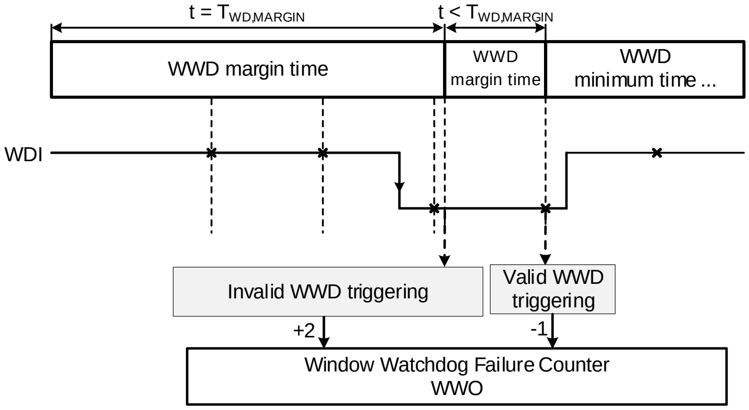
Valid WWD triggering within margin time: When the first three samples (two high one low) of the trigger pulse at pin WDI are inside the $T_{WWD,MIN}$ and only the fourth sample (the second low sample) is inside the $T_{WWD,MARGIN}$, then a “valid WWD triggering” will be detected.

Invalid WWD triggering within minimum time: When four consecutive samples (two high two low) of the trigger pulse at the WDI pin are inside the $T_{WWD,MIN}$, then an “invalid WWD triggering” is detected.

Invalid WWD triggering within margin time: When the first three samples (two high one low) of the trigger pulse at the WDI pin are inside the $T_{WWD,MARGIN}$, and the margin time expires before the fourth sample, then an “invalid WWD trigger” will be detected when the margin time expires and a “valid WWD triggering” will be detected when the fourth sample is detected.



a) *Valid Triggering within $T_{WWD,MARGIN}$ and Invalid Triggering within $T_{WWD,MIN}$*



b) *Invalid Triggering within $T_{WWD,MARGIN}$*

Figure 47. Valid and Invalid Trigger Pulses at Pin WDI

13.2.5 Timing Diagrams

Correct Timing

If the reset output (nRESET pin) (monitoring the microcontroller related voltages) turned high, the timing of $T_{WWD,INIT}$ will be started in INIT state. A valid trigger of the WWD according to the configured trigger selection is expected during the $T_{WWD,INIT}$. The maximum time of the $T_{WWD,INIT}$ is fixed, but it will be terminated as soon as a “Valid WWD trigger” is recognized.

The window watchdog will start timing the $T_{WWD,MIN}$ when a “Valid WWD triggering” has been detected during the $T_{WWD,INIT}$. The $T_{WWD,MIN}$ has a fixed duration that can be determined by SPI command. It starts right after the valid trigger signal, which stops timing $T_{WWD,MARGIN}$ and $T_{WWD,INIT}$. During the $T_{WWD,MIN}$ no trigger signal should be applied. A transition from low to high at the WDI pin is not detected and will not lead to a trigger event,

When a “Valid WWD trigger” signal is detected, the timing of $T_{WWD,MARGIN}$ will be immediately terminated, so the time of the $T_{WWD,MARGIN}$ is variable and depends on the time the microcontrollers schedules the trigger.

If the window watchdog was deactivated in SLEEP state and was active in previous NORMAL state, , the first $T_{WWD,MARGIN}$ timer will start and be indicated by an interrupt at pin INT when the device switches from SLEEP state to WAKE state. The time of the first $T_{WWD,MARGIN}$ timer depends on the configured cycle time.

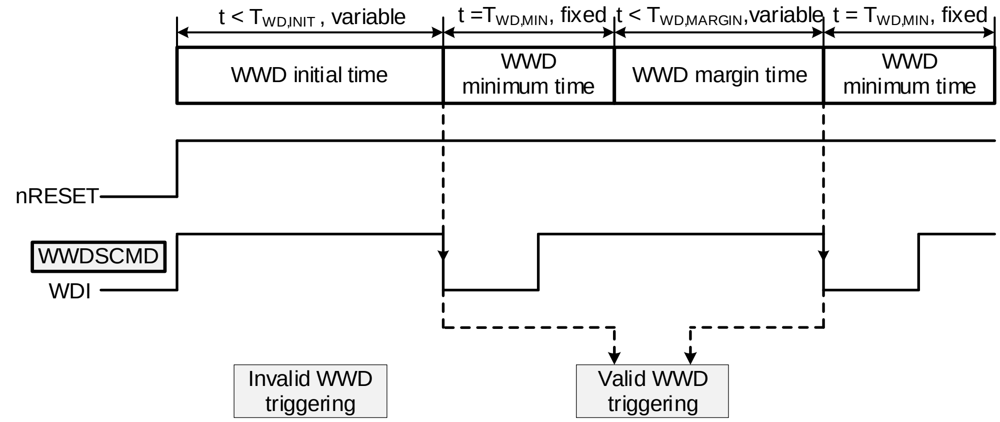


Figure 48. Normal Operation: Correct Triggering

Incorrect Timing: No Trigger within Initial Time

Due to the same typ. length of system initialization timeout T_{INT} as the $T_{WWD,INIT}$, this usually lead to the initialization timeout being finished slightly before or at same time as $T_{WWD,INIT}$ timing, which would skip the interrupt event. Two different situations have to be considered:

1) The maximum time of T_{INT} is longer than the maximum time of the $T_{WWD,INIT}$. In this case, if a valid trigger is not detected within the $T_{WWD,INIT}$, it might lead to an interrupt event after the $T_{WWD,INIT}$ timer ends, which will increase the window watchdog failure counter by two. The system INIT timer continues counting when an invalid triggering is detected in this case until initialization timeout.

2) The maximum time of T_{INT} is shorter than the maximum time of the $T_{WWD,INIT}$. In this case, if a valid trigger is not detected within the $T_{SYS,INT}$, an initialization timeout occurs and this event is not indicated by an interrupt.

If initialization timeout occurs, a “Soft-Reset” will be issued: the nRESET pin will go to low, but the output voltages of the regulators will remain on. After the “Soft-Reset” the nRESET pin turns high again after the power-on reset release delay time t_{RD}. The watchdog will start a $T_{WWD,INIT}$ timer to give the microcontroller the chance to trigger and synchronize to the watchdog period. When a valid trigger signal is detected, the timing of $T_{WWD,INIT}$ will be terminated, so the time of the $T_{WWD,INIT}$ is variable and depends on the trigger. This is counted as a “Valid WWD triggering” and a $T_{WWD,MIN}$ timer is started. The window watchdog failure counter will be decremented by one without an interrupt being issued.

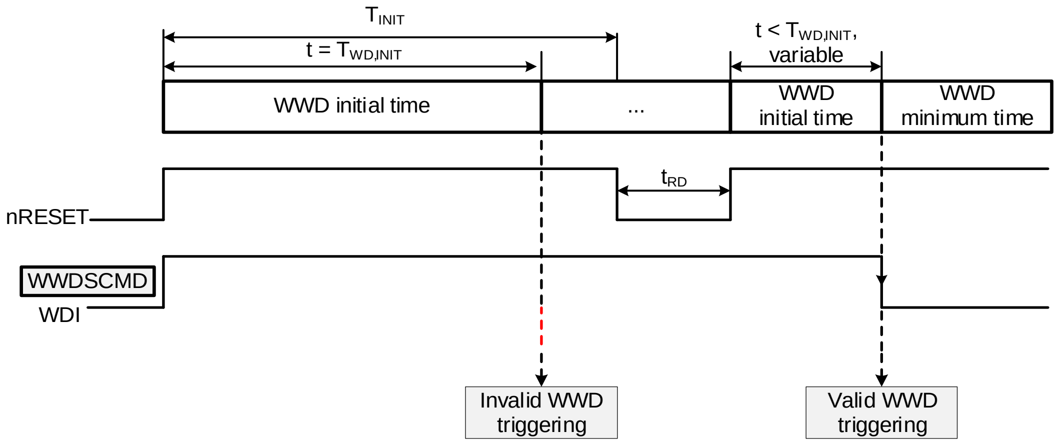


Figure 49. Incorrect Timing: No Trigger within Initial Time (TWD,INIT < TSYS,INIT)

Note: If the window watchdog is not triggered correctly within the next $T_{WWD,INIT}$ of the following INIT phase, a “Hard-Reset” will be issued, which means that the nRESET pin will go to low and the output voltages will also be switched off. After a third invalid triggering during INIT phase, the device starts transition to the FAILSAFE state.

Incorrect timing: No Trigger within $T_{WWD,MARGIN}$

The maximum duration of $T_{WWD,MARGIN}$ can be programmed via SPI. If there is no valid trigger signal during the $T_{WWD,MARGIN}$, it is considered that there is an “Invalid WWD triggering” when the time $t_{WWD,MARGIN}$ expires. An interrupt is generated to indicate this invalid WWD trigger and the window watchdog failure counter will be increased by two. A new $T_{WWD,MARGIN}$ timer will start to give the microcontroller the chance to trigger and synchronize to the watchdog period when an “Invalid WWD trigger” has been detected. During the $T_{WWD,MARGIN}$, a “Valid WWD trigger” terminates the timing of $T_{WWD,MARGIN}$ at any time, so that the time of the $T_{WWD,MARGIN}$ is variable, depending on when the trigger is generated. The window watchdog failure counter will be decremented by one without an interrupt issued when a “Valid WWD trigger” has been detected.

In case of multiple “Invalid WWD trigger” within the $T_{WWD,MARGIN}$, the window watchdog failure counter is incremented again by two until it reaches the configured threshold. In this case a reset will be issued.

When the timing of $T_{WWD,MARGIN}$ has been terminated by a “Valid WWD trigger”, a $T_{WWD,MIN}$ timer is started. Triggering within $T_{WWD,MIN}$ will be considered an "Invalid WWD Trigger".

Whether nRESET is pulled low depends on the value of window watchdog failure counter WWDECNT and the window watchdog error threshold WWDETHR. In the above example, it is assumed that the “Invalid WWD trigger” will not cause the value of WWDECNT to exceed WWDETHR.

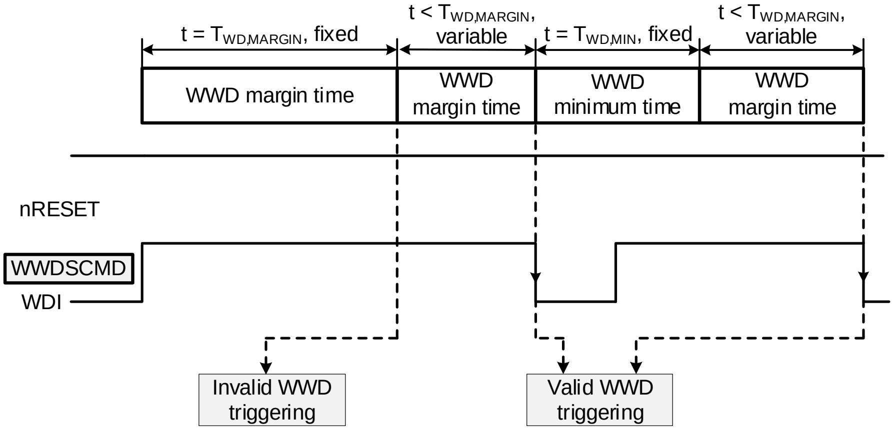


Figure 50. Incorrect Timing: No Trigger within TWWD,MARGIN

Incorrect timing: False Trigger in $T_{WWD,MIN}$

The maximum duration of $T_{WWD,MIN}$ can be programmed via SPI. If there is a trigger signal during the $T_{WWD,MIN}$, it is considered that there is an “Invalid WWD triggering”. An interrupt will be generated to indicate the invalid WWD trigger, and the window watchdog failure counter will be increased by two. The timing of $T_{WWD,MIN}$ will be immediately closed with the “Invalid WWD trigger” and start a $T_{WWD,MARGIN}$ timer to give the microcontroller the chance to trigger and synchronize to the watchdog period. During the $T_{WWD,MARGIN}$, a “Valid WWD triggering” terminates the timing of $T_{WWD,MARGIN}$, which makes the duration of the $T_{WWD,MARGIN}$ variable and depending on the triggering. The window watchdog failure counter will be decremented by one without an interrupt issued when a “Valid WWD trigger” has been detected.

Whether nRESET is pulled low depends on the value of window watchdog failure counter WWDECNT and the window watchdog error threshold WWDETHR. In the above example, it is assumed that the “Invalid WWD trigger” will not cause the value of WWDECNT to exceed WWDETHR.

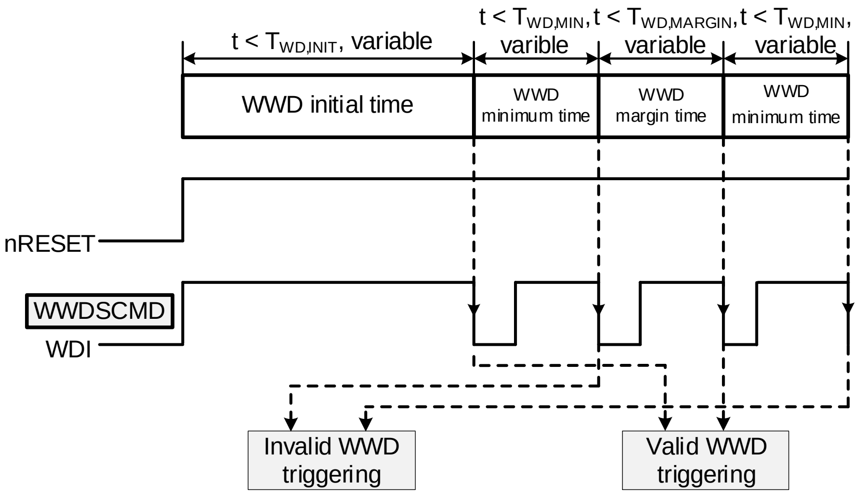


Figure 51. Incorrect Timing: False Trigger within TWWD,MIN

13.3 Functional Watchdog

13.3.1 Principle of Operation and Configuration

The SA47301x integrates a functional or question/answer watchdog to monitor the microcontroller.

In steady state, when the device is configured to use the functional watchdog to detect correct operation of the MCU, the functional watchdog requires a specific message from the MCU before the end of the heartbeat period. The device generates a question for the MCU in FWDQUEST during operation. The answer to each question consists of 4 responses: RESP3, RESP2, RESP1, and RESP0. The MCU shall send these four responses to the device in turn via an SPI command before the heartbeat period has ended. The last response shall be written to the synchronized response register to reset the heartbeat counter.

In INIT, NORMAL and WAKE state, the following parameters of the functional watchdog can be configured using SPI commands:

1) The length of the heartbeat period can be configured according to the needs of the application. (Combination of cycle time WDCYC, WDCYCDIV and number of cycles for heartbeat WDHBTP)
2) The threshold for the functional watchdog failure counter overflow.

13.3.2 Initialization

When the device enters INIT state, the functional watchdog is off by default and can be enabled by an SPI write to WDCFG0.FWDEN.

13.3.3 Normal Operation

The question are listed in the following table followed by the correct responses in the same row.

Table 14. Functional Watchdog Response Definition

QUESTION	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C

7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

The sequence of responses must be kept and the MCU can read FWDRSPC to obtain information about which response needs to be written before sending the response.

For the actual question defined in the table, a complete answer should onsist of 4 subsequent response bytes. All 4 responses shall be sent in the correct order before the heartbeat period overflows as shown below:

1) The first three responses RESP3, RESP2 and RESP1 shall be written into FWDRSP.
2) The last response RESP0 should be written into FWDRSPSYNC to reset the heartbeat timer.

The device considers a sequence “Valid FWD triggering” when the complete answer (all four responses - 32 bits) is correct.

An “Invalid FWD triggering” occurs when one of the events that follows occur:

1) Heartbeat counter expired.
2) Response is incorrect. In this case, invalid FWD triggering is generated when the last synchronized response byte was received.

Like window watchdog, the functional watchdog error counter FWO is decremented by 1 when a valid FWD trigger is generated and increments the functional error counter by 2 when an invalid FWD trigger is generated.

When the functional watchdog error counter FWO is greater than the functional watchdog error threshold which is configured via SPI, a “Move to INIT” event is triggered, followed by heartbeat counter reset and set the functional watchdog error counter FWO to zero.

13.3.4 Functional Watchdog Output FWO

The FWD failure counter is connected to the functional watchdog output FWO which is an internal signal. “Valid FWD triggering” and “Invalid FWD Triggering” are both recorded by the value of the functional watchdog FWO output.

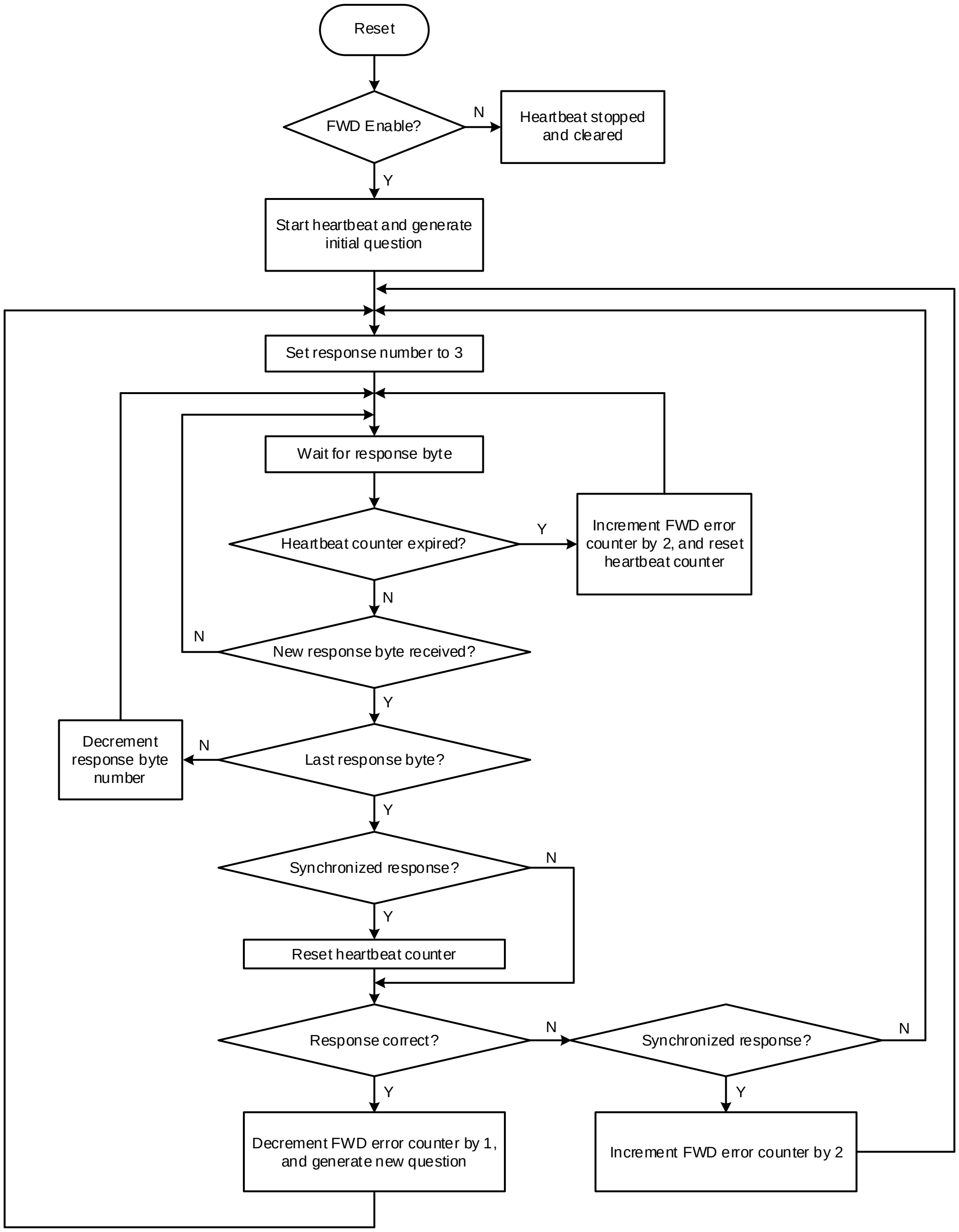


Figure 52. Functional Watchdog Flowchart Diagram

13.3.5 Timing Diagrams

Normal Operation: Correct Triggering

Assume that a “Valid FWD trigger” has happened before and a new question is generated. In parallel the heartbeat counter starts counting up. Before the heartbeat counter overflows, the first three correct responses are sequentially written to the functional watchdog response register, the fourth correct response is finally written to the functional watchdog heartbeat synchronization register. This is considered a “Valid FWD triggering”, and the heartbeat counter will be reset to zero. In this case, a new question is generated and in parallel the heartbeat counter starts counting up.

For a “Valid FWD trigger”, the functional watchdog error counter (FWO) is decremented by 1 if the functional watchdog error counter value is higher than zero.

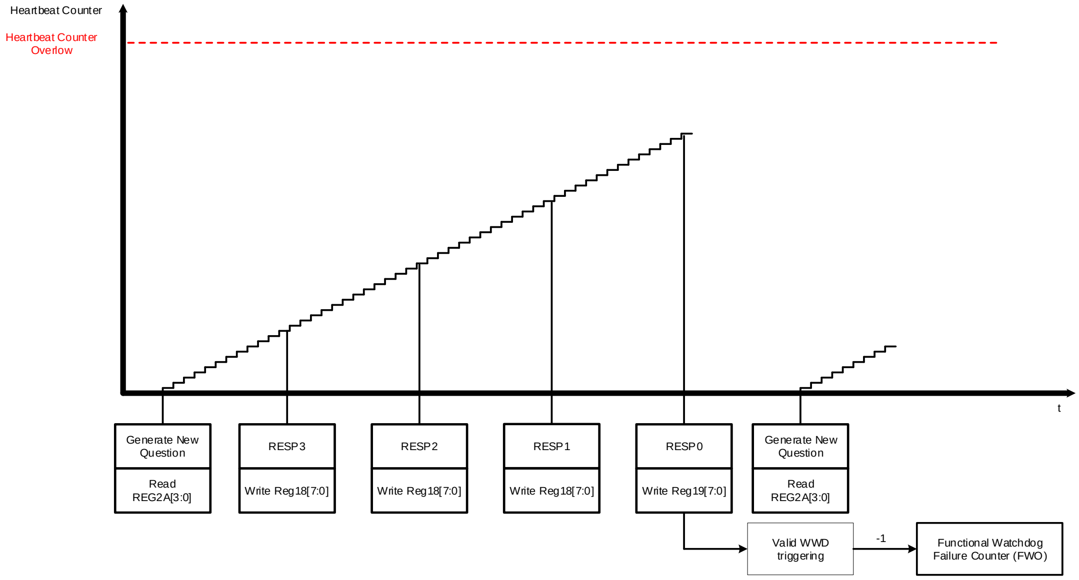


Figure 53. Normal Operation: Correct Triggering

Fault Operation: Synchronization is Missing

Assume that a “Valid FWD triggering” has happened before and a new question is generated, while in parallel the heartbeat counter starts counting up. Before the heartbeat counter overflows, the first three correct responses are sequentially written to the functional watchdog response register, the fourth correct response is erroneously written to the functional watchdog response register, which should be written to the functional watchdog heartbeat synchronization register in normal operation. Since all responses are correct, the sequence of responses is correct and the last not synchronized response was received before the heartbeat counter overflow occurred, the heartbeat counter will not be reset and continue to count. This is regarded as “Valid FWD triggering”, and a new question is generated.

The heartbeat counter is still counting up, waiting for the answer on the new question, until the heartbeat counter overflows. When the heartbeat counter overflows, this is regarded as “Invalid FWD triggering” and the heartbeat counter will be reset to zero. In this case, no new question is generated, and the heartbeat counter starts counting up.

When a “Valid FWD trigger” is detected, the functional watchdog error counter FWO is decremented by 1 (if the functional watchdog error counter value is higher than zero). When a “Invalid FWD trigger” is detected, the functional watchdog error counter FWO is incremented by 2.

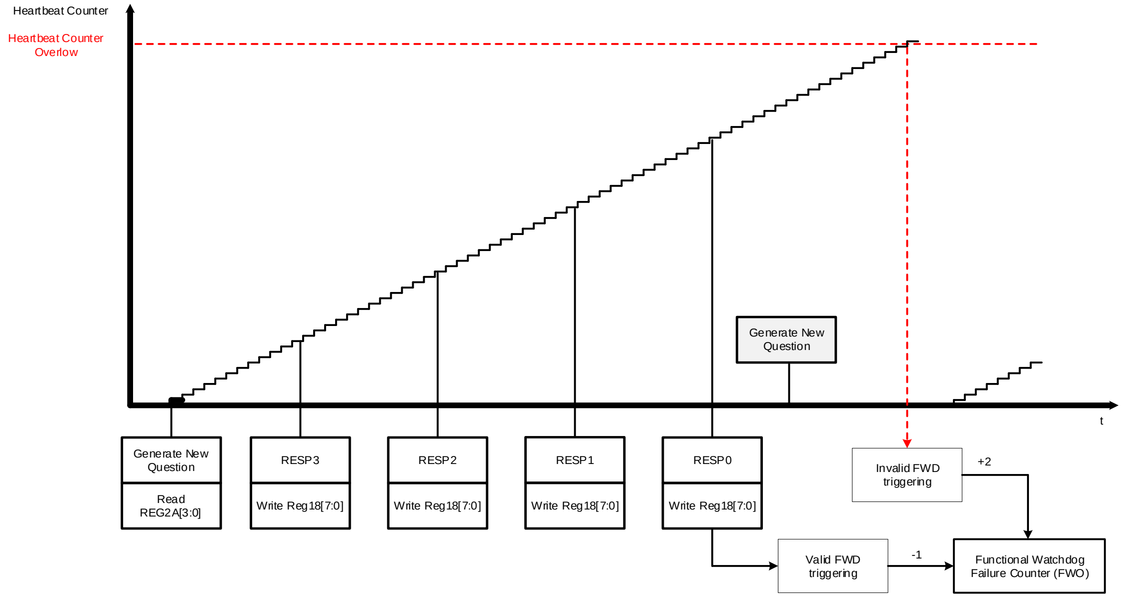


Figure 54. Fault Operation: Synchronization is Missing

Fault Operation: Answer is Wrong

Assume that a "Valid FWD triggering" has happened before and a new question is generated, while in parallel the heartbeat counter starts counting up. Before the heartbeat counter overflows, the first three responses are sequentially written to the functional watchdog response register, the fourth response is written to the functional watchdog heartbeat synchronization register. Because not all responses are correct, this is regarded as "invalid FWD triggering", and the heartbeat counter will be reset. In this case, no new question is generated, but the heartbeat counter starts counting up.

When an "Invalid FWD triggering" is detected, the functional watchdog error counter FWO is incremented by 2.

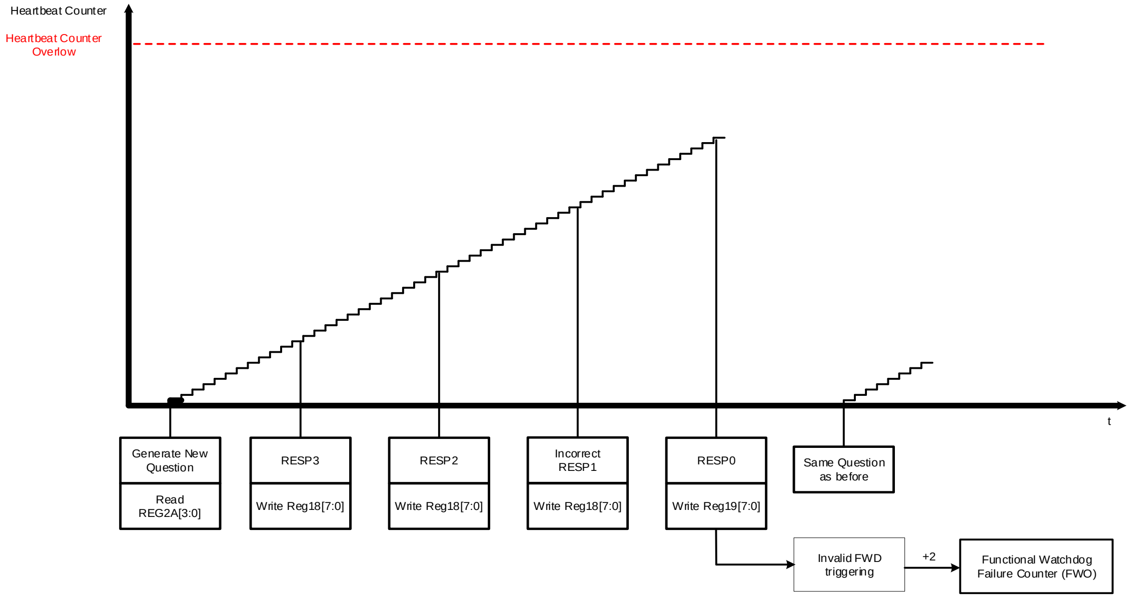


Figure 55. Fault Operation: Answer is Wrong

Fault Operation: Missing Response

Assume that a “Valid FWD triggering” has happened before and a new question is generated, while in parallel the heartbeat counter starts counting up. Before the heartbeat counter overflows, the first two responses are sequentially written to the functional watchdog response register, the fourth response is written to the functional watchdog heartbeat synchronization register. Due to the lack of response RESP1, although the last response is synchronized, the heartbeat counter will not be reset and the functional watchdog will consider that responses are not written completely. The functional watchdog will wait for all four responses to be written while the heartbeat counter continues to count, until the heartbeat counter overflows. This is regarded as “Invalid FWD trigger”.

When a “Invalid FWD trigger” is detected, the functional watchdog error counter FWO is incremented by 2.

There is no fixed time for all four responses, but they must be sent in correct order before the heartbeat counter expires.

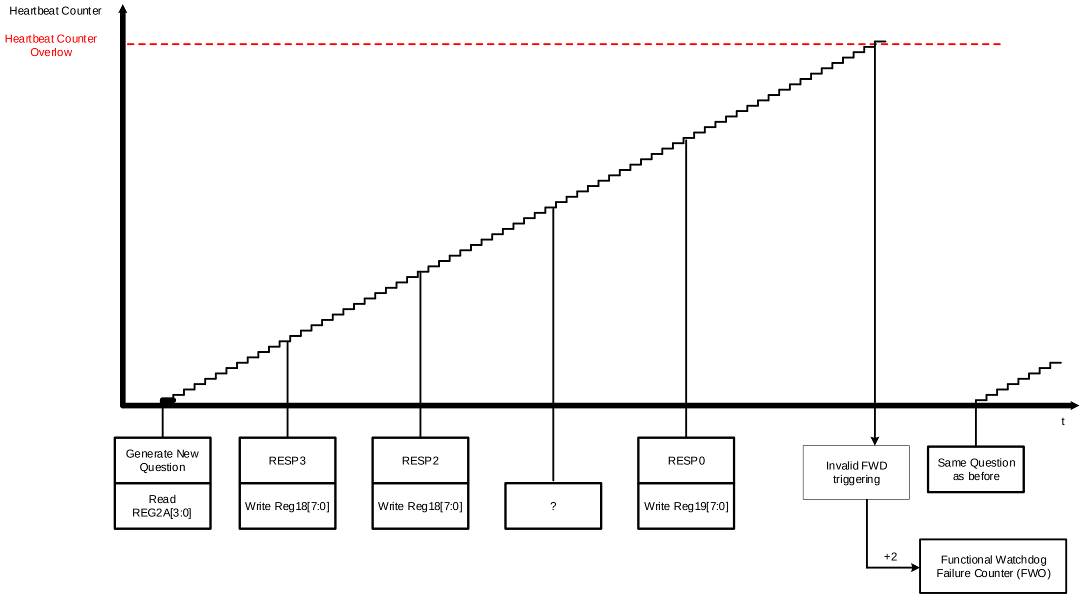


Figure 56. Fault Operation: Answer is Not Complete

14 Safe State Control Function

14.1 Introduction Safe State Control Function

The SA47301x integrates a safe state control function implemented by two safety shutdown paths, SS1 and SS2. The safe state control unit pulls low SS1 and SS2 when a specific fault is triggered. The function monitors the following inputs:

1) The result of error monitor, the SA47301x monitors the input signal of ERR pin which indicates MCU operation status. An unexpected ERR signal can be considered a fault (refer to error monitor function section).

2) OV, UV and StG protection of a related regulator (for details please refer to the chapter Monitoring function).

3) The result of window watchdog or function watchdog, whether watchdog counter overflowed.

4) Thermal shutdown protection of monitoring block.

5) State transition request by SPI. The SS1 and SS2 are pulled high immediately when the device enters NORMAL state, and pulled low when moving out of NORMAL state.

The following parameters of the Safe State Control function can be programmed during INIT, NORMAL, SLEEP and WAKE state, WWD and FWD configuration and error pin configuration via SPI, including disabling of individual functionality via protected registers (for description of states please refer to chapter State machine):

1) The number of invalid watchdog trigger thresholds. The window watchdog and functional watchdog have a failure counter, which can be individually programmed by SPI command to set the threshold values.

2) The immediate reaction or recovery delay reaction setting for the error monitor. The recovery delay time $\triangle t_{REC}$ also can be programmed by SPI command.

3) Delay time between SS1 and SS2.

The safe state control function block is shown as below:

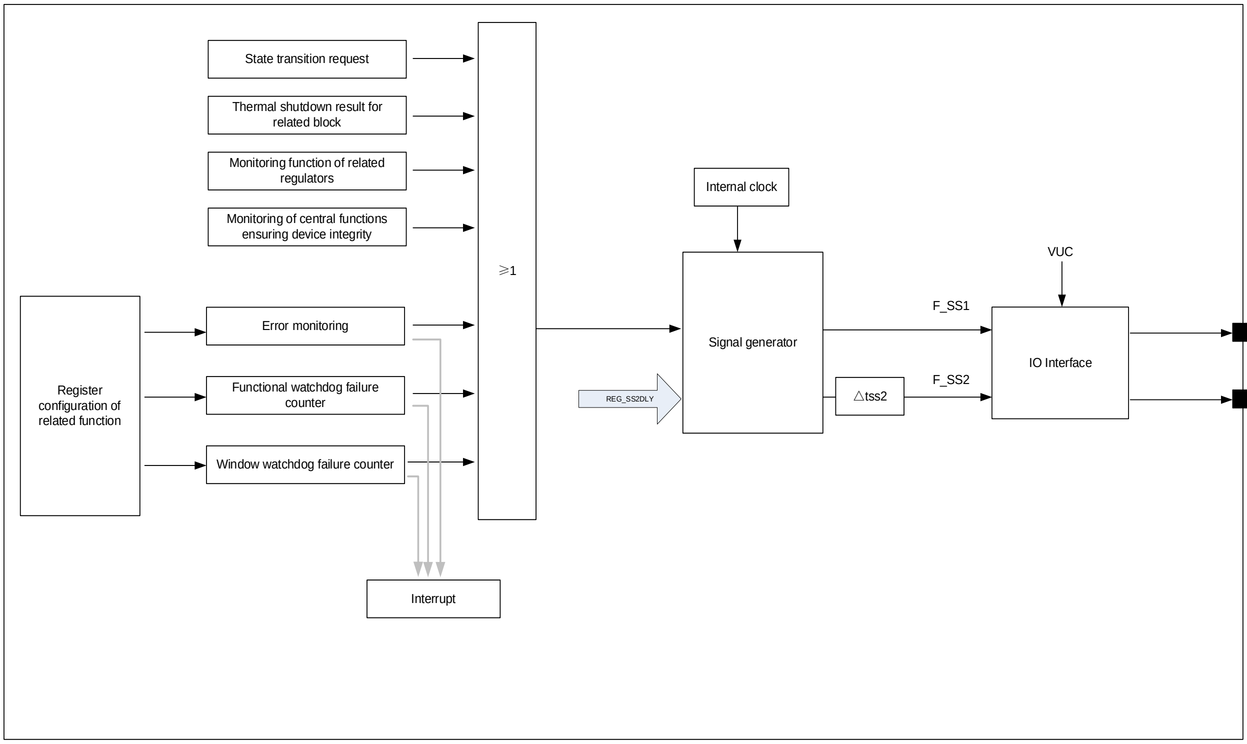


Figure 57. Principle Safe State Control Function

14.2 Reaction to Error Monitoring Signal (Pin ERR)

In the case of fault-free operation of the MCU, the error monitoring function requires a toggling signal to be sent at a determined timing to the ERR pin. A normal switching signal on ERR pin is considered as a "being alive" indication. Stopped switching or switching with unexpected frequency is considered as a fault, and the safe state control block is notified in such events.

14.2.1 Immediate Reaction to ERR Monitoring Failure

It is considered a serious error when any of the following event occurs:

1) Remaining input ERR signal high or low for more than low frequency detection time $\Delta t_{DET,LF}$.

2) Remaining input ERR signal high or low for less than high frequency detection time $\Delta t_{DET,HF}$.

If the ERR pin monitor recovery is disabled, immediate reaction to the error signal will be set when a serious error is detected. Several typical examples are shown as below:

Case 1: ERR signal remains low. When ERR signal remains low for more than low frequency detection time $\Delta t_{DET,LF}$, it is detected as an error. SS1 is pulled low immediately when error detected, and SS2 is pulled low after an optional delay time, Δt_{SS2}.

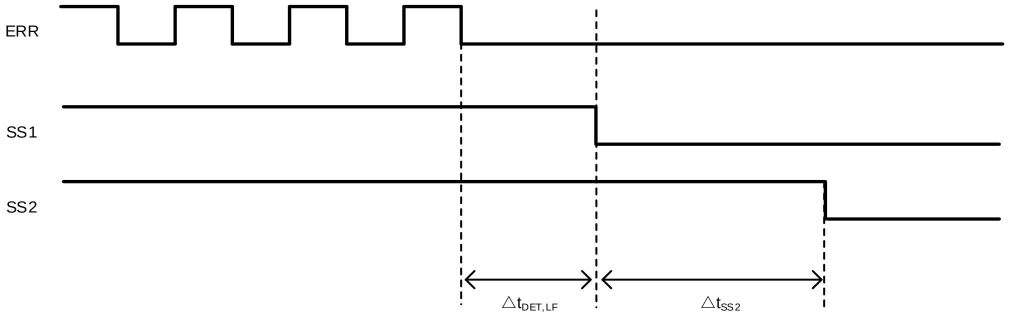


Figure 58. Safe State Reaction on ERR Signal Remain Low

Case 2: ERR signal remains high. When ERR signal remains high for more than low frequency detection time $\Delta t_{DET,LF}$, it is detected as an error. SS1 is pulled low immediately when error detected and SS2 will be pulled low after an optional delay time Δt_{SS2}.

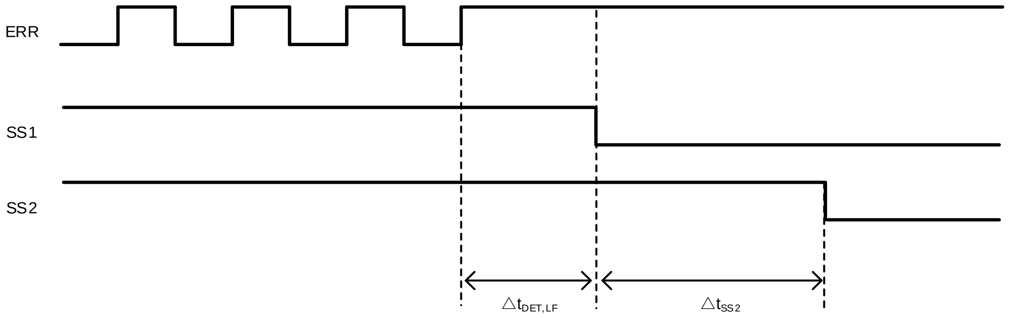


Figure 59. Safe State Reaction on ERR Signal Remain High

Case 3: ERR signal frequency is too high. When the ERR signal remains high or low for less than high frequency detection time $\Delta t_{DET,HF}$, it is detected as an error. SS1 will be pulled low immediately when error detected and SS2 will be pulled low after an optional delay time Δt_{SS2}.

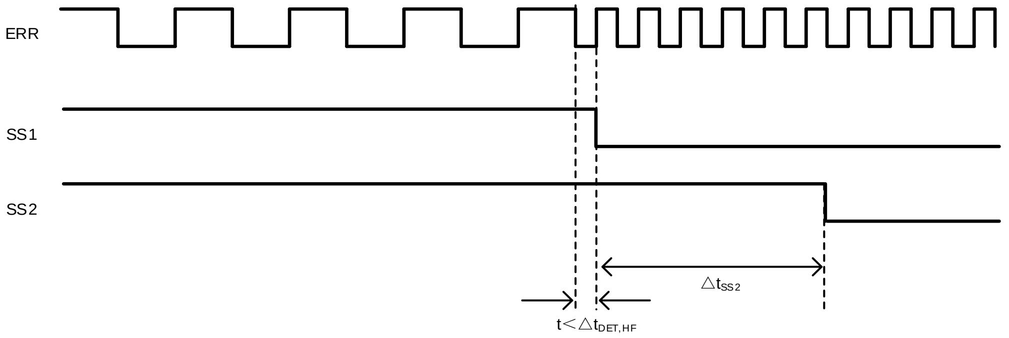


Figure 60. Safe State Reaction on ERR Signal Frequency Too High

Case 4: ERR signal stays high or low too long. If the ERR signal switches with a changing duty-cycle, when the ERR signal remains high or low between $\Delta t_{DET,HF}$ and $\Delta t_{DET,LF}$, no error is detected. When ERR signal remains high or low for more than $\Delta t_{DET,LF}$, it is detected as an error, similar to the cases 1 and 2.

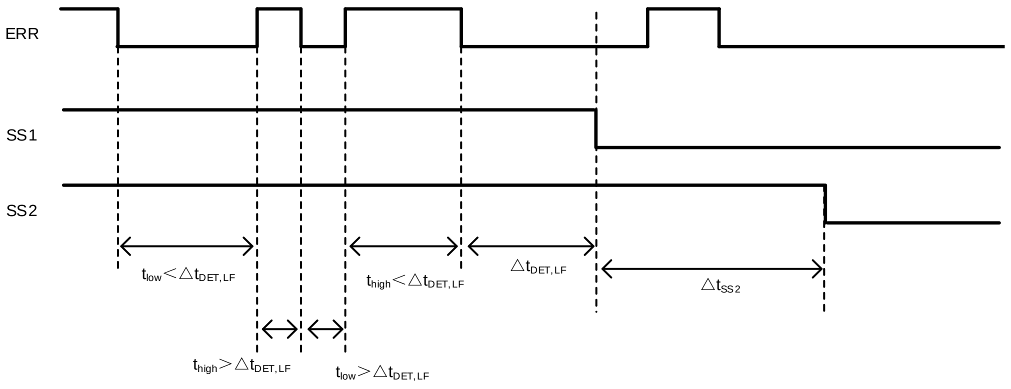


Figure 61. Safe State Reaction on ERR Signal (Duty-cycle Changing and Keep Low or High Too Long)

Case 5: ERR signal remains high or low too short. If the ERR signal switches with a changing duty-cycle, when the ERR signal remains high or low between $\Delta t_{DET,HF}$ and $\Delta t_{DET,LF}$, no error is detected. When ERR signal remains high or low for less than $\Delta t_{DET,HF}$, it is detected as an error, similar to case 3.

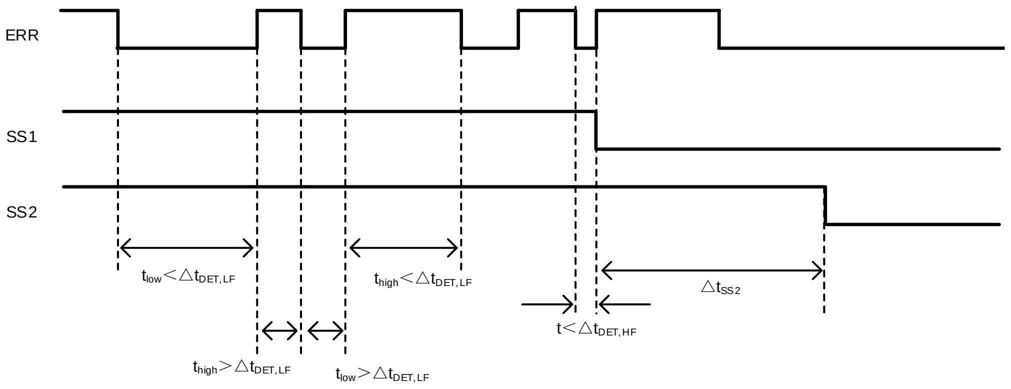


Figure 62. Safe State Reaction on ERR Signal (Duty-cycle Changing and Keep Low or High Too Short)

14.2.2 Recovery Delay Reaction on ERR Monitoring Failure

If ERR pin monitor recovery is enabled, the recovery delay time provide time to the MCU to recover. An interrupt is generated after the error is detected and safe state signal is kept high until Δt_{REC} has expired. If the ERR signal resumes toggling before Δt_{REC} has expired, the safe state signal will stay high all the time.

Several typical examples are shown as below:

Case 1: ERR signal remains low. When the ERR signal remains low for more than low frequency detection time $\Delta t_{DET,LF}$, it is detected as an error. An interrupt will be generated to indicate this error and start the recovery delay time Δt_{REC}. SS1 will be pulled low after Δt_{REC} has expired, and SS2 will be pulled low after an optional delay time Δt_{SS2}.

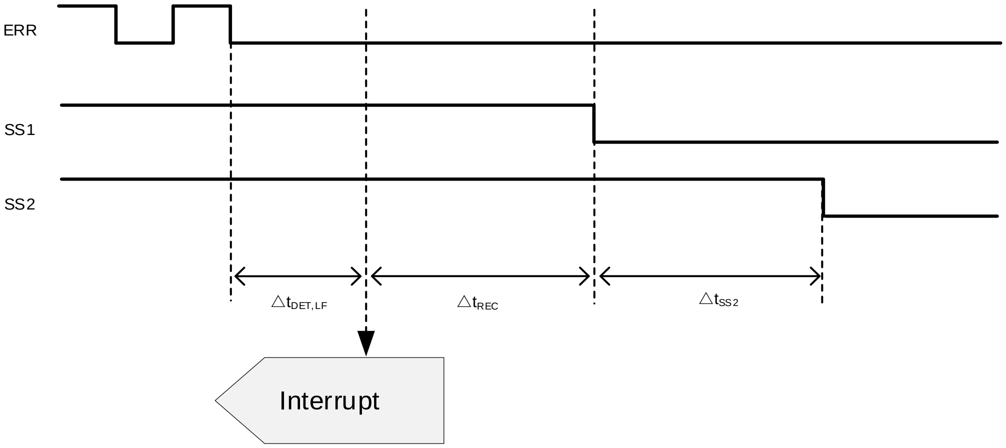


Figure 63. Flow Diagram Reaction on SMU Signal, Error Longer than Recovery Delay Time

Case 2: ERR signal frequency is too high. When the ERR signal remains high or low for less than the high frequency detection time $\Delta t_{DET,HF}$, it is detected as an error. An interrupt will be generated to indicate this error and start the recovery delay time Δt_{REC}. SS1will be pulled low after Δt_{REC} has expired, and SS2 will be pulled low after an optional delay time Δt_{SS2}.

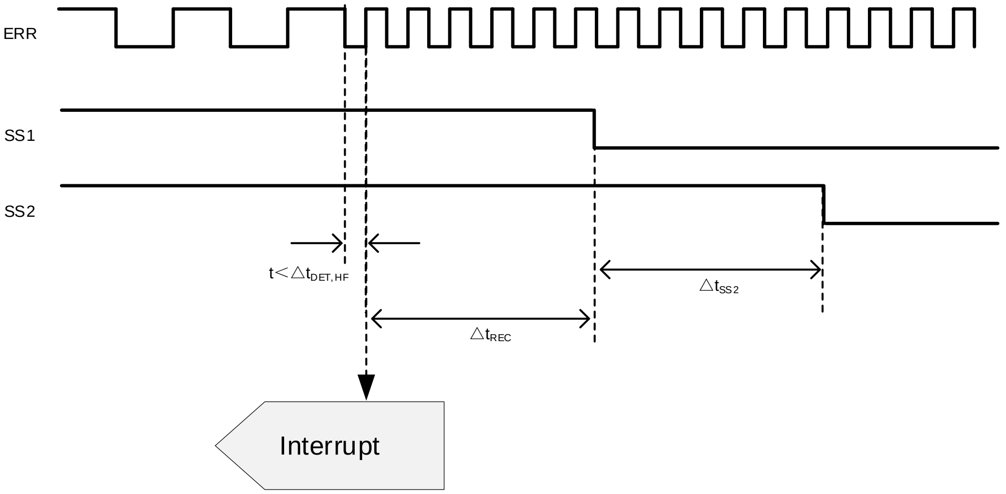


Figure 64. Flow Diagram Reaction on SMU Signal, Error Longer than Recovery Delay Time

(ERR Signal Frequency Too High)

Case 3: ERR signal stops switching and resumes toggling before Δt_{REC} has expired. When the ERR signal remains high or low for more than the low frequency detection time $\Delta t_{DET,LF}$, it is detected as an error. An interrupt will be generated to indicate this error and start the recovery delay time Δt_{REC}. The ERR signal will resume switching before $\triangle t_{REC}$ has expired, and SS, SS2 will stay high all the time.

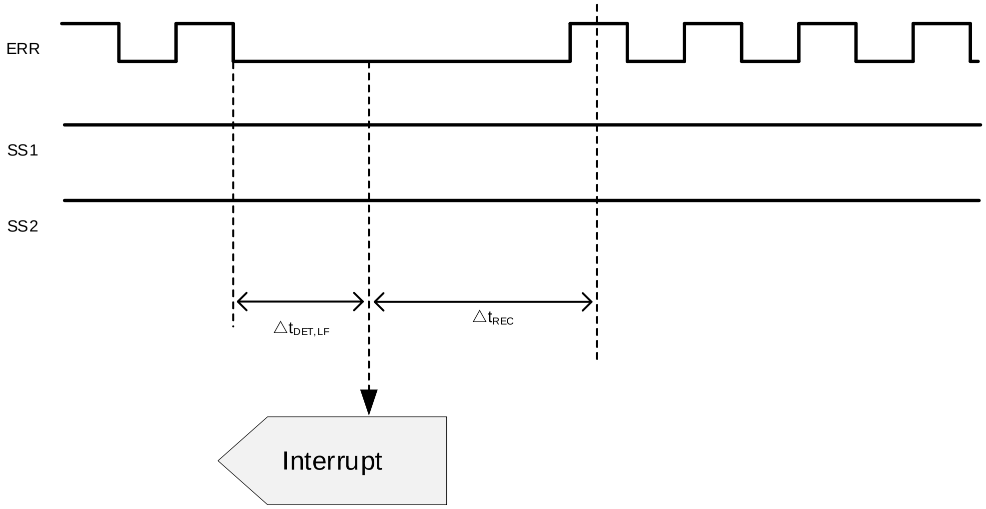


Figure 65. Flow Diagram Reaction on SMU Signal, Error Shorter than Recovery Delay Time

Case 4: ERR signal frequency is too high and resumes toggling with a valid frequency before Δt_{REC} has expired. When the ERR signal remains high or low for less than high frequency detection time $\Delta t_{DET,HF}$, it is detected as an error. An interrupt will be generated to indicate this error and start the recovery delay time Δt_{REC}. The ERR signal will resume switching with a valid frequency before $\triangle t_{REC}$ has expired, so that SS1 and SS2 will stay high all the time.

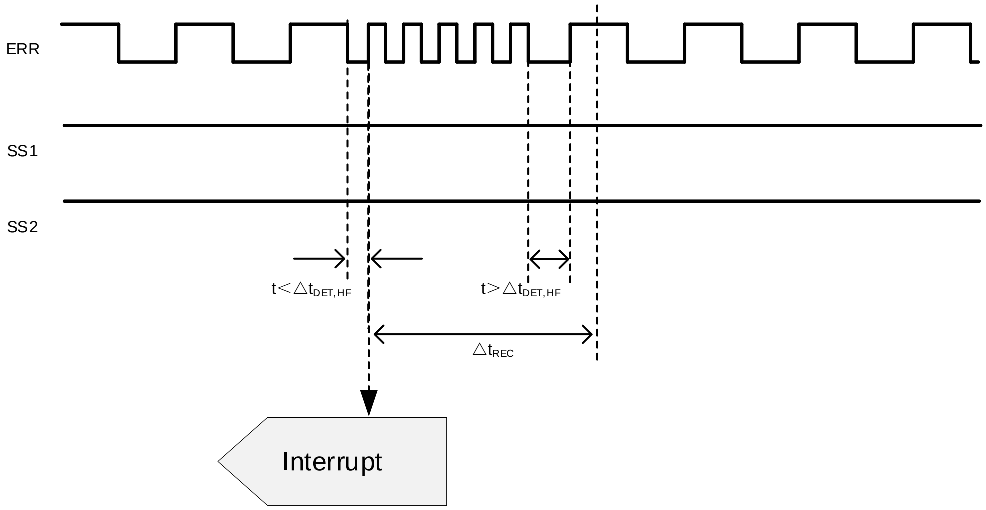


Figure 66. Flow Diagram Reaction on SMU Signal, Error Shorter than Recovery Delay Time

(ERR Signal Frequency Too High)

14.3 Reaction on Error-Triggered State Transitions

The reset output pin, nRESET, is an open-drain output which indicates safety fault events. As soon as a reset condition occurs, the nRESET pin is pulled low.

A "soft reset" condition is defined when the nRESET pin goes low, but the pre and post regulator output voltages are not switched off.

A "hard reset" condition is defined when the nRESET pin goes low and the post regulator output voltages are switched off.

When a “soft reset” event occurs, the falling edge of nRESET signal indicates an error. SS1 is pulled low immediately when nRESET is pulled low, and SS2 is pulled low after an optional delay time Δt_{SS2}.

Note: In the case of an UV event on QUC, a delayed SS2 signal follows VQUC as it is supplied from QUC.

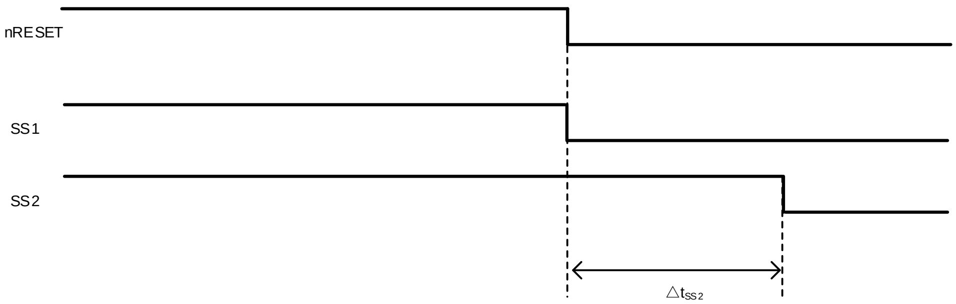


Figure 67. Flow Diagram Reaction on An Error Triggered State Transition- soft reset

When a “hard reset” event occurs, the falling edge of nRESET signal indicates an error. When a “hard reset” event occurs, the supplying post regulator LDO_µC will be switched off, SS1 and SS2 will be pulled low immediately on the nRESET falling edge.

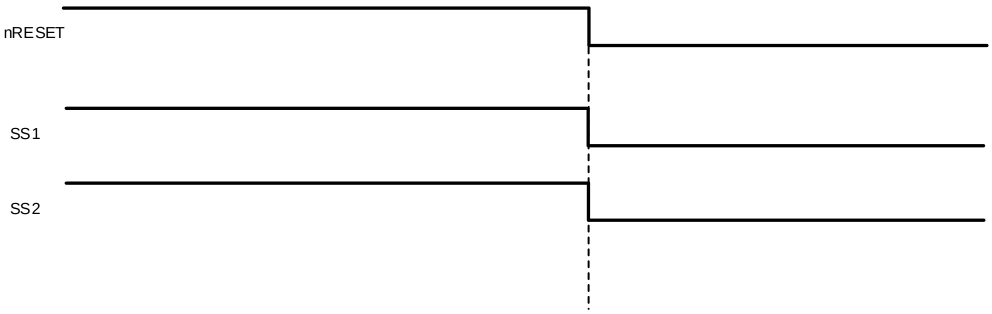


Figure 68. Flow Diagram Reaction on An Error Triggered State Transition- hard reset

14.4 Reaction on Window Watchdog Output (WWO)

The SA47301x integrates a window watchdog with programmable input trigger signal (either pin WDI or trigger via SPI command to WWDSCMD register) and an implemented window watchdog failure counter (WWDSTAT.WWDECNT). The counter increases by two when on an invalid window watchdog trigger, and decreases by one for a valid window watchdog trigger. Any increase or decrease of the watchdog counter is written in the window watchdog status counter. An interrupt is generated by an increment of the window watchdog status counter, but an interrupt won't be generated by the decrement of window watchdog status counter.

The window watchdog status counter is compared with the programmed threshold ΣWWO (RWDCFG0.WWDETHR) to determine whether the overflow happened. If the content of the status counter is equal or higher than ΣWWO, the device will move to INIT state, and both SS1 and SS2 outputs will be pulled low.

In INIT, NORMAL and WAKE-state, the threshold ΣWWO (WDCFG0.WWDETHR) can be used for activating the safe state signals SS1 and SS2 can be changed.

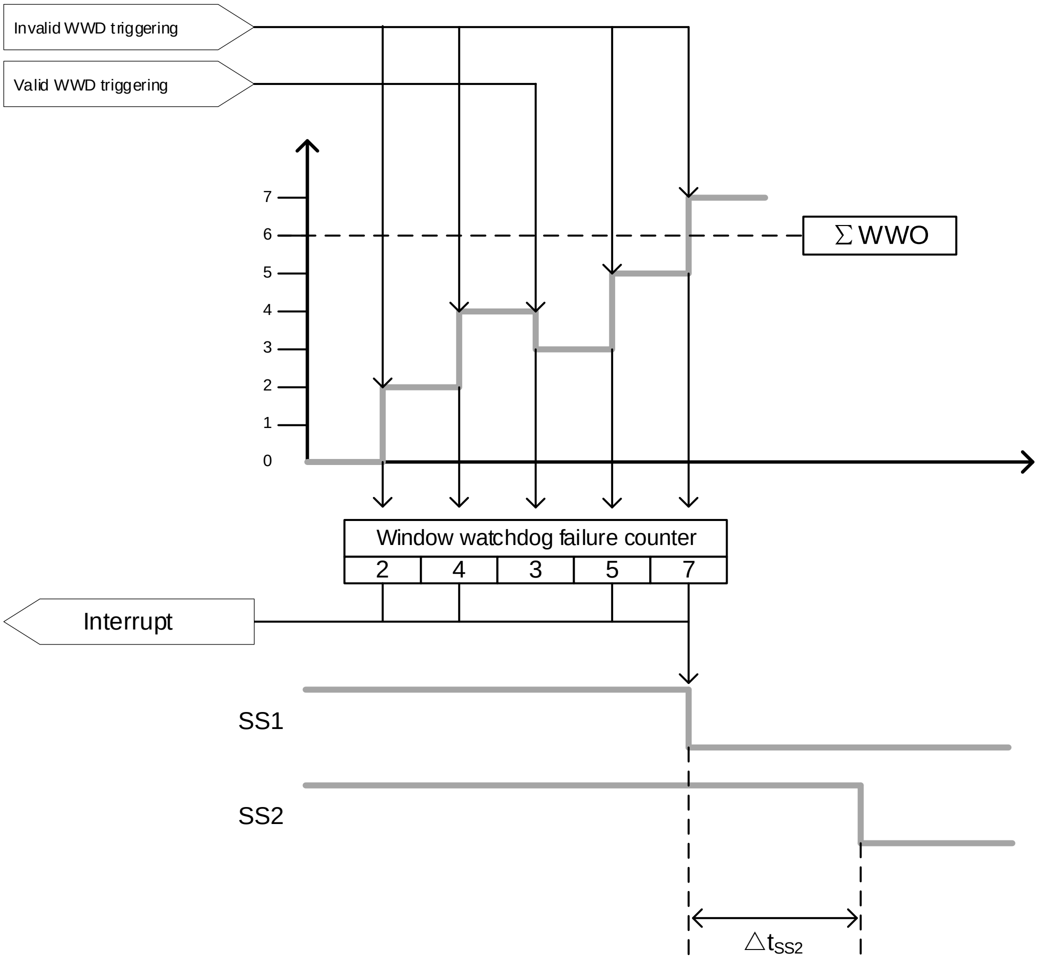


Figure 69. Flow Diagram Reaction on WWO

Figure 69 shows an example of a flow diagram reaction on WWO. In this case, the window watchdog error threshold ΣWWO is set to 6. An invalid watchdog trigger increments the window watchdog status counter by two, this is indicated by an interrupt. A valid watchdog trigger decrements the window watchdog status counter by one, this is not indicated by an interrupt. When the value of window watchdog failure counter is higher than ΣWWO, a watchdog counter overflow event occurs. SS1 will be pulled low immediately when watchdog counter overflows and SS2 will be pulled low after an optional delay time Δt_{SS2}.

14.5 Functional Watchdog Output Reaction (FWO)

The SA47301x integrates a functional watchdog with an implemented functional watchdog failure counter (FWDSTAT1.FWDECNT). The window watchdog and functional watchdog have independent timers and error counters, which allows to run both watchdogs in parallel.

The counter increases by two on an invalid functional watchdog trigger and decrease by one on a valid functional watchdog trigger. Any increase or decrease of watchdog counter is written in the functional watchdog status counter. An interrupt is generated by an increment of the functional watchdog status counter, but interrupt won't be generated by a decrement of functional watchdog status counter.

The functional watchdog status counter is compared with the programmed threshold ΣFWO (RWDCFG1.FWDETHR) to determine whether the overflow happened. If the content of the status counter is equal or higher than ΣFWO, the device will move to INIT state, and both SS1 and SS2 will be pulled low.

In INIT, NORMAL and WAKE-state, the threshold ΣFWO (WDCFG1.FWDETHR) for activating the safe state signals SS1 and SS2 can be changed.

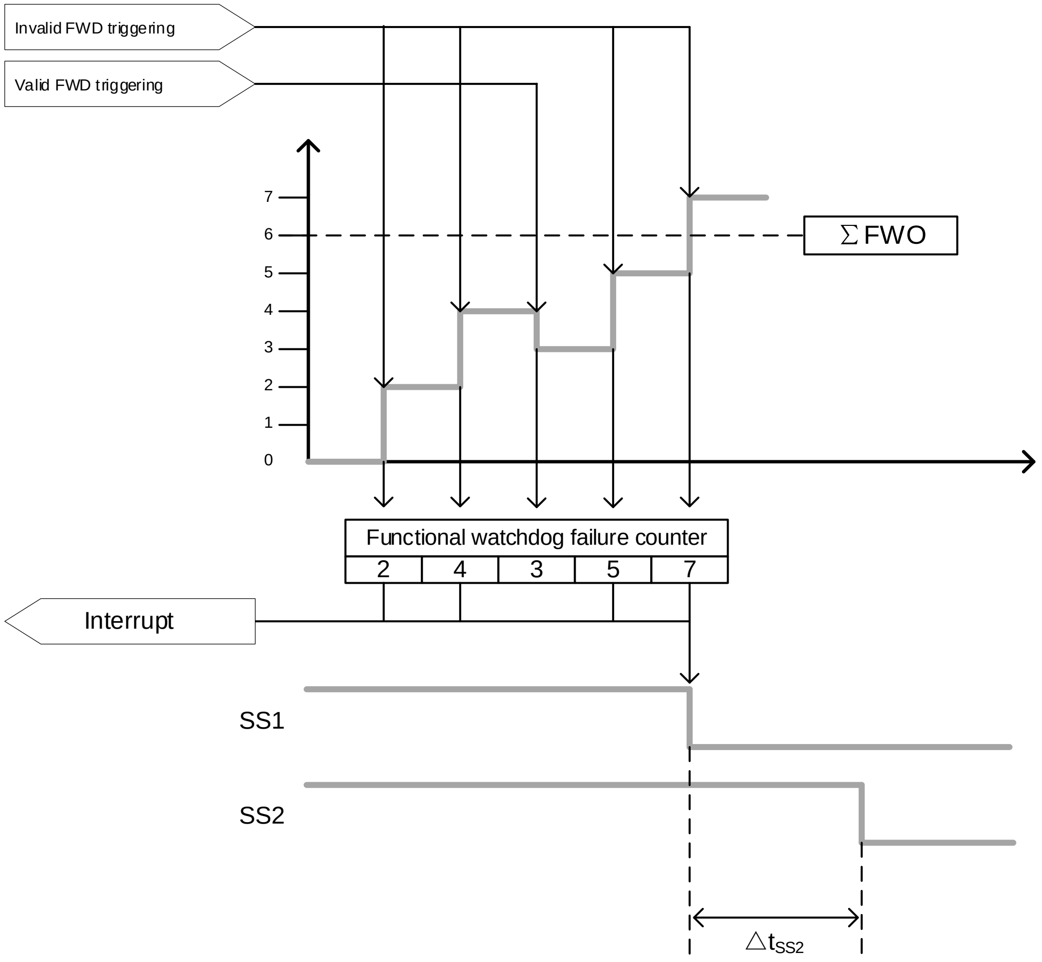


Figure 70. Flow Diagram Reaction on FWO

Figure 70 shows an example of a flow diagram reaction on FWO. In this case, the functional watchdog error threshold ΣFWO is set to 6. An invalid watchdog trigger increments the functional watchdog status counter by two; this is indicated by an interrupt. A valid watchdog trigger decrements the functional watchdog status counter by one; this is not indicated by an interrupt. When the value of functional watchdog failure counter is higher than ΣFWO, a watchdog counter overflow event occurs. SS1 will be pulled low immediately when watchdog counter overflow and SS2 will be pulled low after an optional delay time Δt_{SS2}.

14.6 Reaction on Thermal Shutdown (TSD)

The SA47301x integrates a thermal shutdown protection with dedicated temperature sensors. When TSD occurs, all regulators are off, the device will move to FAILSAFE state.

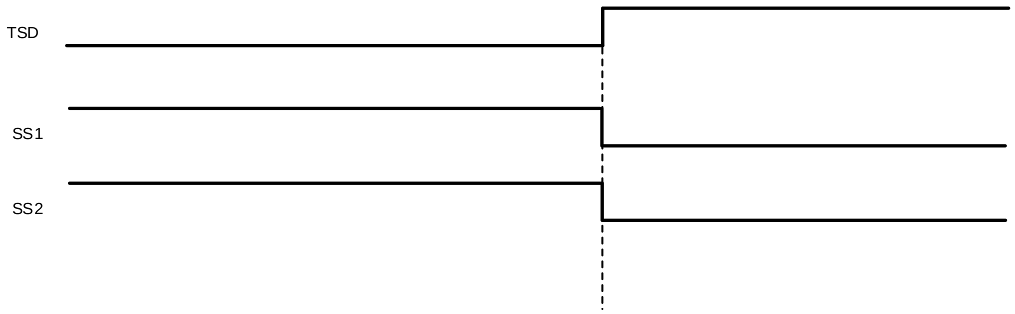
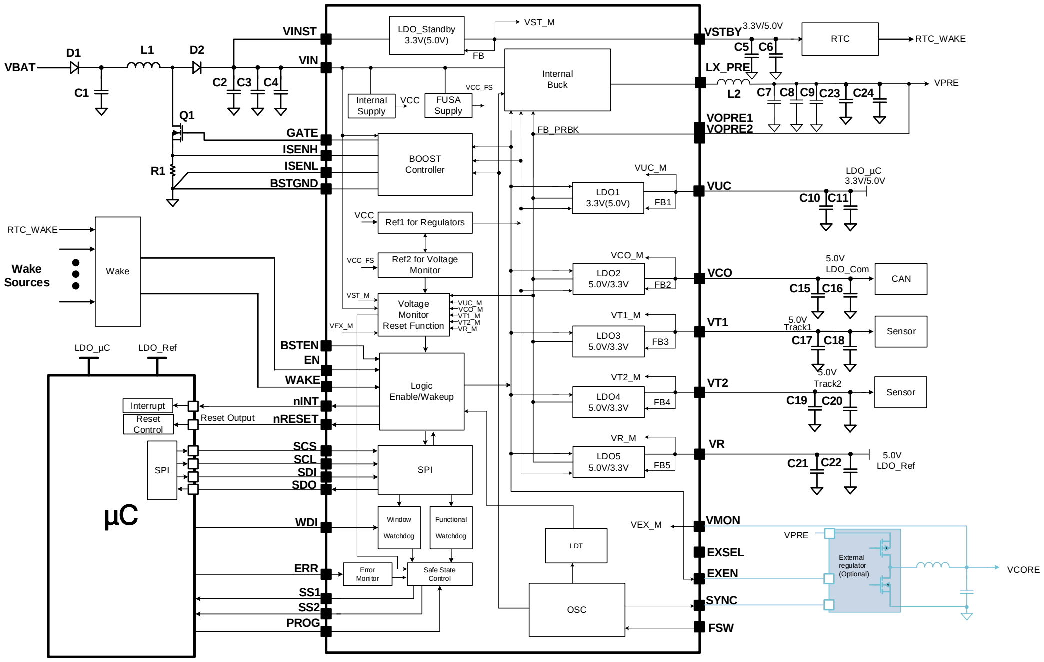


Figure 71. Flow Diagram Reaction on TSD

When the temperature of pre-buck regulator, LDO_UC, or monitoring block is higher than thermal shutdown threshold, an internal TSD signal goes from low to high. SS1 and SS2 will be pulled low immediately with the rising edge of TSD signal

Application Circuit



BOM List

Designator	Description		Part Number	Manufacture
C1	100µF/50V/E-Cap, can be removed if boost is not used		HZA107M050G24VT-F	Cornell Dubilier - CDE
C2	100µF/50V/E-Cap		HZA107M050G24VT-F	Cornell Dubilier - CDE
C3	10µF/50V/1210		KAF32LR71H106KL	KYOCERA AVX
C4, C6, C18, C20	100nF/50V/0603		KAM15AR71H104KT	KYOCERA AVX
C7, C8, C23, C24	400kHz	22µF/16V/1206	GRM31CZ71C226ME15K	Murata Electronics
	2MHz	10µF/16V/1206	KAF31GR71C106KU	KYOCERA AVX
C9, C10, C15	10µF /16V/1206		KAF31GR71C106KU	KYOCERA AVX
C11, C16, C22	100nF/16V/0603		GCM188R71C104KA37J	Murata Electronics
C17, C19	4.7µF/50V/1206		KAM31GR71H475KL	KYOCERA AVX
C5, C21	4.7µF/16V/1206		1206YC475K4T2A	KYOCERA AVX
L1	22µH, Can be removed if boost is not used		MSS1278H-223MLD	Coilcraft
L2	400kHz	22µH	MSS1278H-223MED	Coilcraft
	2MHz	4.7µH	784774047	Wurth Elektronik
Q1	60V/>3A		BSL606SNH6327	INFINEON
D1, D2	40V/>3A		MBRS340T3	ONSEMI
R1	0.1Ω/1206R		LTR18EZPJLR10	ROHM Semiconductor

Layout Design

A good PCB layout is quite important to reduce the ripple and to enhance the line and load transients, as well as to achieve better noise, better EMI and loop stability.

The recommended layout of power lines is illustrated in bellow. It is recommended to follow the below PCB layout guidelines:

- At least four-layer PCB with a common ground plane is recommended.
- Traces of switching nodes (LX_PRE) should be short and wide.
- Place input capacitors on VIN, VINST and VOPRE as close as possible to the device, please refer to the layout position of C_{VIN}, C_{VINST} and C_{VOPRE} in the diagram.
- Place output capacitors on VSTBY, VT1, VT2, VCO, VUC and VR as close as possible to the device.
- It is recommended to use parallel capacitors to get lower ESR.
- Drill multiple vias at the GND pins of all input and output capacitors, and drill multiple vias on the exposed pad of the chip to enhance heat dissipation capability and reduce ground plane impedance.

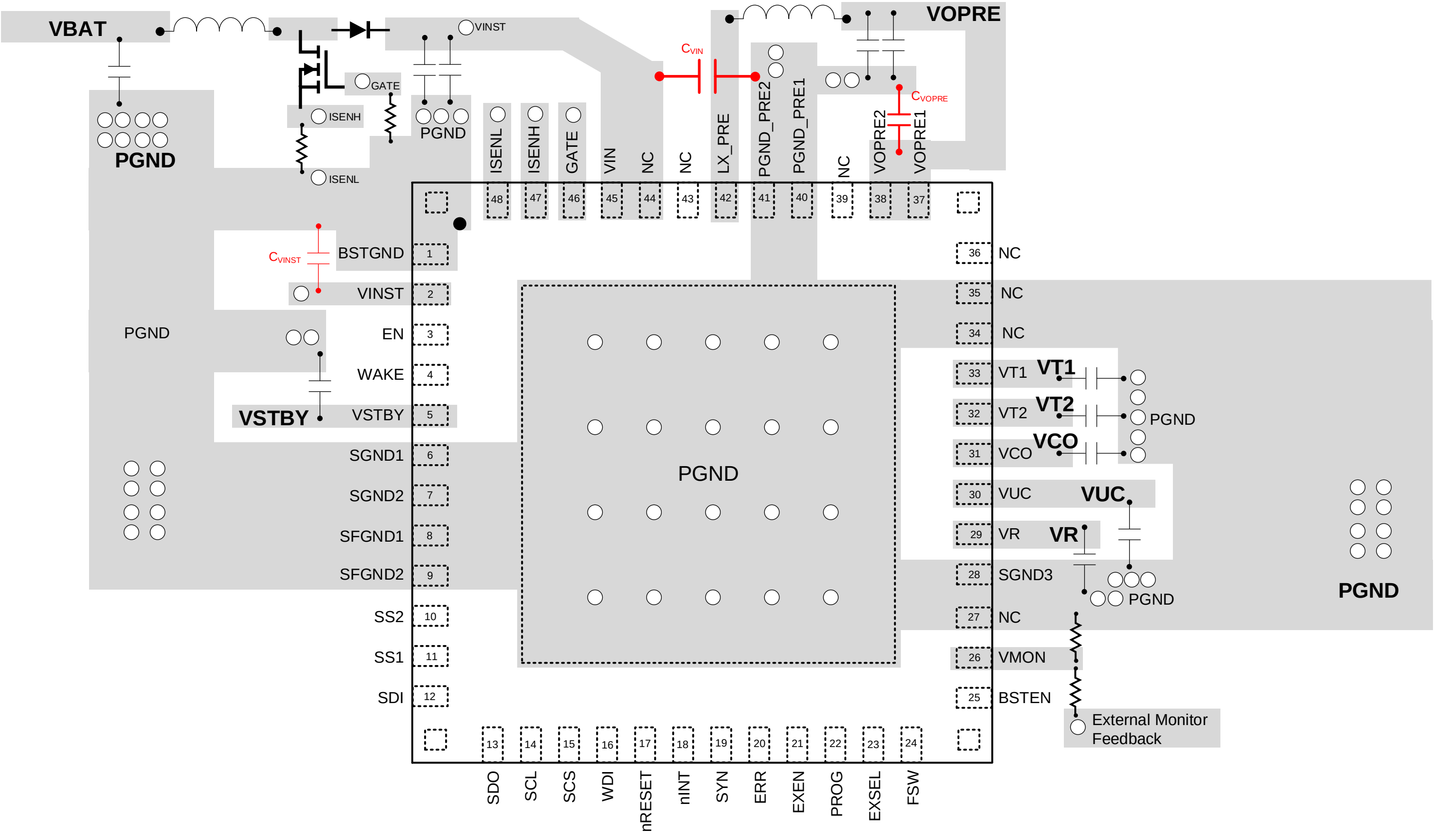


Figure 72. Suggested PCB Layout

SPI - Serial Peripheral Interface

1 Introduction

1.1 Main Functions

The Serial Peripheral Interface bus (SPI bus) is a synchronous serial communication link that uses a controller-peripheral architecture and operates in full duplex mode. The SA47301x communicates in peripheral mode and the controller (MCU) initiates the data frame. The SCS pin is used for peripheral chip select which allows multiple peripheral devices connected to SPI bus. The MCU pulls low the SCS pin and generates the clock signal with a lower than maximum allowable frequency to start the communication.

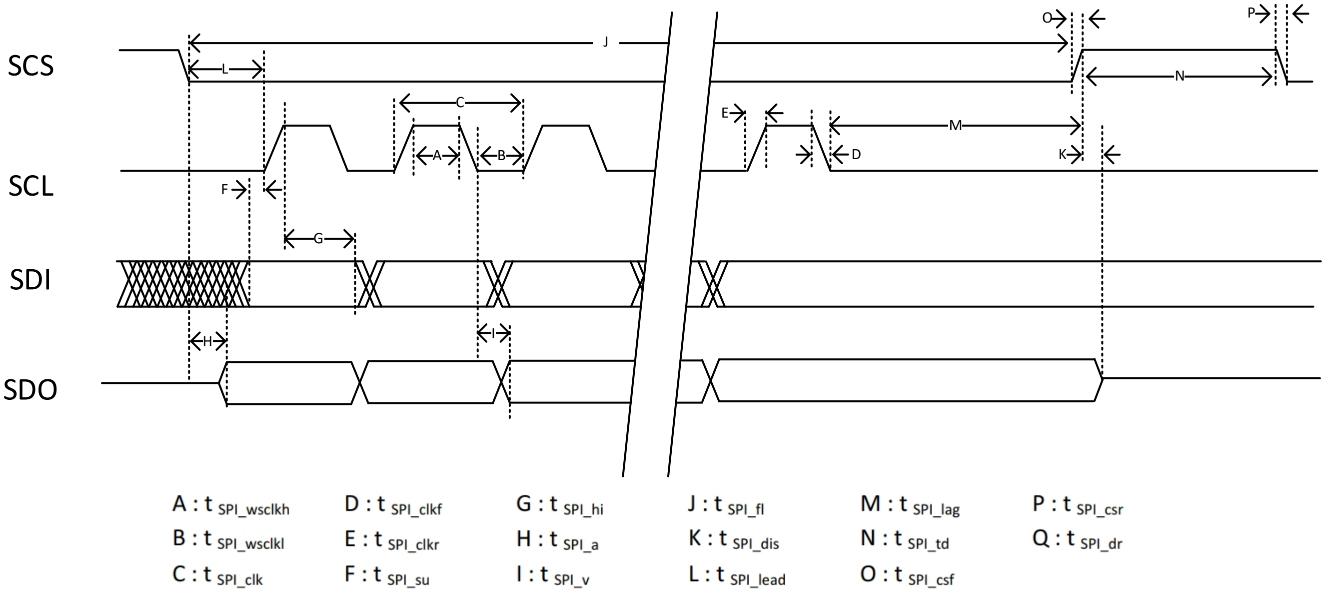


Figure 73. SPI Timing

1.2 Functional Description

The data on pin SDI (Data Input) and SDO (Data Output) are captured on the rising edge of pin SCL (SPI clock) and shifted on the falling edge of pin SCL.

The structure of a valid SPI sequence is shown below:

- CMD-bit: read or write selection. A read operation has to start with CMD-bit being 1’b0 and a write operation has to start with CMD-bit being 1’b1.
- A5~A0 bits: Register address.
- D7~D0 bits: Control bits. In read command, SDI[D7:D0] bits are recommended to be 0. In write command, SDI[D7:D0] bits are the data that needs to be written to the register.
- T bit: parity message sent by the MCU. The data for the parity calculation consists of CMD-bit, SDI[A5:A0], SDI[D7:D0]. If the number of ‘1’ in the SDI data stream is odd, the parity bit will be set to ‘1’, otherwise the parity bit should be set to 0.

For write operations, the write command to SDI is looped back to SDO.

The structure of the output data for a valid SPI sequence is presented below:

- Most significant bit: 1’b1.
- S5~S0 bits: Status bits are all set to 0 in read operation.

- D7~D0 bits: Control bits. For read commands, SDO[D7:D0] bits are the data of corresponding register bits.
- T bit: Parity message sent by the SA47301x. The data for the parity calculation consists of CMD-bit, SDO[S5:S0], SDO[D7:D0]. If the number of '1' in the SDO data stream is odd, the parity bit will be set to '1', otherwise the parity bit should be set to 0.

In the written data, parity checks are performed on the CMD bit, the six address bits and the eight data bits.

If the state machine (FSM) is in INIT state, NORMAL state, WAKE state or SLEEP state, the peripheral device can be configured at any time through SPI. The maximum clock frequency of SPI is decreased during SLEEP state.

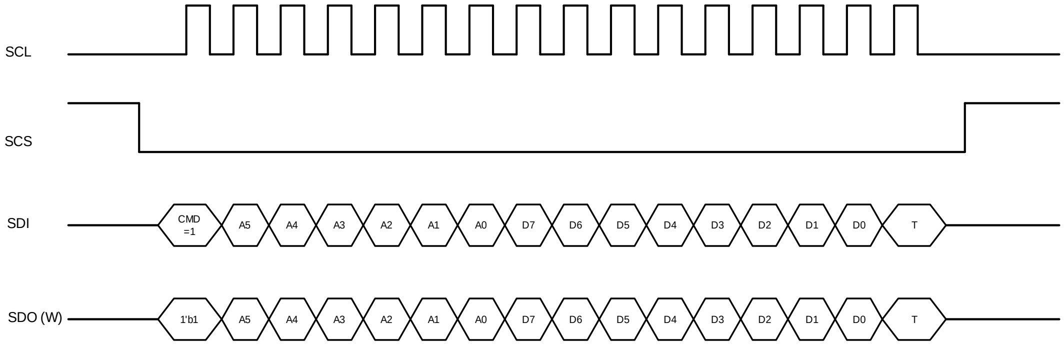


Figure 74. Write to a Register

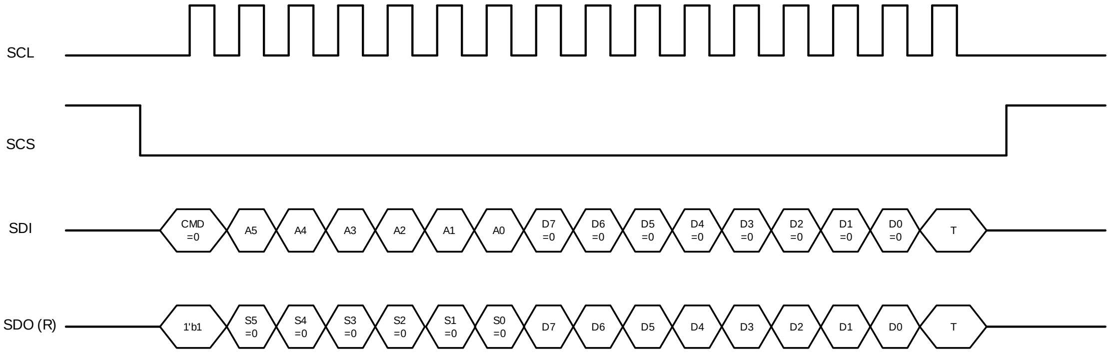


Figure 75. Read from a Register

1.3 SPI Errors

In order to ensure normal communication between MCU and the SA47301x, read and write commands sent by the MCU must meet the following rules:

1) SCS is low for less than frame duration time t_{SPI_fl}. if the SCS is low for more than frame duration time t_{SPI_fl} during write command, write data is ignored and the output driver for SDO is turned off internally by the device after t_{SPI_fl}. As long as SCS is low for less than t_{SPI_fl}, it will provide read data every SPI clock cycle. The invalid frame duration status flag is set and an interrupt is generated when this SPI error occurs.
2) When SCS is low, the number of SPI clock cycles is 16. If the number of clock cycles is wrong during write command, write data will be ignored. If the number of clock cycles is different than 16 during read command, the device will provide read data each SPI clock cycle. The wrong number of SPI clock cycle status flag is set and an interrupt is generated when this SPI error occurs.
3) The parity bit is correct during write command. If the parity bit is wrong during write, write data is ignored. The parity error status flag is set and an interrupt is generated when this SPI error occurs.

Interrupts on SPI errors are initiated only after SCS has been driven high or the frame time-out occurred.

2 SPI Write Access to Protected Registers

In order to prevent accidental overwriting, some specific registers (0x04-0x0A) are password protected registers. The MCU can read the LOCK bit in the register PROTSTAT to check the status of the protection.

A dedicated 32-bit UNLOCK sequence send by SPI is needed for write access to these protected registers. The UNLOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xAB; 2:0xEF; 3:0x56; 4:0x12), these four bytes have to be sent consecutively to the register KEY without any other SPI command in between. The device will reset the sequence detection when any of the following events occur:

1) Other write access in between.
2) Read operation in between.

An interrupt is generated to indicate the above wrong operation and a new sequence from beginning is needed for another UNLOCK try.

The MCU can check whether each written byte is correct and writing access to protected register is unlocked by reading the register PROTSTAT. All protected registers can be modified if the UNLOCK sequence has been performed successfully.

The MCU shall read back the protected register values and verify the correctness by checking data to ensure proper writing to the protected configuration request registers. Since the data bits written to the protected configuration request registers are send back inverted during the read operation, the MCU can check the correctness of the written data by following steps:

1) Writes the expected value to the protected register when access to protected register is unlocked.
2) Read back the protected register values.
3) The MCU can calculate an XOR of the register data read and expected. If the register data is correct, the results should be 0xFF. The SA47301x will not check the correctness of the values in the register.

The access to the protected registers is possible in INIT, NORMAL and WAKE states.

A dedicated 32-bit LOCK sequence send by SPI is needed to make the configuration of these protected registers take effect. The LOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xDF; 2:0x34; 3:0xBE; 4:0xCA). These four bytes have to be sent consecutively to the register KEY without any other SPI commands in between. The device will reset the sequence detection when any of the following event occurs:

1) Other write access in between.
2) Read operation in between.

An interrupt is generated to indicate a wrong operation and a new sequence, starting from the beginning, is needed for another LOCK try.

The MCU can check whether each written byte is correct and writing access to protected register is locked by reading the register PROTSTAT. All protected register data cannot be modified if the LOCK sequence has been performed successfully.

The configuration registers and all internal functions will be updated with the values from the protected configuration request registers after a successful LOCK sequence is detected. To guarantee that all registers are configured properly, the MCU can write a new value into a particular register or read back a register which is supposed to be unchanged. After successfully execution of the LOCK sequence (RSYSPCFG0, RSYSPCFG1, RWDCFG0, RWDCFG1, RFWDCFG, RWWDCFG0, RWWDCFG1), all protected configuration request registers will be taken over into the configuration so that the SA47301x does not support partial reconfiguration of the protected registers.

An internal configuration time of max. 60μs (delay until any new commands are present) has to be considered after the LOCK sequence to ensure that the new configuration is being used.

A list of the protected registers is shown below：

1) All watchdog configuration registers for window watchdog and functional watchdog, and enabling of watchdog while the state machine is in SLEEP state.

2) All Error pin monitoring configuration registers, and enabling of Error pin monitoring while the state machine is in SLEEP state.

3) A dedicated register to enable or disable the LDO_Stby.

4) Delay time between SS1 and SS2.

It is always possible to read the protected configuration registers.

3 SPI Write Initiated State Transition Request and Regulator Configuration

Two separated registers DEVCTRL and DEVCTRLN include the following requests:

1) State transition request includes “go to INIT”, “go to NORMAL”, “go to SLEEP”, “go to STANDBY” and “go to WAKE”.

2) Tracker 2 enable/disable request.

3) Tracker 1 enable/disable request.

4) LDO_COM enable/disable request.

5) LDO_REF enable/disable request.

The transition of the State machine can be initiated using SPI commands. Because the SPI command contains the state transition request command and some post regulators enabling/disabling command, if the state of any selectable voltage source (post regulators include Tracker1, Tracker2, LDO_COM and LDO_REF) is expected to change for the next state, this information has to be sent together with the command into the same register. The same approach can be applied to the particular post regulator which the setting is supposed to change when the state needs to kept unchanged.

The request data must be sequentially written to two separate registers (DEVCTRL and DEVCTRLN) for requesting a state transition and/or a change of the LDO configuration. The request data is valid and will be taken over with the rising edge of the SCS at the end of the second command only when all of the following conditions are met:

1) The data written to DEVCTRLN have to be inverted bitwise compared to the data written to DEVCTRL.

2) First DEVCTRL and second DEVCTRLN without any other SPI command in between.

If the request data sequence is written incorrectly or DEVCTRLN is not inverted for DEVCTRL, the request is invalid and will be rejected, an interrupt is generated to indicate this error and the corresponding status flag (NO_OP) is set. According to the State Machine, if the state transition request is invalid, the request is ignored without issuing an interrupt.

Register Description

1 Register Type Abbreviations Table

Register Type Abbreviations	Description
*R0	Registers that are being reset only in case of a POR.
*R1	Registers that are being reset only in case of STANDBY and a POR.
*R2	Registers that are being reset only in case of FAILSAFE, STANDBY and a POR.
*R3	Registers that are being reset in case of “Move to INIT” event, FAILSAFE, STANDBY and a POR.
r	Bits that are readable (read)
rw	Bits that are readable and writable (read-write)
rwp	Bits that are readable and writable but protected by register PROTCFG (read-write-protected)
rw1c	Bits that are readable and to clear the bit you have to write a 1 to it. (read-write-1-to-clear). Flag-bits are updated based on the occurred condition.
rwhc	Bits that are readable and writable after writing the operation is triggered, once this is done successfully the bit is cleared by hardware. (read-write-hardware-cleared)
rwhu	Bits that are readable and writable, after the operation the bit is updated by hardware. (read-write-hardware-updated)

2 Register Map Summary

Register Address	Register Name	Reset (Default) Value (HEX)	Register Description	Type
0x00	DEVCFG0	0x08	Device Configuration 0	**Bit[7:6] *R0** Bit[5:0] *R2
0x01	DEVCFG1	0x06	Device Configuration 1	*R0
0x02	DEVCFG2	0x00	Device Configuration 2	*R2
0x03	PROTCFG	0x00	Protection Register	*R2
0x04	SYSPCFG0	0x01	Protected System Configuration Request 0	***R0**
0x05	SYSPCFG1	0x08	Protected System Configuration Request 1	Bit [7:5] *R1 Bit [4:0] *R3
0x06	WDCFG0	0x9B	Protected Watchdog Configuration Request 0	*R3
0x07	WDCFG0	0x09	Protected Watchdog Configuration Request 1	*R3
0x08	FWDCFG	0x0B	Protected Functional Watchdog Configuration Request	*R3
0x09	WWDCFG0	0x06	Protected Window Watchdog Configuration Request 0	*R3
0x0A	WWDCFG1	0x0B	Protected Window Watchdog Configuration Request 1	*R3
0x0B	RSYSPCFG0	0x01	System Configuration 0 Status	*R0
0x0C	RSYSPCFG1	0x08	System Configuration 1 Status	Bit [7:5] *R1 Bit [4:0] *R3
0x0D	RWDCFG0	0x9B	Watchdog Configuration 0 Status	*R3
0x0E	RWDCFG1	0x09	Watchdog Configuration 1 Status	*R3
0x0F	RFWDCFG	0x0B	Functional Watchdog Configuration Status	*R3
0x10	RWWDCFG0	0x06	Window Watchdog Configuration 0 Status	*R3
0x11	RWWDCFG1	0x09	Window Watchdog Configuration 1 Status	*R3
0x12	WKTIMCFG0	0x00	Wake Timer Configuration 0	***R0**
0x13	WKTIMCFG1	0x00	Wake Timer Configuration 1	***R0**
0x14	WKTIMCFG2	0x00	Wake Timer Configuration 2	***R0**

0x15	DEVCTRL	0x00	Device Control Request	*R2
0x16	DEVCTRLN	0x00	Device Control Inverted Request	*R2
0x17	WWDSCMD	0x00	Window Watchdog Service Command	*R2
0x18	FWDRSP	0x00	Functional Watchdog Response Command	*R2
0x19	FWDRSPSYNC	0x00	Functional Watchdog Response Command with Synchronization	*R2
0x1A	SYSFAIL	0x00	Failure Status Flags	*R1
0x1B	INITERR	0x00	Init Error Status Flags	*R2
0x1C	IF	0x00	Interrupt Flags	*R2
0x1D	SYSSF	0x00	System Status Flags	*R2
0x1E	WKSF	0x00	Wakeup Status Flags	*R2
0x1F	SPISF	0x00	SPI Status Flags	*R2
0x20	MONSF0	0x00	Monitor Status Flags 0	*R1
0x21	MONSF1	0x00	Monitor Status Flags 1	*R1
0x22	MONSF2	0x00	Monitor Status Flags 2	*R2
0x23	MONSF3	0x00	Monitor Status Flags 3	*R1
0x24	OTFAIL	0x00	Over Temperature Failure Status Flags	*R1
0x25	OTWRNSF	0x00	Over Temperature Warning Status Flags	*R2
0x26	VMONSTAT	0x00	Voltage Monitor Status	*R2
0x27	DEVSTAT	0x00	Device Status	*R2
0x28	PROTSTAT	0x01	Protection Status	*R1
0x29	WWDSTAT	0x30	Window Watchdog Status	*R3
0x2A	FWDSTAT0	0x00	Functional Watchdog Status 0	*R3
0x2B	FWDSTAT1	0x00	Functional Watchdog Status 1	*R3
0x2C	ABIST_CTRL0	0x00	ABIST Control0	Bit [7:4] *R1 Bit [3:0] *R2
0x2E	ABIST_SELECT0	0x00	ABIST Select 0	*R2
0x2F	ABIST_SELECT1	0x00	ABIST Select 1	*R2
0x30	ABIST_SELECT2	0x00	ABIST Select 2	*R2
0x31	BCK_FREQ_CHANGE	0x00	Buck Switching Frequency Change	*R2
0x32	BCK_FRE_SPREAD	0x00	Buck Frequency spread	*R2
0x33	BCK_MAIN_CTRL	0x00	Buck Main Control	*R2
0x36	Function Control	0x01	Function Control Register	*R0
0x3C	MCSMON	0x00	Microcontroller Supervision Monitor	*R2
0x3F	GTM	0x02	Global Test Mode	*R2

◆ Slave Device Address: 59H(5AH or 5BH)+W/R

Module	Base Address	End Address	Note
BusInterface	0x00	0x3F	Slave Interface

3 Register and Data

◆ Device Configuration 0 Register Address: 00H

Register Name		DEVCFG0		Device Configuration Register 0			
Address				0x00			
Name	Bit	Type	Reset Value	Description			
WKTIMEN	7	rw	0	Wake timer enable			
				0=Wake timer disabled		1=Wake timer enabled in SLEEP or STANDBY state	
WKTIMCYC	6	rw	0	Wake timer cycle period			
				0=1ms		1=1s	
Reserved	5:4	/	0				
TRDEL	3:0	rw	1000	Transition delay to Standby and Sleep State			
				0000=100us	0001=200us	0010=300us	0011=400us
				0100=500us	0101=600us	0110=700us	0111=800us
				1000=900us	1001=1000us	1010=1100us	1011=1200us
				1100=1300us	1101=1400us	1110=1500us	1111=1600us

◆ Device Configuration 1 Register Address: 01H

Register Name		DEVCFG1		Device Configuration Register 1			
Address				0x01			
Name	Bit	Type	Reset Value	Description			
Reserved	7:4	/	0000				
RESDEL	3:0	rw	0110	nRESET release delay time			
				0000=200us	0001=400us	0010=800us	0011=1ms
				0100=2ms	0101=4ms	0110=10ms	0111=15ms
				1000=30ms	1001=60ms	/	/

◆ Device Configuration 2 Register Address: 02H

Register Name		DEVCFG2		Device Configuration Register 2	
Address				0x02	
Name	Bit	Type	Reset Value	Description	
EXSEL	7	r	Depend on Pin EXSEL	External buck regulator enable status	
				0= External buck regulator disabled	1= External buck regulator enabled
BSTEN	6	r	Depend on Pin BSTEN	Step-up converter enable status	
				0= Disabled	1= Enabled
FSW	5	r	Depend on Pin FSW	Step-down converters frequency selection status	
				0=Step-down converters runs on low frequency range	1=Step-down converters runs on high frequency range
CMONEN	4	rw	0	LDO_UC current monitor enable for transition to a low power state For STANDBY and SLEEP transition. The setting is overwritten in	

				SLEEP as current monitoring is always enabled.			
				0= Disabled	1= Enabled		
CTHR	3:2	rw	00	LDO_UC current monitoring threshold value			
				00=10mA	01=30mA	10=60mA	11=100mA
SYNCPHA	1	rw	0	External synchronization output phase			
				0=No phase shift	1=180 phase shift		
SYNCEN	0	rw	0	Synchronization output for external buck regulator enable			
				0=Disable	1=Enable		

◆

Protection Register Address: 03H

Register Name		**PROTCFG**		**Protection Register**
Address				0x03
Name	Bit	Type	Reset Value	Description
KEY	7:0	rw	00000000	Protection key Protection key register to request write access to protected registers. Unlock: write 32-bit sequence of 4 consecutive bytes (1: 0xAB 2:0xEF 3:0x56 4:0x12) to unlock access to protected registers. Lock: write 32-bit sequence of 4 consecutive bytes (1: 0xDF 2:0x34 3:0xBE 4:0xCA) to lock access to protected registers. All configured values are applied to SSC and WD module after the lock. AB H Key 1 to unlock protected registers. EF H Key 2 to unlock protected registers. 56 H Key 3 to unlock protected registers. 12 H Key 4 to unlock protected registers. DF H Key 1 to lock protected registers. 34 H Key 2 to lock protected registers. BE H Key 3 to lock protected registers. CA H Key 4 to lock protected registers.

◆

Protected System Configuration Request 0 Register Address: 04H

Register Name		**SYSPCFG0**		**Protected System Configuration Request 0 Register**	
Address				0x04	
Name	Bit	Type	Reset Value	Description	
Reserved	7:1	r	0000000	not used bits -shall be written as 0 and will always return 1 upon read	
STBYEN	0	rwp	1	LDO_STBY enable	
				0=Disable	1=Enable

◆

Protected System Configuration Request 1 Register Address: 05H

Register Name		**SYSPCFG1**		**Protected System Configuration Request 1 Register**			
Address				0x05			
Name	Bit	Type	Reset Value	Description			
SS2DEL	7:5	rwp	000	SS2 pin pull low delay time program Applied for transitions from NORMAL to INIT, WAKE and SLEEP state			
				000=no delay	001=10ms	010=50ms	011=100ms
				100=250ms	101=1250ms	110=2500ms	/
ERRSLPEN	4	rwp	0	Error monitor enable in SLEEP State			
				0= ERR pin monitor is disabled in SLEEP state	1= ERR pin monitor can be active in SLEEP state depending on ERREN bit value.		

ERREN	3	rwp	1	Error monitor enable program			
				0= Disabled	1= Enabled		
ERRRECEN	2	rwp	0	ERR pin monitor recovery delay enable program			
				0= Disabled	1= Enabled		
ERRRECTIM	1:0	rwp	00	ERR pin monitor recovery delay time program			
				00=1ms	01=2.5ms	11=5ms	11=10ms

◆

Protected Watchdog Configuration Request 0 Register Address: 06H

Register Name		**WDCFG0**		**Protected Watchdog Configuration Request 0**	
Address				0x06	
Name	Bit	Type	Reset Value	Description	
WWDETHR	7:4	rwp	1001	Window watchdog error counter threshold program WWD error threshold to generate reset and enter INIT state.	
				0000=0 times，0001=1 time … 1111=15 times	
WWDEN	3	rwp	1	Window watchdog enable program	
				0= Disabled	1= Enabled
FWDEN	2	rwp	0	Functional watchdog enable program	
				0= Disabled	1= Enabled
WWDTSEL	1	rwp	1	Window watchdog source selection This is ignored when window watchdog is disabled.	
				0= External WDI input used as a WWD source	1= WWD is triggered by SPI write to WWDSCMD register
WDCYC	0	rwp	1	Watchdog cycle time program	
				0=0.1ms tick period	1=1ms tick period

◆

Protected Watchdog Configuration Request 1 Register Address: 07H

Register Name		**WDCFG1**		**Protected Watchdog Configuration Request 1**	
Address				0x07	
Name	Bit	Type	Reset Value	Description	
Reserved	7	/	0	not used bits shall be written as 0 and will always return 1 upon read	
				/	
WDCYCDIV	6	rwp	0	Request enable of additional divider by 10 for watchdog cycle time (WDCYC) configuration, Data bits are sent inverted to SPI upon read access.	
				0=Disabled	1=Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled
Reserved	5	/	0	not used bits shall be written as 0 and will always return 1 upon read	
				/	
WDSLPEN	4	rwp	0	Watchdog enable in SLEEP state progaram	
				0= Disabled in SLEEP state	1= Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode
FWDETHR	3:0	rwp	1001	Functional watchdog error counter threshold program FWD error threshold to generate reset and enter INIT state.	
				0000=0 times，0001=1 time … 1111=15 times	

◆

Protected Functional Watchdog Configuration Request Register Address: 08H

Register Name		FWDCFG		Protected Functional Watchdog Configuration Request			
Address				0x08			
Name	Bit	Type	Reset Value	Description			
Reserved	7:5	/	000	not used bits shall be written as 0 and will always return 1 upon read			
				/			
WDHBTP	4:0	rwp	01011	Functional watchdog heartbeat timer period Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).			
				00000=50wd cycles	00001=100 wd cycles	00010=150 wd cycles	00011=200 wd cycles
				00100=250wd cycles	00101=300 wd cycles	00110=350 wd cycles	00111=400 wd cycles
				01000=450wd cycles	01001=500 wd cycles	01010=550 wd cycles	01011=600 wd cycles
				01100=650wd cycles	01101=700 wd cycles	01110=750 wd cycles	01111=800 wd cycles
				10000=850wd cycles	10001=900 wd cycles	10010=950 wd cycles	10011=1000 wd cycles
				10100=1050wd cycles	10101=1100 wd cycles	10110=1150 wd cycles	10111=1200 wd cycles
				11000=1250wd cycles	11001=1300 wd cycles	11010=1350 wd cycles	11011=1400 wd cycles
				11100=1450wd cycles	11101=1500 wd cycles	11110=1550 wd cycles	11111=1600 wd cycles

◆

Protected Window Watchdog Configuration Request 0 Register Address: 09H

Register Name		WWDCFG0		Protected Window Watchdog Configuration Request 0			
Address				0x09			
Name	Bit	Type	Reset Value	Description			
Reserved	7:5	/	/	not used bits shall be written as 0 and will always return 1 upon read			
				/			
CW	4:0	rwp	00110	Window watchdog T_{MIN} program Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).			
				00000=50wd cycles	00001=100 wd cycles	00010=150 wd cycles	00011=200 wd cycles
				00100=250wd cycles	00101=300 wd cycles	00110=350 wd cycles	00111=400 wd cycles
				01000=450wd cycles	01001=500 wd cycles	01010=550 wd cycles	01011=600 wd cycles
				01100=650wd cycles	01101=700 wd cycles	01110=750 wd cycles	01111=800 wd cycles
				10000=850wd cycles	10001=900 wd cycles	10010=950 wd cycles	10011=1000 wd cycles
				10100=1050wd cycles	10101=1100 wd cycles	10110=1150 wd cycles	10111=1200 wd cycles
				11000=1250wd cycles	11001=1300 wd cycles	11010=1350 wd cycles	11011=1400 wd cycles
				11100=1450wd cycles	11101=1500 wd cycles	11110=1550 wd cycles	11111=1600 wd cycles

◆ **Protected Window Watchdog Configuration Request 1 Register Address: 0AH**

Register Name		WWDCFG1		Protected Window Watchdog Configuration Request 1			
Address				0x0A			
Name	Bit	Type	Reset Value	Description			
Reserved	7:5	/	/	not used bits shall be written as 0 and will always return 1 upon read			
				/			
OW	4:0	rwp	01011	Window watchdog T_{MARGIN} program Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).			
				00000=50wd cycles	00001=100 wd cycles	00010=150 wd cycles	00011=200 wd cycles
				00100=250wd cycles	00101=300 wd cycles	00110=350 wd cycles	00111=400 wd cycles
				01000=450wd cycles	01001=500 wd cycles	01010=550 wd cycles	01011=600 wd cycles
				01100=650wd cycles	01101=700 wd cycles	01110=750 wd cycles	01111=800 wd cycles
				10000=850wd cycles	10001=900 wd cycles	10010=950 wd cycles	10011=1000 wd cycles
				10100=1050wd cycles	10101=1100 wd cycles	10110=1150 wd cycles	10111=1200 wd cycles
				11000=1250wd cycles	11001=1300 wd cycles	11010=1350 wd cycles	11011=1400 wd cycles
				11100=1450wd cycles	11101=1500 wd cycles	11110=1550 wd cycles	11111=1600 wd cycles

◆ **System Configuration 0 Status Register Address: 0BH**

Register Name		RSYSPCFG0		System Configuration 0 Status Register	
Address				0x0B	
Name	Bit	Type	Reset Value	Description	
Reserved	7:1	/	0000000	not used bits shall be written as 0 and will always return 1 upon read	
				/	
STBYEN	0	r	1	LDO_STBY enable status Current configuration of LDO_STBY enable. Valid for all device states except FAILSAFE	
				0=Disabled	1=Enabled

◆ **System Configuration 1 Status Register Address: 0CH**

Register Name		RSYSPCFG1		System Configuration 1 Status Register			
Address				0x0C			
Name	Bit	Type	Reset Value	Description			
SS2DEL	7:5	r	0	SS2 pull low delay time status Current configuration of SS2 pin delay time applied for transitions from NORMAL to INIT, WAKE and SLEEP state. Bits have different reset class than whole register. The Bits are reset according to *R2			
				000=no delay	001=10ms	010=50ms	011=100ms
				100=250ms	101=1250ms	110=2500ms	/
ERRSLPEN	4	r	0	ERR pin monitor functionality enable status while the device is in SLEEP state			
				0= ERR pin monitor is disabled in SLEEP		1= ERR pin monitor can be active in SLEEP depending on ERREN bit	

					value
ERREN	3	r	1	ERR pin monitor enable status	
				0= Disabled	1= Enabled
ERRRECEN	2	r	0	ERR pin monitor recover enable status	
				0= Disabled	1= Enabled
ERRREC	1:0	r	0	ERR pin monitor recovery time status Current configuration of ERR pin monitor recovery time.	
				00=1ms	01=2.5ms
				10=5ms	11=10ms

◆

Watchdog Configuration 0 Status Register Address: 0DH

Register Name		**RWDCFG0**		**Watchdog Configuration 0 Status Register**	
Address				0x0D	
Name	Bit	Type	Reset Value	Description	
WWDETHR	7:4	r	1001	Current configuration of WWD error counter threshold to generate reset and enter INIT state.	
WWDEN	3	r	1	Window watchdog enable status Current configuration of WWD enable.	
				0= Disabled	1= Enabled
FWDEN	2	r	0	Functional watchdog enable status Current configuration of FWD enable.	
				0= Disabled	1= Enabled
WWDTSEL	1	r	1	Window watchdog trigger selection status Current configuration of WWD trigger selection. This is ignored when window watchdog is disabled.	
				0= External WDI input used as a WWD trigger	1= WWD is triggered by SPI write to WWDSCMD register
WDCYC	0	r	1	Current configuration of watchdog cycle time	
				0=0.1ms tick period	1= 1ms tick period

◆

Watchdog Configuration 1 Status Register Address: 0EH

Register Name		**RWDCFG1**		**Watchdog Configuration 1 Status Register**	
Address				0x0E	
Name	Bit	Type	Reset Value	Description	
Reserved	7	/	0		
WDCYCDIV	6	r	0	Additional divider by 10 for watchdog cycle time (WDCYC) configuration enable status	
				0=Disable	1=Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled
Reserved	5	/	0		
WDSLPEN	4	r	0	Current configuration of WD functionality enable for SLEEP state.	
				0= Disabled	1= Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode
FWDETHR	3:0	r	1001	Functional watchdog error counter threshold status Current configuration of FWD error counter threshold to generate reset and enter INIT state.	

◆

Functional Watchdog Configuration Status Register Address: 0FH

Register Name		RFWDCFG		Functional Watchdog Configuration Status Register			
Address				0x0F			
Name	Bit	Type	Reset Value	Description			
Reserved	7:5	/	000				
WDHBTP	4:0	r	01011	Current configuration of FWD heartbeat timer period defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).			
				00000=50wd cycles	00001=100 wd cycles	00010=150 wd cycles	00011=200 wd cycles
				00100=250wd cycles	00101=300 wd cycles	00110=350 wd cycles	00111=400 wd cycles
				01000=450wd cycles	01001=500 wd cycles	01010=550 wd cycles	01011=600 wd cycles
				01100=650wd cycles	01101=700 wd cycles	01110=750 wd cycles	01111=800 wd cycles
				10000=850wd cycles	10001=900 wd cycles	10010=950 wd cycles	10011=1000 wd cycles
				10100=1050wd cycles	10101=1100 wd cycles	10110=1150 wd cycles	10111=1200 wd cycles
				11000=1250wd cycles	11001=1300 wd cycles	11010=1350 wd cycles	11011=1400 wd cycles
				11100=1450wd cycles	11101=1500 wd cycles	11110=1550 wd cycles	11111=1600 wd cycles

◆

Window Watchdog Configuration 0 Status Register Address: 10H

Register Name		RWWDCFG0		Windows Watchdog Configuration 0 Status Register			
Address				0x10			
Name	Bit	Type	Reset Value	Description			
Reserved	7:5	/	000				
CW	4:0	r	00110	Current configuration of WWD T_{MIN} defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC)			
				00000=50wd cycles	00001=100 wd cycles	00010=150 wd cycles	00011=200 wd cycles
				00100=250wd cycles	00101=300 wd cycles	00110=350 wd cycles	00111=400 wd cycles
				01000=450wd cycles	01001=500 wd cycles	01010=550 wd cycles	01011=600 wd cycles
				01100=650wd cycles	01101=700 wd cycles	01110=750 wd cycles	01111=800 wd cycles
				10000=850wd cycles	10001=900 wd cycles	10010=950 wd cycles	10011=1000 wd cycles
				10100=1050wd cycles	10101=1100 wd cycles	10110=1150 wd cycles	10111=1200 wd cycles
				11000=1250wd cycles	11001=1300 wd cycles	11010=1350 wd cycles	11011=1400 wd cycles
				11100=1450wd cycles	11101=1500 wd cycles	11110=1550 wd cycles	11111=1600 wd cycles

◆ Window Watchdog Configuration 1 Status Register Address: 11H

<table>
<tr><th colspan="2">Register Name</th><th colspan="2">RWWDCFG1</th><th colspan="4">Windows Watchdog Configuration 1 Status Register</th></tr>
<tr><td colspan="2">Address</td><td colspan="2"></td><td colspan="4">0x11</td></tr>
<tr><td>Name</td><td>Bit</td><td>Type</td><td>Reset Value</td><td colspan="4">Description</td></tr>
<tr><td>Reserved</td><td>7:5</td><td>/</td><td>000</td><td colspan="4"></td></tr>
<tr><td rowspan="9">OW</td><td rowspan="9">4:0</td><td rowspan="9">r</td><td rowspan="9">01011</td><td colspan="4">Current configuration of WWD T_{MARGIN} defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC)</td></tr>
<tr><td>00000=50wd cycles</td><td>00001=100 wd cycles</td><td>00010=150 wd cycles</td><td>00011=200 wd cycles</td></tr>
<tr><td>00100=250wd cycles</td><td>00101=300 wd cycles</td><td>00110=350 wd cycles</td><td>00111=400 wd cycles</td></tr>
<tr><td>01000=450wd cycles</td><td>01001=500 wd cycles</td><td>01010=550 wd cycles</td><td>01011=600 wd cycles</td></tr>
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<tr><td>11100=1450wd cycles</td><td>11101=1500 wd cycles</td><td>11110=1550 wd cycles</td><td>11111=1600 wd cycles</td></tr>
</table>

◆ Wake Timer Configuration 0 Register Address: 12H

Register Name		WKTIMCFG0		Wake Timer Configuration 0 Register
Address				0x12
Name	Bit	Type	Reset Value	Description
TIMVALL	7:0	rw	00000000	Wake timer value lower bits Bits (7:0) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).

◆ Wake Timer Configuration 1 Register Address: 13H

Register Name		WKTIMCFG1		Wake Timer Configuration 1 Register
Address				0x13
Name	Bit	Type	Reset Value	Description
TIMVALM	7:0	rw	00000000	Wake timer value middle bits Bits (15:8) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).

◆ Wake Timer Configuration 2 Register Address: 14H

Register Name		WKTIMCFG2		Wake Timer Configuration 2 Register
Address				0x14
Name	Bit	Type	Reset Value	Description
TIMVALH	7:0	rw	00000000	Wake timer value higher bits Bits (23:16) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).

◆ Device Control Request Register Address: 15H

Register Name		DEVCTRL		Device Control Request Register
Address				0x15
Name	Bit	Type	Reset Value	Description
TRK2EN	7	rw	0	Request tracker2 enable 0=VT2 will be disabled after valid request 1= VT2 will be enabled after valid request
TRK1EN	6	rw	0	Request tracker1 enable 0=VT1 will be disabled after valid request 1=VT1 will be enabled after valid request
COMEN	5	rw	0	Request LDO_COM enable 0= VCO will be disabled after valid request 1= VCO will be enabled after valid request
Reserved	4	/	0	
VREFEN	3	rw	0	Request LDO_REF enable 0= VR will be disabled after valid request 1= VR will be enabled after valid request
STATEREQ	2:0	rwhc	000	Request for device state transition Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW. 000=NONE 001=INIT 010=NORMAL 011=SLEEP 100=STANDBY 101=WAKE 110=RESERVED 111=RESERVED

◆ Device Control Inverted Request Register Address: 16H

Register Name		DEVCTRLN		Device Control Inverted Request Register
Address				0x16
Name	Bit	Type	Reset Value	Description
TRK2EN	7	rw	0	Request tracker2 enable 0=VT2 will be enabled after valid request 1= VT2 will be disabled after valid request
TRK1EN	6	rw	0	Request tracker1 enable 0=VT1 is enabled after valid request 1=VT1 is disabled after valid request
COMEN	5	rw	0	Request LDO_COM enable 0= VCO will be enabled after valid request 1= VCO will be disabled after valid request
Reserved	4	/	0	
VREFEN	3	rw	0	Request LDO_REF enable 0= VR will be enabled after valid request 1= VR will be disabled after valid request
STATEREQ	2:0	rwhc	000	Request for device state transition Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW. 000= RESERVED 001= RESERVED 010= WAKE 011= STANDBY 100= SLEEP 101= NORMAL 110= INIT 111= NONE

◆ Window Watchdog Service Commend Register Address: 17H

Register Name		WWDSCMD		Window Watchdog Service Commend Register
Address				0x17
Name	Bit	Type	Reset Value	Description
TRIG_STATUS	7	r	0	Last SPI trigger received
Reserved	6:1	/	00000	
TRIG	0	rw	0	Window watchdog SPI trigger command. Read TRIG_STATUS bit first and write inverted value to TRIG bit.

◆ Functional Watchdog Response Command Register Address: 18H

Register Name		FWDRSP		Functional Watchdog Response Command Register
Address				0x18
Name	Bit	Type	Reset Value	Description
FWDRSP	7:0	rw	00000000	Functional watchdog response. Write functional watchdog response bytes to this register

◆ Functional Watchdog Response Command with Synchronization Register Address: 19H

Register Name		FWDRSPSYNC		Functional Watchdog Response Command with Synchronization Register
Address				0x19
Name	Bit	Type	Reset Value	Description
FWDRSPS	7:0	rw	00000000	Functional watchdog heartbeat synchronization response. Write the last functional watchdog response byte to this register to synchronize/restart the heartbeat.

◆ Failure Status Flags Register Address: 1AH

Register Name		SYSFAIL		Failure Status Flags Register	
Address				0x1A	
Name	Bit	Type	Reset Value	Description	
INITF	7	rw1c	0	INIT failure flag INIT failure due to the third time INIT failure in row.	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
ABISTERR	6	rw1c	0	ABIST operation interrupted flag ABIST interrupted by any fault/event which is not part of ABIST	
				0= No fault, write 0 - no action	0= Fault occurred, write 1 to clear the flags
Reserved	5:3	/	000		
VMONF	2	rw1c	0	Voltage monitors failure flag Voltage monitor failure occurred which lead to FAILSAFE.	
				0=No fault, write 0 - no action	1=Fault occurred, write 1 to clear the flags, read MONSF0, MONSF1 and MONSF3 for details
OTF	1	rw1c	0	Over temperature failure flag	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags, read OTFAIL for details
VOLSELER	0	rwhc	0	Double Bit error on voltage selection flag Device entered FAILSAFE state due to internal voltage selection failure.	
				No fault, write 0 - no action	Fault occurred, write 1 to clear the flags

◆

Init Error Status Flags Register Address: 1BH

Register Name		INITERR		Init Error Status Flags Register	
Address				0x1B	
Name	Bit	Type	Reset Value	Description	
HARDERS	7	rw1c	0	Hard reset flag Hard reset has been generated due to the second INIT failure in row.	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
SOFTRES	6	rw1c	0	Soft reset flag Soft reset has been generated due to the first INIT failure.	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
ERRF	5	rw1c	0	MCU error monitor failure flag	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
FWDF	4	rw1c	0	Functional watchdog error counter overflow failure flag Functional watchdog error counter reached the error threshold.	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
WWDF	3	rw1c	0	Window watchdog error counter overflow failure flag Window watchdog error counter reached the error threshold	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
VMONF	2	rw1c	0	Voltage monitor failure flag Voltage monitor failure occurred which lead to INIT.	
				0=No fault, write 0 - no action	1=Fault occurred, write 1 to clear the flags, read MONSF2 for details
Reserved	1:0	rw1c	0		

◆

Interrupt flags Register Address: 1CH

Register Name		IF		Interrupt Flags Register	
Address				0x1C	
Name	Bit	Type	Reset Value	Description	
INTMISS	7	r	0	Interrupt not serviced in time flag Interrupt has not been serviced within $t_{INT,TO}$ time	
				0= No interrupt timeout happened	1= Interrupt timeout happened, cleared by hardware when all other flags in IF are cleared.
ABIST	6	rw1c	0	Requested ABIST operation performed flag	
				0= No fault, write 0 - no action	1= Fault occurred, write 1 to clear the flags
OTF	5	rw1c	0	Over temperature failure interrupt flag	
				0= No fault, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag, read OTFAIL for details
OTW	4	rw1c	0	Over temperature warning interrupt flag	
				0= No fault, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag, read OTWRNSF for details
MON	3	rw1c	0	Monitor interrupt flag	
				0= No fault, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag, read MONSF0, MONSF1, MONSF2 and MONSF3 for details
SPI	2	rw1c	0	SPI interrupt flag	
				0=No fault, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag, read SPISF for details
WK	1	rw1c	0	Wake interrupt flag Only set if device generates an interrupt when leaving SLEEP state.	

				0= No interrupt, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag, read WKSF for details
SYS	0	Rw1c	0	System interrupt flag	
				0= No interrupt, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag, read SYSSF for details

◆

System Status Flags Register Address: 1DH

Register Name		**SYSSF**		**System Status Flags Register**	
Address				0x1D	
Name	Bit	Type	Reset Value	Description	
Reserved	7:6	rw1c	0	/	
NO_OP	5	rw1c	0	State transition request failure flag Requested state transition via DEVCTRL & DEVCTRLN could not be performed because of wrong protocol.	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
TRFAIL	4	rw1c	0	Transition to low power states failed flag Transition to low power failed either due to the LDO_UC current monitor, WAK high level or a rising edge on ENA during transition delay time.	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
ERRMISS	3	rw1c	0	MCU error miss status flag Set only when SYSPCFG1.ERRRECEN='1'	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
FWDE	2	rw1c	0	Functional watchdog error interrupt flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
WWDE	1	rw1c	0	Window watchdog error interrupt flag	
				0= No fault, write 0 - no action	1= Interrupt flag active, write 1 to clear the flag
CFGE	0	rw1c	0	Protected configuration double bit error flag Double bit error occurred on protected configuration register. Status registers shall be read in order to determine which configuration has changed.	
				0= No interrupt, write 0 - no action	1= Event detected, write 1 to clear the flag

◆

Wakeup Status Flags Register Address: 1EH

Register Name		**WKSF**		**Wakeup Status Flags Register**	
Address				0x1E	
Name	Bit	Type	Reset Value	Description	
WAKST	7	r	0	WAKE input status	
				0= Voltage at pin WAKE is in low level signal range	1= Voltage at pin WAKE is in high level signal range
ENST	6	r	0	ENA input status	
				0= Voltage at pin EN is in low level signal range	1= Voltage at pin EN is in high level signal range
Reserved	5	/	0		
WKSPI	4	rw1c	0	Wakeup from SLEEP by SPI flag (GoToWAKE)	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
WKTIM	3	rw1c	0	Wake timer wakeup flag Bit will also be set if STANDBY state left because of wake timer expired.	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
CMON	2	rw1c	0	LDO_UC current monitor threshold wakeup flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

EN	1	rw1c	0	EN signal wakeup flag Bit will also be set if FAILSAFE or STANDBY state left because of EN.	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
WAKE	0	rw1c	0	WAKE signal wakeup flag Bit will also be set if FAILSAFE or STANDBY state left because of WAKE.	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆ SPI Status Flags Register Address: 1FH

Register Name		SPISF		SPI Status Flags Register	
Address				0x1F	
Name	Bit	Type	Reset Value	Description	
Reserved	7:5	rw1c	0	/	
LOCK	4	rw1c	0	LOCK or UNLOCK procedure error flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
DURE	3	rw1c	0	SPI frame duration error flag SCS low for more than 2 ms	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
Reserved	2	/	0		
LENE	1	rw1c	0	SPI frame length invalid flag, Number of detected SPI clock cycles different than 16.	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
PARE	0	rw1c	0	SPI frame parity error flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆ Monitor Status Flags 0 Register Address: 20H

Register Name		MONSF0		Monitor Status Flags 0 Register	
Address				0x20	
Name	Bit	Type	Reset Value	Description	
TRK2SG	7	rw1c	0	Tracker2 short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
TRK1SG	6	rw1c	0	Tracker1 short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
VREFSG	5	rw1c	0	LDO_REF short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
COMSG	4	rw1c	0	LDO_COM short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
VMONSG	3	rw1c	0	External buck short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
STBYSG	2	rw1c	0	LDO_STBY short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
UCSG	1	rw1c	0	LDO_UC short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
PREGSG	0	rw1c	0	Pre-regulator voltage short to ground status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆

Monitor Status Flags 1 Register Address: 21H

Register Name		MONSF1		Monitor Status Flags 1 Register	
Address				0x21	
Name	Bit	Type	Reset Value	Description	
TRK2OV	7	rw1c	0	Tracker2 over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
TRK1OV	6	rw1c	0	Tracker1 over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
VREFOV	5	rw1c	0	LDO_REF over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
COMOV	4	rw1c	0	LDO_COM over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
VMONOV	3	rw1c	0	External buck over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
STBYOV	2	rw1c	0	LDO_STBY over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
UCOV	1	rw1c	0	LDO_UC over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
PREGOV	0	rw1c	0	Pre-regulator voltage over voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆

Monitor Status Flags 2 Register Address: 22H

Register Name		MONSF2		Monitor Status Flags 2 Register	
Address				0x22	
Name	Bit	Type	Reset Value	Description	
TRK2UV	7	rw1c	0	Tracker2 under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
TRK1UV	6	rw1c	0	Tracker1 under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
VREFUV	5	rw1c	0	LDO_REF under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
COMUV	4	rw1c	0	LDO_COM under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
VMONUV	3	rw1c	0	External buck under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
STBYUV	2	rw1c	0	LDO_STBY under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
UCUV	1	rw1c	0	LDO_UC under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

PREGUV	0	rw1c	0	Pre-regulator voltage under voltage status flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆ Monitor Status Flags 3 Register Address: 23H

Register Name		**MONSF3**		**Monitor Status Flags 3 Register**	
Address				0x23	
Name	Bit	Type	Reset Value	Description	
BIASHI	7	rw1c	0	Bias current too high flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
BIASLOW	6	rw1c	0	Bias current too low flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
BG12OV	5	rw1c	0	Bandgap comparator over voltage condition flag (VBG1 ≥ VBG2 + 4%)	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
BG12UV	4	rw1c	0	Bandgap comparator under voltage condition flag (VBG1 ≤ VBG2 - 4%)	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
Reserved	3:1	/	0		
VBATOV	0	rw1c	0	Supply voltage VIN over voltage flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆ Over Temperature Failure Status Register Address: 24H

Register Name		**OTFAIL**		**Over Temperature Failure Status Register**	
Address				0x24	
Name	Bit	Type	Reset Value	Description	
MON	7	rw1c	0	Monitoring over temperature flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
Reserved	6:5	/	0		
COM	4	rw1c	0	LDO_COM over temperature flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
Reserved	3:2	/	0		
UC	1	rw1c	0	LDO_UC over temperature flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
PREG	0	rw1c	0	Pre-regulator over temperature flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆ **Over Temperature Warning Status Flags Register Address: 25H**

Register Name		OTWRNSF		Over Temperature Warning Status Flags Register	
Address				0x25	
Name	Bit	Type	Reset Value	Description	
Reserved	7:6	/	0		
VREF	5	rw1c	0	LDO_REF overload flag (over current for more than 1ms)	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
COM	4	rw1c	0	LDO_COM over temperature warning flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
Reserved	3	/	0		
STDBY	2	rw1c	0	LDO_STBY overload flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
UC	1	rw1c	0	LDO_UC over temperature warning flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag
PREG	0	rw1c	0	Pre-regulator over temperature warning flag	
				0= Write 0 - no action	1= Event detected, write 1 to clear the flag

◆ **Voltage Monitor Status Register Address: 26H**

Register Name		VMONSTAT		Voltage Monitor Status Register	
Address				0x26	
Name	Bit	Type	Reset Value	Description	
TRK2ST	7	r	0	Tracker2 voltage ready status	
				0= Voltage is out of range or not enabled	1= Voltage is OK
TRK1ST	6	r	0	Tracker1 voltage ready status	
				0= Voltage is out of range or not enabled	1= Voltage is OK
VREFST	5	r	0	LDO_REF voltage ready status	
				0= Voltage is out of range or not enabled	1= Voltage is OK
COMST	4	r	0	LDO_COM voltage ready status	
				0= Voltage is out of range or not enabled	1= Voltage is OK
VMONST	3	r	0	External buck ready status	
				0= Voltage is out of range or not enabled	1= Voltage is OK
STBYST	2	r	0	LDO_STBY voltage ready status	
				0= Voltage is out of range or not enabled	1= Voltage is OK
Reserved	1	/	0		
PREGST	0	r	0	Pre regulator (FB) voltage status	
				0= Voltage is out of range or not enabled	1= Voltage is OK

◆ **Device Status Register Address: 27H**

Register Name		DEVSTAT		Device Status Register
Address				0x27
Name	Bit	Type	Reset Value	Description
TRK2EN	7	r	0	Tracker2 voltage enable status

				0= Voltage is disabled		1= Voltage is enabled	
TRK1EN	6	r	0	Tracker1 voltage enable status			
				0= Voltage is disabled		1= Voltage is enabled	
COMEN	5	r	0	LDO_COM enable status			
				0= Voltage is disabled		1= Voltage is enabled	
STBYEN	4	r	0	Standby LDO enable status			
				0= Voltage is disabled		1= Voltage is enabled	
VREFEN	3	r	0	LDO_REF enable status			
				0= Voltage is disabled		1= Voltage is enabled	
STATE	2:0	r	0	Device state			
				000=NONE	001=INIT	010=NORMAL	011=SLEEP
				100=STANDBY	101=WAKE	110=RESERVED	111=RESERVED

◆

Protection Status Register Address: 28H

Register Name		PROTSTAT		Protection Status Register	
Address				0x28	
Name	Bit	Type	Reset Value	Description	
KEY4OK	7	r	0	Key4 ok status Information about validity of the 4th received protection key byte	
				0= Key not valid	1= Key valid
KEY3OK	6	r	0	Key3 ok status Information about validity of the 3rd received protection key byte	
				0= Key not valid	1= Key valid
KEY2OK	5	r	0	Key2 ok status Information about validity of the 2nd received protection key byte	
				0= Key not valid	1= Key valid
KEY1OK	4	r	0	Key1 ok status Information about validity of the 1st received protection key byte	
				0= Key not valid	1= Key valid
Reserved	3:1	/	000		
LOCK	0	r	1	Protected register lock status	
				0=Access is unlocked	1=Access is locked

◆

Window Watchdog Status Register Address: 29H

Register Name		WWDSTAT		Window Watchdog Status Register
Address				0x29
Name	Bit	Type	Reset Value	Description
Reserved	7:4	/	0000	/
WWDECNT	3:0	r	0000	Window watchdog error counter status

◆

Functional Watchdog Status 0 Register Address: 2AH

Register Name		FWDRSPOK		Functional Watchdog Status Register
Address				0x2A
Name	Bit	Type	Reset Value	Description
Reserved	7	/	0	

FWDRSPOK	6	r	0	Functional watchdog response check error status 0= Response message is wrong 1= All received bytes in response message are correct
FWDRSPC	5:4	r	11	Functional watchdog response counter value
FWDQUEST	3:0	r	0000	Functional watchdog question

◆ Functional Watchdog Status 1 Register Address: 2BH

Register Name		**FWDSTAT1**		**Functional Watchdog Status 1 Register**
Address				0x2B
Name	Bit	Type	Reset Value	Description
Reserved	7:4	/	0000	
FWDECNT	3:0	r	0000	Functional watchdog error counter status

◆ ABIST Control 0 Register Address: 2CH

Register Name		**ABIST_CTRL0**		**ABIST_CTRL0 Register**
Address				0x2C
Name	Bit	Type	Reset Value	Description
STATUS	7:4	r	0000	ABIST global error status ABIST status information after requested operation has been performed, information shall only be considered valid, once START bit is cleared. Bits have different reset class than whole register. The Bits are reset according to *R1). 0101= Selected ABIST operation performed with no errors 1010= Selected ABIST operation performed with errors, check respective SELECT registers
INT	3	rw	0	Safety path selection Select whether safe state or interrupt related comparator shall be tested. 0= safe state related comparators shall be tested 1= interrupt related comparators shall be tested
SINGLE	2	rw	0	ABIST Sequence selection Select whether a single comparator shall be tested or all comparators in predefined sequence 0= Predefined sequence 1= Single comparator test
PATH	1	rw	0	Full path test selection Select the path which should be covered by ABIST operation 0= Comparator only 1= Comparator and corresponding deglitching logic, shall be selected in case contribution to respective safety measure needs to be tested
START	0	rwhc	0	Start ABIST operation The ABIST operation itself will be started. This bit is cleared after ABIST operation has been performed 0=Operation done 1=Start operation

◆ ABIST SELECT 0 Register Address: 2EH

Register Name		ABIST_SELECT0		ABIST Select 0 Register	
Address				0x2E	
Name	Bit	Type	Reset Value	Description	
TRK2OV	7	rwhu	0	Select TRK2 OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
TRK1OV	6	rwhu	0	Select TRK1 OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VREFOV	5	rwhu	0	Select LDO_REF OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
COMOV	4	rwhu	0	Select LDO_COM OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMONOV	3	rwhu	0	Select External buck OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
STBYOV	2	rwhu	0	Select LDO_STBY OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
UCOV	1	rwhu	0	Select LDO_UC OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
PREGOV	0	rwhu	0	Select Pre-regulator OV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

◆ **ABIST SELECT 1 Register Address: 2FH**

Register Name		**ABIST_SELECT 1**		**ABIST Select 1 Register**	
Address				0x2F	
Name	Bit	Type	Reset Value	Description	
TRK2UV	7	rwhu	0	Select TRK2 UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
TRK1UV	6	rwhu	0	Select TRK1 UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VREFUV	5	rwhu	0	Select LDO_REF UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
COMUV	4	rwhu	0	Select LDO_COM UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
VMONUV	3	rwhu	0	Select External buck UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
STBYUV	2	rwhu	0	Select LDO_STBY UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
UCUV	1	rwhu	0	Select LDO_UC UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
PREGUV	0	rwhu	0	Select Pre-regulator UV comparator for ABIST operation	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

◆ **ABIST SELECT 2 Register Address: 30H**

Register Name		**ABIST_SELECT 2**		**ABIST Select 2 Register**	
Address				0x30	
Name	Bit	Type	Reset Value	Description	
BIASHI	7	rwhu	0	Select bias current too high	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BIASLOW	6	rwhu	0	Select bias current too low	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
BG12OV	5	rwhu	0	Select bandgap comparator OV condition (VBG1 ≥ VBG2 + 4%)	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

BG12UV	4	rwhu	0	Select bandgap comparator UV condition (VBG1 ≤ VBG2 - 4%)	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
INTOV	3	rwhu	0	Select internal supply OV condition	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
Reserved	2:1	/	0		
VBATOV	0	rwhu	0	Select supply VIN/VINST overvoltage	
				0= Not selected	1= Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

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Buck Switching Frequency Change Register Address: 31H

Register Name		**BCK_FREQ_CHANGE**		**Buck Switching Frequency Change Register**
Address				0x31
Name	Bit	Type	Reset Value	Description
Reserved	7:3	/	0000	
BCK_FREQ_SEL	2:0	rw	0000	BUCK switching frequency change For hi and low switching mode. New value needs to be validated via data_valid procedure
				000=No Change
				001=Change buck frequency by approx.. +1.5% from Fosc_bck
				010=Change buck frequency by approx.. +3% from Fosc_bck
				011=Change buck frequency by approx.. +4.5% from Fosc_bck
				100=No Change
				101=Change buck frequency by approx.. -1.5% from Fosc_bck
				110=Change buck frequency by approx.. -3% from Fosc_bck
				111=Change buck frequency by approx.. -4.5% from Fosc_bck

◆

Buck Frequency Spread Register Address: 32H

Register Name		**BCK_FRE_SPREAD**		**Buck Frequency Spread Register**			
Address				0x32			
Name	Bit	Type	Reset Value	Description			
FRE_SP_THR	7:0	rw	00000000	Spread spectrum Select the percentage of frequency spread(+/-). The mean frequency is reduced by the percentage as well keeping the maximum frequency at the nominal frequency selected by FSW.			
				00000000=No Spread	00101011=6%	01010101=6%	10000000=6%
				10101010=6%	11010101=6%	11111111=6%	

◆

Buck Main Control Register Address: 33H

Register Name		**BCK_MAIN_CTRL**		**Buck Main Control Register**
Address				0x33
Name	Bit	Type	Reset Value	Description
BUSY	7	r	0	DATA_VALID parameter update ready status

				0=Update done	1=Update ongoing
DATA_VALID	6	rw	0	Enable buck update Update Command to load new parameter for stepdown regulator (after configuration write 1 to update and write 0 after BUSY flag is cleared to proceed operation)	
				0=No action	1=Load new parameters
Reserved	5:0	/	000000		

◆ Function Control Register Address: 36H

Register Name		FCR		Function control register	
Address				0x36	
Name	Bit	Type	Reset Value	Description	
Reserved	7:2	/	0		
VR_OV_FS	1	rw	0	VR OV Enter Failsafe state	
				0=Enter Failsafe mode if VR OV event happen	1=Keep in current state if VR OV event happen
LDO_UC_CUR	0	rw	1	LDO_UC Current Limit	
				0=600mA	1=850mA

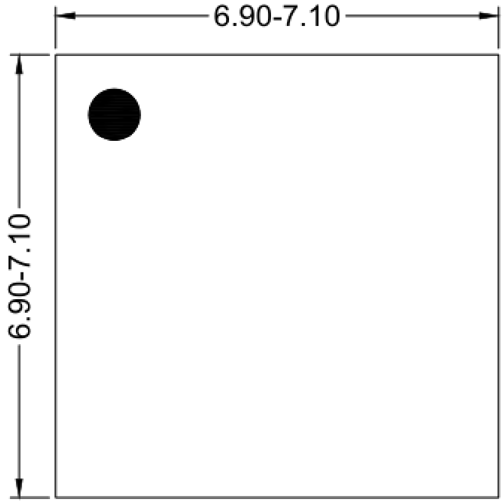
◆ MCU Program Support Address: 3CH

Register Name		MCSMON		Microcontroller supervision monitor Register	
Address				0x3C	
Name	Bit	Type	Reset Value	Description	
PROG	7	rw	0	MCU programming support enable (OR combination with PROG pin)	
				0= Disabled via SPI (unless enabled by PROG pin high)	1= Enabled via SPI (independent of PROG pin)
MPSIN	6	r	0	MCU programming support enable (OR combination with PROG bitfield)	
				0= Disabled via pin PROG (unless enabled by PROG bitfield being set)	1= Enabled via pin PROG (independent of PROG bitfield)
Reserved	5:0	/	000000		

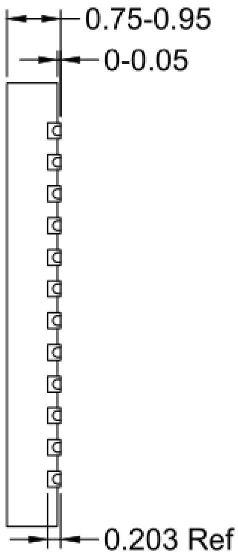
◆ Global Test Mode Register Address: 3FH

Register Name		GTM		Global Test Mode Register	
Address				0x31	
Name	Bit	Type	Reset Value	Description	
Reserved	7:2	/	000000		
NTM	1	r	1	Test mode inverted status	
				0= Device is in test mode	1= Device is in normal mode
TM	0	r	0	Test mode status	
				0= Device is in normal mode	1= Device is in test mode

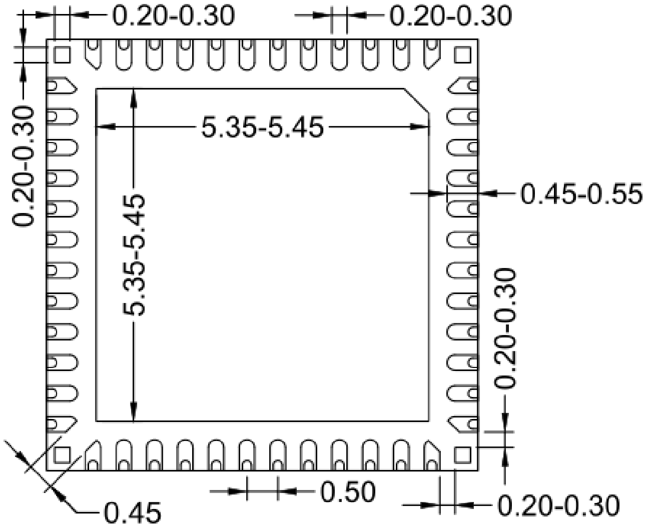
QFN7×7-48 Package Outline Drawing



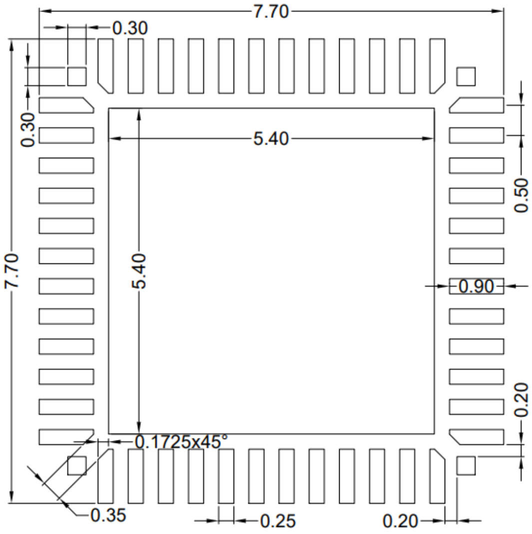
Top View



Side View



Bottom View



Recommended Pad Layout

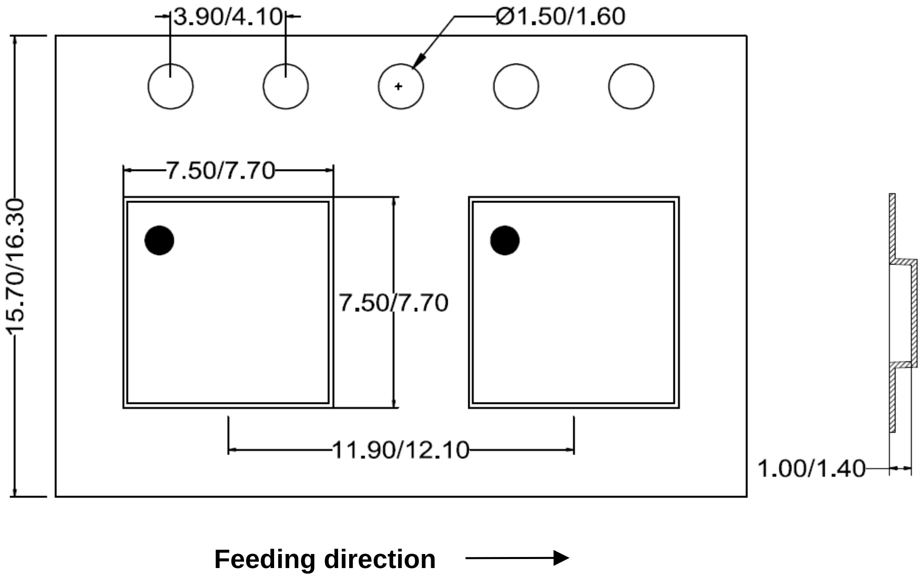
(Reference Only)

Note: *All dimensions in millimeters and exclude mold flash & metal burr.*

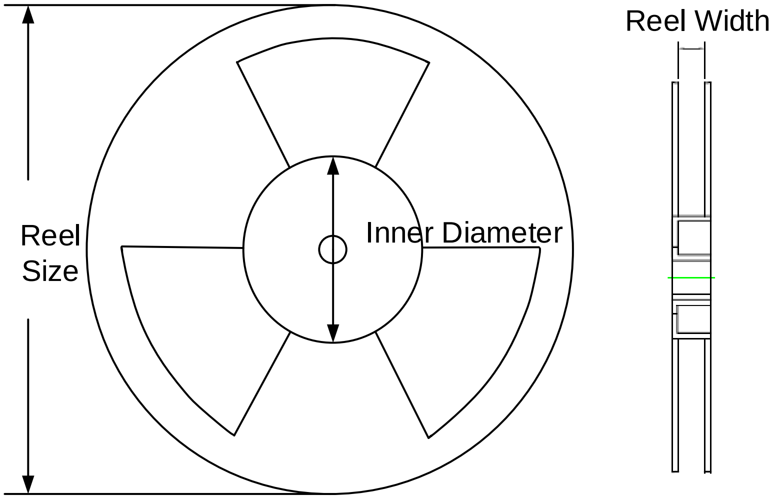
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation

QFN7×7



Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Inner Diameter (mm)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel (pcs)
QFN7x7-48	16	12	13"	100	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Sep.05, 2025	Revision 1.0	SA47301QJQ initial release.	-
Nov.28, 2025	Revision 1.0a	SA47301BQJQ/SA47301CQJQ/SA4701DQJQ initial release.	-
Mar.04, 2026	Revision 1.0A	Update detailed information in Tape and Reel.	Page 131

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