SY3135AS21-J00

Ultra-High Sensitivity ALS for Under OLED Application

General Description

The SY3135AS21-J00 is an ultra-small ambient light sensor (ALS) featuring ultra-high sensitivity. Its fast integration time of less than 1ms makes it ideal for applications where the sensor is placed under the OLED display, which eliminates the need for a separate display panel cutout in cellphones and smart watches.

The SY3135AS21-J00 incorporates photodiode (PD) arrays with various coatings to achieve visible and full-spectrum sensing. It integrates two independent Analog-Digital-Converters (ADCs) that operate in parallel to provide synchronous digital count outputs.

The device's very short integration time enables synchronized readings during the display blanking period via the VSYNC input, minimizing the display interference during normal operation. The interrupt pin can be configured to trigger at programmable FIFO levels, eliminating the need to poll sensor status. It features an SMBus-compatible I^2C interface, allowing for easy connection to a microcontroller.

The SY3135AS21-J00 is designed with a fast integration time, high signal-to-noise ratio (SNR) performance, I^2C interface, and a wide operating temperature range, making it ideal for applications where placing the light sensor under an OLED display is required.

Features

- Electrical Operation Performance:
  - Power Supply Voltage: 1.7V - 2.0V
  - Operating Current: 220μA
  - Shutdown Current: Less Than 15μA
  - Operating Temperature: -40°C to +85°C
- Ambient Light Sensing:
  - Two Parallel 16-bit ADCs
  - Programmable Integration Time (IT) for Both Normal and Fast Operation Modes
  - Programmable Gain Settings Ranging From 1x to 256x
- 512 Bytes FIFO, with Programmable Interrupt Threshold Levels
- Selectable FIFO Sources, Allowing Selection of ADC Data to Be Written to the FIFO
- BT Substrate with Transparent Molding Compound
- Package Size: 2.0mm×1.0mm×0.35mm

Applications

- Under-OLED ALS for Cellphones and Watches
- Laptops and Notebooks
- TV Panels
- Industrial Control

Typical Application

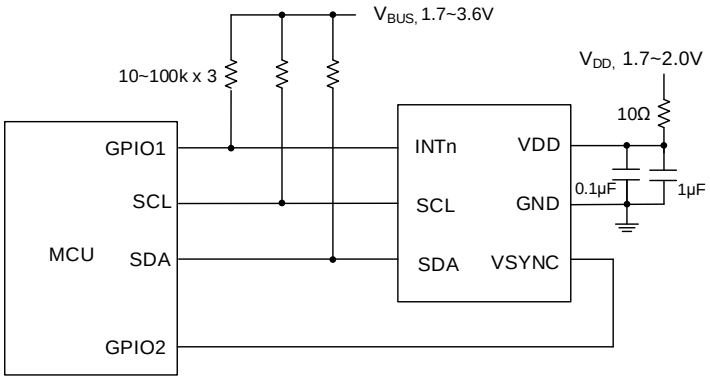


Figure 1. Typical Application Schematic

Ordering Information

Part Number	Package Type	Top Mark	MSL	Delivery Quantity
SY3135AS21-J00	LGA2×1-6 RoHS-Compliant and Halogen-Free	N/A	3	3000 pcs/reel

Block Diagram

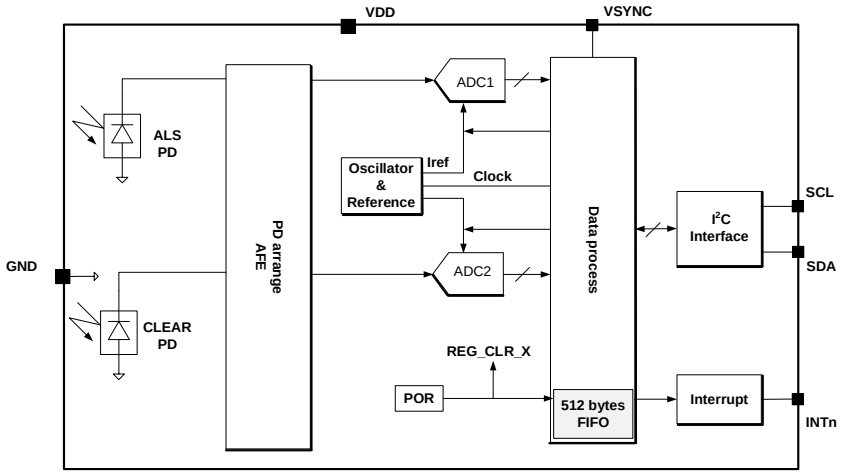
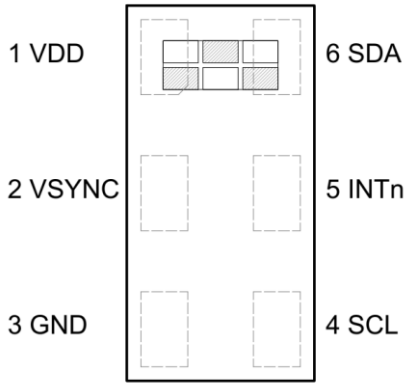


Figure 2. Block Diagram

Device Pinout (top view)



Pin No.	Pin Name	Pin Description
1	VDD	Positive supply: 1.7V to 2.0V.
2	VSYNC	External synchronization input.
3	GND	Power supply ground. All voltages are referenced to GND.
4	SCL	I²C clock line. The I²C bus lines can be pulled from 1.7V to 3.6V.
5	INTn	Interrupt output with open-drain configuration, low-level active.
6	SDA	I²C data line. The I²C bus lines can be pulled high to a rail between 1.7V to 3.6V.

Absolute Maximum Ratings (T_A=25°C unless otherwise specified) (Note 1)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.3	2.2	V
I^2C Bus Voltage	V_{I^2C}	-0.3	4	
INTn and Synchronization Terminal Voltage	V_{INTn}, V_{SYNC}	-0.3	4	
I^2C Bus Current	I_{I^2C}		10	mA
HBM	ESD	±2000		V
CDM		±500		V
Latch Up		±200		mA

Recommended Operating Conditions (T_A=25°C unless otherwise specified) (Note 3)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	1.7		2.0	V
Storage Temperature	T_{STG}	-40		+100	°C
Operating Temperature	T_{OPR}	-40		+85	°C

Electrical and Optical Characteristics

(V_{DD} = 1.8V, T_A = 25°C, unless otherwise specified. (Note 4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.7	1.8	2.0	V
Supply Current When Powered Down	I_{DD_SD}	PON=0		-	15	μA
Supply Current When One Channel is in Normal Mode	I_{DD_single}	ALS_EN=1 or CLEAR_EN=1, PON=1	120	160	200	μA
Supply Current when All Channels are in Normal Mode	I_{DD_all}	ALS_EN=CLEAR_EN=1, PON=1	165	220	275	μA
Supply Voltage Range for I^2C Interface	V_{I^2C}		1.7	-	3.6	V
Low-Level Input Voltage of SCL and SDA	V_{IL}		-	-	0.55	V
High-Level Input Voltage of SCL and SDA	V_{IH}		1.25	-	-	V
SDA Current Sinking Capability	I_{SDA}	V_{OL} = 0.4V	2.7	5	-	mA
Low-Level Output Voltage of SDA	V_{OL}	I_{OL}=4mA	-	-	0.4	V
Input Leakage for SDA, SCL	I_{Leak}		-10	-	10	μA
Full Scale of ADC Output	$DATA_{ADC\_FS}$	Integration Time≥6.25ms	-	-	65535	Counts
Gain Ratio	ALS/CLEAR channel gain ratio	256x/128x	1.8	2.00	2.2	
		128x/64x	1.8	2.00	2.2	
ADC Integration Time	IT	ALS_IT1=0	23.75	25	26.25	ms
ALS Channel Output Count	$DATA_{ALS}$	IT=50ms, Gain=256x, Ev=8.5lux, white LED 6500k	4630	5145	5660	Counts
Clear Channel Output Count	$DATA_{CLEAR}$		10690	11875	13060	Counts
Dark Count of ALS Channel		IT=100ms, GAIN=256x, Ev=0 lux[6]			3	Counts
Dark Count of CLEAR Channel					5	

I²C Timing Specifications

(V_{DD} = 1.8V, T_A = 25°C, unless otherwise specified) (Note 5)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Clock Frequency	f_{SCL}		-	-	1000	kHz
Capacitance for Each SDA and SCL Pin	C_i		-	-	10	pF
Hold Time (repeated) START Condition	$t_{HD:STA}$		0.6	-	-	µs
Low Period of the SCL Clock	t_{LOW}		1.3	-	-	µs
High Period of the SCL Clock	t_{HIGH}		0.6	-	-	µs
Set-Up Time for a Repeated START Condition	$t_{SU:STA}$		0.6	-	-	µs
Data Hold Time	$t_{HD:DAT}$		30	-	-	ns
Data Set-Up Time	$t_{SU:DAT}$		100	-	-	ns
Set-Up Time for STOP Condition	$t_{SU:STO}$		0.6	-	-	µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	-	-	µs
Rise Time of Both SDA and SCL	t_R	$R_{pull-up}$ = 10kΩ, C_b = 10pF	-		120	ns
Fall Time of SDA and SCL	t_F	$R_{pull-up}$ = 10kΩ, C_b = 10pF	-		120	ns
Capacitive Load for Each Bus Line	C_b		-	-	0.4	nF

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c−bus.org/references/.

Note 3: The device is not guaranteed to function outside its recommended operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: Dark count of ALS channel maximum value, measured and trimmed based on a custom setup. Contact the vendor for additional details and a firmware driver example.

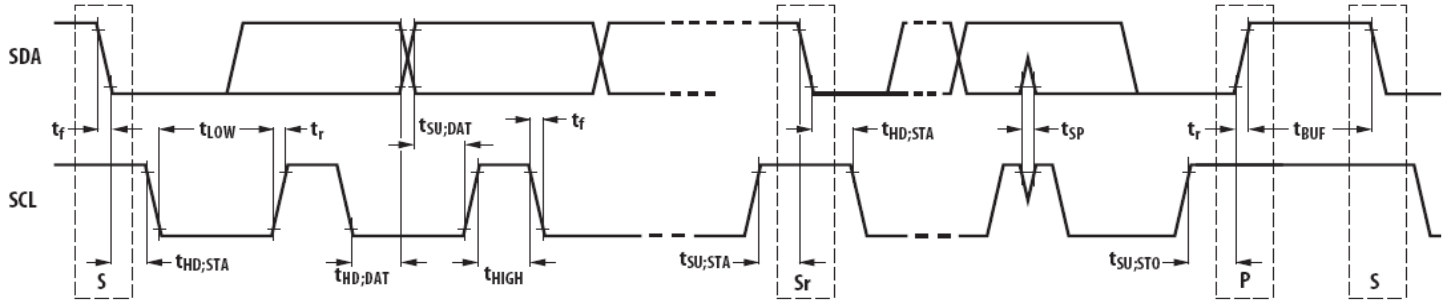
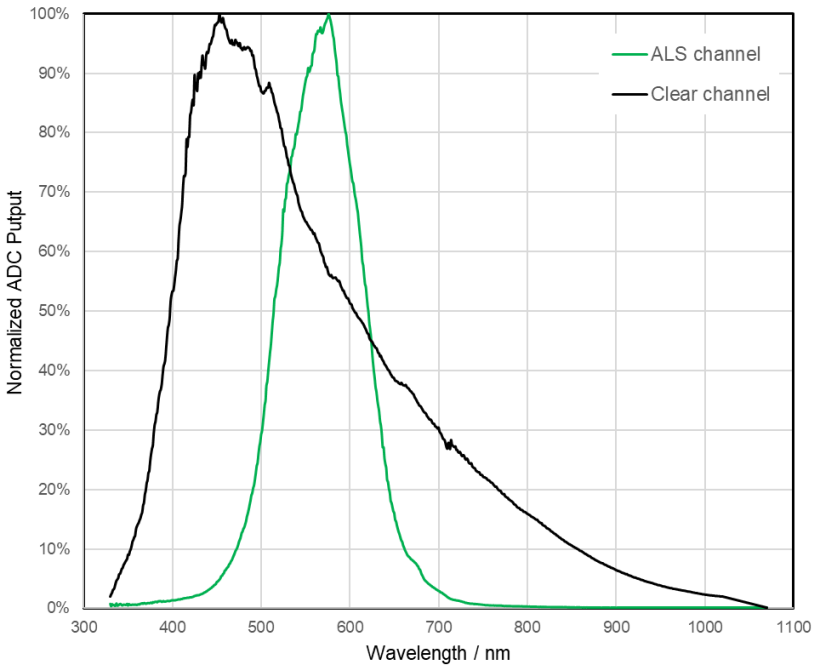


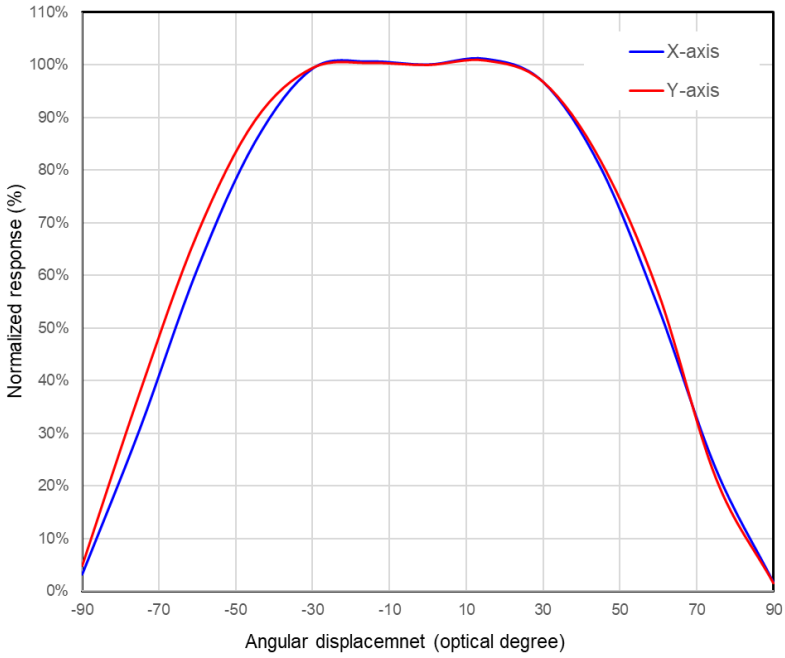
Figure 3. I²C Timing Diagram

Typical Characteristics

Relative Spectral Response



Normalized Output vs. Angular Displacement



Interrupt Function

The ambient light sensing interrupt flag (AINT_FLAG) is triggered by low and high thresholds set in registers 0x14 to 0x17. The device includes a persistence filter (A_PRST), which allows the user to determine the number of consecutive readings that must meet the interrupt conditions before an interrupt is triggered.

AINT_FLAG will be asserted when the acquired ADC data exceeds the high threshold or falls below the low threshold. The host can clear the interrupt flag using a command, as detailed in Table 2. If AINT_EN bit is enabled (logic 1), the INTn pin will be pulled low when an interrupt event occurs. If disabled, the INTn pin will remain in a high impedance (Hi-Z) state and will not reflect the AINT_FLAG status. Refer to Table 16 for details of how and when interrupt events occur.

Figure 4 is an illustration of the internal logic for interrupts (assuming A_PRST=0).

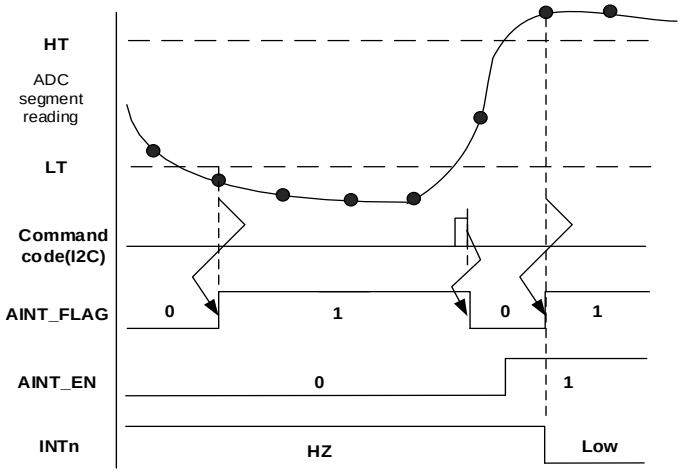


Figure 4. ALS Window Interrupt

I²C Read / Write Register Data

The I²C peripheral address of the SY3135AS21-J00 is 0x44 (0b'1000100). Figures 5 and 6 illustrate the protocol for writing to or reading from the registers. The initial 8-bit data following the write operation represents either the register address or a special function, as detailed in Table 2.

A : Acknowledge (0)
NA : Not Acknowledged (1)
P : Stop Condition
R : Read (1)
W : Write (0)
S : Start Condition
Sr : Repeat Start
... : Continuation of Protocol
□ : Controller to Peripheral
▒ : Peripheral to Controller

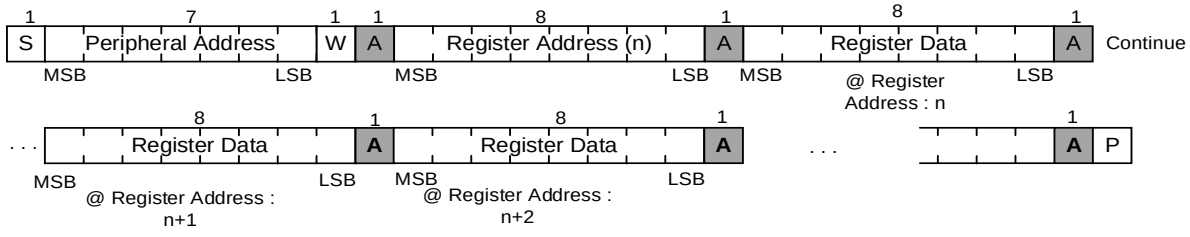


Figure 5. I²C Write-Register-Data Protocol

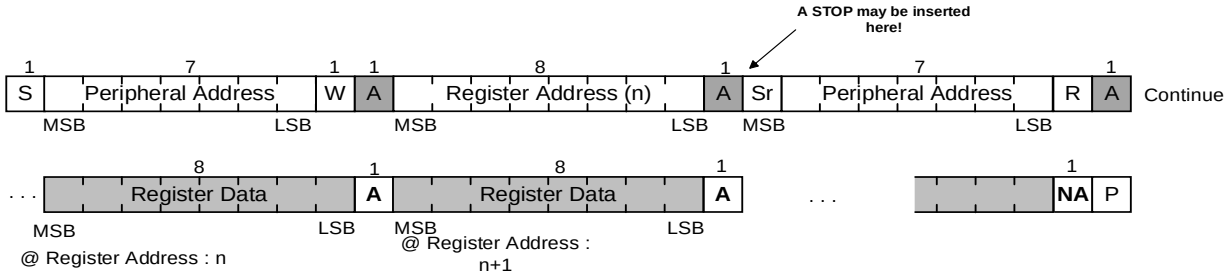


Figure 6. I²C Read-Register-Data Protocol

Register Map

Table 1. Registers and Register Bits

REG Address	REG Name	Bit								
		7	6	5	4	3	2	1	0	Default
0x00	COM_TEST	Chip ID								0x33
0x01	ALS_CON1	ALS_EN	CLEAR_EN	Reserved	ALS_IT	CLEAR_IT	Reserved	STEP1_EN	PON	0x00
0x02	ALS_CON2	ALS_IT1[7:0]								0x00
0x03	ALS_CON3	ALS_IT2[8:1]								0x00
0x04	ALS_CON4	ALS_IT2[11:9]			IT2_CYCLE[4:0]					0x00
0x06	ALS_CON5	CLEAR_STEP0_GAIN[3:0]				CLEAR_STEP1_GAIN[3:0]				0x00
0x07	ALS_CON6	ALS_STEP0_GAIN[3:0]				ALS_STEP1_GAIN[3:0]				0x00
0x08	PD_CON1	Write 0xE9 when initialized								0x00
0x09	PD_CON2	ALS_IT2[0]	Reserved			Write 0x6 when initialized				0x00
0x0A	PD_CON3	Write 0x2C when initialized								0x00
0x0B	PD_CON4	Write 0x2C when initialized								0x00
0x0C	FIFO_CON	FINT_EN	OVWR_EN	FIFO_SOURCE[5:0]						0x00
0x0D	SYNC_CON1	SYNC_EN[1:0]		SYNC_IT2_EN	SYNC_IT1_EN	Reserved				0x00
0x0E	SYNC_CON2	SYNC_DELAY[7:0]								0x00
0x0F	INT_CON	AINT_EN	A_PRST[1:0]		AINT_SOURCE[3:0]				Reserved	0x00
0x10	WAIT_CON	AWAIT_TIME[7:0]								0x00
0x14	ALS_LTL	ALS_LOWTHRES[7:0]								0x00
0x15	ALS_LTH	ALS_LOWTHRES[15:8]								0x00
0x16	ALS_HTL	ALS_HIGHTHRES[7:0]								0xFF
0x17	ALS_HTH	ALS_HIGHTHRES[15:8]								0xFF
0x18	ALS_FIFO_TH	ALS_FIFO_THRES[7:0]								0x00
0x1D	FIFO_FLAG	FINT_FLAG	FIFO_EMPTY	FIFO_FULL	Unused					0x00
0x1E	INT_FLAG	AINT_FLAG	IT1_VALID	IT2_VALID	Unused					0x00
0x22	CLEAR0_DATAL	CLEAR_STEP0_DATA[7:0]								0x00
0x23	CLEAR0_DATAH	CLEAR_STEP0_DATA[15:8]								0x00
0x24	ALS0_DATAL	ALS_STEP0_DATA[7:0]								0x00
0x25	ALS0_DATAH	ALS_STEP0_DATA[15:8]								0x00
0x28	CLEAR1_DATAL	CLEAR_STEP1_DATA[7:0]								0x00
0x29	CLEAR1_DATAH	CLEAR_STEP1_DATA[15:8]								0x00
0x2A	ALS1_DATAL	ALS_STEP1_DATA[7:0]								0x00
0x2B	ALS1_DATAH	ALS_STEP1_DATA[15:8]								0x00
0x30	FIFO_LV_CNT	FIFO_LV_CNT[7:0]								0x00
0x31	FIFO_R_CLR	FIFO_R_CNT_CLR(read active)								0x59
0x32	FIFO_A_DATAL	FIFO_DATA[7:0]								0x00
0x33	FIFO_A_DATAH	FIFO_DATA[15:8]								0x00
0x34	FIFO_R_CNTL	FIFO_R_CNT[7:0]								0x00
0x35	FIFO_R_CNTH	(Write 0)						FIFO_R_CNT[9:8]		0x00
0x53	TEST_CON4	Write 0x02 when initialized								0x00

Table 2. Command Code

Bit	Access	Default	Name	Function / Operation
7:4				0111: special function Others: register address
3:0			Register Address / Special Function Register	Special function: 0010: clears FIFO interrupt flag and FIFO data 0100: clears ALS interrupt flag 0110: clears IT1_VALID flag 1000: clears IT2_VALID flag 1010: restarts ADC process 1101: set all registers to the default value Others: reserved

Chip ID Register (0x00)

This read-only register holds a fixed data value of 0x33. Read this register through the I^2C interface to identify the device. Additionally, it serves as a tool to verify whether the communication link has been successfully established.

Table 3. Register 0x01 (ALS_CON1) – ALS Sensing Configuration 1

Bit	Access	Default	Name	Function / Operation
7	RW	0	ALS_EN	When =0, ALS channel ADC is disabled When =1, ALS channel ADC is enabled
6	RW	0	CLEAR_EN	When =0, CLEAR channel ADC is disabled When =1, CLEAR channel ADC is enabled
5	RW	0	Reserved	Reserved, write 0
4	RW	0	ALS_IT	When =0, ALS ADC is operating with IT set by ALS_IT1 When =1, ALS ADC is operating with IT set by ALS_IT2
3	RW	0	CLEAR_IT	When =0, CLEAR ADC is operating with IT set by ALS_IT1 When =1, CLEAR ADC is operating with IT set by ALS_IT2
2	RW	0	Reserved	Reserved, write 0
1	RW	0	STEP1_EN	When =0, only STEP0 is executed for all ADCs. STEP1 is ignored When =1, both STEP0 and STEP1 are executed for all ADCs
0	RW	0	PON	When =0, the internal oscillator and reference are shut down When =1, internal oscillator and reference are enabled

Table 4. Register 0x02 (ALS_CON2) – ALS Sensing Configuration 2

Bit	Access	Default	Name	Function / Operation
7:0	RW	0	ALS_IT1[7:0]	This byte configures the integration time for normal operation mode. Detailed integration time can be calculated as 25ms * (ALS_IT1+1), which ranges from 25ms to 6400ms

Table 5. Register 0x03 (ALS_CON3) – ALS Sensing Configuration 3

Bit	Access	Default	Name	Function / Operation
7:0	RW	0	ALS_IT2[8:1]	This byte, along with ALS_IT2 [11:9] at register 0x04 and ALS_IT2 [0] at register 0x09, configures integration time for fast operation mode. Detailed integration time can be calculated as 6.25μs * (ALS_IT2+1), which ranges from 6.25μs to 25.6ms

Table 6. Register 0x04 (ALS_CON4) –ALS Sensing Configuration 4

Bit	Access	Default	Name	Function / Operation
7:5	RW	0	ALS_IT2[11:9]	Integration time configuration for fast operation mode. Refer to the descriptions in Table 5

4:0	RW	0	IT2_CYCLE[4:0]	These 5 bits determine that STEP0 or STEP1 will execute (IT2_CYCLE+1) cycles before changing to the next step status. If set, STEP0 will execute the specified number of cycles, and STEP1 will execute the same cycle count. This configuration only applies when the device operates in fast operation mode.

The diagram below shows the operation of a channel ADC based on the integration time (IT) settings:

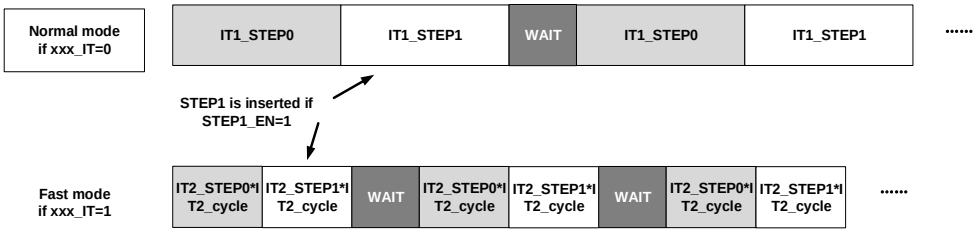


Table 7. Register 0x06 (ALS_CON5) –ALS Sensing Configuration 5

Bit	Access	Default	Name	Function / Operation
7:4	RW	0	CLEAR_STEP0_GAIN[3:0]	For bits 7:4, see the following: 0010, gain setting is 256x 0011, gain setting is 128x 0100, gain setting is 64x 0101, gain setting is 32x 0110, gain setting is 16x 0111, gain setting is 8x 1000, gain setting is 4x 1001, gain setting is 2x 1010, gain setting is 1x others, reserved
3:0	RW	0	CLEAR _STEP1_GAIN[3:0]	Similar definition to CLEAR _STEP0_GAIN at bits[7:4]

Table 8. Register 0x07 (ALS_CON6) –ALS Sensing Configuration 6

Bit	Access	Default	Name	Function / Operation
7:4	RW	0	ALS_STEP0_GAIN[3:0]	Gain Settings: 0010, gain setting is 256x 0011, gain setting is 128x 0100, gain setting is 64x 0101, gain setting is 32x 0110, gain setting is 16x 0111, gain setting is 8x 1000, gain setting is 4x 1001, gain setting is 2x 1010, gain setting is 1x others, reserved
3:0	RW	0	ALS _STEP1_GAIN[3:0]	Similar definition to ALS _STEP0_GAIN bits[7:4]

Table 9. Register 0x08 (PD_CON1) –Photodiode Configuration 1

Bit	Access	Default	Name	Function / Operation
7:0	RW	0		User must write 0xE9 to this byte during initialization.

Table 10. Register 0x09 (PD_CON2) –Photodiode Configuration 2

Bit	Access	Default	Name	Function / Operation
7	RW	0	ALS_IT2[0]	Integration time configuration of fast operation mode. Refer to the descriptions in Table 5.
6:4	RW	0	Reserved	Reserved, write 0
3:0	RW	0		User must write 0x6 to these 4 bits during initialization.

Table 11. Register 0x0A (PD_CON3) –Photodiode Configuration 3

Bit	Access	Default	Name	Function / Operation
7:0	RW	0		User must write 0x2C to this byte during initialization.

Table 12. Register 0x0B (PD_CON4) –Photodiode Configuration 4

Bit	Access	Default	Name	Function / Operation
7:0	RW	0		User must write 0x2C to this byte during initialization.

Table 13. Register 0x0C (FIFO_CON) –FIFO Configuration

Bit	Access	Default	Name	Function / Operation
7	RW	0	FINT_EN	When =0, the interrupt pin is HZ and irrelevant to internal bit status. When =1, the interrupt pin is asserted based on the FINT_FLAG bit status.
6	RW	0	OVWR_EN	When =0, data is overwritten after the FIFO becomes full and the level counter resets. When =1, new data is discarded after the FIFO becomes full.
5:0	RW	0	FIFO_SOURCE[5:0]	For bits 5:0, see the following: x1xxxx: CLEAR channel STEP0 data is pushed into FIFO xx1xxx: ALS channel STEP0 data is pushed into FIFO xxxx1x: CLEAR channel STEP1 data is pushed into FIFO xxxxx1: ALS channel STEP1 data is pushed into FIFO Others: reserved If the specified bit is cleared, the corresponding data won't be pushed into FIFO.

Each bit within the FIFO_SOURCE [5:0] register controls whether the data from a specified channel is pushed into the FIFO. If multiple bits are set, all corresponding source data will be pushed into the FIFO following the CLEAR\ALS_STEP0\1 sequence. Therefore, when retrieving data from the FIFO, the user must keep track of the FIFO_SOURCE configuration to accurately assemble the channel data.

Table 14. Register 0x0D (SYNC_CON1) –Synchronization Configuration 1

Bit	Access	Default	Name	Function / Operation
7:6	RW	0	SYNC_EN[1:0]	External Synchronization: 00: external synchronization function is disabled 01: rising edge is used to trigger synchronization 10: falling edgy is used to trigger synchronization 11: reserved
5	RW	0	SYNC_IT2_EN	When =0, IT2 synchronization is not used When =1, IT2 synchronization is triggered by the external edge
4	RW	0	SYNC_IT1_EN	When =0, IT1 synchronization is not used When =1, IT1 synchronization is triggered by the external edge
3:0	RW	0	Reserved	Reserved, write 0

The external SYNC signal can initiate IT1 (normal operation) mode and IT2 (fast operation) mode. The description below focuses on the combination of the IT2 and synchronization modes, as normal operation mode typically does not require synchronization.

The SYNC function operates similarly when IT1 is triggered by an external signal. IT2 initiates after the SYNC_DELAY period is over, which means that at the end of the SYNC_DELAY, the integration cycle starts. When SYNC_DELAY is set to 0, the integration cycle starts immediately after the SYNC trigger signal.

For both Case 1 and Case 2, if the IT time of STEP0, or the cumulative time of STEP0 and STEP1, is shorter than the duration of the VSYNC signal, no delay is inserted between the end time and the next start signal.

For Case 3, if the STEP0 IT time exceeds the duration of the VSYNC signal, any starting signal during the STEP0 IT time is disregarded until the integration is completed. No delay is introduced between the completion of the current cycle and the next start signal.

This scenario is mirrored in Case 4, where the combined duration of STEP0 and STEP1 exceeds the VSYNC signal width.

In Case 5, if a WAIT time is implemented, any start signal received before this wait time has fully elapsed will be ignored. If the IT2_CYCLE setting is activated, the starting signal will be blocked until the end of the successive cycles.

The above operation configurations apply to all ADCs in the system.

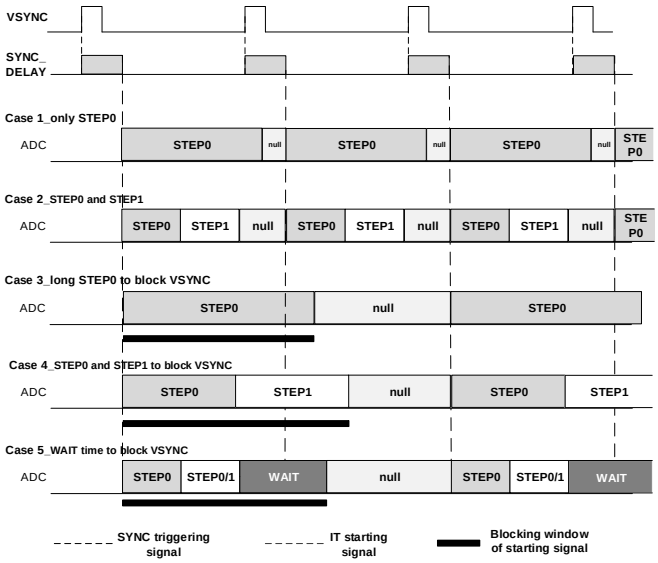


Figure 7. SYNC Timing Diagram

Table 15. Register 0x0E (SYNC_CON2) – Synchronization Configuration 2

Bit	Access	Default	Name	Function / Operation
7:0	RW	0	SYNC_DELAY[7:0]	This byte configures the delay time between the triggering edge and the sync mode start signal. Total delay time can be calculated as 25μs *(SYNC_DELAY)

Table 16. Register 0x0F (INT_CON) – Interrupt Configuration

Bit	Access	Default	Name	Function / Operation
7	RW	0	AINT_EN	When =0, the interrupt pin is HZ and irrelevant to the internal bit status When =1, the interrupt pin will react according to the AINT_FLAG bit
6:5	RW	0	A_PRST[1:0]	For bits 6:5, see the following: 00: AINT_FLAG is set if 1 reading trips the threshold value 01: AINT_FLAG is set if 4 readings trip the threshold value 10: AINT_FLAG is set if 8 readings trip the threshold value 11: AINT_FLAG is set if 15 readings trip the threshold value

4:1	RW	0	AINT_SOURCE[3:0]	Refer to the description below for details.
0	RW	0	Reserved	Reserved, write 0

AINT_SOURCE controls when AINT_FLAG will be set. The truth table below demonstrates how the interrupt is generated and how the interrupt flag changes.

AINT_SOURCE	Bit 3	Bit 2	Bit 1	Bit 0	Function
VALID Type Interrupt	0	0	0	0	No data valid interrupt will be generated
			0	1	AINT_FLAG will be set once IT2_VALID=1
			1	0	AINT_FLAG will be set once IT1_VALID=1
			1	1	Reserved
Window type interrupt by STEP0 data	0	1	0	0	Reserved
			0	1	Reserved
			1	0	CLEAR channel STEP0 data is used to compare with the threshold for setting the interrupt flag
			1	1	ALS channel STEP0 data is used to compare with the threshold
Window Type Interrupt by STEP1 Data	1	0	0	0	Reserved
			0	1	Reserved
			1	0	CLEAR channel STEP1 data is used to compare with the threshold for setting the interrupt flag.
			1	1	ALS channel STEP1 data is used to compare with the threshold
Window Type Interrupt by STEP0 or STEP1 Data	1	1	0	0	Reserved
			0	1	Reserved
			1	0	CLEAR channel STEP0 and STEP1 data are used to compare with the threshold for setting the interrupt flag
			1	1	ALS channel STEP0 and STEP1 data are used to compare with the threshold

Table 17. Register 0x10 (WAIT_CON) – Wait Function Configuration

Bit	Access	Default	Name	Function / Operation
7:0	RW	0	AWAIT_TIME[7:0]	When STEP_EN=0, this byte configures the wait time between two adjacent STEP0 segments. When STEP_EN=1, this byte configures the wait time inserted between STEP1 and the next STEP0 segment. Wait time is calculated as 1.563ms * (AWAIT TIME+1)

Table 18. Register 0x14~0x17 – ALS Channel Interrupt Threshold Registers

Addr	Access	Default	Name	Function / Operation
0x14	RW	0	ALS_LOWTHRES[7:0]	Lower byte of ALS low threshold
0x15	RW	0	ALS_LOWTHRES[15:8]	Upper byte of ALS low threshold
0x16	RW	0xFF	ALS_HIGHTHRES[7:0]	Lower byte of ALS high threshold
0x17	RW	0xFF	ALS_HIGHTHRES[15:8]	Upper byte of ALS high threshold

Table 19. Register 0x18(ALS_FIFO_TH) – FIFO Threshold Level for Interrupt

Addr	Access	Default	Name	Function / Operation
0x18	RW	0	ALS_FIFO_THRES[7:0]	FIFO interrupt threshold. When FIFO data bytes equal 2*ALS_FIFO_THRES, a FIFO level interrupt will occur, and FINT_FLAG will be set

Table 20. Register 0x1D (FIFO_FLAG) – FIFO Flag

Bit	Access	Default	Name	Function / Operation
7	RO	0	FINT_FLAG	When =0, no FIFO interrupt has occurred since last power-on or last “clear” When =1, a FIFO interrupt event occurred since specific data was written into the FIFO
6	RO	0	FIFO_EMPTY	When =0, no FIFO empty interrupt has occurred since last power-on or last “clear” When =1, all data in FIFO is read and FIFO is empty
5	RO	0	FIFO_FULL	When =0, no FIFO full interrupt has occurred since last power-on or last “clear” When =1, all data in FIFO is new and has not been accessed previously
4:0	RO	0	Unused	Unused

For the FIFO interrupt, the FINT_FLAG is set whenever the number of data bytes in the FIFO_LV_CNT exceeds the threshold specified in the ALS_FIFO_THRES register, signaling that the user-defined FIFO level has been reached. When FINT_EN is activated, the INTn pin is driven low when an interrupt occurs. If FINT_EN is not enabled, the INTn pin remains in a high impedance (HZ) state and does not respond to changes in the FINT_FLAG bit status.

FIFO_LV_CNT is increased automatically once every ADC cycle is finished. When FIFO_LV_CNT is 255, the FIFO_FULL flag is set. When all FIFO data is read through the I^2C, the FIFO_EMPTY flag is set.

Table 21. Register 0x1E (INT_FLAG) – Interrupt Flag

Bit	Access	Default	Name	Function / Operation
7	RO	0	AINT_FLAG	When =0, no ALS interrupt has occurred since power-on or last “clear” When =1, an ALS interrupt event occurred
6	RO	0	IT1_VALID	When =0, no data is updated in normal operation mode since power-on or last “clear” When =1, new data was updated into registers after last “clear”
5	RO	0	IT2_VALID	When =0, no data is updated in fast operation mode since power-on or last “clear” When =1, new data is updated into registers after last “clear”
4:0	RO	0	Unused	Unused

If STEP1_EN=0, IT1_VALID is set once STEP0 is completed, and set after STEP1 is completed if STEP1_EN=1.

If STEP1_EN=0, IT2_VALID is set once STEP0 is completed, and set after STEP1 is completed if STEP1_EN=1. If IT2_CYCLE is set, IT2_VALID is set at the end of the last successive cycle.

Table 22. Register 0x22~0x2B – ALS Channel Data Read

Addr	Access	Default	Name	Function / Operation
0x22	RO	0	CLEAR_STEP0_DATA[7:0]	Lower byte of CLEAR STEP0 segment reading
0x23	RO	0	CLEAR _STEP0_DATA[15:8]	Upper byte of CLEAR STEP0 segment reading
0x24	RO	0	ALS_STEP0_DATA[7:0]	Lower byte of ALS STEP0 segment reading
0x25	RO	0	ALS _STEP0_DATA[15:8]	Upper byte of ALS STEP0 segment reading
0x28	RO	0	CLEAR_STEP1_DATA[7:0]	Lower byte of CLEAR STEP1 segment reading
0x29	RO	0	CLEAR_STEP1_DATA[15:8]	Upper byte of CLEAR STEP1 segment reading
0x2A	RO	0	ALS_STEP1_DATA[7:0]	Lower byte of ALS STEP1 segment reading
0x2B	RO	0	ALS_STEP1_DATA[15:8]	Upper byte of ALS STEP1 segment reading

Table 23. Register 0x30 (FIFO_LV_CNT) – Actual FIFO Level

Addr	Access	Default	Name	Function / Operation
0x30	RO	0	FIFO_LV_CNT[7:0]	This byte indicates the actual FIFO level counter. When FIFO_LV_CNT equals ALS_FIFO_THRES, a FIFO level interrupt occurs and FINT_FLAG is set

FIFO Reading Counter Clear Register (0x31)

Reading this register automatically resets the FIFO reading counter in register 0x30. By default, reading this register will return a value of 0x59.

Table 24. Register 0x32~0x33 – FIFO Data of ALS and CLEAR Channel

Addr	Access	Default	Name	Function / Operation
0x32	RO	0	FIFO_DATA[7:0]	Lower byte of current FIFO reading
0x33	RO	0	FIFO_DATA[15:8]	Upper byte of current FIFO reading

Table 25. Register 0x34 (FIFO_R_CNTL) – Actual Reading of FIFO Level

Addr	Access	Default	Name	Function / Operation
0x34	RO	0	FIFO_R_CNT[7:0]	Lower 8 bits of the actual reading of the FIFO level counter

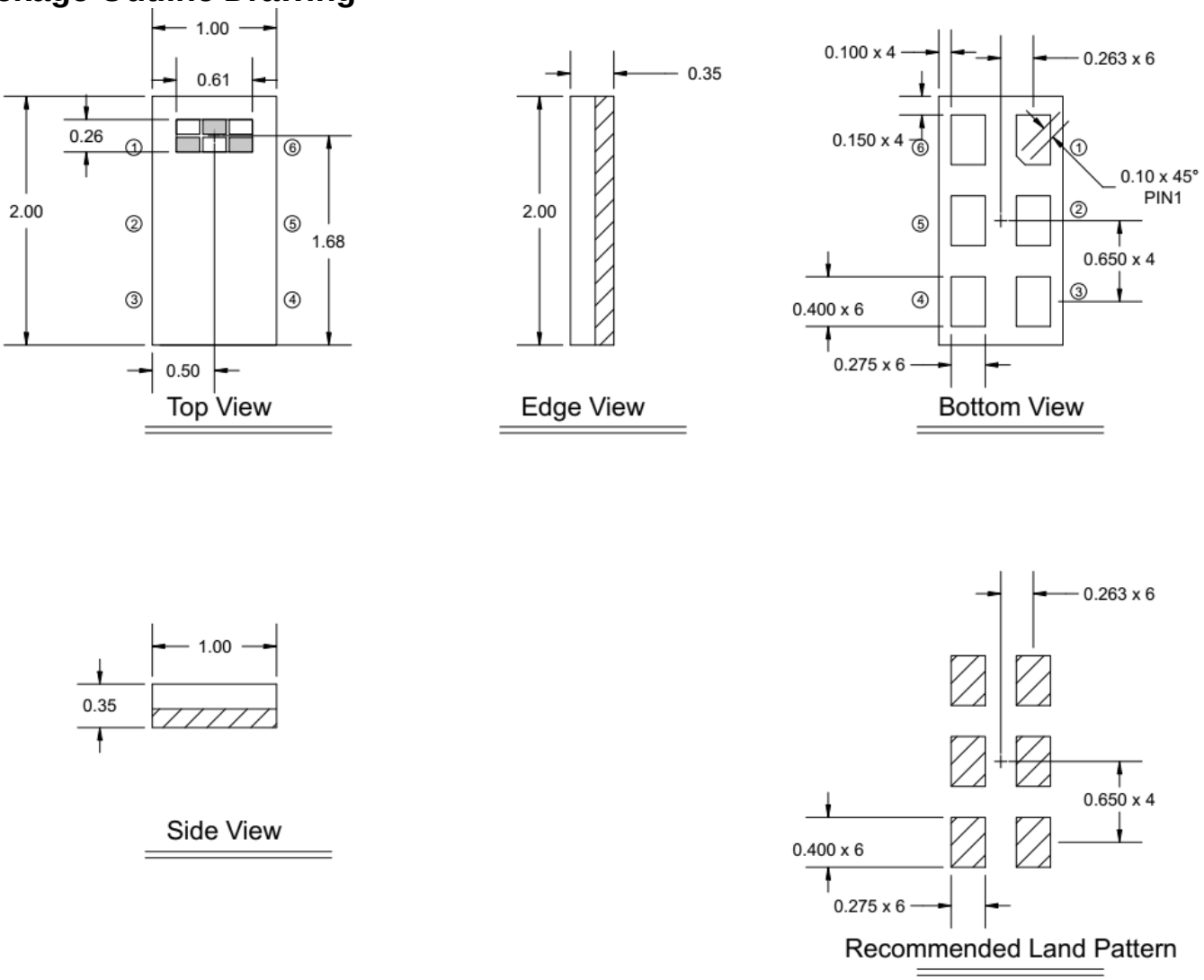
Table 26. Register 0x35 (FIFO_R_CNTH)–Actual Reading of FIFO Level

Bit	Access	Default	Name	Function / Operation
7:2	RO	0	Unused	Unused
1:0	RO	0	FIFO_R_CNT[9:8]	Upper 2 bits of the actual reading of the FIFO level counter

Table 27. Register 0x53 (TEST_CON4) –Photodiode Configuration 3

Bit	Access	Default	Name	Function / Operation
7:0	RW	0		User must write 0x02 to this byte during initialization.

Package Outline Drawing

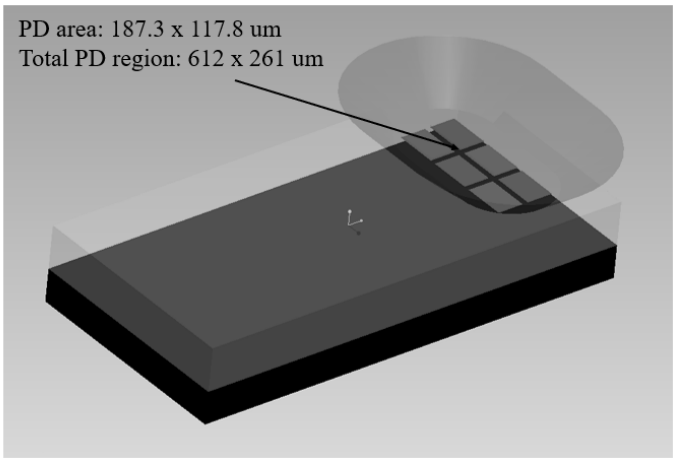


Note 1: Sensing PD center is at coordinate (0.50, 1.68). The total PD sensing area is 612μm×261μm
Note 2: Grey photodiodes are ALS PDs, white ones are CLEAR PDs
Note 3: All tolerances are ±0.1mm unless otherwise noted

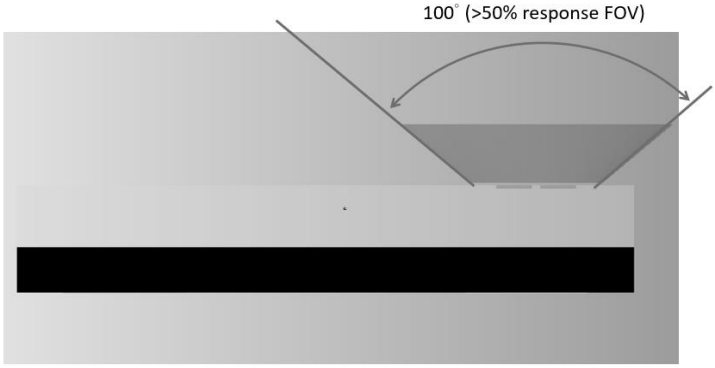
3D Product Drawing

Refer to the following 3D drawing of the SY3135AS21-J00: ALS and Clear PD (photodiode) FOV (field of view).

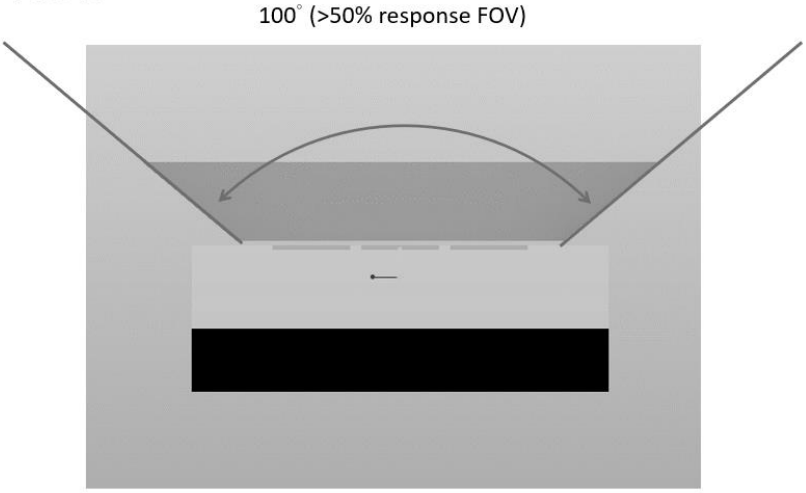
3D drawing



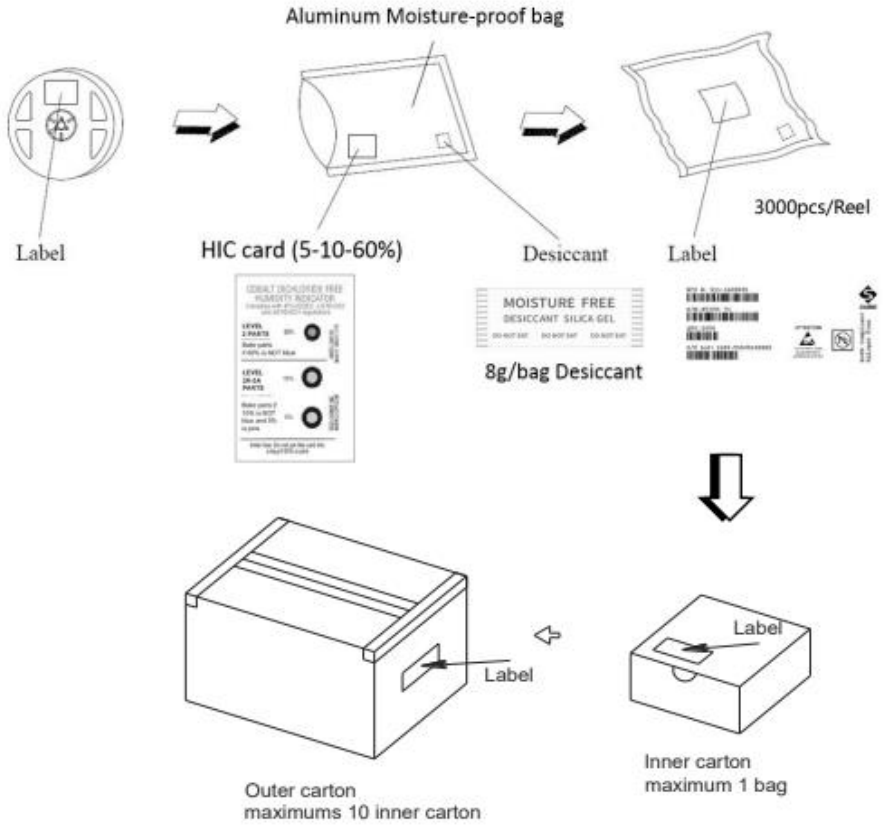
Side View



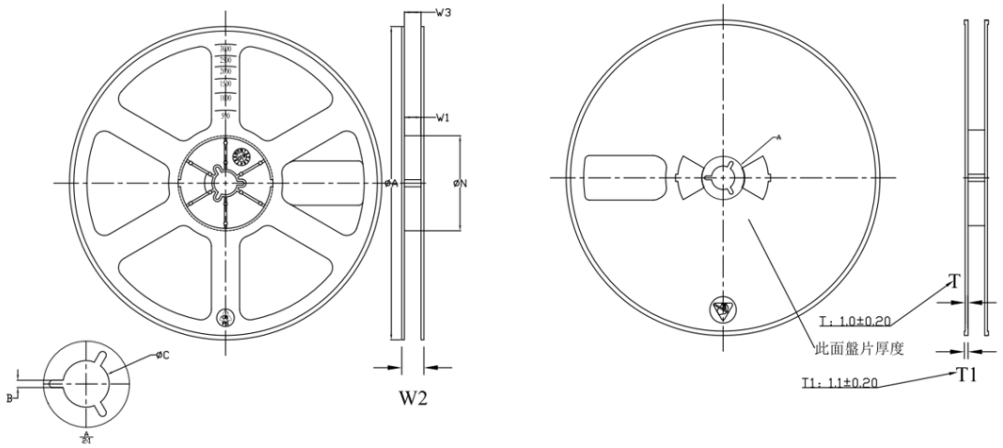
Side View



Packaging Specifications

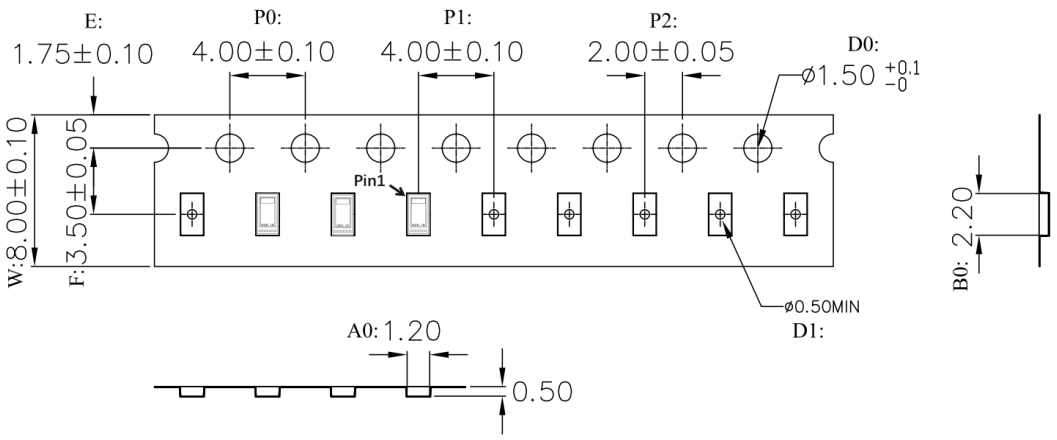


- **Dimensions of Reel (Units: mm)**



PRODUCT SPECIFICATIONS							
TAPE WIDTH	øA±1.0	øN±0.5	W1±0.5	W2 MAX	$W3^{+3}_{-1}$	$øC^{+0.3}_{-0.2}$	$B^{+0.3}_{-0.3}$
DPR-11D-B*	178	54	9.5	15.0	9.4	13.2	2.2

- **Tape Dimensions (Units: mm)**



Note: All dimensions in millimeters and exclude mold flash and metal burr.

Recommended Storage Method

Proper storage measures are recommended as soon as the bag is opened to prevent moisture absorption. The following conditions should be observed if bags are not available:

- Storage temperature: 10°C to 30°C
- Storage humidity: ≦60%RH max.
- Storage Time: ≦168hr max.

Moisture-Proof Package

To avoid moisture absorption by the resin, the product should be stored under the following conditions:

- Temperature: 23 ± 5°C
- Relative humidity: 60% (max)
- Baking is required if the devices have been stored unopened for more than 24 months and the HIC card is not discolored.

ESD Precaution

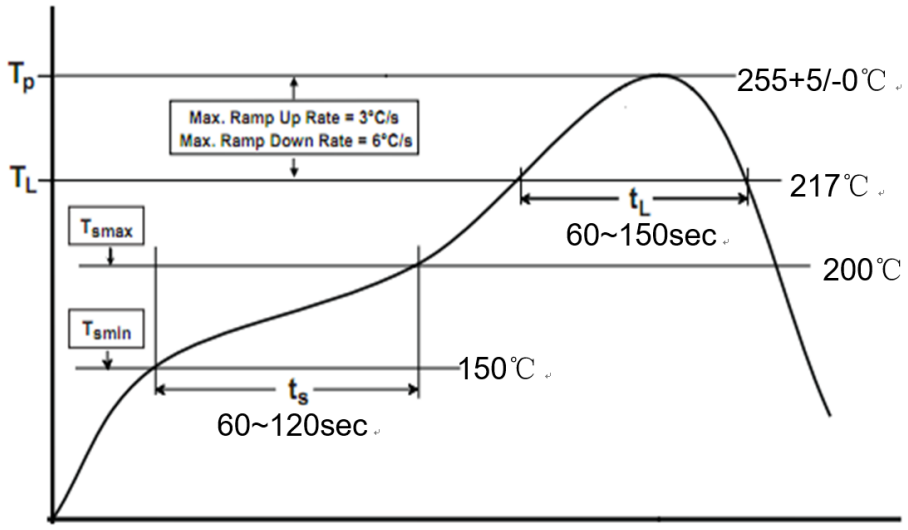
Proper storage and handling procedures should be followed to prevent ESD damage to the devices, especially when removed from the anti-static bag. Electro-Static Sensitive Devices warning labels are on the packaging.

Manual Soldering Corrections

Make any necessary soldering corrections manually.

The temperature must not exceed 350°C (using a 25W soldering iron) for a duration of no more than 3 seconds. Do not apply soldering to the same pin more than once.

Recommended Solder Profile



Note 1: Reflow soldering should not be done more than three times.

Note 2: Do not put stress on the devices during the heating stage while soldering.
Note 3: Do not warp the circuit board after soldering.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Jul. 29, 2025	Initial Release	

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