



SILERGY

# SA51510

## Analog Class-D Audio IC for Automotive Application

### General Description

The SA51510 is a high efficiency mono Class-D audio power amplifier for automotive emergency call (e-Call), telematics, instrument cluster and acoustic vehicle alerting system (AVAS) applications. It can output 22W into 4Ω load at less than 10% THD+N from a 14.4V supply. The product can operate on a wide voltage range with battery supply. The adjustable power limit function allows user to set a virtual voltage rail lower than supply voltage to limit the amount of current through the speaker. Output DC detection circuit prevents speaker damage from long-time current stress if the input capacitors are damaged or shorts exist on the inputs.

The SA51510 can drive a mono speaker as low as 2Ω. The high efficiency of the amplifier allows eliminating an external heat sink when playing music.

Over current protection can protect amplifier from output short to GND, PVDD, and output-to-output. The over current protection, DC protection and over temperature protection includes an auto-recovery feature. The amplifier also has built-in load diagnostic function designed for detecting the status of output connections at start. It supports the following diagnostics: speaker wire shorted to GND or PVDD, speaker cross-shortened and speaker open. The diagnostics result is reported by I<sup>2</sup>C registers and FAULTZ pin.

The SA51510 is available in a compact TSSOP16E package.

### Features

- Wide Voltage Range
  - 4.5V to 28V with Under and Over Voltage Protection
  - 40V Load-dump Protection per ISO-16750-2
- High Output Power Capability
  - 22 W/4 Ω, 10% THD+N at 14.4V
  - 38W/8Ω, 1% THD+N at 28V
- Excellent Audio performance
  - 0.03% THD+N at 1W/4 Ω 12V
  - 102dB A-weighted SNR
- Comprehensive Protection
  - Under Voltage, Over Voltage, Over Temperature, Over Current, DC Detection Protection with Auto Recovery
  - Selectable Power Limit Function for Speaker Protection
- Load Diagnostic Functions:
  - Open and Shorted Output Load
  - Output-to-ground and Output-to-PVDD Shorts and Shorted Output Indicator
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3
- Differential/Single-ended Input
- I<sup>2</sup>C Deglitch
- Spread Spectrum and Programmable Edge Rate to Optimize EMC Performance

### Applications

- Automotive Clusters
- Automotive Emergency Call Systems (eCall)
- Automotive Telematics
- Automotive Acoustic Vehicle Alerting System (AVAS)

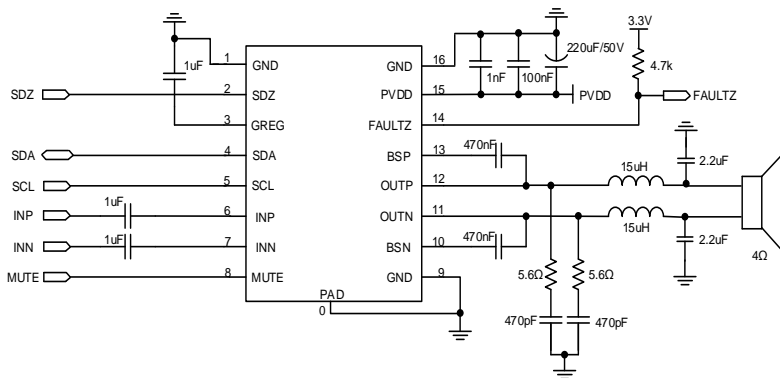


Figure 1. Typical Application Circuit

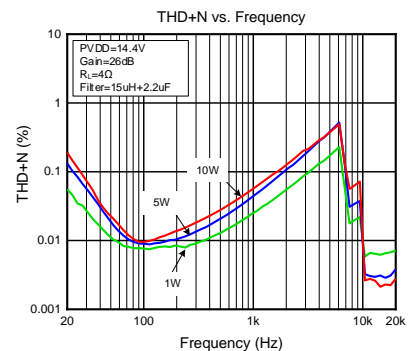


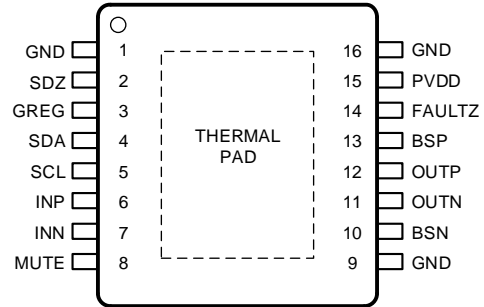
Figure 2. THD+N vs. Frequency

## Ordering Information

Ordering Part Number	Package Type	Top Mark
SA51510HFP	TSSOP16E RoHS Compliant and Halogen Free	EUKxyz

*x=year code, y=week code, z=lot number code*

## Pinout (Top View)



Pin Name	Pin No	Type (1)	Pin Description
SDZ	2	DI	Hardware shutdown pin, active low.
FAULTZ	14	DO	Open drain output used to display fault status, active low.
GREG	3	P	Internal regulator output. Decouple to GND with at least a 1 $\mu$ F capacitor as close to pin as possible. This pin must not be used to drive external circuit.
INP	6	AI	Positive audio input. Biased at 2.4V, a DC block capacitor should be used on this pin.
INN	7	AI	Negative audio input. Biased at 2.4V, a DC block capacitor should be used on this pin.
MUTE	8	DI	Hardware can be pulled up to PVDD with resistor.
PVDD	15	P	Power supply. Decouple to GND with a 0.1 $\mu$ F and a 1nF capacitor with the smallest capacitor placed as close to pins as possible. A 220 $\mu$ F or greater capacitor for low frequency noise filtering.
BSP	13	AI	Bootstrap supply for positive high-side FET. Connect a 470nF ceramic capacitor between the BSP and the OUTP pin.
OUTP	12	PO	Class-D H-bridge positive output.
GND	1,9,16	P	Power Ground.
BSN	10	AI	Bootstrap supply for negative high-side FET. Connect a 470nF ceramic capacitor between the BSN and the OUTN pin.
OUTN	11	PO	Class-D H-bridge negative output.
SDA	4	DIO	I <sup>2</sup> C serial control data input and output.
SCL	5	DI	I <sup>2</sup> C serial clock input.
Thermal Pad	—	—	Should be soldered to ground with multiple vias for best heat dissipation and electrical performance.

**Note 1:** Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout

## Block Diagram

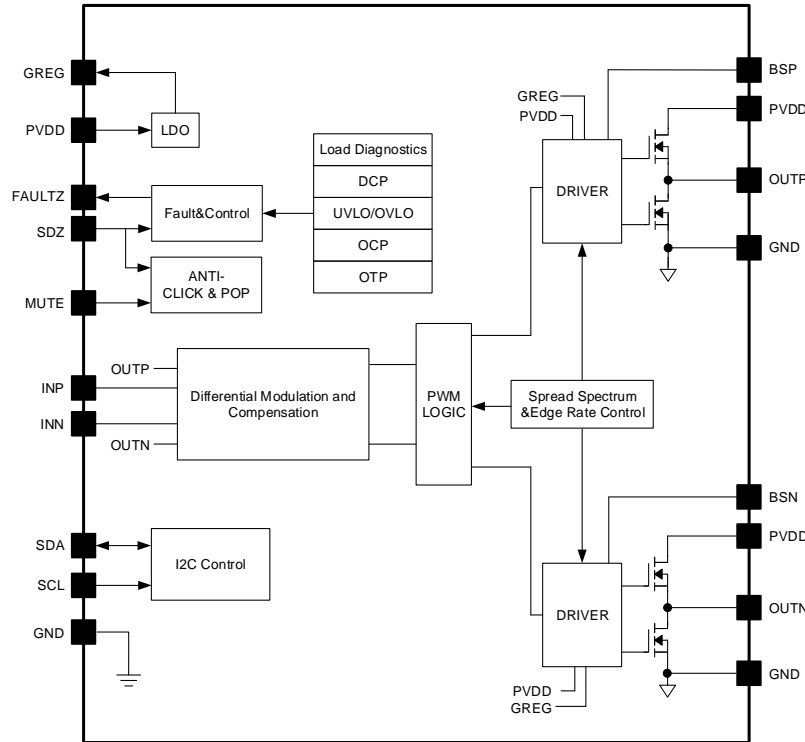


Figure 3. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
V <sub>DD</sub> , Supply Voltage PVDD	-0.3	34	V
V <sub>DD,MAX</sub> , Transient supply voltage: PVDD ( t ≤ 400ms exposure )	-1	40	
OUT <sub>x</sub>	-1	34	
BS <sub>x</sub> to OUT <sub>x</sub>	-0.3	4	
V <sub>I</sub> , Interface Pin Voltage SDZ, MUTE, FAULTZ	-0.3	PVDD +0.3	
INP, INN	-0.3	3.6	
SDA, SCL	-0.3	GREG +0.3	
T <sub>J</sub> , Operating Junction Temperature	-40	150	°C
T <sub>stg</sub> , Operating Storage Temperature	-65	150	

Thermal Information (2)	Min	Typ	Max	Unit
θ <sub>JA</sub>		28.4		°C/W
θ <sub>JC</sub> (top)		20		
θ <sub>JC</sub> (bottom)		2.6		
θ <sub>JB</sub>		15.3		
ψ <sub>JT</sub>		0.3		

Recommended Operating Conditions	Min	Max	Unit
V <sub>DD</sub> , Supply Voltage PVDD	4.5	28	V
V <sub>IH</sub> , High-Level Input Voltage SDZ, MUTE	1.25	3.3	
V <sub>IL</sub> , Low-Level Input Voltage SDZ, MUTE	0	0.5	
R <sub>L</sub> , Minimum Load Resistance Output Configuration	1.8		Ω
T <sub>A</sub> , Operating Ambient Temperature Range	-40	125	°C

**Electrical Characteristics**  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $\text{PVDD}=12\text{V}$ ,  $\text{R}_L=4\Omega$ , default P2C setting, typical values are test at  $T_A=25^{\circ}\text{C}$ , unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
DC Characteristics	PVDD	$V_{DD}$	4.5		28	V	
	Quiescent Supply Current	$I_Q$	SDZ=high, no load, no snubber		12		mA
			SDZ=high, with $4\Omega$ load, $5.6\Omega+470\text{pF}$ snubber, $15\mu\text{H}+2.2\mu\text{F}$ filter (3)		18.4		
			SDZ=low, no load, no snubber		5.2		
	High-Level Input Voltage	$V_{IH}$	SDZ, MUTE	1.3			V
	Low-Level Input Voltage	$V_{IL}$	SDZ, MUTE			0.5	V
	Low-Level Output Voltage	$V_{OL}$	FAULTZ, $\text{R}_{PULL-UP}=100\text{k}\Omega$			0.5	V
	High-Level Input Current	$I_{IH}$	$V_I=12\text{V}$ , $V_{DD}=18\text{V}$			1	$\mu\text{A}$
	Low-Level Input Current	$I_{IL}$	$V_I=0\text{V}$ , $V_{DD}=18\text{V}$			1	$\mu\text{A}$
	Drain-Source on-State Resistance	$\text{R}_{\text{DSON}}$	$V_{DD}=12\text{V}$ , $I_d=200\text{mA}$ , $T_J=25^{\circ}\text{C}$ , includes bonding wire and metallization resistance		180		$\text{m}\Omega$
	Gain	G	No load	19	20	21	dB
				25	26	27	
				31	32	33	
				35	36	37	
	Turn-on Time (3)	$t_{\text{ON}}$	From SDZ high to PWM on		300		ms
Turn-off Time (3)	$t_{\text{OFF}}$	From SDZ low to PWM off		58		ns	
Class-D Output Offset Voltage (Measured Differentially)	$ V_{\text{OS}} $	$T_J=25^{\circ}\text{C}$ , no input signal, Gain=26dB		1.5	10	mV	
Gate Drive Supply	GREG	SDZ=high, no input signal	3.2	3.4	3.6	V	
PWM Frequency	$f_{\text{PWM}}$	Selectable for AM avoidance		400		kHz	
				500			
AC Characteristics (3)	Power Supply Ripple Rejection	PSRR	$V_{\text{ripple}}=200\text{mV}_{\text{PP}}$ , Gain=20dB, 1kHz, inputs AC-coupled to GND		-65		dB
	Output Power	$P_o$	$\text{PVDD}=6\text{V}$ , $\text{R}_L=2\Omega$ , $f=1\text{kHz}$ , $\leq 1\% \text{THD+N}$		4.4		W
			$\text{PVDD}=10\text{V}$ , $\text{R}_L=2\Omega$ , $f=1\text{kHz}$ , $\leq 1\% \text{THD+N}$		11.9		
			$f=1\text{kHz}$ , $\leq 1\% \text{THD+N}$		12.3		
			$\text{PVDD}=14.4\text{V}$ , $\text{R}_L=4\Omega$ , $f=1\text{kHz}$ , $\leq 10\% \text{THD+N}$		22		
			$\text{PVDD}=12\text{V}$ , $\text{R}_L=8\Omega$ , $f=1\text{kHz}$ , $\leq 10\% \text{THD+N}$		9.4		
			$\text{PVDD}=28\text{V}$ , $\text{R}_L=8\Omega$ , $f=1\text{kHz}$ , $\leq 1\% \text{THD+N}$		38.1		
	Total Harmonic Distortion + Noise	THD+N	$f=1\text{kHz}$ , $P_o=1\text{W}$		0.03		%
Output Integrated Noise Floor	$V_n$	$T_J=25^{\circ}\text{C}$ , 20Hz to 20kHz, A-weighted filter, Gain=20dB		62		$\mu\text{V}$	
Signal to Noise Ratio	SNR	Max output at $\text{THD+N}<1\%$ , $f=1\text{kHz}$ , Gain=20dB, A-weighted, $\text{PVDD}=12\text{V}$		102		dB	
Protection (3)	$V_{DD}$ Under Voltage Lockout Threshold	$V_{\text{UVLO\_RISE}}$	$V_{DD}$ Rising to exit UVLO		3.9	4.3	V
		$V_{\text{UVLO\_FALL}}$	$V_{DD}$ Falling to enter UVLO	3.2	3.6		V
	$V_{DD}$ Over Voltage Lockout Threshold	$V_{\text{OVLO\_RISE}}$	$V_{DD}$ Rising to enter OVLO		35.5	36.6	V
		$V_{\text{OVLO\_FALL}}$	$V_{DD}$ Falling to exit OVLO	32.4	33.8		V
	Thermal Shutdown Temperature	$T_{\text{SD}}$			150		$^{\circ}\text{C}$
	Thermal Shutdown Hysteresis	$T_{\text{HYS}}$			15		$^{\circ}\text{C}$
	Short Circuit Protection (3)	$I_{\text{SC}}$	$T_J=25^{\circ}\text{C}$		6.8		A
	Over Current Protection (3)	$I_{\text{OC}}$	$T_J=25^{\circ}\text{C}$ , full-bridge overload		5		A
DC Detection Time (3)	$t_{\text{DCDET}}$			605		ms	

	DC Detection Threshold (Output Differential Duty-cycle) (3)				19		%
Load Diagnostics	Voltage to Detect a Short from OUT Pin(s) to Power			6			V
	Resistance to Detect a Short from OUT Pin(s) to Ground					50	$\Omega$
	Open Load Detection Threshold		Including speaker wires	70	100	180	$\Omega$
	Short Load Detection Threshold		Including speaker wires	0.6	1.2	1.8	$\Omega$
I <sup>2</sup> C	SDA/SCL High-level Input Voltage			1.3			V
	SDA/SCL Low-level Input Voltage					0.5	V
	SDA High-level Output Voltage		R <sub>PULL-UP</sub> =100k $\Omega$ to 3.3V	3			V
	SDA Low-level Output Voltage		3mA sink current			0.3	V

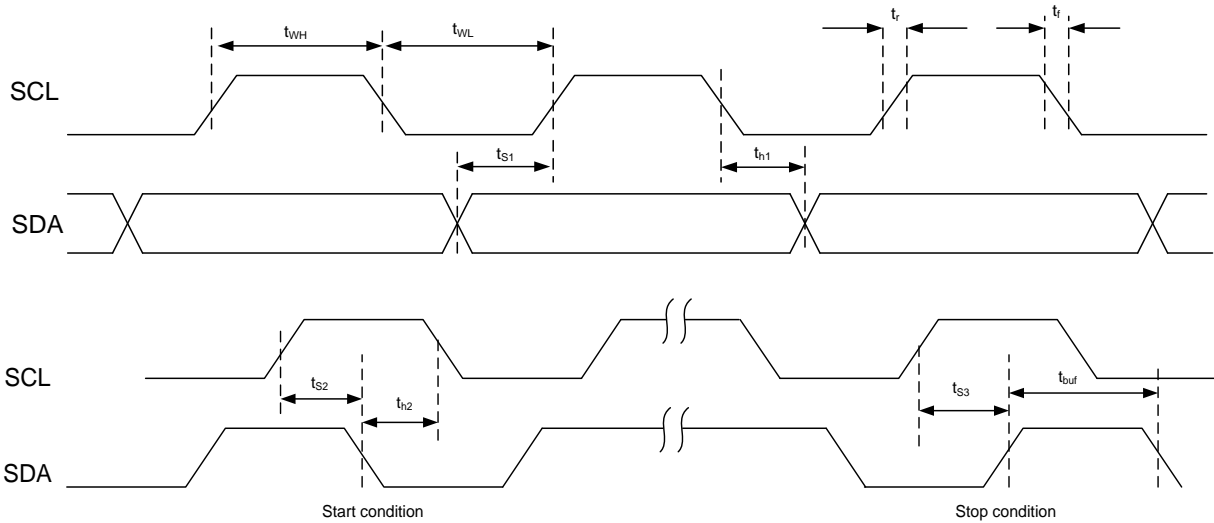
**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a high effective four layers thermal conductivity test board of JEDEC 51-7.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

I <sup>2</sup> C Timing Requirements for Control Port					
Parameter	Symbol	Test Condition	Min	Max	Unit
SCL Frequency	$f_{SCL}$	No wait states		400	kHz
SCL and SDA Rise Time	$t_r$			300	ns
SCL and SDA Fall Time	$t_f$			300	ns
SCL High Duration Time	$t_{WH}$		0.6		$\mu$ s
SCL Low Duration Time	$t_{WL}$		1.3		$\mu$ s
SDA to SCL Setup Time	$t_{S1}$		250		ns
SCL to SDA Hold Time	$t_{h1}(1)$		0		ns
Free Time between Stop and Start Condition	$t_{buf}$		1.3		$\mu$ s
SCL to Start Condition	$t_{S2}$		0.6		$\mu$ s
Start Condition to SCL Hold Time	$t_{h2}$		0.6		$\mu$ s
SCL to Stop Condition	$t_{S3}$		0.6		$\mu$ s

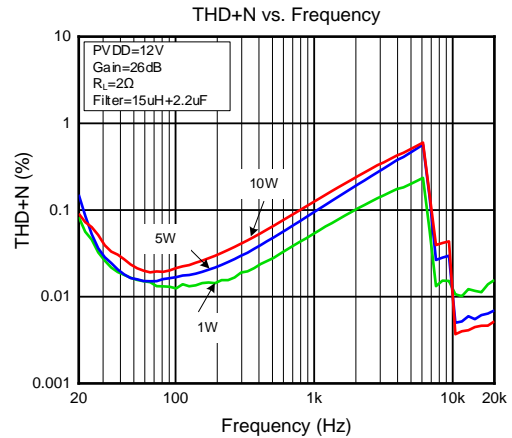
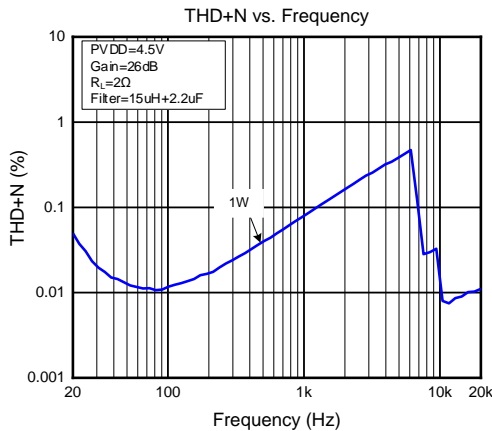
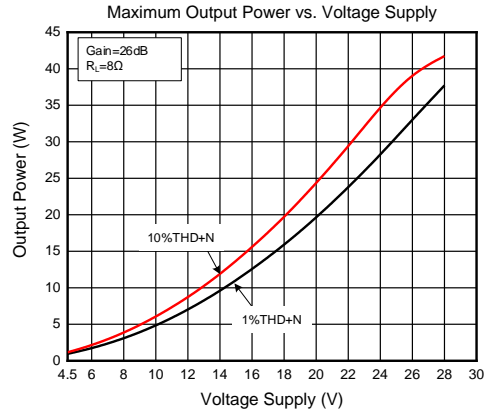
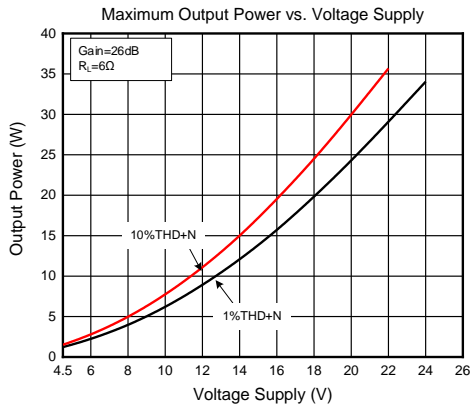
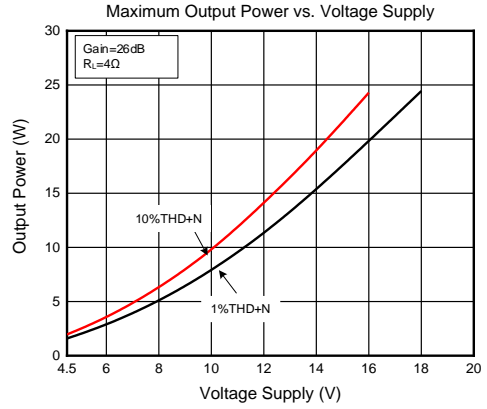
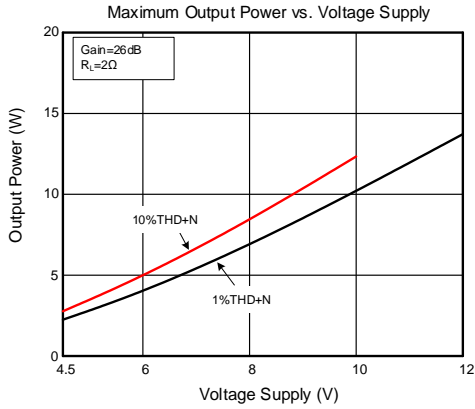
**Note 1:** A device must internally provide a hold time of at least  $t_f$  for the SDA signal to bridge the undefined region of the falling edge of SCL.

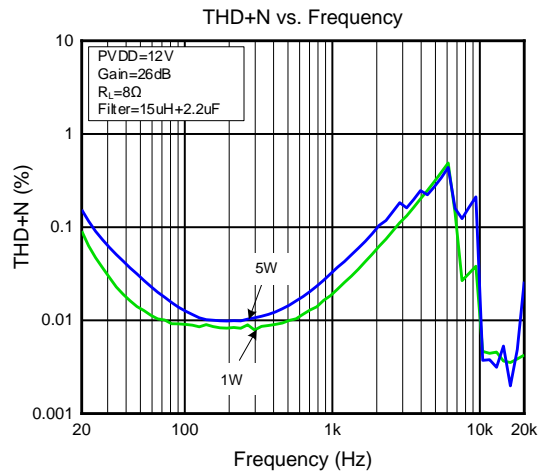
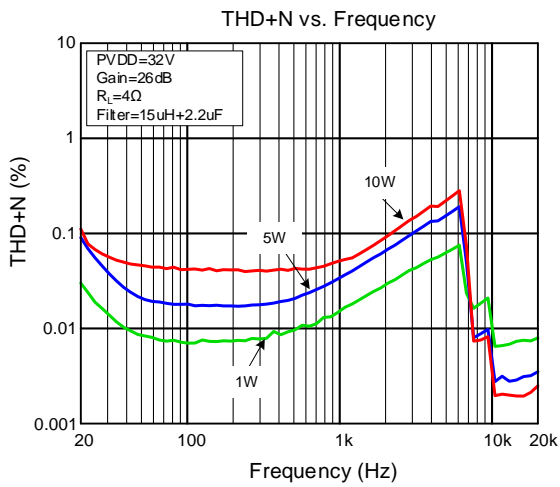
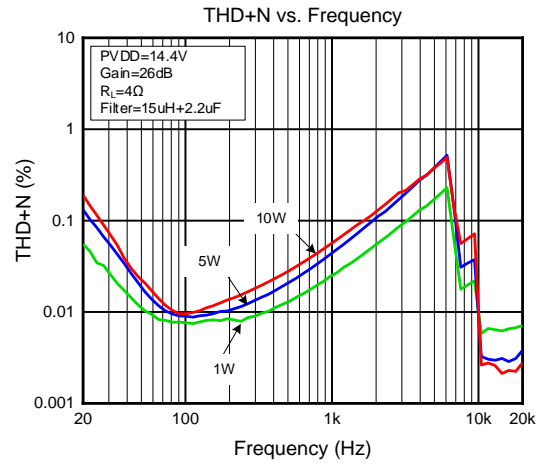
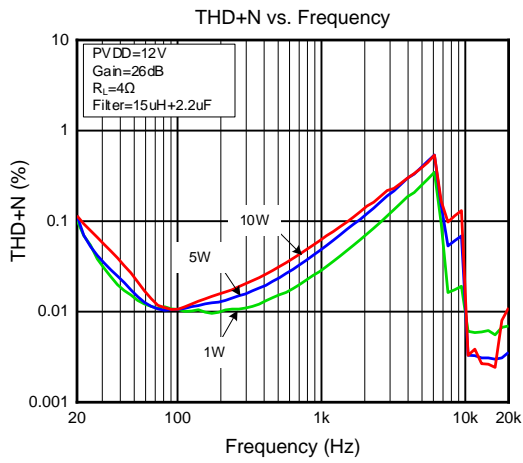
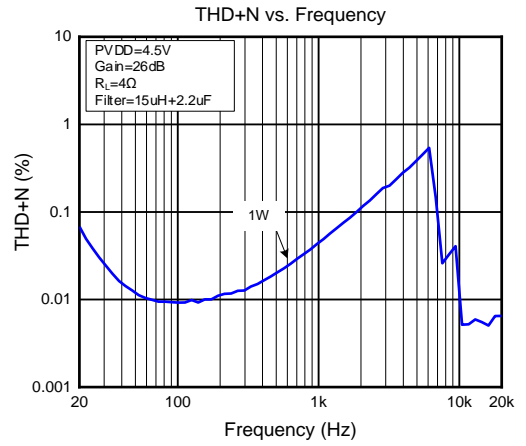
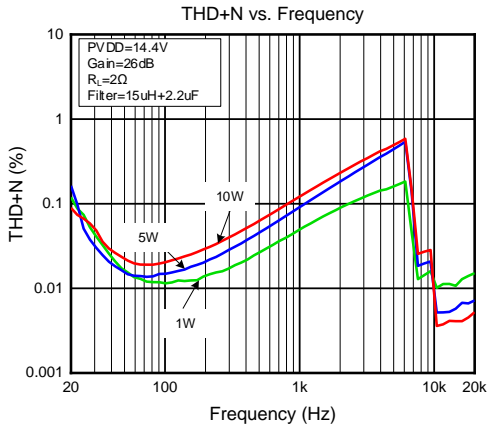


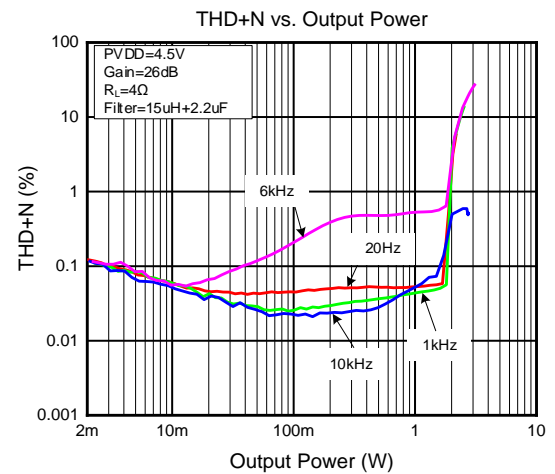
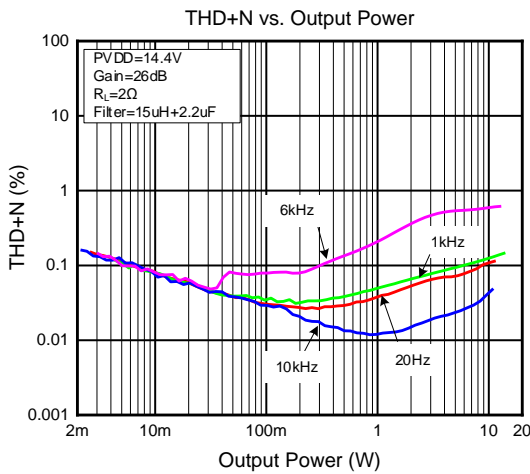
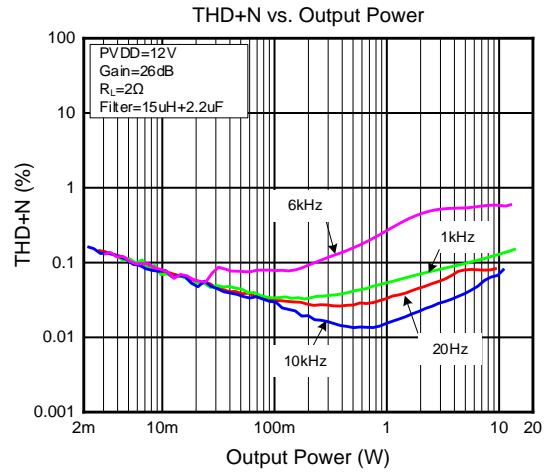
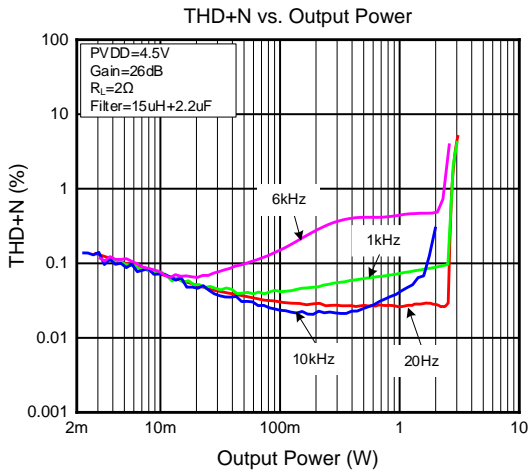
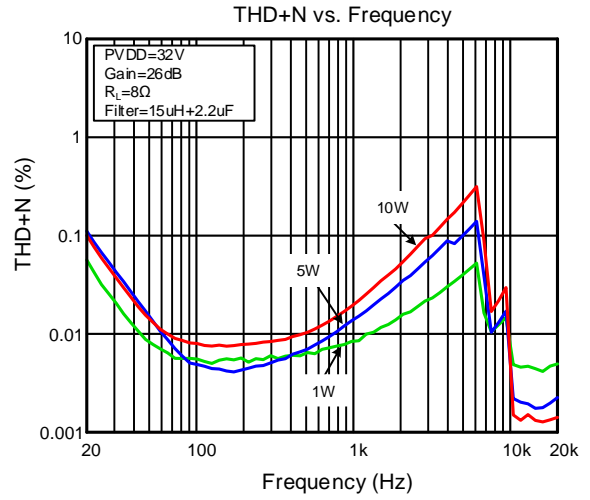
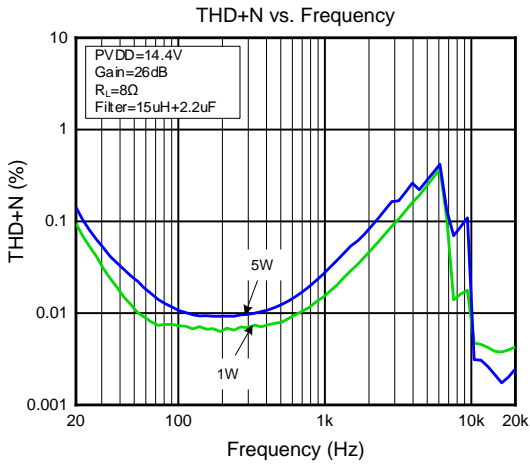
**Figure 4. I<sup>2</sup>C Timing Diagram**

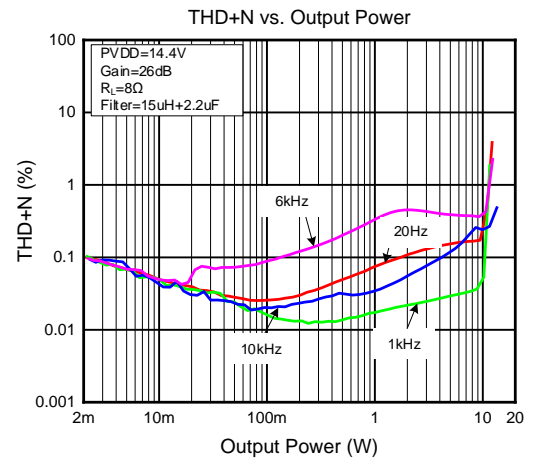
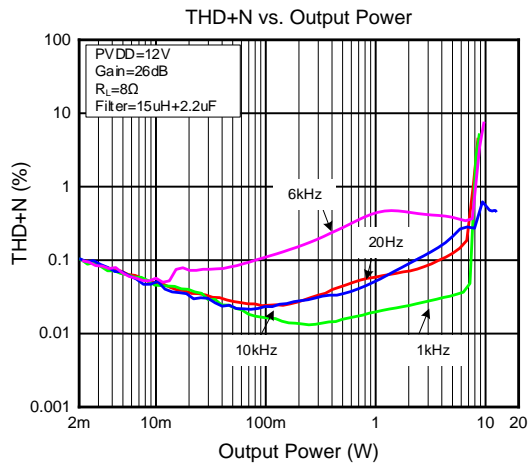
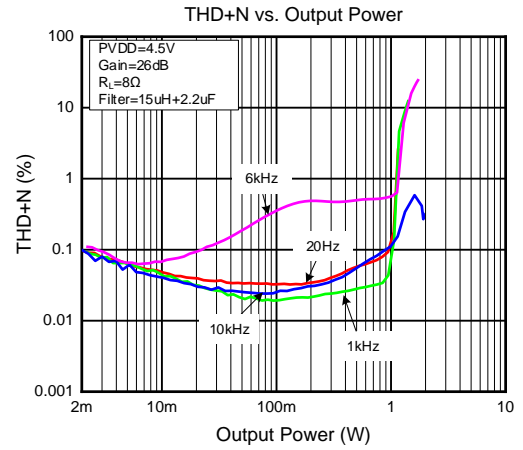
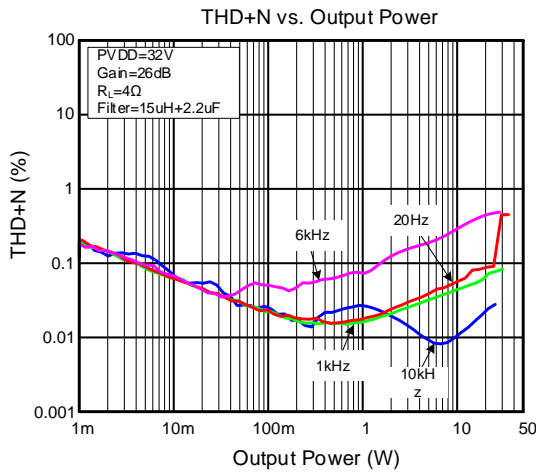
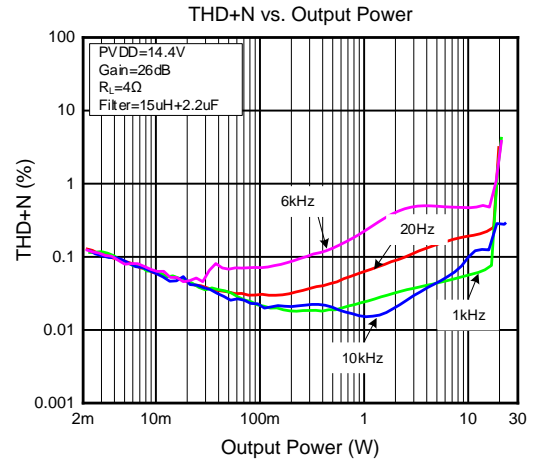
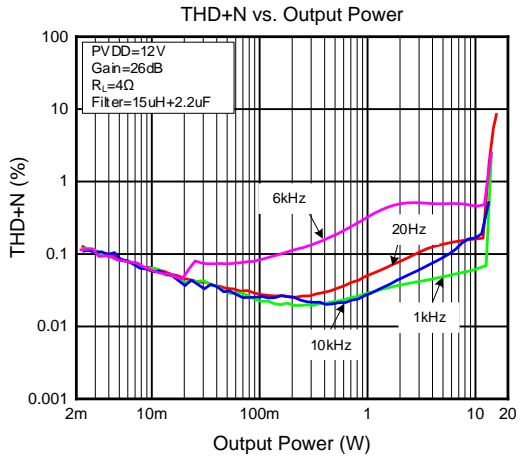
## Typical Performance Characteristics

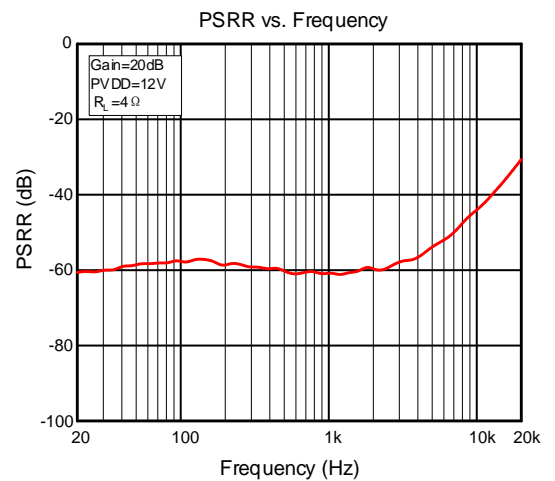
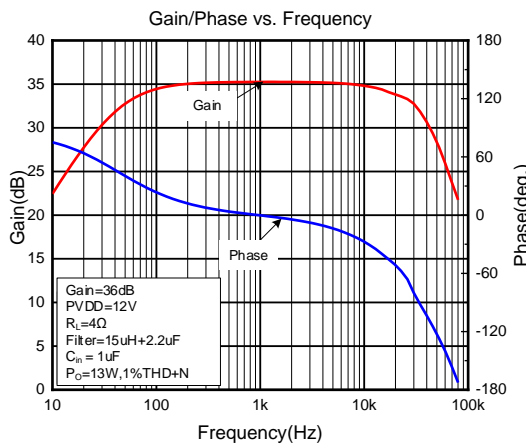
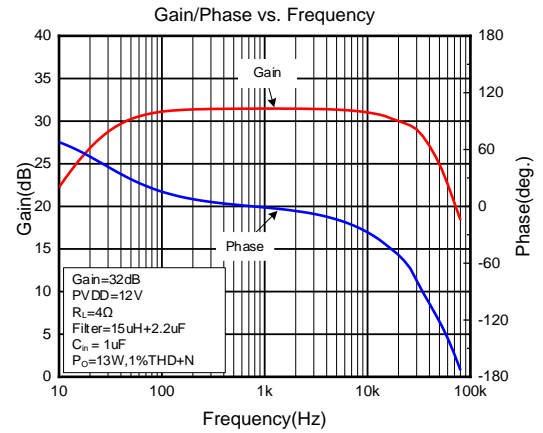
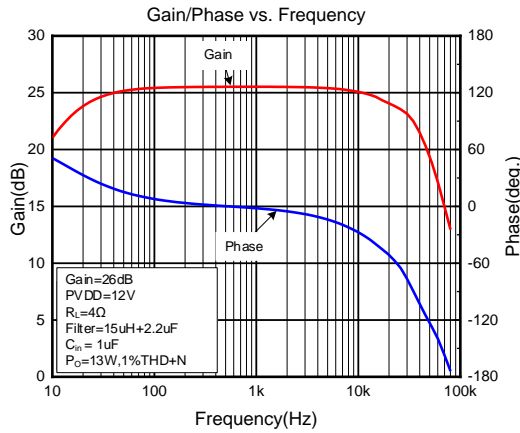
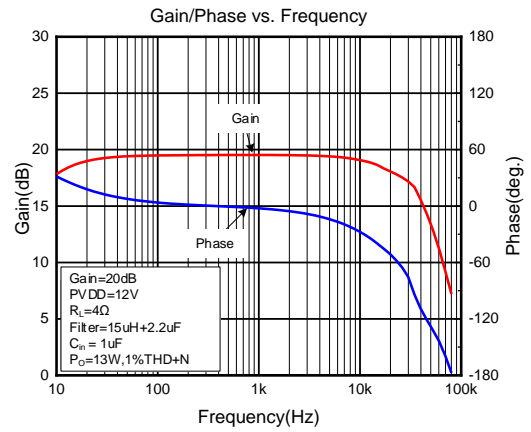
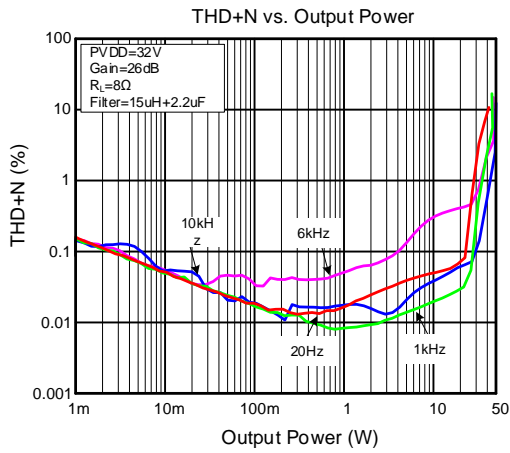
(All measurements taken at 1 kHz, unless otherwise noted.)

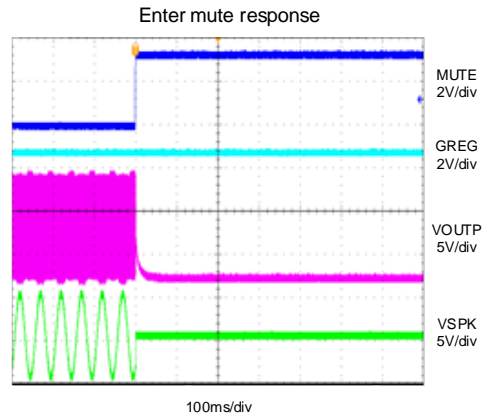
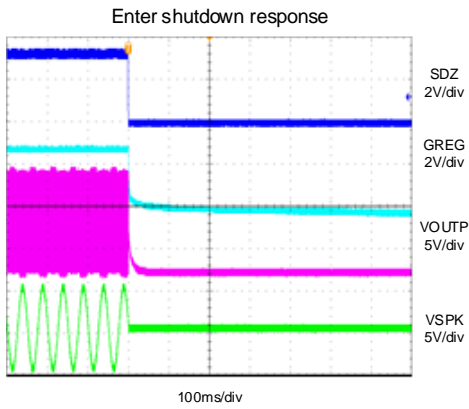
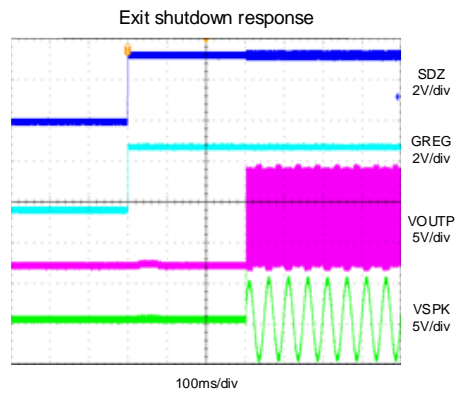
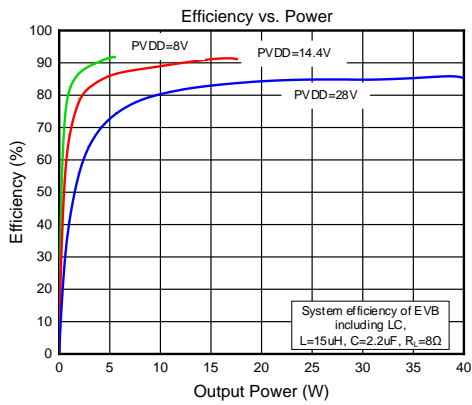
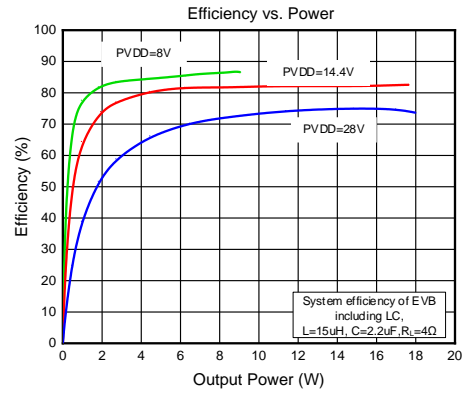
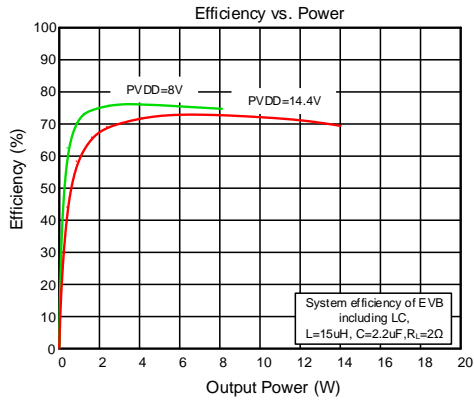


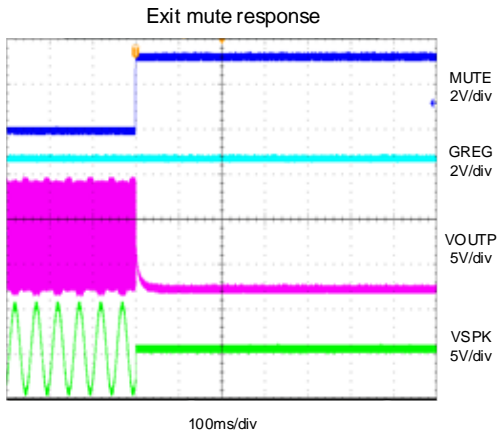












## Detailed Description

The SA51510 is a high-performance mono analog audio amplifier IC used in the automotive applications which is AEC-Q100 qualified with temperature grade1 (-40°C to 125°C), HBM ESD classification level H2, and CDM ESD classification level C3 per AEC-Q100-011 Rev.D.

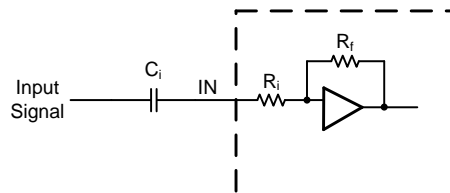
The function operations of SA51510 are as follows:

### Gain Setting and Input Resistance

The gain of the SA51510 is set by bit7 and bit6 of Control register (0x03). By varying the input resistors inside the amplifier, the various gains are achieved. The respective gains and input resistance are listed in Table 1. There is  $\pm 10\%$  variation in input resistance from production variation, so the input resistance of the amplifier varies from a minimum of  $4.6\text{k}\Omega \pm 10\%$  to a maximum of  $30\text{k}\Omega \pm 10\%$  when the gain is changed. As a result, if a single capacitor is used in the input high-pass filter, the  $-3\text{ dB}$  or cutoff frequency may change when changing gain steps.

**Table 1. Gain and Input Impedance**

Amplifier Gain (dB)	Input Impedance (k $\Omega$ )
20	30
26	15
32	7.5
36	4.6



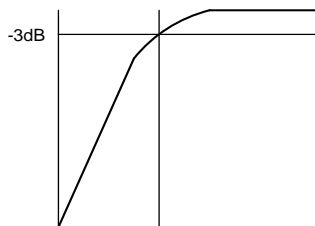
**Figure 5. Input Impedance**

Use formula 1 to calculate the  $-3\text{dB}$  frequency. Use the values listed in Table 1 for  $R_i$ .

$$f_c = \frac{1}{2\pi \cdot R_i \cdot C_i} \quad (1)$$

### Input Capacitor, Ci

The performance at low frequency (bass) is affected by the corner frequency ( $f_c$ ) of the high-pass filter composed of input resistor ( $R_i$ ) and input capacitor ( $C_i$ ), as determined by the formula (1). The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level.



**Figure 6. -3dB Frequency of HPF**

The resistance of input resistors is different at different gain setting. Consider the specification calls for a flat bass response down to 20Hz. Formula 1 is reconfigured as formula 2.

$$C_i = \frac{1}{2\pi \cdot R_i \cdot f_c} \quad (2)$$

Choose  $C_i$  such that  $f_{-3dB}$  is well below the lowest frequency of interest. Typically, a  $1\mu F$  ceramic capacitor is suggested. For best audio quality, use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or ceramic capacitor.

## Differential Input

The SA51510 has an internal fully differential input structure which can provide more outstanding common mode rejection ratio. When using SA51510 with a differential input source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input.

In addition, the SA51510 can be used with a single-ended source, AC-ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. The input signal connection is shown as Figure 7.

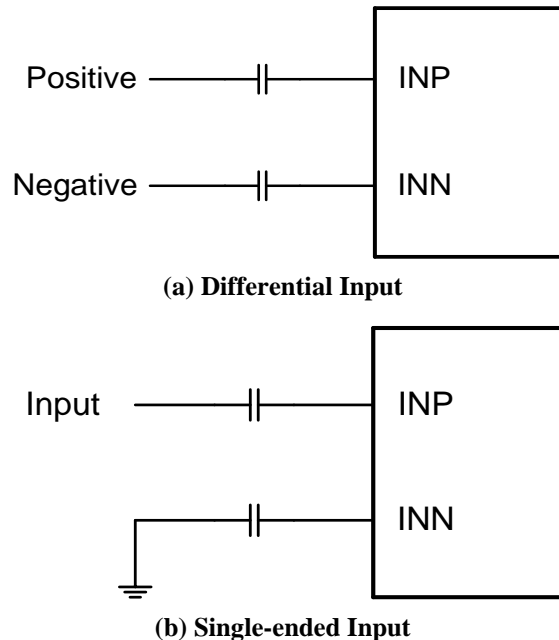


Figure 7. Input Signal Connection

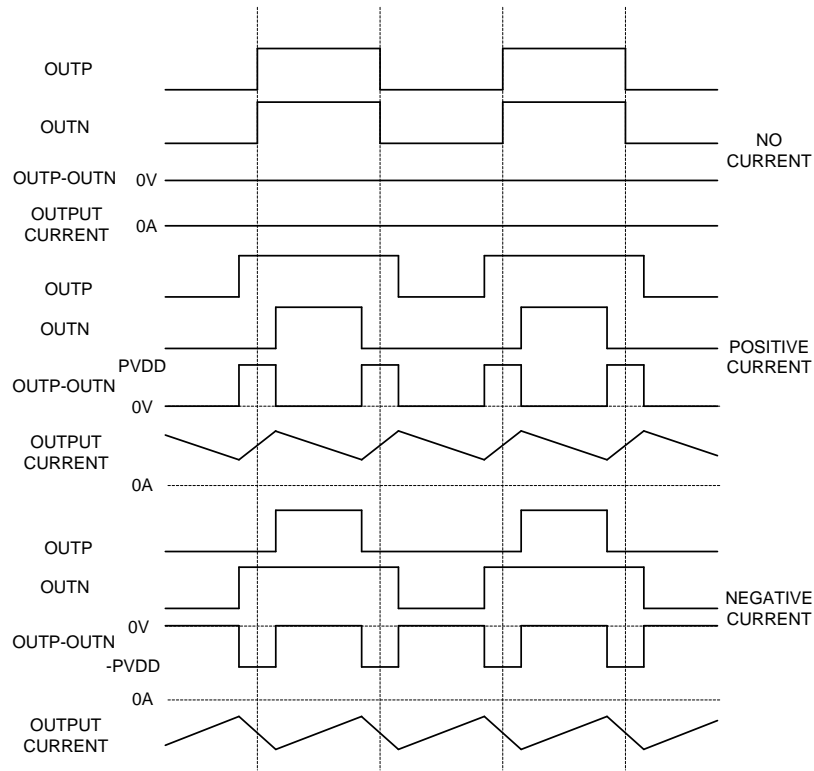
## SDZ and Mute Operation

The SA51510 employs a shutdown mode of operation designed to reduce supply current during periods of nonuse for power conservation. Pull down the SDZ pin, the amplifier will enter shutdown mode, then the internal LDO is disabled, MOSFET stay in Hi-Z state for low power dissipation, and the slave I<sup>2</sup>C device can't be visited. Pull high SDZ pin, the amplifier will exit shutdown mode, perform load diagnostics and drive speaker for music as Figure 9 shown.

The SA51510 has a mute mode to make the amplifier output silent, which is active high on MUTE pin. Pull down MUTE pin to return to normal play mode after shorter than  $20\mu s$ .

## Modulation Scheme

The SA51510 uses BD mode modulation scheme, as shown in Figure 8. In BD mode, the two half-bridge switch in phase but the input signal for the modulators is inverted. Each output port is switching from 0V to the power supply voltage. When the OUTP and OUTN are in phase with each other and there is no input signal, there is almost no current into the speaker. When output voltages are positive, the duty cycle of OUTP is greater than 50% and OUTN is less than 50%. When output voltages are negative, the duty cycle of OUTP is less than 50% and OUTN is greater than 50%. The voltage across the speaker is at 0V throughout most of the switching period, reducing the switching current, which reduces any  $I^2R$  losses in the load.



**Figure 8. BD Mode Modulation**

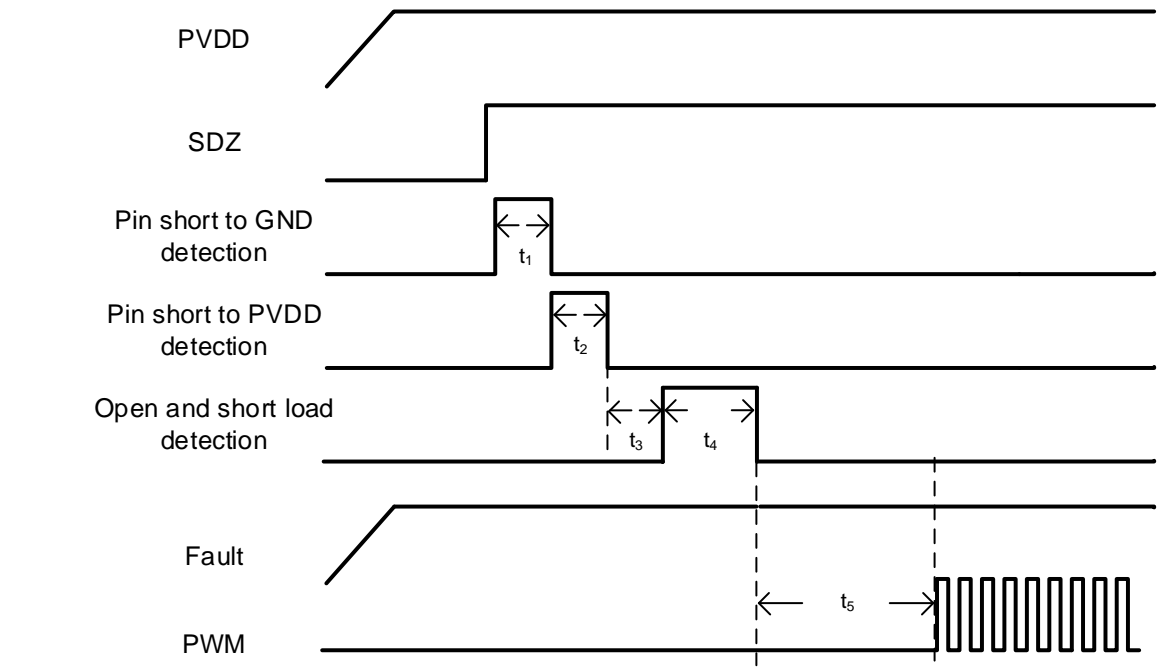
## Load Diagnostics and Timing

The SA51510 has built-in load diagnostic function designed for detecting the status of output connections at start. It includes the following diagnostics:

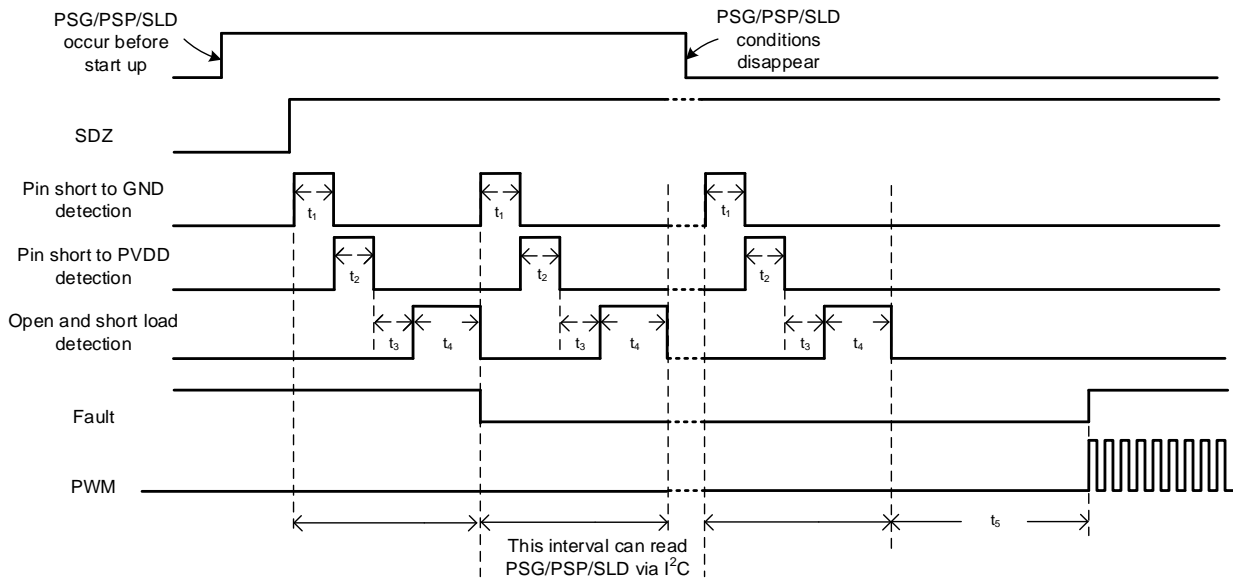
- Output short to Ground (PSG)
- Output short to Power (PSP)
- Shorted load (SLD)
- Open load (OLD)

The diagnostics result is reported by Fault register(0x01) and Status and Load Diagnostic register(0x02). The load diagnostic function will run after pulling high SDZ pin and auto recovery from over current, direct current, over temperature, under voltage or over voltage error. The device will diagnosis whether the output is a short to GND, short to PVDD, the load is shorted and the load is open sequentially, and if a fault is diagnosed, subsequent detection will be skipped until next cycle. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning. The load diagnostic takes approximately 150ms (typical) to detect the four-load status, and then wait 150ms (typical) for control system to acquire a LD result. Except open load error, any other fault condition will put the output in a Hi-Z state and FAULTZ pin be pulled down. If there is no error in load diagnostics, the amplifier will start for output PWM sequence for audio signal. At default I<sup>2</sup>C setting, bit5 of Control register 2(0x04) is 0, the I<sup>2</sup>C report of PSG(PSP) of OUTP and OUTN are incorporative, that is no matter OUTP or OUTN detected PSG(PSP)error, bit 1(bit 0) of register 0x02 will be 1. But the PSG(PSP) detection of OUTP and OUTN are separated, so the I<sup>2</sup>C report of this two errors can be separated when bit5 of Control register 2(0x04) is 1, at this moment, bit1(bit 0) of register 0x02 will represent PSG(PSP) error of OUTP, and bit 6 (bit 7) of register 0x04 will represent PSG(PSP) error of OUTN.

The timing sequence of load diagnostics is shown in Figure 9.



(a) Normal or OLD



(b) PSG/PSP/SLD Detect Continuously

- $t_1$ : PSG detect time, typical 3ms;
- $t_2$ : PSP detect time, typical 3ms;
- $t_3$ : interval time, typical 3ms;
- $t_4$ : OLD/SLD detect time, typical 141ms;
- $t_5$ : waiting time, typical 150ms.

Figure 9. Load Diagnostics Timing

In addition, if SA51510 is used in eCall system, where will do load diagnostic all the time unless an emergency happens, because of the timing variation, the recommended SDZ pull down time is at  $215\text{ms} \pm 15\text{ms}$  after SDZ pull up, which is appropriate to avoid entering play mode.

## PLIMIT

The PLIMIT circuit can limit the output peak-to-peak voltage to a certain level which is lower than supply voltage to limit the amount current of speaker for the purpose limiting the output power. This function is realized by limiting the duty cycle to a fixed maximum value. The limited output voltage can be set by bit3-bit5 of Control register (0x03). There are 7 selectable output voltage.

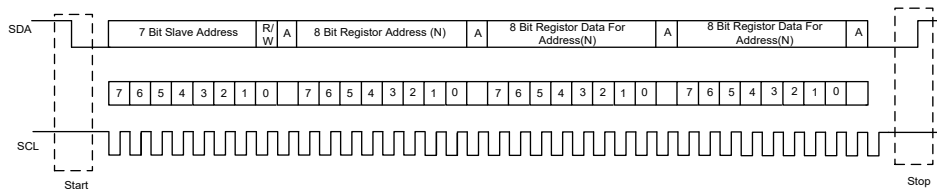
## I<sup>2</sup>C Serial Control Interface

The SA51510 employs I<sup>2</sup>C bus transfer protocol to communicate with system. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. SA51510 is always an I<sup>2</sup>C slave device.

The following function can be controlled by I<sup>2</sup>C interface:

- Changing gain setting to 20 dB, 26 dB, 32 dB, or 36 dB
- Controlling PLIMIT peak voltage value
- Reporting load diagnostic results
- Reporting the fault of protection
- Changing of switching frequency for AM radio avoidance

The SA51510 has a bidirectional I<sup>2</sup>C interface that compatible with the I<sup>2</sup>C bus protocol. A 100 kHz and 400 kHz data transfer rates are available for single-byte and multi-byte read/write. A multi-master bus or wait state insertion are not possible. Through the I<sup>2</sup>C control, it is easily to program registers and check device status without delay. The device address of SA51510 is 0xD8.

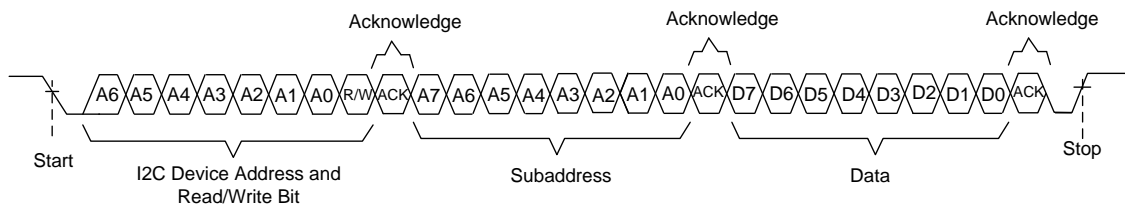


**Figure 10. Typical I<sup>2</sup>C Sequence**

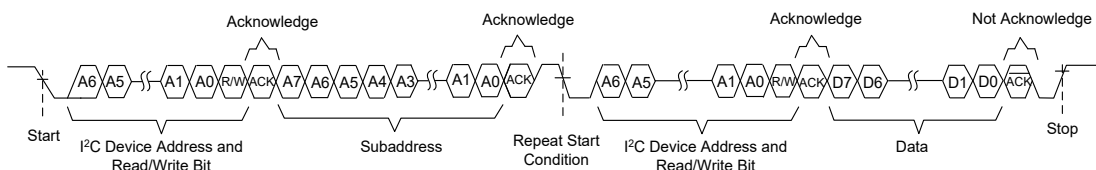
## Single and Multiple Byte Transfers

From sub addresses 0x01 to 0x04, the I<sup>2</sup>C serial port control interface offers single-byte and multi-byte read/write operations.

The DAP responds to data one byte at a time during multi-byte read operations, starting from the assigned sub-address, only when the master device continues to respond to confirm. If a particular sub address does not contain  $8 \cdot N$  bits, the unused bits will be read as logical 0.



**Figure 11. Single Byte Write Transfer**



**Figure 12. Single Byte Read Transfer**

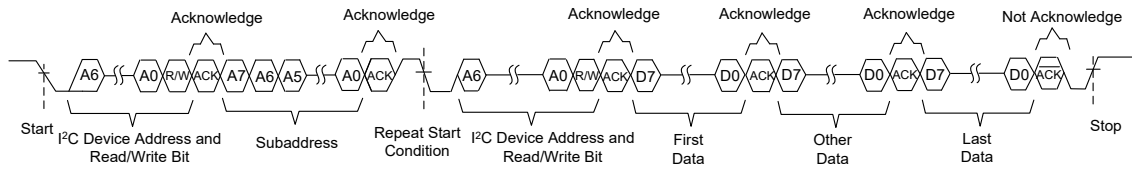


Figure 13. Multiple-Byte Read Transfer

### BSN and BSP

Only NMOSFETs be used as both high side and low side in half-bridge output stages. So bootstrap capacitors are required for the high side of each output to switch correctly. Typically, a 470nF ceramic capacitor, rated voltage at least 16V, should be connected from OUTx to its corresponding bootstrap pin BSx.

The bootstrap capacitors are connected between the BSx pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

### GREG Supply

The GREG supply powers the gates of the output full bridge transistors. Add a 1μF capacitor to ground at this pin.

### Spread Spectrum

SA51510 supports spread spectrum mode to improve EMC performance. Spread spectrum is a technique of modulating the oscillator frequency with a slowly varying signal to broaden the switching spectrum, thereby reducing the spectral density of the EMI. The Spread spectrum can be enabled by bit4-bit3 of Control Register 2(0x04), the frequency range  $\Delta f$  is  $\pm 25\text{kHz}$  (375kHz to 425kHz for PWM frequency 400kHz) and frequency of modulation profile(fm) can be set to 25.4kHz (0x04[4:3]=2b'01), 12.7kHz (0x04[4:3]=2b'10), 6.4kHz (0x04[4:3]=2b'11).

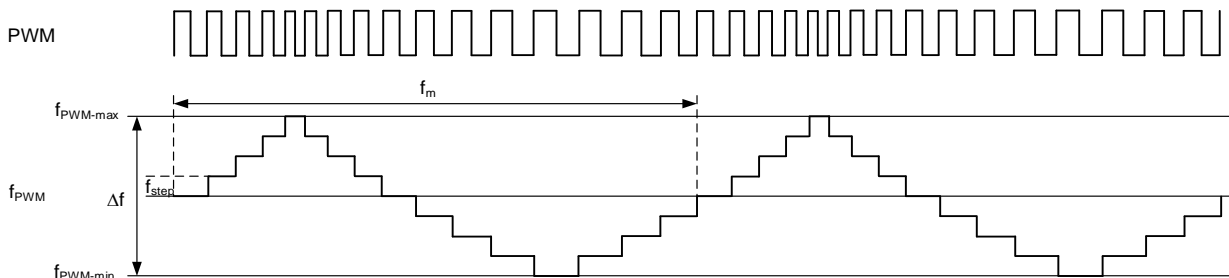
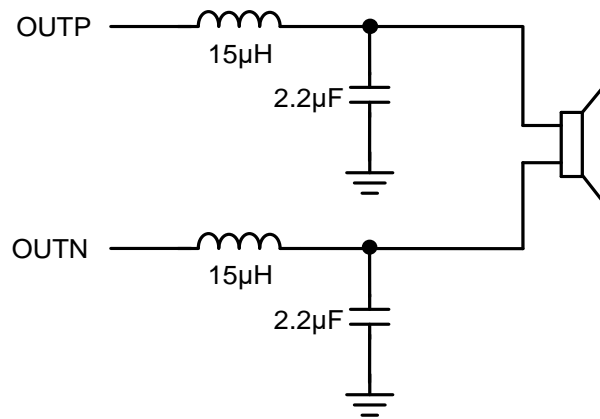


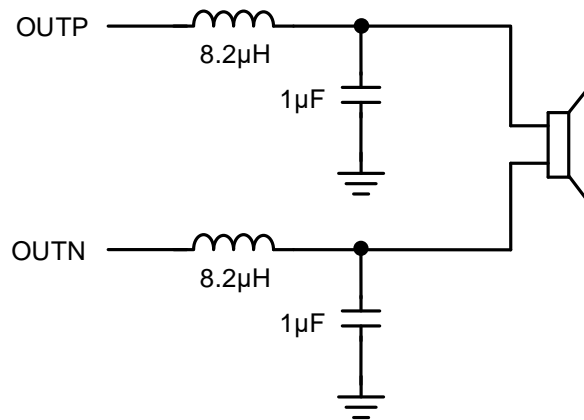
Figure14. Spread spectrum operation

### Output LC Filter

If the traces from the SA51510 to speaker are not short or to satisfy the EMI requirement, it is recommended to add the output LC filter to eliminate the high frequency emissions. The cutoff frequency of LC filter must less than the Class-D switching frequency to filtering out switching frequency and its harmonics. The filter can be chosen according to needed cutoff frequency and quality factor Q. Figure 15 are two typical filter structures.



(a) Cutoff Frequency is 27kHz,  $Q=0.766$ , Speaker Impedance =  $4\Omega$



(b) Cutoff Frequency is 55kHz,  $Q=0.698$ , Speaker Impedance =  $4\Omega$

Figure 15. Typical LC Output Filter

## Protection Circuits

The device is fully protected against short circuit, over temperature, DC-detect, over voltage and under voltage.

### Over-current Protection (OCP)

To protect speaker drivers from over-current damage, SA51510 has built-in short-circuit protection circuit. When the wires connected to speakers are shorted to each other or shorted to GND or to PVDD, over current detectors will activate. Once over current detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The over current fault is reported on FAULTZ pin as a low state and I<sup>2</sup>C register. The latch will be cleared after 775ms and the device will auto-recovery.

### Under Voltage Lockout (UVLO) and Over Voltage Lockout (OVLO)

When the PVDD voltage is lower than the under voltage or rises above over voltage lockout threshold voltage, the device will enter into shutdown mode and internal logic is reset. The UVLO and OVLO can be reported on the FAULTZ pin and Fault Register. Operation resumes when PVDD rises above the UVLO threshold with hysteresis or falls below OVLO threshold with hysteresis.

### Over Temperature Protection (OTP)

If the internal junction temperature of SA51510 is higher than 150°C, the device will enter into shutdown mode and internal logic is reset. This is not a latched fault. The over temperature fault is cleared and the amplifier return to normal operation once the temperature of junction is reduced by 15°C.

**DC Detection**

SA51510 has DC detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit measures the difference of the PWM duty cycle, if it exceeds 20% (for example, 60%, -40%) for more than 605ms at the same polarity, the amplifier will enter into Hi-Z state and the protection latch is engaged. A DC-detect fault is reported on the FAULTZ pin as a low state and I<sup>2</sup>C register. The device will auto-recovery after DC protect 775ms.

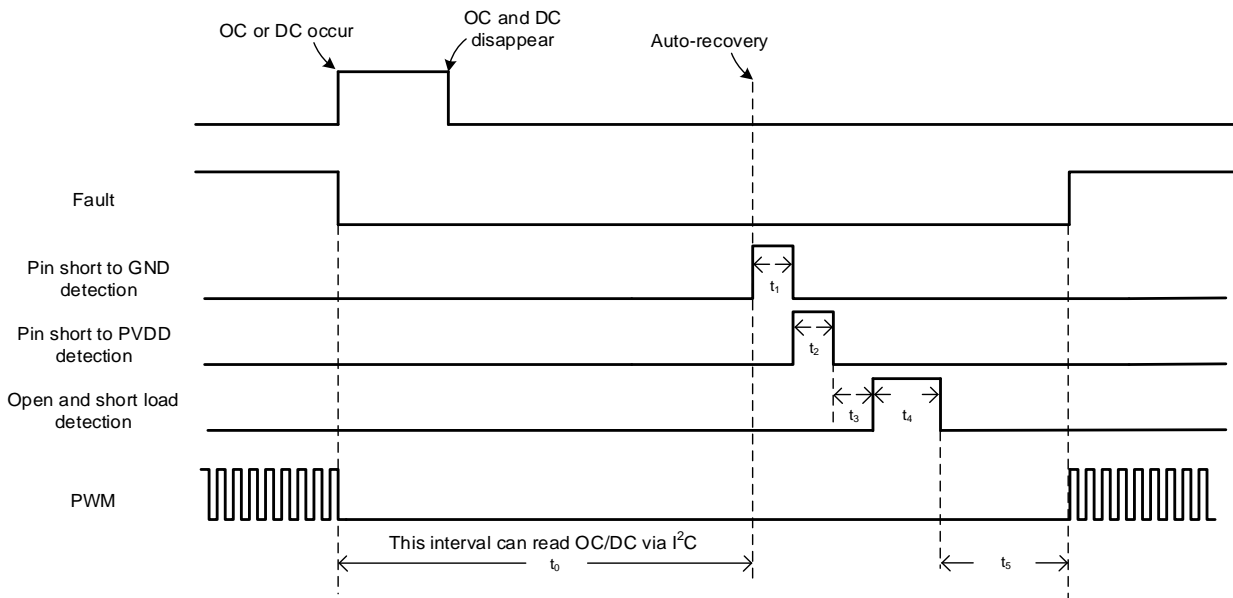
**Fault and Actions**

The following tables list fault and actions.

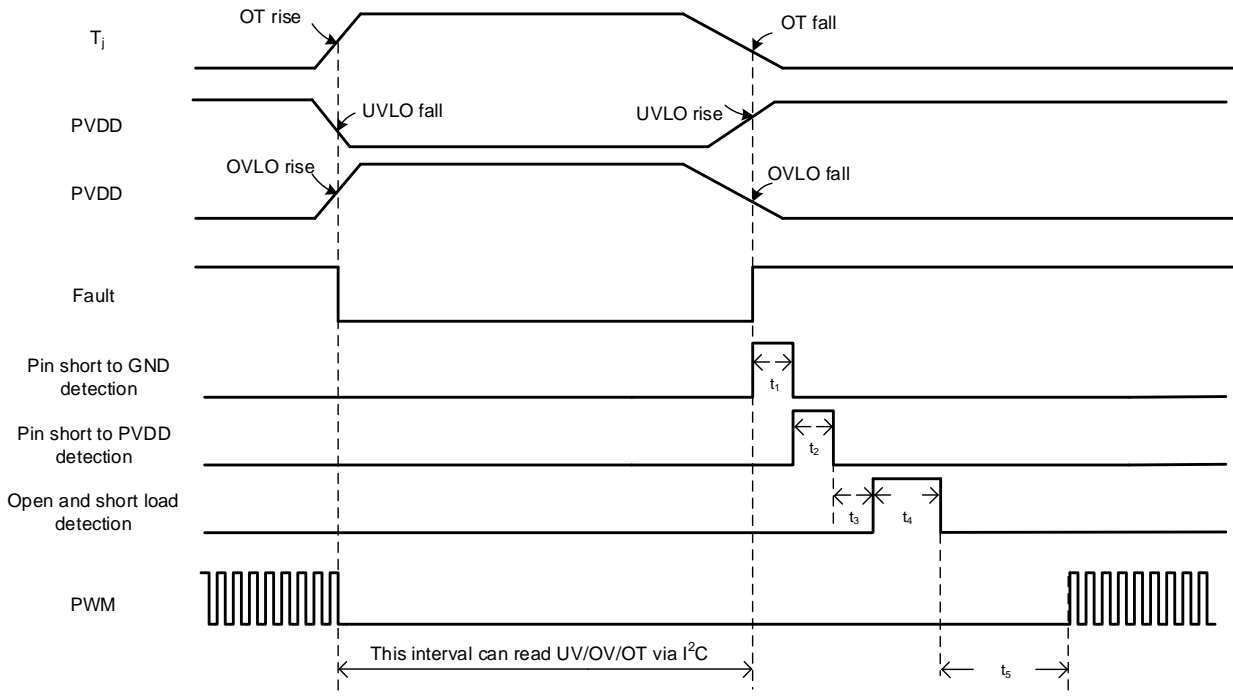
Fault Event	Fault Event Category	Monitoring Modes	Reporting Method	Action Result	Clearing
UV	Voltage fault	Except shutdown	I <sup>2</sup> C + FAULTZ pin	Hi-Z	Auto recovery when fault condition disappears
OV					
OTP	Thermal				
OC fault	Output channel fault	play			Auto recovery after 775ms and repeat load diagnostic until pass, then PWM out after 150ms
DC detect					
PSG PSP SLD	Diagnostic	Perform on start up or auto-recovery	I <sup>2</sup> C	Output normally	Repeat load diagnostic until pass
OLD					Cycle power or pull down SDZ

**Auto-recovery**

The timing of auto-recovery from over current, direct current, over temperature, under voltage and over voltage are shown in Figure 16.



(a) Auto-recovery from OCP/DCP



**(b) Auto-recovery from OTP/UVLO/OVLO**

$t_0$ : auto-recovery time from OCP and DCP, typical 775ms;

$t_1$ : PSG detect time, typical 3ms;

$t_2$ : PSP detect time, typical 3ms;

$t_3$ : interval time, typical 3ms;

$t_4$ : OLD/SLD detect time, typical 141ms;

$t_5$ : waiting time, typical 150ms.

**Figure 16. Auto-recovery Feature**

## Register Map

I <sup>2</sup> C Address									
Description	Fixed Address							Read/Write Bit	I <sup>2</sup> C Address
	MSB	6	5	4	3	2	1	LSB	
I <sup>2</sup> C Write	1	1	0	1	1	0	0	0	0xD8
I <sup>2</sup> C Read	1	1	0	1	1	0	0	1	0xD9

I <sup>2</sup> C Address Register Summary		
Description	R/W	Register Description
0x01	R	Latched Fault Register
0x02	R	Status and Load Diagnostic Register
0x03	R/W	Control Register
0x04	R/W	Control Register 2

Fault Register (0x01)								
D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	0	0	0	0	0	0	0	No faults, default value
-	-	-	-	-	-	-	1	Reserved
-	-	-	-	-	-	1	-	Reserved
-	-	-	-	-	1	-	-	A load-diagnostics faults has occurred
-	-	-	-	1	-	-	-	Over current shutdown has occurred
-	-	-	1	-	-	-	-	PVDD under-voltage has occurred
-	-	1	-	-	-	-	-	PVDD over-voltage has occurred
-	1	-	-	-	-	-	-	DC offset protection has occurred
1	-	-	-	-	-	-	-	Over-temperature shutdown has occurred

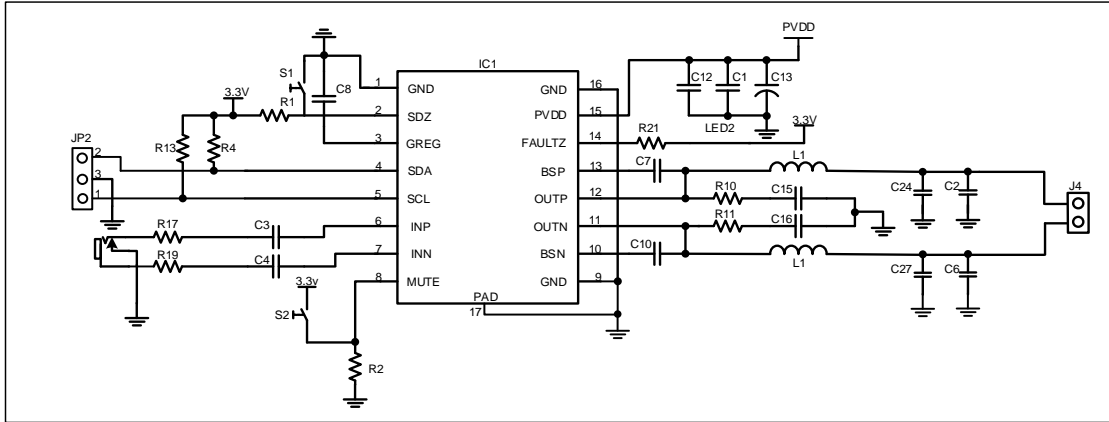
Status and Load Diagnostic Register (0x02)								
D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	0	0	0	0	0	0	0	No diagnostic faults, default value
-	-	-	-	-	-	-	1	Output short to PVDD when 0x04 D5 is 0 OUTP short to PVDD when 0x04 D5 is 1
-	-	-	-	-	-	1	-	Output short to Ground when 0x04 D5 is 0 OUTP short to Ground when 0x04 D5 is 1
-	-	-	-	-	1	-	-	Open load
-	-	-	-	1	-	-	-	Shorted load
-	-	-	1	-	-	-	-	In a fault condition (OC/OT/DC/UV/OV)
-	-	1	-	-	-	-	-	Performing load
-	1	-	-	-	-	-	-	In mute mode
1	-	-	-	-	-	-	-	In play mode

Control Register (0x03)								Function Description
D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	1	1	0	0	0	Default value. 26dB gain, switching frequency is 400kHz. Power limit function disable
-	-	-	-	-	-	-	1	Switching frequency set to 500kHz
-	-	-	-	-	1	1	-	reserved
-	-	1	1	0	-	-	-	Power limit to 14V peak output
-	-	1	0	1	-	-	-	Power limit to 11.8V peak output
-	-	1	0	0	-	-	-	Power limit to 9.8V peak output
-	-	0	1	1	-	-	-	Power limit to 8.4V peak output
-	-	0	1	0	-	-	-	Power limit to 7V peak output
-	-	0	0	1	-	-	-	Power limit to 5.9V peak output
-	-	0	0	0	-	-	-	Power limit to 5V peak output
0	0	-	-	-	-	-	-	20dB gain
1	0	-	-	-	-	-	-	32dB gain
1	1	-	-	-	-	-	-	36dB gain

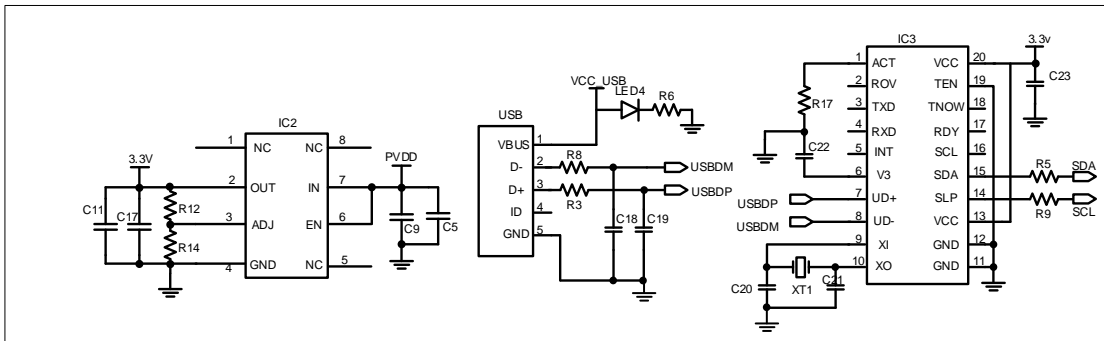
Control Register 2 (0x04)								Function Description
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	1	0	Default. Not check PSG_N/PSP_N, no spread spectrum, fast edge
1	-	-	-	-	-	-	-	OUTN short to Ground when 0x04 D5 is 1
-	1	-	-	-	-	-	-	OUTN short to PVDD when 0x04 D5 is 1
-	-	1	-	-	-	-	-	Enable of PSG/PSP of OUTP and OUTN separation
-	-	-	-	-	-	-	1	reserved
-	-	-	-	-	0	0	-	Medium fast edge
-	-	-	-	-	1	0	-	Slow edge
-	-	-	-	-	1	1	-	Medium slow edge
-	-	-	0	1	-	-	-	25.5kHz fm with $\pm 25$ kHz range
-	-	-	1	0	-	-	-	12.7kHz fm with $\pm 25$ kHz range
-	-	-	1	1	-	-	-	6.4kHz fm with $\pm 25$ kHz range

# Application

## Typical Application Schematic



(a). SA51510 Peripheral Circuit



(b). USB To I2C Circuit (Not Necessary)

Figure 17. SA51510 EVM Schematic

## BOM List

Designator	Description	Part Number	Manufacturer
IC1	Analog class-D audio amplifier for automotive, TSSOP16E	SA51510HFP	Silergy
IC2	36V 300mA LDO Regulator, SO8E	SA21345AFCA	Silergy
IC3	USB Bus Convert chip, SSOP20	CH341T	
J1,J4	Connector, B2PS-VH(LF)(SN)		
J2	Header, XH2.54-3P		
J5	JACK-PJ307G		
LIN	JACK-RCA		
USB	MUSB-05-F-AB-SM-A		
LED4	LED, Green, SMD(0805)		
XT1	Oscillator, 12MHz		
C1,C5	Ceramic Capacitor, 10uF/50V(1206)		
C11	Ceramic Capacitor, 10uF/10V(0603)		
C3,C4	Ceramic Capacitor, 1uF/16V(0603)		
C7,C10	Ceramic Capacitor, 470nF/16V(0603)		
C8	Ceramic Capacitor, 2.2uF/10V(0805)		
C9,C12	Ceramic Capacitor, 100nF/50V(0603)		
C17,C22,C23	Ceramic Capacitor, 100nF/10V(0603)		
C15,C16	Ceramic Capacitor, 470pF/50V(0603)		
C18,C19,C20,C21	Ceramic Capacitor, 33pF/10V(0603)		
C24,C26	Configuration1:2.2uF/50V(0805)		
	Configuration2:1uF/50V(0805)		
C2,C6	NC		
C13	Electrolytic capacitor, 220uF/50V		
R1,R21	Resistor,100k(0603)		
R5,R7,R17,R19	Resistor,0Ω(0603)		
R3,R8	Resistor,10Ω(0603)		
R2,R4,R6,R7,R13	Resistor,4.7k(0603)		
R10,R11	Resistor,5.6Ω(0805)		
R16	Resistor,360K(0805)		
R23,R24	NC		
L1	Configuration1:15uH		
	Configuration2:8.2uH		
S1,S2	Light Touch Switches, SMD, 3.5mmx2.9mm	EVPAA202K	

## Power Supply Recommendations

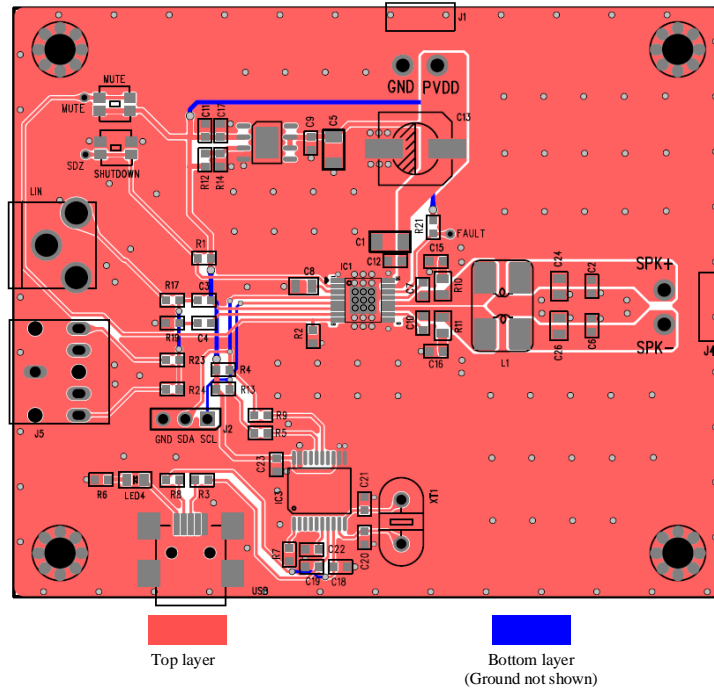
Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVDD and GND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1nF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1μF or 1μF as close as possible to the device PVDD leads works best. For low frequency noise filtering, a 220μF or greater capacitor (tantalum or electrolytic type) is suggested.

## PCB Layout Guidelines

In order to obtain excellent thermal dissipation and EMC performance of SA51510, PCB layout must be carefully considered.

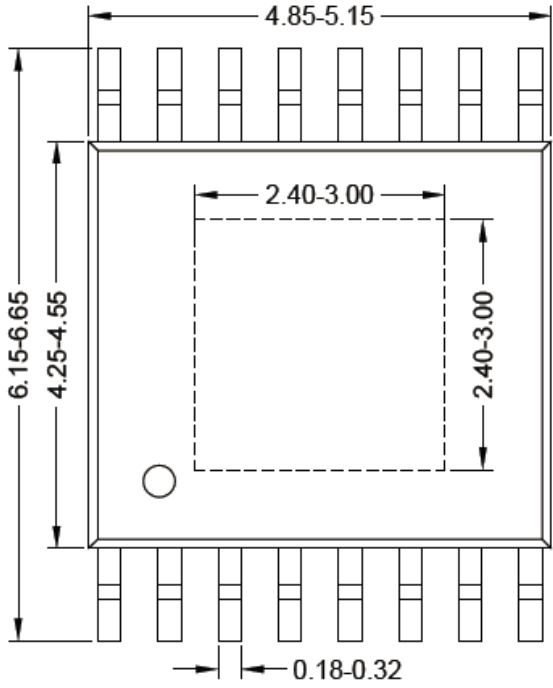
- Provide a separate short and thick power line to SA51510 to decrease voltage drop.
- The high-frequency decoupling capacitors of PVDD and GREG should be placed as close to the PVDD pin and GREG pin as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. These capacitors should select low ESR ceramic capacitor.
- The input capacitors should be close to SA51510 INN and INP input pins, the input line should be parallel to suppress noise coupling.

- The LC filter should be placed as close to the output terminals as possible for the best EMI performance. Keep the current loop from each of the outputs through the inductor and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be larger for application. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

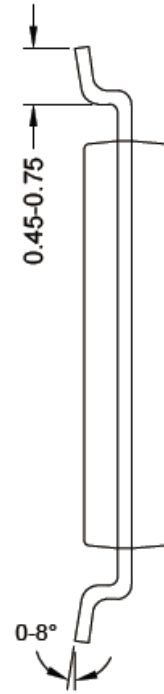


**Figure 18. PCB Layout Guidance**

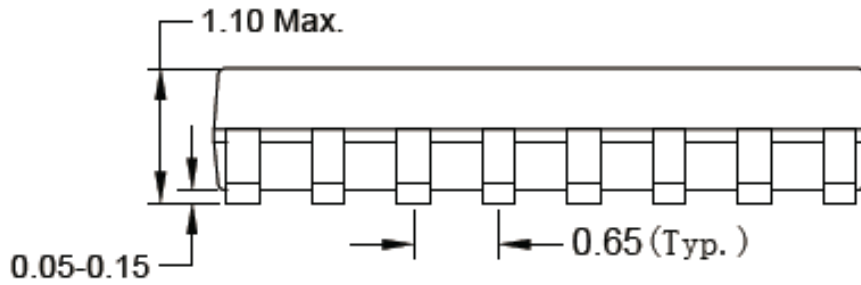
TSSOP16E Package Outline Drawing



Top View



Side View A

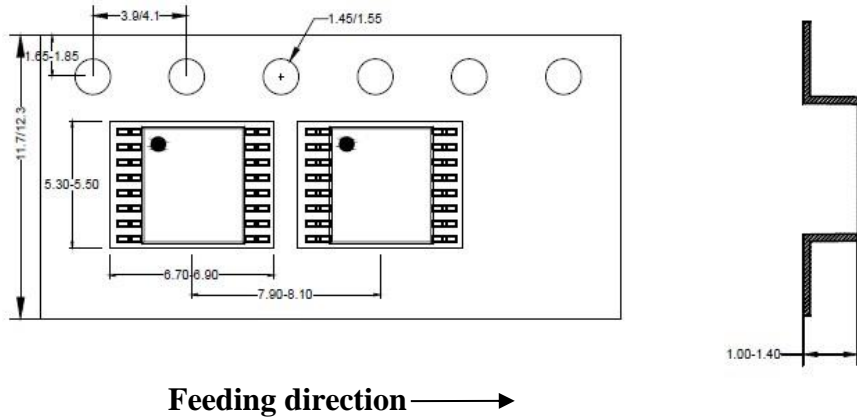


Side View B

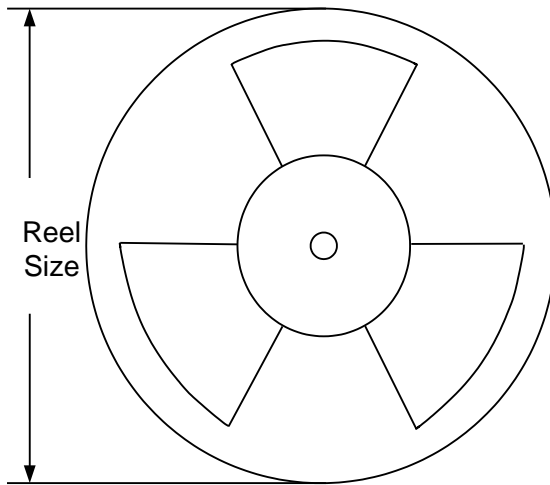


### Taping & Reel Specification

#### TSSOP16E Taping Orientation



#### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
TSSOP16E	12	8	13"	400	400	3000

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
Rev 1.0	07/08/2024	Production Release	
Rev 0.9A	07/08/2023	In Bom list, designator C7,C10 is changed from 220nF/50V to 470nF/16V	26
Rev 0.9	05/26/2023	Initial Release	

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