SY28480

18V, 50A E-Fuse Switch

General Description

The SY28480 is a 0.76mΩ ultra-low on-resistance E-fuse for using in high current applications such as base stations and servers.

The SY28480 integrates overcurrent protection to against over load and output hard short event. The SY28480 also offer an analog output for high accurate load current monitor and provide programmable soft start time to fit different output cap and reduce the inrush current.

The SY28480 is available in a compact QFN5×5-32 package.

Applications

- Servers
- Base Station
- Hot Swap Applications

Features

- Wide Input Range: 4.5 V to 18 V
- Up to 60 A Peak Current Output, 50 A Continuous
- Integrated N-Channel MOSFET with 0.76 mΩ Ultra Low R_{ON}
- Adjustable Slew Rate Control
- Adjustable Current Limit
- Accurate Analog Load Current Monitor
- Adjustable Over Current Alert Output
- Temperature Indicator
- Fault Detection with Status OK Output
- Can be used in Parallel for Higher Current Applications
- Auto-Retry Mode for Following Protection Features
  - Soft Start Duration Timeout
  - Thermal Shutdown
  - Fast Short-Circuit Protection
  - Current Limiting Response Timeout
- Compact Package Minimizes the Board Space: QFN 5 mm × 5 mm-32

Typical application

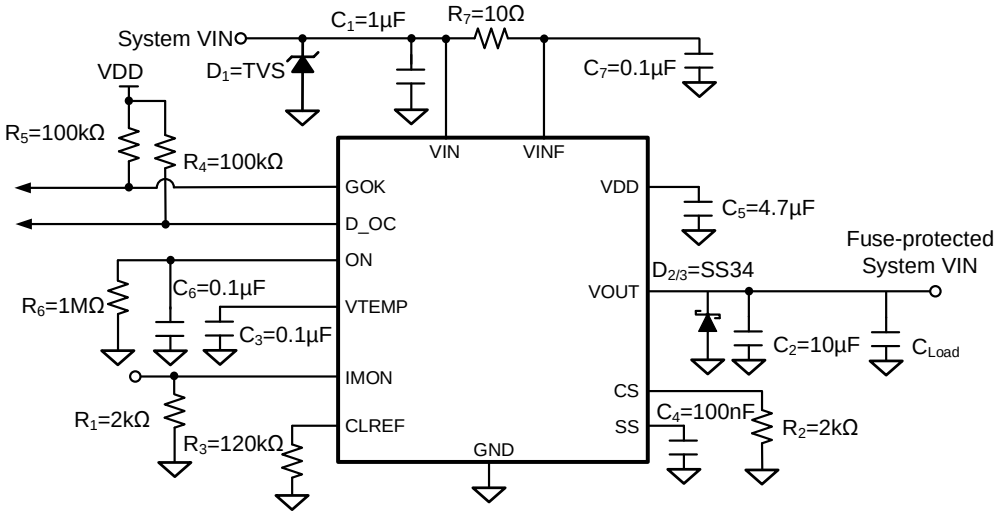


Figure1. Schematic Diagram

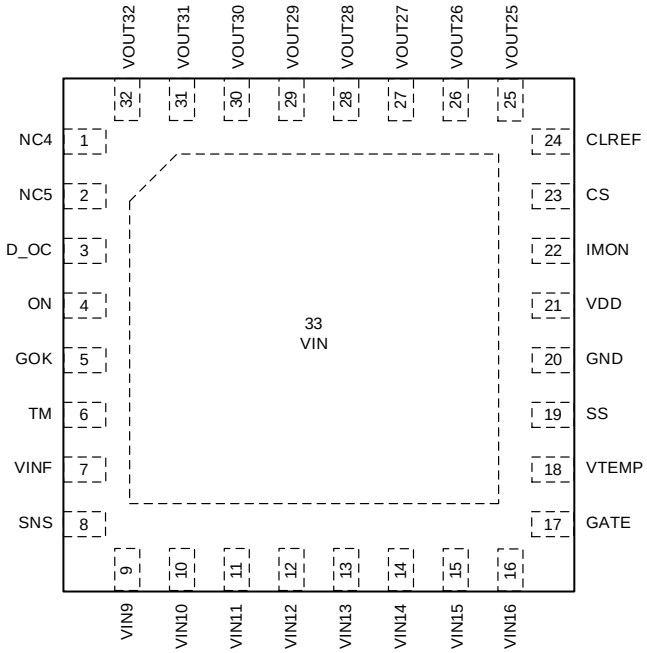
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY28480QEQ	QFN5×5-32 RoHS Compliant and Halogen Free	**DQD*xyz***

Device code: DQD

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin number	Pin Description
NC4	1	No electrical connection internally. May connect to any potential.
NC5	2	No electrical connection internally. May connect to any potential.
D_OC	3	Over current indicator output (open drain). Low indicates the device is limiting current. The D_OC output does not report current limiting during soft-start.
ON	4	Enable output pull down resistance control.
GOK	5	OK status indicator output (open drain). Low indicates that the device was turned off by a fault.
TM	6	Test pin. Do not connect to this pin. Leave floating.
VINF	7	Control circuit power supply input. Connect to VIN pins through an RC filter.
SNS	8	Internal FET sense pin. Do not connect to this pin. Leave floating.
VIN09	9	Input of high current output switch.
VIN10	10	Input of high current output switch.
VIN11	11	Input of high current output switch.
VIN12	12	Input of high current output switch.
VIN13	13	Input of high current output switch.
VIN14	14	Input of high current output switch.
VIN15	15	Input of high current output switch.
VIN16	16	Input of high current output switch.
GATE	17	Internal FET gate pin. Do not connect to this pin. Leave floating.
VTEMP	18	Analog temperature monitor output.
SS	19	Soft Start time programming pin. Connect a capacitor to this pin to set the soft start time.
GND	20	Ground.

Pin Name	Pin number	Pin Description
VDD	21	Linear regulator output.
IMON	22	Analog current monitor output.
CS	23	Current sense feedback output (current). Scaling the voltage developed at this pin with a resistor to ground makes this also an input for several current limiting functions and over current indicator D_OC.
CLREF	24	Current limit set point input for normal operation (after soft-start).
VOUT25	25	Output of high current output switch.
VOUT26	26	Output of high current output switch.
VOUT27	27	Output of high current output switch.
VOUT28	28	Output of high current output switch.
VOUT29	29	Output of high current output switch.
VOUT30	30	Output of high current output switch.
VOUT31	31	Output of high current output switch.
VOUT32	32	Output of high current output switch.
VIN33	33	Input of high current output switch.

Block Diagram

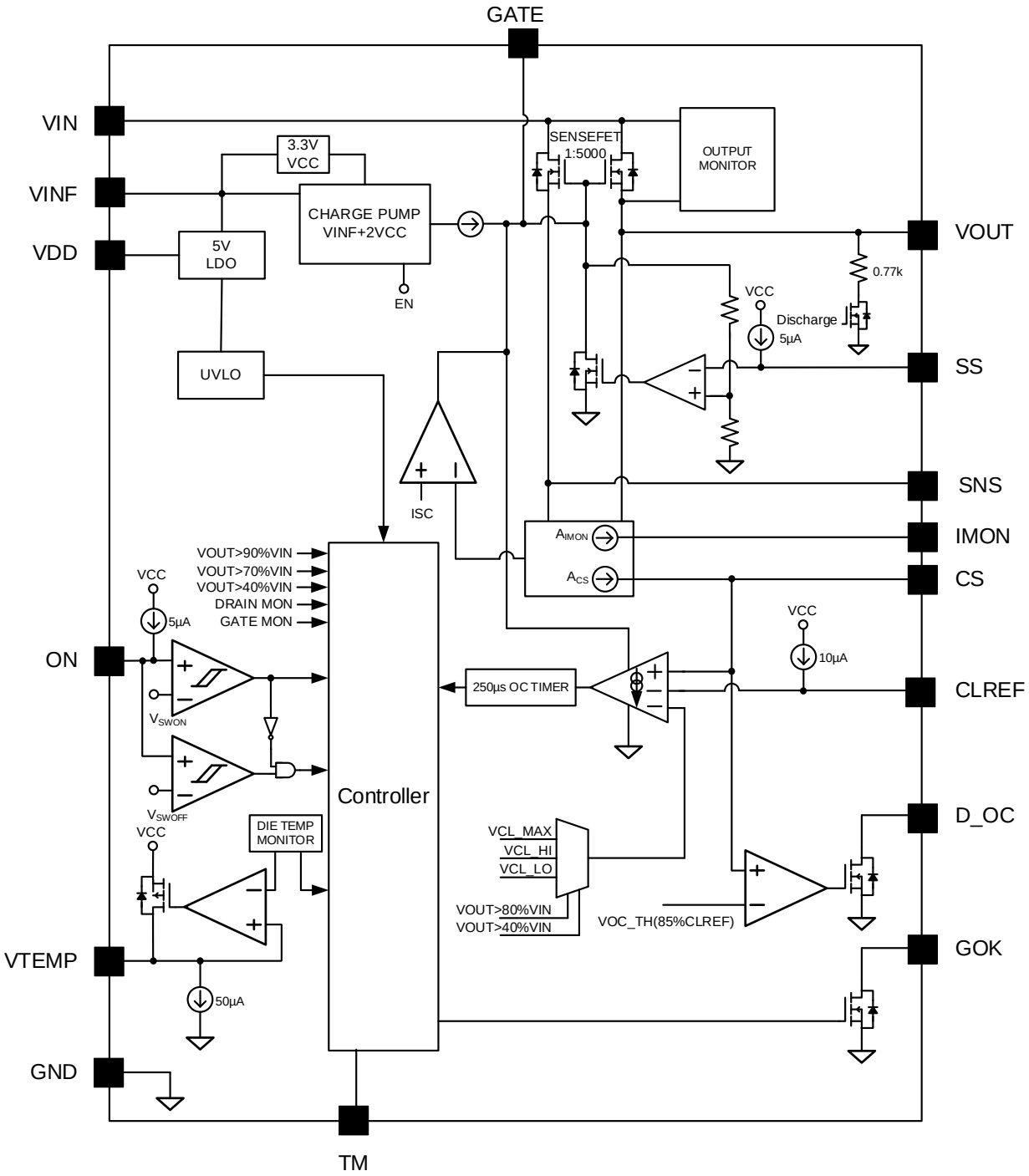


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VINx, VINF	-0.3	20	V
VOUTx	-0.3V/-1V(<500ms)	20	
VDD	-0.3	6	
GOK, D_OC, ON, VTEMP, CLREF, IMON, CS, SS	-0.3	VDD+0.3	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	28	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	21.3	
P_D Power Dissipation T_A = 25°C	3.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN, VINF	4.5	18	V
VDD, GOK, D_OC, ON, VTEMP, CLREF, IMON, CS, SS	0	5.5	
Maximum Continuous Output Current: I_{AVE}		50	A
Peak Output Current: I_{PEAK}		60	
VDD Output Load Capacitance Range: C_{VDD}	2.2	10	µF
VTEMP Output Load Capacitance Range: C_{VTEMP}	0.1		
Soft-start Duration: t_{SS}	10	100	ms
CS Load Resistance Range: R_{CS}	1.8	4	kΩ
CLREF Voltage Range: V_{CLREF}	0.2	1.4	V
Junction Temperature, Operating	-40	125	°C

Electrical Characteristics

(VINx=VINF=12V, V_{ON}=3.3V, C_{VINF}=0.1μF, C_{VDD}=4.7μF, C_{VTEMP}=0.1μF, R_{VTEMP} = 1kΩ, C_{SS}=100nF, T_J=-40°C to 125°C, typical values are T_J=25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VINF INPUT						
Quiescent Current	I_Q	V_{ON}>1.4V, null load		1.44	3.0	mA
		V_{ON}>1.4V, fault			3.0	mA
		V_{ON}<0.8V		1.44	3.0	mA
		V_{ON}<0.8V, VINF=16V			3.0	mA
VDD REGULATOR						
VDD Output Voltage	V_{DD_NL}	I_{VDD} = 0 mA, VINF = 6 V	4.6	4.95	5.2	V
VDD Load Capability	I_{DDLOAD}	VINF = 5.5 V			30	mA
VDD Current Limit	I_{DD_CL}	VINF = 12 V and VINF = 6 V	40	70		mA
VDD Dropout Voltage		I_{VDD} = 25 mA, VINF = 4.5 V		85	200	mV
UVLO Rising Threshold	V_{DD_UVR}		4.1	4.3	4.5	V
UVLO Falling Threshold	V_{DD_UVF}		3.8	4.0	4.2	V
ON INPUT						
Bias Current	I_{ON}	From pin into a 0 V or 1.5 V source	4.0	5.0	6.0	μA
Switch ON Threshold	V_{SWON}		1.3	1.4	1.5	V
Switch OFF Threshold	V_{SWOFF}			1.2		V
Switch ON Delay Timer	t_{ON}	From ON transitioning above V_{SWON} to SS start	0.6	1.0	2.5	ms
Switch OFF Delay Time (Note 4)	t_{OFF}	From ON transitioning below V_{SWOFF} to GATE pulldown		1		μs
ON Current Source Clamp Voltage	V_{ON_CLMP}	Max pull-up voltage of current source		3.0		V
Output Pull-down Resistance	R_{PD}	V_{OUT} = 12 V, PD mode = 1		0.77		kΩ
SS PIN						
Bias Current	I_{SS}	From pin into a 0 V or 1 V source	4.62	5.15	5.62	μA
Gain to VOUT	AVSS		9.6	10	10.4	V/V
SS Pull-down Voltage	V_{OL_SS}	0.1 mA into pin during ON delay		3		mV
GOK OUTPUT						
Output Low Voltage	V_{OL_GOK}	I_{GOK} = 1 mA			0.1	V
Off-state Leakage Current	I_{LK_GOK}	V_{GOK}= 5 V			1.0	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
IMON/CS OUTPUT							
IMON or CS Current (single eFuse) Based on 10μA/A+1.5μA	I_{IMON}/I_{CS}	T_J = 0 to 85°C	I_{OUT} = 5 A (Note 4)		51.5		μA
			I_{OUT} = 10 A (Note 4)		101.5		μA
			I_{OUT} = 25 A (Note 4)		251.5		μA
			I_{OUT} = 50 A (Note 4)		501.5		μA
Accuracy (single eFuse)		T_J = 0 to 85°C	I_{OUT} = 5 A (Note 4)	-6		+6	%
			I_{OUT} = 10 A (Note 4)	-4		+4	%
			I_{OUT} = 25 A (Note 4)	-4		+4	%
			I_{OUT} = 50 A (Note 4)	-4		+4	%
Pre-Biased Offset Current Load for Auto-Zero Op-Amp	I_{AZ_BIAS}				1.5		μA
CURRENT LIMIT & CLREF PIN							
Current Limit Voltage	V_{CL_TH}	If V_{CS}>V_{CL_TH} current limiting regulation occurs via gate		95	98	101	%V_{CLREF}
Current Limit Trigger Threshold During Start-up	I_{CL_LOTH}	V_{OUT}<40%V_{IN}, V_{CLREF}>0.15 V, R_{CS}=2kΩ (Note 5)		2			A
Current Limit Clamp Voltage	V_{CL_LO}	V_{OUT}<40%V_{IN}, V_{CLREF}>0.15 V		135	152	165	mV
	V_{CL_HI}	40%V_{IN}<V_{OUT}<80%V_{IN}, V_{CLREF}>0.5 V		480	504	520	mV
Max Current Limit Reference Voltage	V_{CL_MX}	V_{OUT}>80%V_{IN}, V_{CLREF}>1.6 V		1.55	1.6	1.65	V
Response Time (Note 4)	t_{CL_REG}	V_{CS}>V_{CLREF} until current limiting			100		μs
CLREF Bias Current	I_{CL}	From pin into a 1.2 V source		9.6	10	10.4	μA
CLREF Current Source Clamp Voltage	V_{CL_CLMP}	Max pull-up voltage of current source			3.0		V
FET Turn-off Timer	t_{CL_LA}	Delay between current limit detection and FET turn-off (GOK = 0)			250		μs
D_OC OUTPUT							
Overcurrent Threshold	V_{OC_TH}	If V_{CS}>VOC_TH D_OC pin pulls low		83	86	90	%V_{CLREF}
Output Low Voltage	V_{OL_DOC}	I_{DOC} = 1 mA				0.1	V
Off-state Leakage Current	I_{LK_DOC}	V_{DOC}= 5 V				1.0	μA
Delay (rising) (Note 4)		V_{CS} < limit until D_OC rising			1.0		μs
Delay (falling) (Note 4)		V_{CS} > limit until D_OC falling			1.0		μs
SHORT CIRCUIT PROTECTION							
Current Threshold (Note 4)	I_{SC}				80		A
Response Time (Note 4)	t_{SC}	From I_{OUT}>I_{LIMSC} until gate pulldown			500		ns
VTEMP OUTPUT							
Bias Voltage	$V_{VTEMP25}$	At 25°C			550		mV
Gain (Note 4)	A_VTEMP	0°C ≤T_J ≤125°C			10		mV/°C
Load Capability	R_VTEMP	At 25°C			1		kΩ
Pulldown Current	I_VTEMP	At 25°C			50		μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown						
Temperature Shutdown (Note 4)	T_{TSD}	GOK pulls down		140		°C
Temperature Shutdown Hysteresis (Note 4)	T_{HYS}			20		°C
OUTPUT SWITCH(FET)						
On Resistance	$R_{DS(ON)}$	T_J = 25°C		0.76	1.0	mΩ
Off-state leakage current	I_{DSOFF}	VIN = 16 V, V_{ON}<1.2 V, T_J = 25°C			1.0	μA
FAULT DETECTION						
V_{DS} Short Threshold	V_{DS_TH}	Startup postponed if V_{OUT} > V_{DS_TH} at V_{ON} >V_{SWON} transition		90		%VIN
V_{DS} Short OK Threshold	V_{DS_OK}	Startup resumed if V_{OUT} < V_{DS_OK} any time after postponed		70		%VIN
V_{GD} Short Threshold	V_{DG_TH}	Startup postponed if V_G >V_{DG_TH} at V_{ON} > V_{SWON} transition		3.1		V
V_{GD} Short OK Threshold	V_{DG_OK}	Startup resumed if V_G < V_{DG_OK} any time after postponed		3.0		V
V_G Low Threshold (Note 4)	V_{G_TH}	Restart if V_{GD} < V_{G_TH} after t_{SSF_END} or t_{GATE_FLT}		3.4		V
V_{OUT} Low Threshold (Note 4)	V_{OUTL_TH}	Restart if V_{OUT} <V_{OUTL_TH} after t_{SSF_END}		90		%VIN
Gate Fault Timer (Note 4)	t_{GATE_FLT}	Time from V_{GD} <V_{G_TH} transition after t_{SSF_END} completed		200		ms
Startup Timer Failsafe (Note 4)	t_{SSF_END}	Time from V_{ON} >V_{SWON} transition, Max programmable soft-start time		200		ms
AUTO-RETRY						
Auto-Retry Delay	t_{DLY_RETRY}	Delay from power-down to retry of startup		1000		ms

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is simulated in the natural convection at T_A = 25°C on Silergy EVB test board.

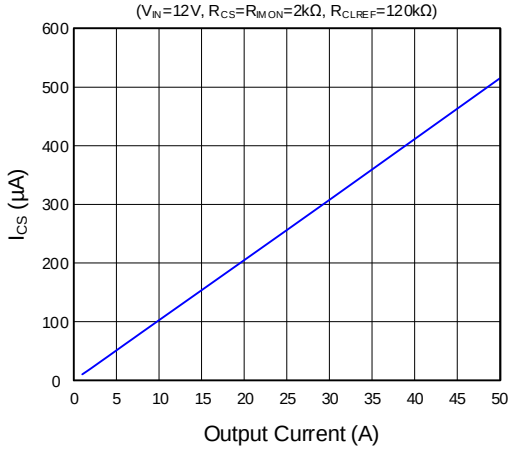
Note 3: The device is not guaranteed to function outside its operating conditions.

Note4: Guaranteed by design but not production tested.

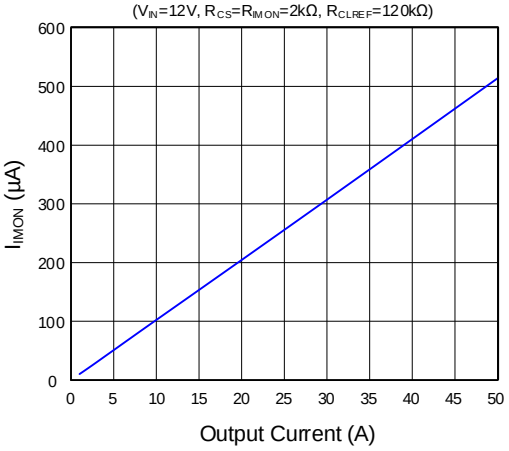
Note5: I_{CL_LOTH} indicates the threshold that triggers the timing of current limit when V_{OUT}<40%V_{IN} and V_{CLREF}>0.15V, but not the actual current limit clamp threshold. If I_{OUT}>I_{CL_LOTH} for a continuous duration > t_{CL_LA}, then the device restarts.

Typical Performance Characteristics

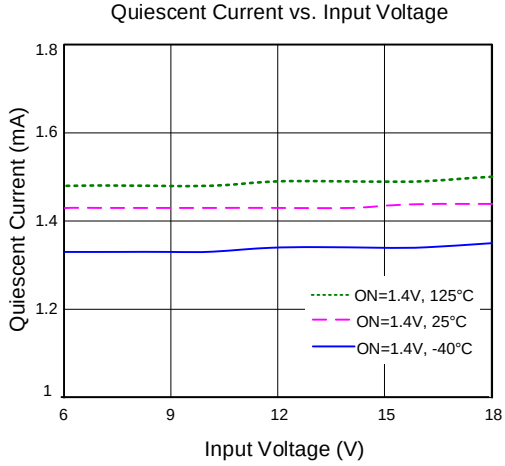
I_{CS} vs. Output Current
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



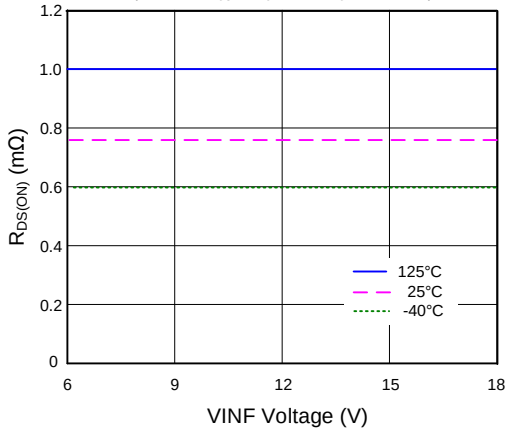
I_{IMON} vs. Output Current
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



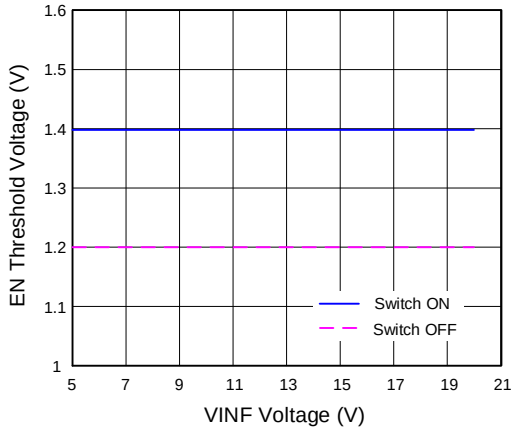
Quiescent Current vs. Input Voltage



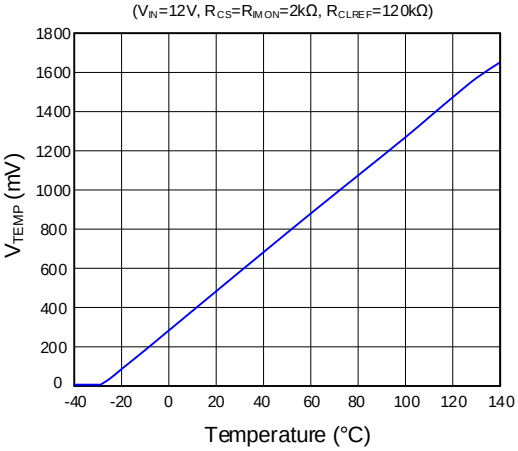
$R_{DS(ON)}$ vs. VINF Voltage
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



EN Threshold vs. VINF Voltage
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)

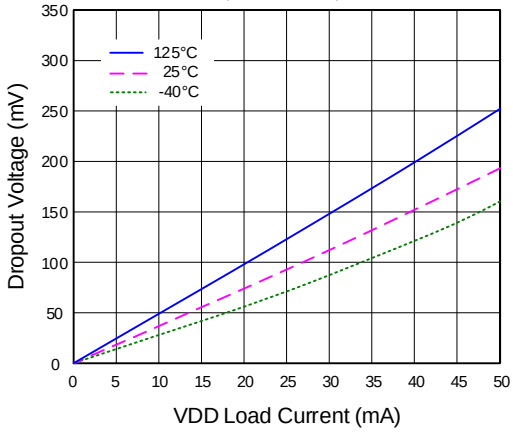


V_{TEMP} vs. Temperature
(V_{IN}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ)



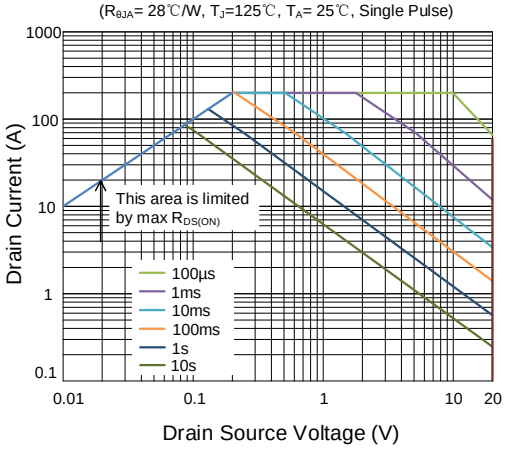
Dropout Voltage vs. VDD Load

(V_{IN}=V_{VINF}=4.5V)



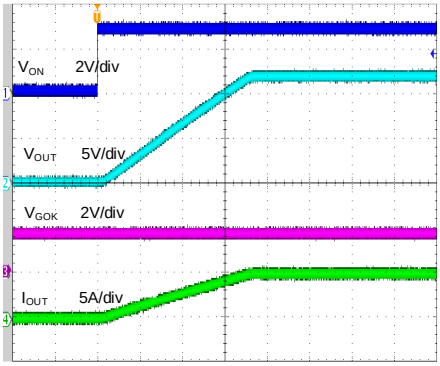
Internal FET’s Safe Operating Area

($R_{\theta JA}$= 28℃/W, T_J=125℃, T_A= 25℃, Single Pulse)



Startup from ON

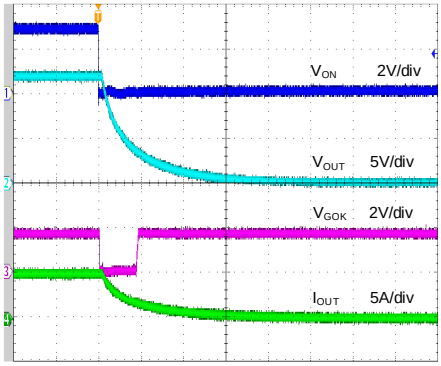
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (20ms/div)

Shutdown from ON

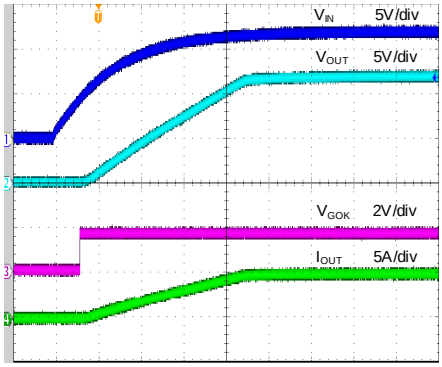
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (20µs/div)

Startup from V_{IN}

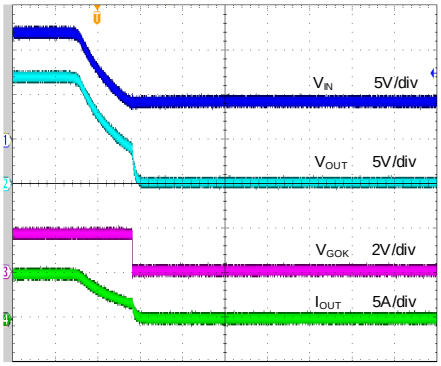
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (20ms/div)

Shutdown from V_{IN}

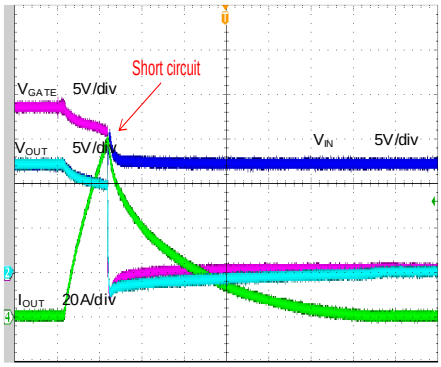
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, 2.4Ω Load)



Time (400µs/div)

Short Circuit Response

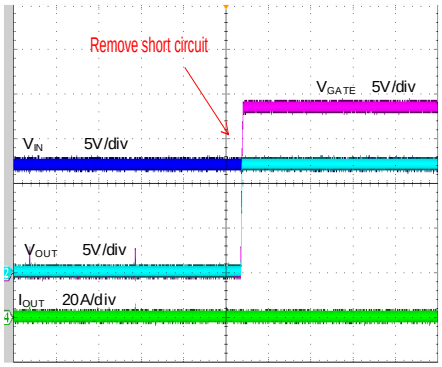
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF)



Time (40μs/div)

Short Circuit Recovery

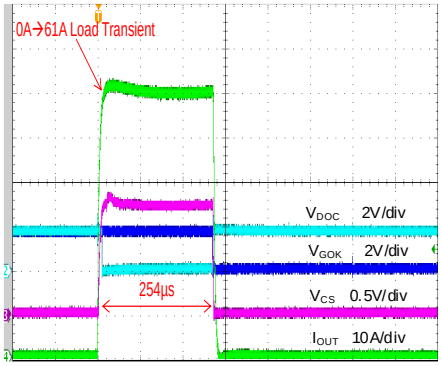
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF)



Time (400ms/div)

Current Limit Response During Normal Operation

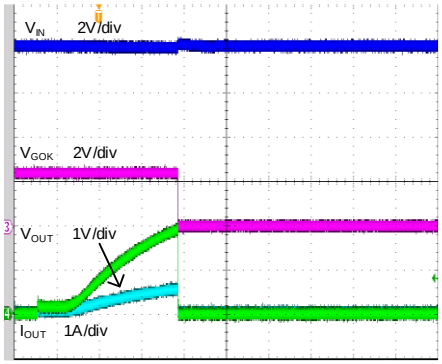
(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF)



Time (100μs/div)

Current Limit Response During Start-up

(V_{IN}=V_{VINF}=12V, R_{CS}=R_{IMON}=2kΩ, R_{CLREF}=120kΩ, C_{SS}=220nF, Load=0.3Ω)



Time (2ms/div)

Operation

The SY28480 is a current limited N-channel MOSFET co-packaged with a smart hot swap controller designed for servers or hot swap applications. It incorporates the over temperature protection, over current protection, and short circuit protection. It can be used either alone, or in a parallel configuration for higher current applications.

VDD Output

The SY28480 provide a 5V output VDD source with current limit upto I_{DD_CL}. Shall connect this pin a 2.2μF to 10μF to GND. And place as close as possible to SY28480.

ON/OFF Control

Without under voltage and any other faults occurring, the output switch will turn on when V_{ON} is above V_{SWON}. When V_{ON} is below V_{SWOFF}, the switch will turn off.

If V_{ON} is between V_{PDOFF} and V_{SWOFF} for longer than t_{PD_DEL}, a 0.77kΩ pull-down resistance to ground is applied to VOUT.

The ON pin sources a 5μA pull up current, connect a capacitor from ON pin to GND can program the startup delay time after VIN is higher than UVLO.

Programmable soft start time

The SY28480 can program output start up time by connect a capacitor from SS pin to GND. Soft start capacitor can be calculated by:
$C_{SS}=(t_{SS}\times I_{SS}\times AV_{SS})/V_{IN}$ (where t_{SS} is the target soft-start time). The recommended range of t_{SS} is 10-100ms. The Soft Start Time vs. C_{SS} curve is shown in Figure3:

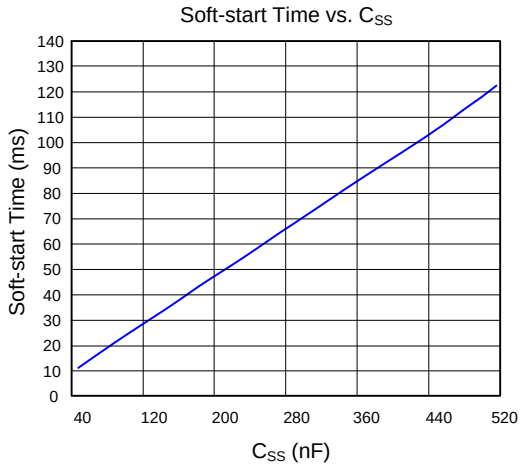


Figure3. Soft Start Time vs. C_{SS}

For parallel application, the SS pins shall be connected together to share one soft start cap so that no slew rate is consistent of each other. The same soft start time make the charging current of each device is same so that the inrush current is balanced.

GOK Output (Gate OK)

The GOK pin is an open-drain output that is pulled low to report the fault under the following conditions:

VDD	VON	Condition	GOK
<UVLO	X	X	Low
>UVLO	Low	VDS OK fail	Low
>UVLO	Low	VGD OK fail	Low
>UVLO	High	VOUT<90%*VIN, after soft start done	Low
>UVLO	High	VGS OK fail after t_{SSF_END}	Low
>UVLO	High	VGS OK fail after t_{GATE_FLT}	Low
>UVLO	High	Current limit lasts longer than t_{OC_LA}	Low
>UVLO	High	Junction over temperature	Low

Usually, GOK can't be used as power good to indicate the output voltage is in the normal range. Bringing VDD below the UVLO voltage or V_{ON} <V_{SWOFF} is required to release a latching condition.

IMON Output (Current Monitor)

The IMON pin sources a current A_{IMON}, which is proportional (10μA/A) to load current. Connect a resistor from this pin to GND to get voltage signal that can be connect to ADC to monitor the load current. Connect a cap from this pin to GND can act as a low pass filter for ADC converter.

CLREF Pin (Current Limit and Over-Current Reference)

The voltage on CLREF pin act as a reference of current limit regulation point. This pin internal will source a 10μA current. Connect a resistor from this pin to GND, can program the current limit threshold. The V_{CLREF} value can be calculated by: $V_{CLREF}=I_{CL}\times R_{CLREF}$
The voltage is also can be given by an external voltage source or a DAC. The recommended voltage range for CLREF is between 0.2V to 1.4V.

CS Input/Output (Current Set)

The CS pin sources a current A_{CS} that is proportional (A_{CS}=10μA/A) to load current. Connect a resistor from

this pin to GND to get voltage which act as a feedback signal of current limit regulation loop.
During normal operation (V_{ON} > V_{SWON} for longer than t_{SS_END}). When the voltage on CS pin, VCS, higher V_{CL_TH} (V_{CL_TH} is equals to V_{CLREF}, and will be clampled at V_{CL_MX}, if V_{CL_TH}>V_{CL_MX}), the internal current limit loop will regulate the output current based on formula: I_{OUT} = V_{CL_TH} /(R_{CS} × A_{CS})

Start up with fold back current

During startup (V_{ON} > V_{SWON} for less than t_{SS_END}), the voltage different between VIN and VOUT is large. A folded back current limit threshold can reduce the power dissipation during start up. The fold back current is depend on the VOUT.

- When VOUT < 40% of VIN, V_{CL_TH} = V_{CL_LO} or V_{CLREF} (whichever is lower).
- When VOUT is between 40% and 80% of VIN, V_{CL_TH} = V_{CL_HI} or V_{CLREF} (whichever is lower).
- When VOUT exceeds 80% of VIN, V_{CL_TH} = V_{CL_MX} or V_{CLREF} (whichever is lower).

If a current limiting condition exists anytime for a continuous duration > t_{CL_LA}, then the device shutdown and restart.
The recommended range of RCS is between 1.8kΩ and 4kΩ. This pin do not connect a capacitor from this pin to GND.

VINF Pin

VINF is the power supply input for internal control circuit. Connect an RC filter, a 10Ω resistor, and a ceramic capacitor ⩾0.1μF as close as possible to this pin.

CS AMP OFFSET BIAS

The SY28480 pre-biased an offset to keep internal high accurate auto-zero amplifier works at null load or light load condition.

The internal IMON and CS current source follow below relationship: I_{OUT} = (I_{CS} - I_{AZ_BIAS})/10μ and I_{OUT} = (I_{MON} - I_{AZ_BIAS})/10μ.

For typical 1.5μA I_{AZ_BIAS}, there has 0.15A positive offset in I_{OUT} sense.

DOC Output (Over-current Indicator)

The D_OC pin is an open-drain output that indicates when an over current condition exists after soft start is complete. When the voltage on the CS pin, VCS is higher than V_{OC_TH}, D_OC is pulled low. If VCS is lower than V_{OC_TH}, D_OC is high impedance and can be pulled high by external pull up resistor

VTEMP Output (Temperature Indicator)

VTEMP is a voltage output proportional 10mV/°C to device junction temperature, with an offset voltage. if multiple VTEMP outputs are connected, the voltage of all VTEMP outputs will be driven to the voltage produced by the hottest SY28480. A 0.1μF capacitor or greater must be connected from the VTEMP pin to ground. The V_{VTEMP} value can be calculated by:
V_{VTEMP}=$V_{VTEMP25}$+(T_{TEMP}-25ºC)×A_{VTEMP}
(where T_{TEMP} is the current temperature)

Auto-Retry Restart

When the following protection is triggered, the power FET will be shut down and after a delay time, t_{DLY_RETRY}, SY28480 will restart.

Excessive Current Limiting: If a current limiting condition exists anytime for a continuous duration > t_{CL_LA}.
Excessive Soft Start Duration: If V_{OUT} < V_{OUTL_TH} when t_{SSF_END} expires.
Short Circuit Protection: If switch current exceeds I_{SC}
Over-Temperature Shutdown: If the FET controller temperature > T_{TSD}.

FET Fault Detection

The device contains various FET monitoring circuits:

- VIN to VOUT short, non-auto-retry condition. If the device is disabled and VOUT > V_{DS_TH} then GOK is pulled low and the device is prevented from powering up. The device is allowed to power up once VOUT < V_{DS_OK}.
- GATE to VIN short, non-auto-retry condition. If the device is disabled and GATE (Pin 8) > V_{DG_TH}, then GOK is pulled low and device is prevented from powering up. The device allowed to power up once GATE < V_{DG_OK}.
- GATE leakage-startup.
  If (GATE – VINF) < V_{G_TH} at t_{SSF_END}, then GOK is pulled low and FET restarts.
- GATE leakage-normal operation.
  If (GATE – VINF) < V_{G_TH} for t_{GATE_FLT} time after the soft start timer completes, then GOK is pulled low and device restarts.

FET SOA Limits

Power FET's SOA should not be exceeded. In-built timed current limits and fault-monitoring circuit make the power FET work within SOA limits in normal operation status.

Multiple Fuse Power Up

When multiple SY28480 are paralleled together, the SY28480s will turn on together. Keeping the current

through each switch within 1 A (typical) helps to prevent overstress on each switching during soft start.

If all parallel SY28480 SS pins are short circuit, all SY28480s are shutdown when one of them is in Auto-Retry stage because SS is forced to pull down during Auto-Retry stage. Please set all ON pins pull down or reset their VDD and reset circuit to avoid paralleled multiple SY28480 encounter fault.

Input Filter Capacitor

A 1μF or larger input ceramic capacitor is strongly recommended to be placed close to the VIN. A VOUT short will cause ringing on the VIN without the VIN capacitor. It could cause the N-MOSFET electrical over stress when the VIN transient exceeds the absolute maximum voltage rating even for a short duration.

Transient Voltage Suppressor

The SY28480 specifies an absolute maximum voltage of 20V and is designed to tolerate brief over voltage events due to hot plug surges. To protect the SY28480 from an over voltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ20CA between the VIN and GND pins.

OUT Schottky Diode

An anti-parallel schottky diode is suggested to be placed near the VOUT pin to absorb the negative ringing. A low forward voltage and large forward current schottky diode is recommend.

Hot Plug Application

In hot plug scenario, the rapid slew rate of input voltage will be coupled to the internal control circuit through the VINF, resulting in internal logic abnormalities. So the VINF needs to be connected to the VIN through an RC filter. Connect an RC filter, a 10Ω resistor, and a ceramic capacitor ⩾0.1μF, to reduce the voltage slew rate on VINF.

PCB Layout Guide

For best performance of the SY28480, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible and use at least 2-ounce copper for all power traces.
2. Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
3. Locate the output capacitor as close to the connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient performance.
4. Input and output filter capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.
5. Locate the RC filter as close to VINF as possible to stabilize the bias supply.

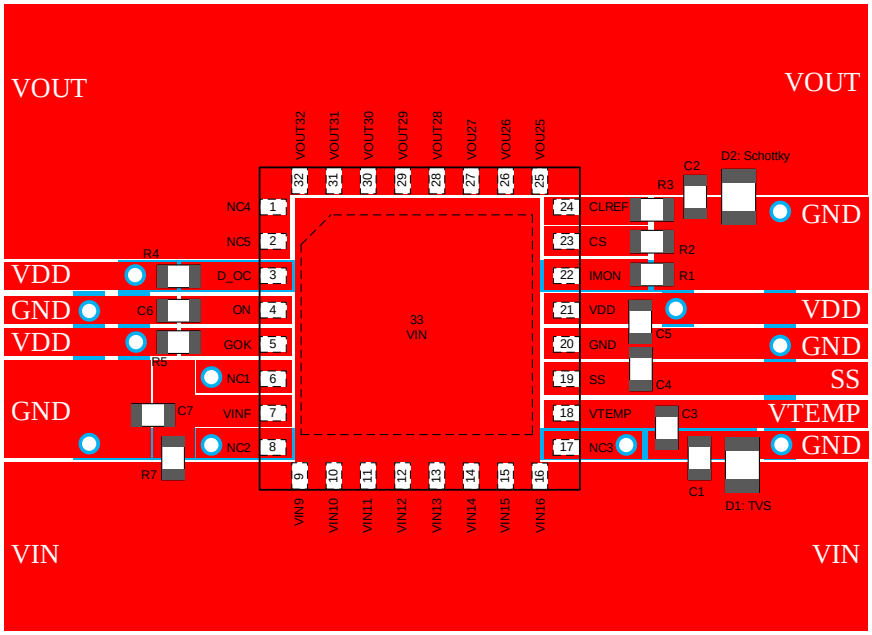
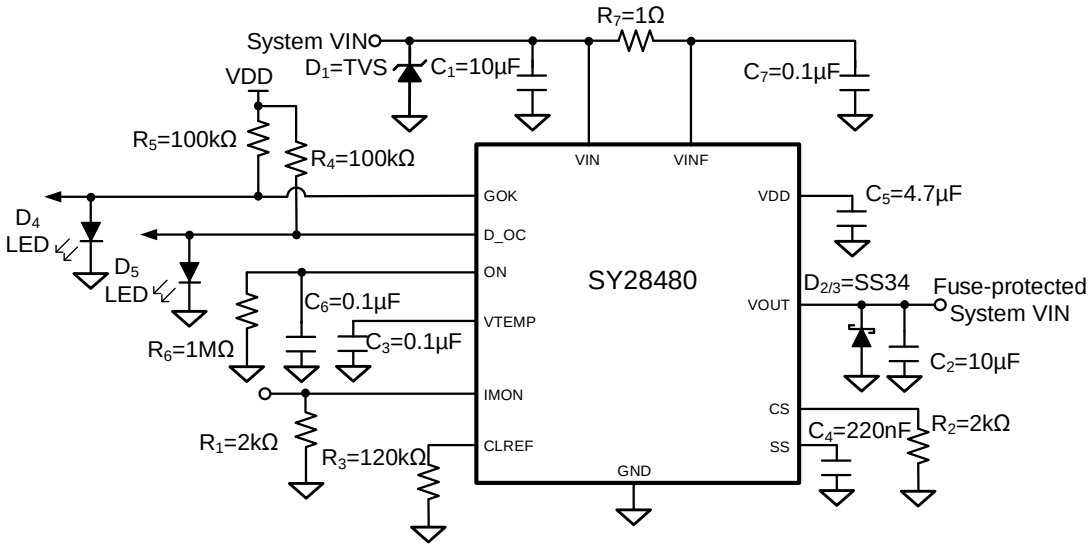


Figure 4. PCB Layout Suggestion

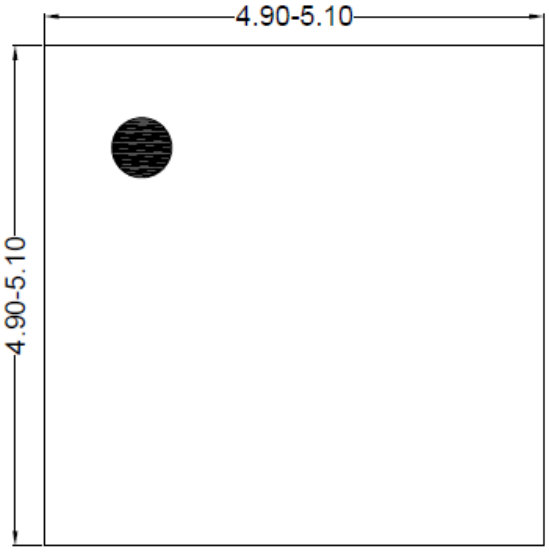
Schematic



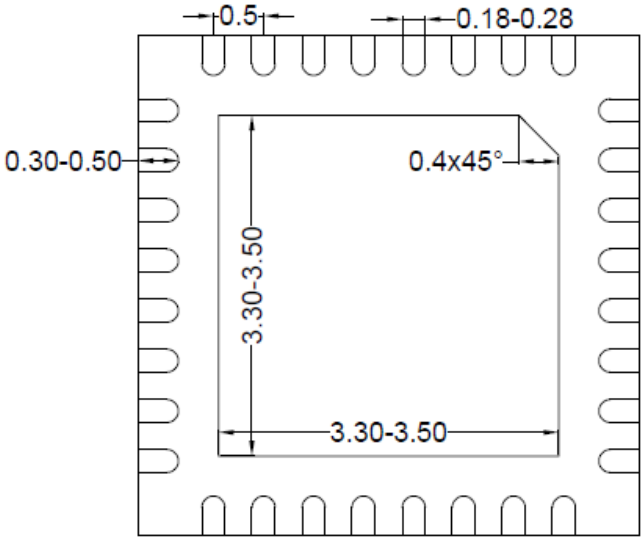
BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	10μF/50V, 1206	GRT31CR61H106KE01L	Murata
C_2	10μF/50V, 1206	GRT31CR61H106KE01L	Murata
C_3	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
C_4	220nF/50V, 0603	CGA3E3X7R1H224K080AE	Murata
C_5	4.7μF/16V, 0603	GRM185R61C475KE11D	Murata
C_6, C_7	0.1μF/50V, 0603	GCJ188R71H104KA12	Murata
R_1	2kΩ, 0603	RC0603FR-072KL	YAGEO
R_2	2kΩ, 0603	RC0603FR-072KL	YAGEO
R_3	120kΩ, 0603	RC0603FR-07120KL	YAGEO
R_4	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_5	100kΩ, 0603	RC0603FR-07100KL	YAGEO
R_6	1MΩ, 0603	RC0603FR-071ML	YAGEO
R_7	1Ω, 0603	RC0603FR-071RL	YAGEO
D_1	TVS/20V	SMAJ20CA	PHY
$D_{2/3}$	Schottky/40V	SS34	TOSHIBA
$D_{4/5}$	LED	/	/

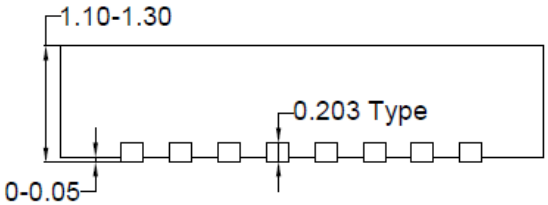
QFN5.0×5.0-32 Package Outline Drawing



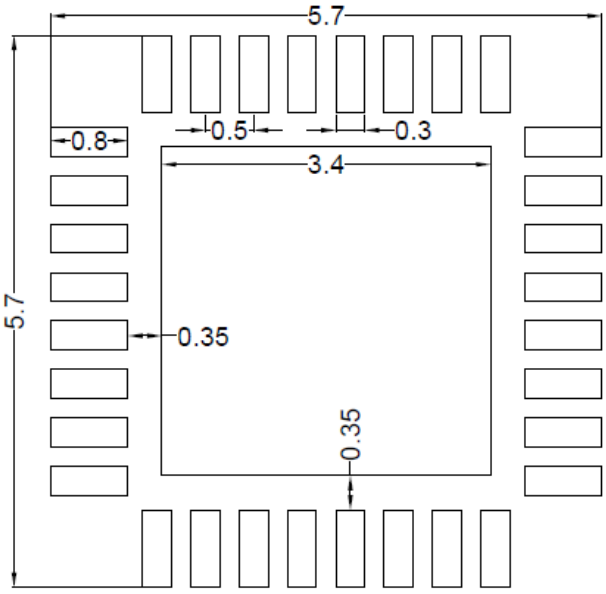
Top view



Bottom view



Side view

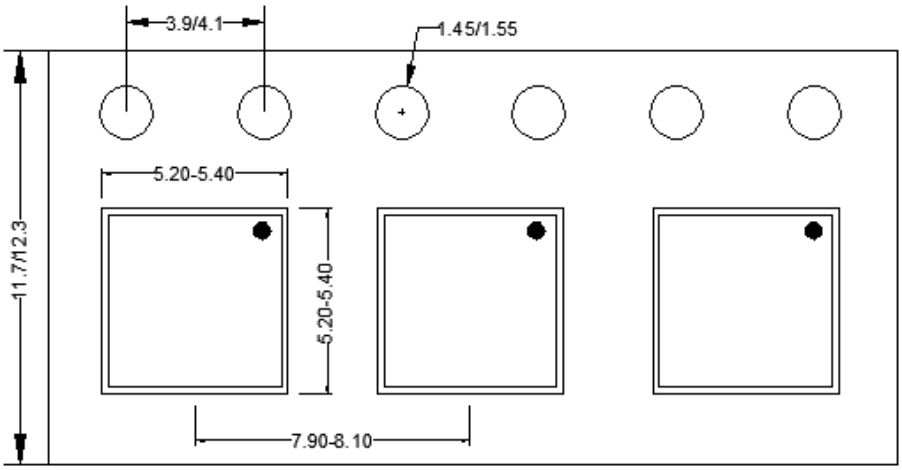


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;

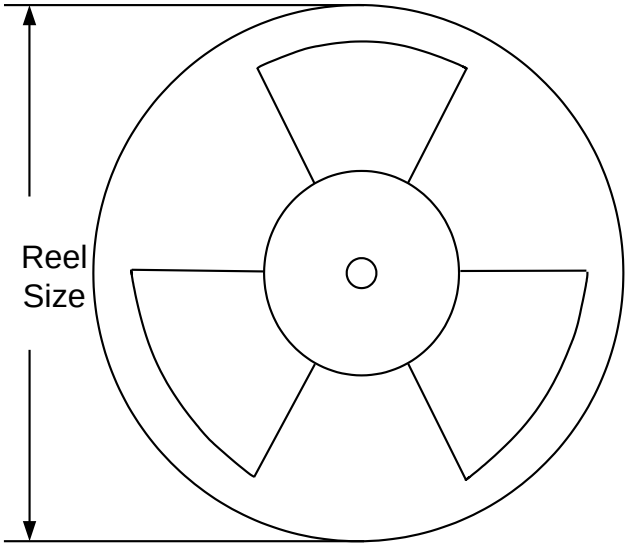
Taping & Reel Specification

1. Taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.27, 2025	Revision 1.0A	1. The capacitor between the VINF pin and the GND changed from 1μF to 0.1μF; 2. Update the application description of “ON/OFF Control ” (Page 12) 3. Update the application description of “GOK Output (Gate OK)” (Page 12) 4. Update the application description of “VINF Pin” (Page 13) 5. Update the application description of “Hot Plug Application” (Page14)
Dec. 13, 2023	Revision 1.0	Initial Release

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