SY81102, SY81102E, SY81102C, SY81102B

High Efficiency, 2A, 18V Input Synchronous Buck Converter

General Description

The SY81102x is high efficiency synchronous buck converter operates over a wide input voltage range of 4.5V to 18V, and can deliver an output current up to 2A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The high pseudo-constant switching frequency enables using small external inductor and capacitor values.

The device uses constant on-time and ripple-based control strategy to achieve fast transient response for applications with high step-down ratios. It also provides cycle-by-cycle current limit protection, output under voltage protection and over temperature protection.

Only the input and output capacitors, inductor, feedback resistor divider and feedforward capacitor need to be selected for the targeted application specifications.

The SY81102x is available in a compact SOT23-6 package.

Part Number	Frequency	Mode
SY81102ABT	500kHz	PFM
SY81102EABT	500kHz	FCCM
SY81102CABT	1200kHz	PFM
SY81102BABT	1400kHz	FCCM

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 130mΩ Top, 105mΩ Bottom
- Wide Input Voltage Range: 4.5V ~ 18V
- Up to 2A Output Current
- ±1.5% 0.6V Reference
- Precise EN Threshold
- Pulse-Frequency Modulation (PFM) Mode Operation for SY81102 and SY81102C
- Forced Continuous Conduction Mode (FCCM) Operation for SY81102E and SY81102B
- Internal Soft-Start Limits the Inrush Current
- Support Smooth Startup with Pre-Biased Output
- 500kHz Switching Frequency Minimizes the External Components for SY81102 and SY81102E
- 1200kHz Switching Frequency Minimizes the External Components for SY81102C
- 1400kHz Switching Frequency Minimizes the External Components for SY81102B
- Constant On-time and Ripple-Based Control to Achieve Fast Transient Responses
- Stable with 10µF C_{OUT}
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact Package: SOT23-6

Applications

- Set-Top Box
- Portable TV
- DSL Modem
- LCD TV
- IP Camera
- Networking

Typical Application

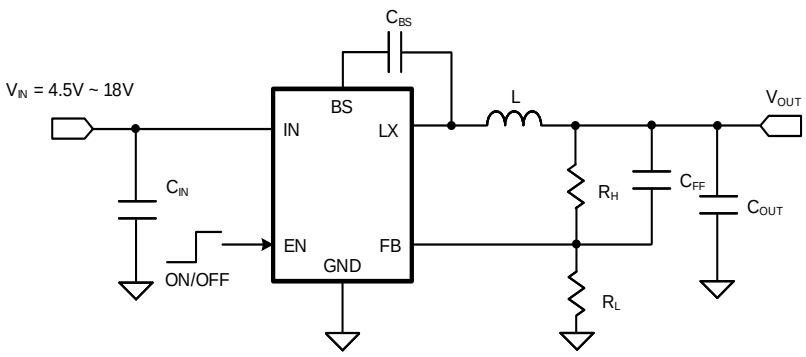


Figure1. Typical Application Circuit

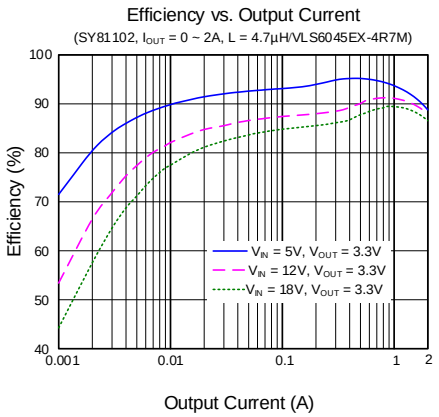


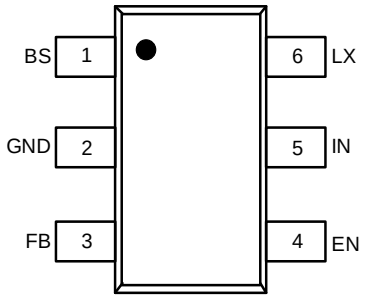
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY81102ABT	SOT23-6 RoHS Compliant and Halogen Free	**HJKx*yz***
SY81102EABT	SOT23-6 RoHS Compliant and Halogen Free	**HRHx*yz***
SY81102CABT	SOT23-6 RoHS Compliant and Halogen Free	**KAKx*yz***
SY81102BABT	SOT23-6 RoHS Compliant and Halogen Free	**KANx*yz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1µF ceramic capacitor between the BS and the LX pin.
2	GND	Ground pin.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
4	EN	Enable pin. Pull this pin higher than EN rising threshold to turn on the device and pull this pin lower than EN falling threshold to turn off the device. Do not leave this pin floating.
5	IN	Input pin. Decouple this pin from the GND pin with at least a 10µF ceramic capacitor.
6	LX	Inductor pin. Connect this pin to the switching node of inductor.

Block Diagram

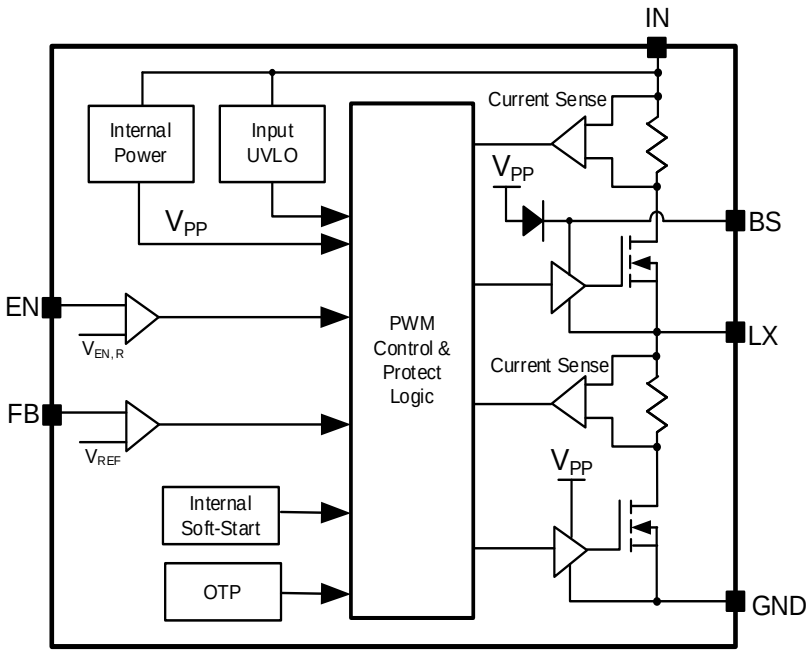


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	19	V
EN, LX	-0.3	IN + 0.3	
LX, 10ns duration	-5	IN + 3	
BS-LX, FB	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	55	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	6.5	
P_D Power Dissipation T_A = 25°C	1.8	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4.5	18	V
Output Voltage	0.6	9.2	
Continuous Output Current		2	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, C_{OUT} = 10μF, T_J = 25°C, I_{OUT} = 1A unless otherwise specified (note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		4.5		18	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	V_{IN} rising			4.45	
	UVLO Hysteresis	$V_{IN,HYS}$			0.3		
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{FB} = V_{REF} × 105%, only for SY81102, SY81102C		200	280	μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		5	10	μA
Output	Voltage Range	V_{SET}		0.6		9.2	V
	FB Reference Voltage	V_{REF}		0.591	0.6	0.609	
	FB Input Current	I_{FB}	V_{FB} = 1V	-50		50	nA
	Turn On Delay Time	$t_{ON,DLY}$	From EN high to LX starts switching (Note 5)		180		μs
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET}	0.5	1	1.6	ms
	UVP Threshold	V_{UVP}			33		%V_{REF}
	UVP Delay Time	$t_{UVP,DLY}$			100		μs
	UVP Hiccup On-Time	$t_{HICCUP,ON}$			1.5		ms
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$			4.5		
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
	Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	
	Input Current	I_{EN}	V_{EN} = 3.3V		0		μA
MOSFET	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			130		mΩ
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			105		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$		3			A
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$		2			
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$	Only for SY81102E, SY81102B	0.8			
Frequency	Switching Frequency	f_{SW}	I_{OUT} = 1A, CCM, only for SY81102, SY81102E		500		kHz
			I_{OUT} = 1A, CCM, only for SY81102C		1200		
			I_{OUT} = 1A, CCM, only for SY81102B		1400		
	Minimum On-Time	$t_{ON,MIN}$			50		ns
	Minimum Off-Time	$t_{OFF,MIN}$			100		
OTP	Temperature	T_{OTP}	(Note 5)		150		˚C
	Temperature Hysteresis	T_{HYS}	(Note 5)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 6cm×6cm size, two-layer Silergy Evaluation Board with 2-oz copper. Case temperature θ_{JC} is measured at Pin 6.

Note 3: The device is not guaranteed to function outside its operating conditions.

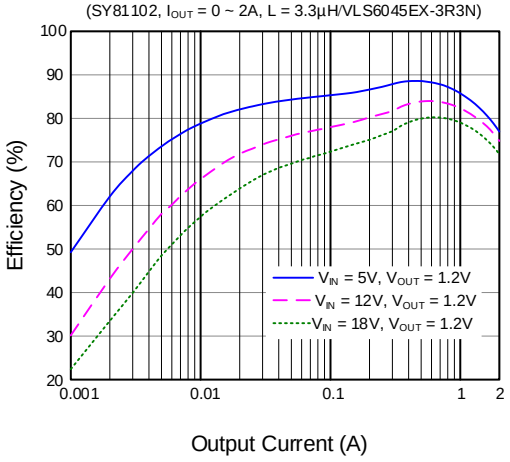
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25°C$. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

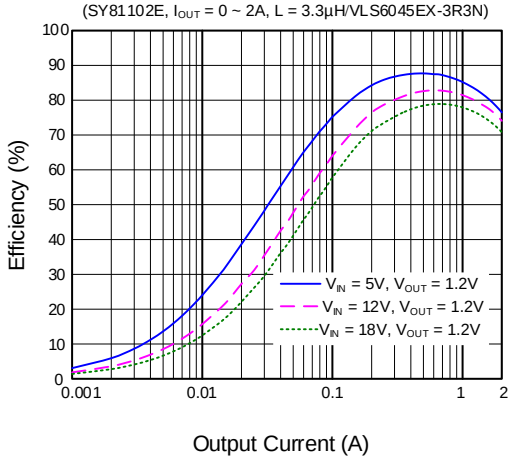
(SY81102xABT, T_A = 25°C, V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, C_{OUT} = 10µF, unless otherwise noted)

Efficiency vs. Output Current
(SY81102, I_{OUT} = 0 ~ 2A, L = 3.3µH/VLS6045EX-3R3N)



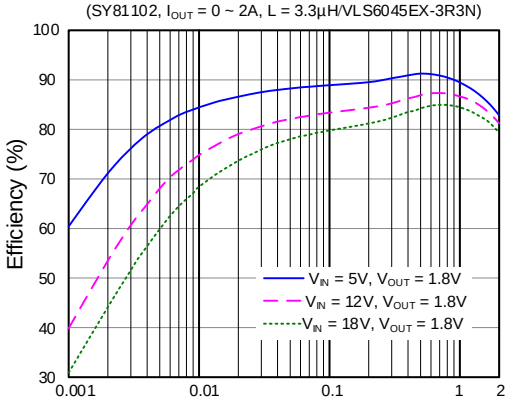
Output Current (A)

Efficiency vs. Output Current
(SY81102E, I_{OUT} = 0 ~ 2A, L = 3.3µH/VLS6045EX-3R3N)



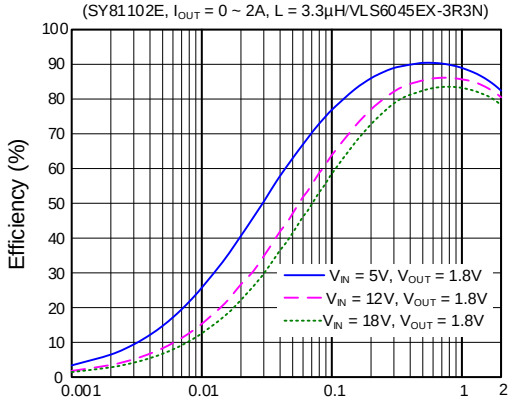
Output Current (A)

Efficiency vs. Output Current
(SY81102, I_{OUT} = 0 ~ 2A, L = 3.3µH/VLS6045EX-3R3N)



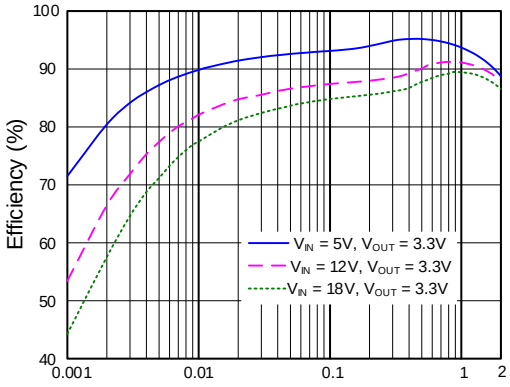
Output Current (A)

Efficiency vs. Output Current
(SY81102E, I_{OUT} = 0 ~ 2A, L = 3.3µH/VLS6045EX-3R3N)



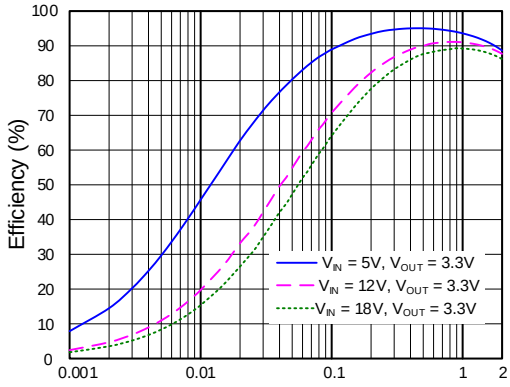
Output Current (A)

Efficiency vs. Output Current
(SY81102, I_{OUT} = 0 ~ 2A, L = 4.7µH/VLS6045EX-4R7M)



Output Current (A)

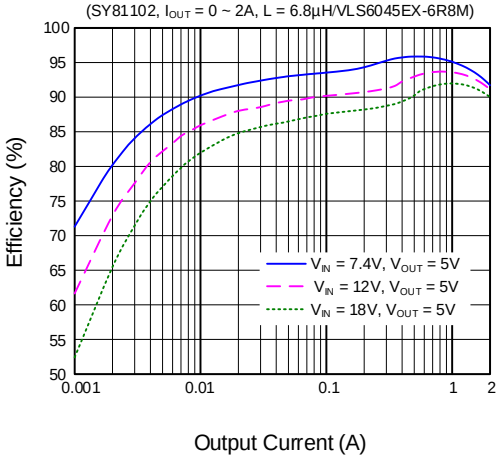
Efficiency vs. Output Current
(SY81102E, I_{OUT} = 0 ~ 2A, L = 4.7µH/VLS6045EX-4R7M)



Output Current (A)

Efficiency vs. Output Current

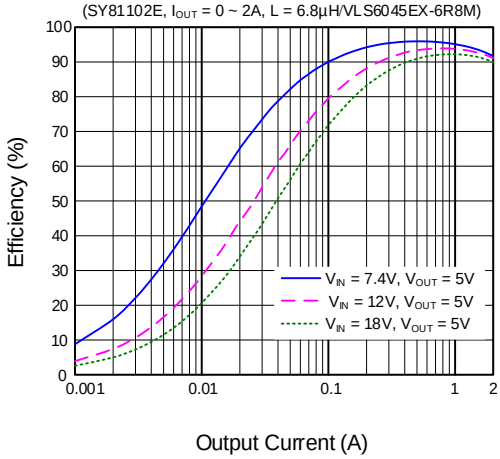
(SY81102, I_{OUT} = 0 ~ 2A, L = 6.8µH/VLS6045EX-6R8M)



Output Current (A)

Efficiency vs. Output Current

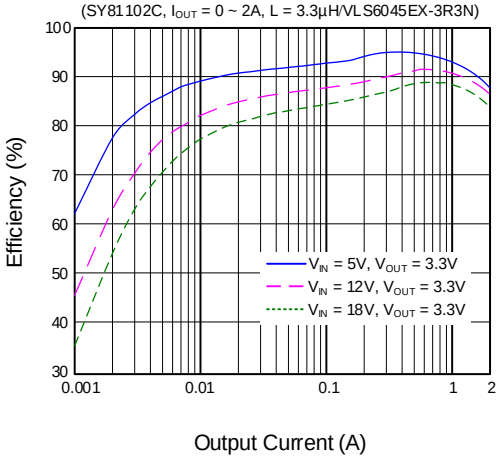
(SY81102E, I_{OUT} = 0 ~ 2A, L = 6.8µH/VLS6045EX-6R8M)



Output Current (A)

Efficiency vs. Output Current

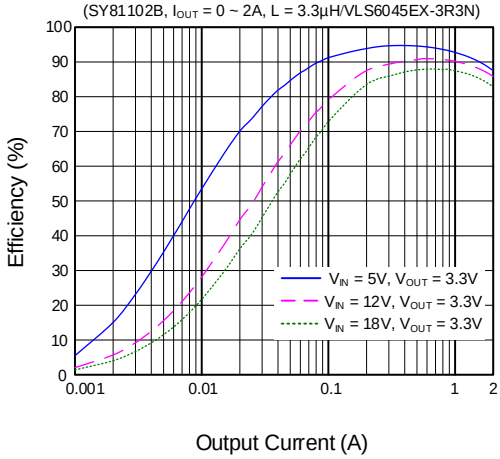
(SY81102C, I_{OUT} = 0 ~ 2A, L = 3.3µH/VLS6045EX-3R3N)



Output Current (A)

Efficiency vs. Output Current

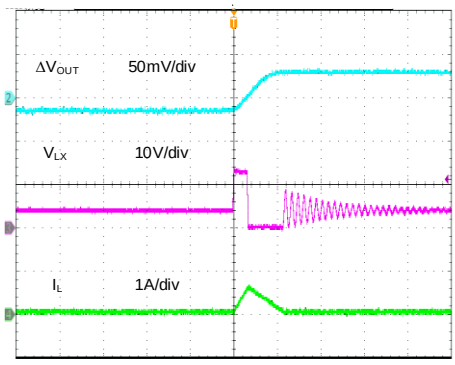
(SY81102B, I_{OUT} = 0 ~ 2A, L = 3.3µH/VLS6045EX-3R3N)



Output Current (A)

Output Ripple

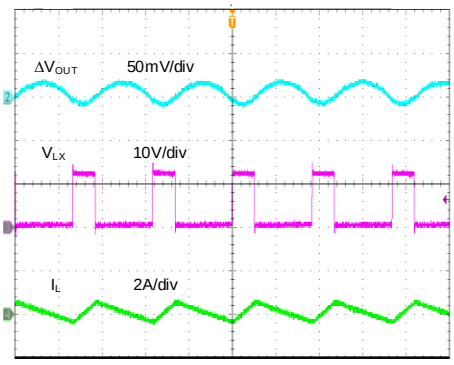
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A)



Time (1µs/div)

Output Ripple

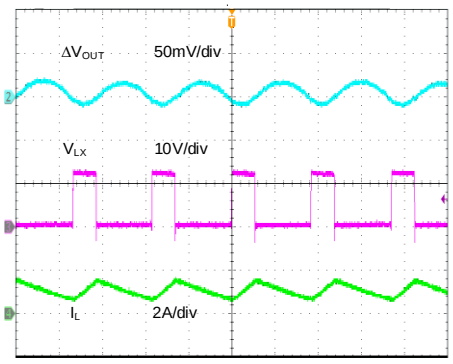
(SY81102E, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A)



Time (1µs/div)

Output Ripple

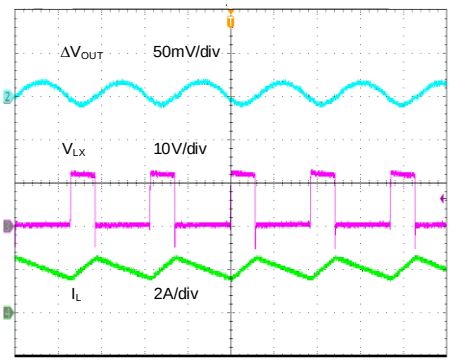
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A)



Time (1μs/div)

Output Ripple

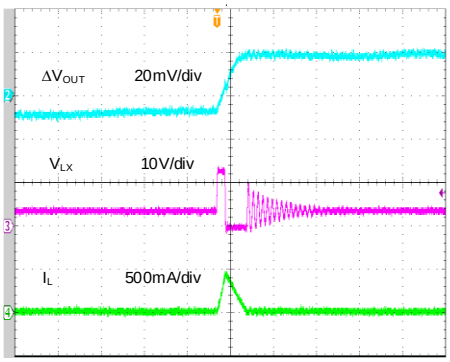
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A)



Time (1μs/div)

Output Ripple

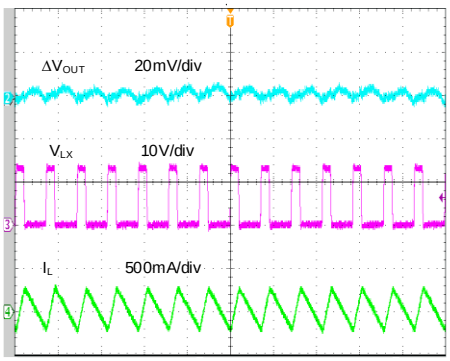
(SY81102C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A, L= 3.3μH)



Time (1μs/div)

Output Ripple

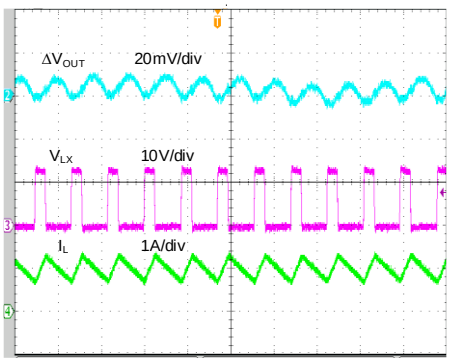
(SY81102B, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A, L= 3.3μH)



Time (1μs/div)

Output Ripple

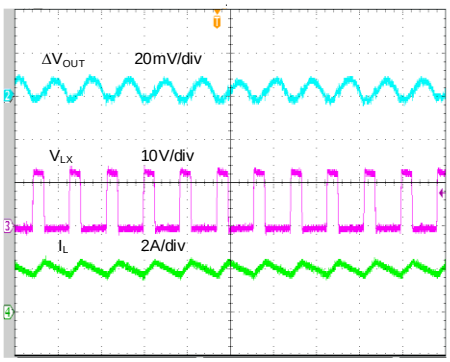
(SY81102C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A, L= 3.3μH)



Time (1μs/div)

Output Ripple

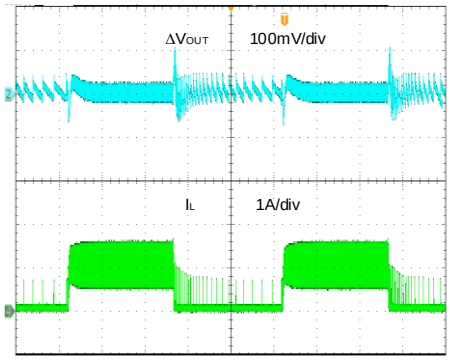
(SY81102C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, L= 3.3μH)



Time (1μs/div)

Load Transient

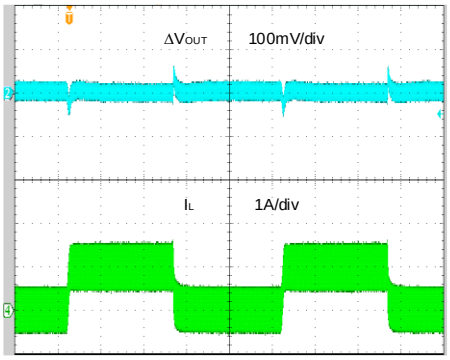
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 1A)



Time (400μs/div)

Load Transient

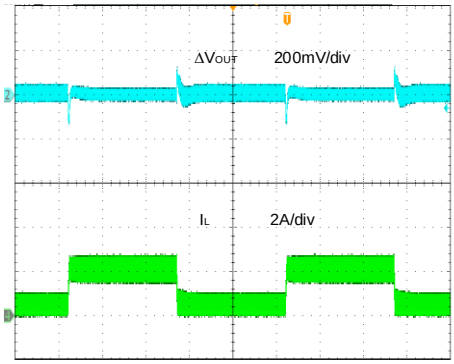
(SY81102E, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 1A)



Time (400μs/div)

Load Transient

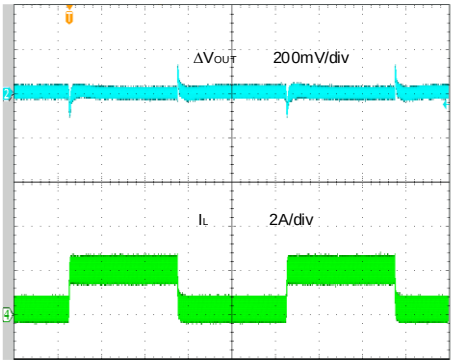
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.2A ~ 2A)



Time (400μs/div)

Load Transient

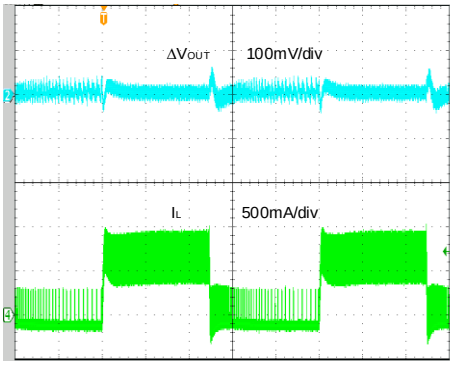
(SY81102E, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.2A ~ 2A)



Time (400μs/div)

Load Transient

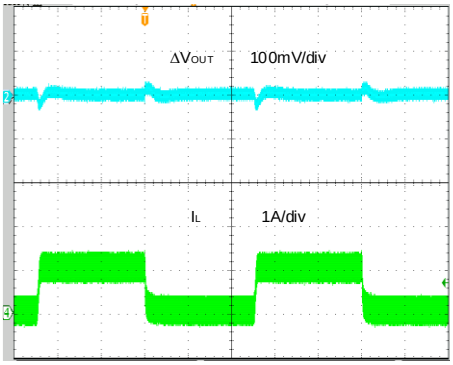
(SY81102C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 1A, L= 3.3μH)



Time (400μs/div)

Load Transient

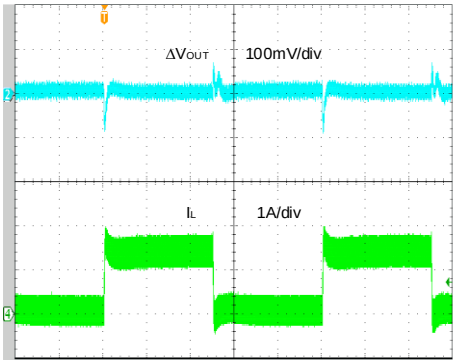
(SY81102B, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ 1A, L= 3.3μH)



Time (400μs/div)

Load Transient

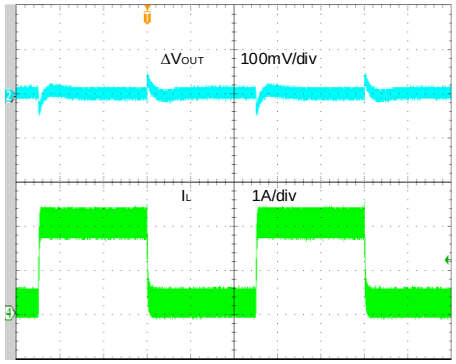
(SY81102C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.2A ~ 2A, L= 3.3μH)



Time (400μs/div)

Load Transient

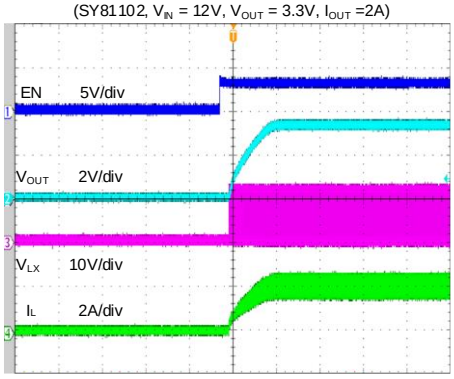
(SY81102B, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.2A ~ 2A, L= 3.3μH)



Time (400μs/div)

Startup from Enable

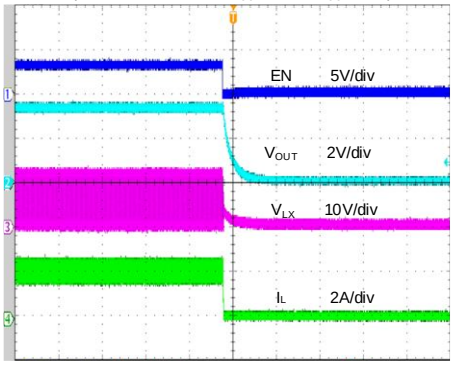
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} =2A)



Time (800μs/div)

Shutdown from Enable

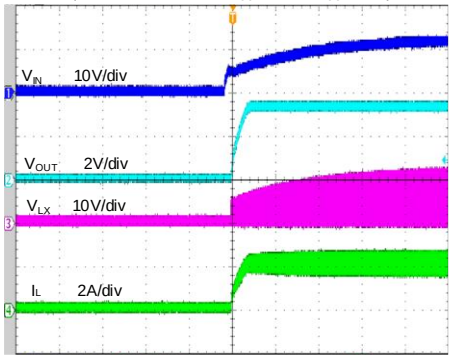
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A)



Time (200μs/div)

Startup from V_{IN}

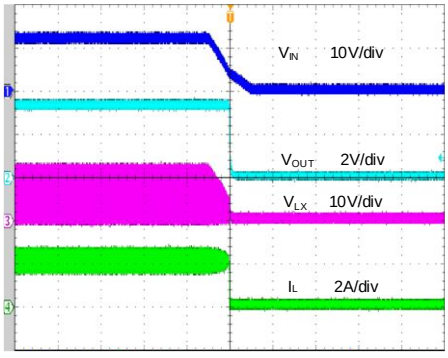
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A)



Time (2ms/div)

Shutdown from V_{IN}

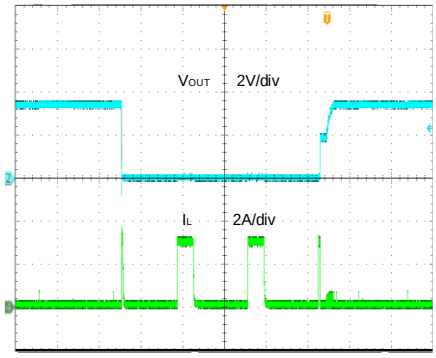
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A)



Time (2ms/div)

Short Circuit Protection

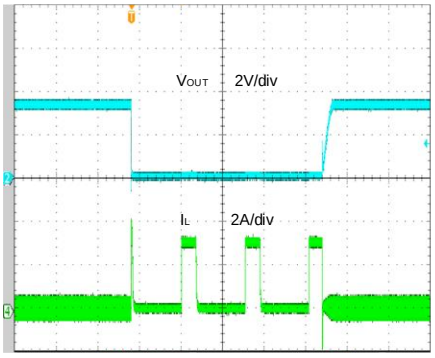
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ short)



Time (4ms/div)

Short Circuit Protection

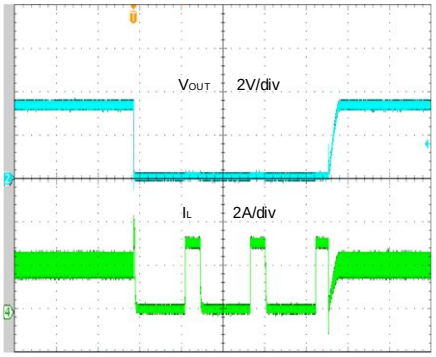
(SY81102E, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A ~ short)



Time (4ms/div)

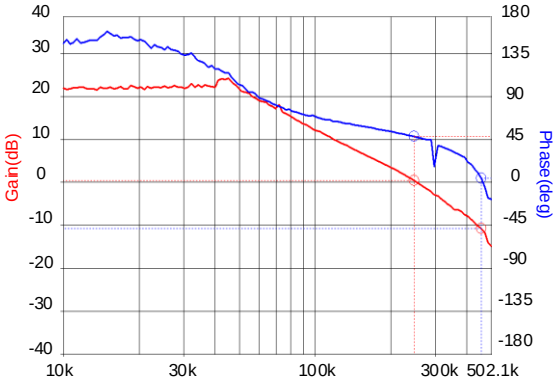
Short Circuit Protection

(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A ~ short)



Time (4ms/div)

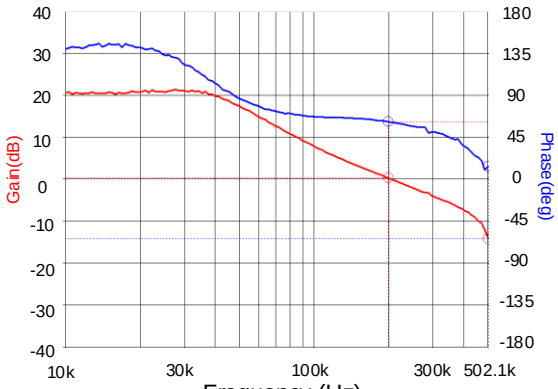
Bode Plot
(SY81102, V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 2A)



Red Cursor Information:
Band Width: 254.075 kHz
Phase Margin: 47.197 deg

Blue Cursor Information:
Frequency: 464.118 kHz
Gain: -11.167 dB

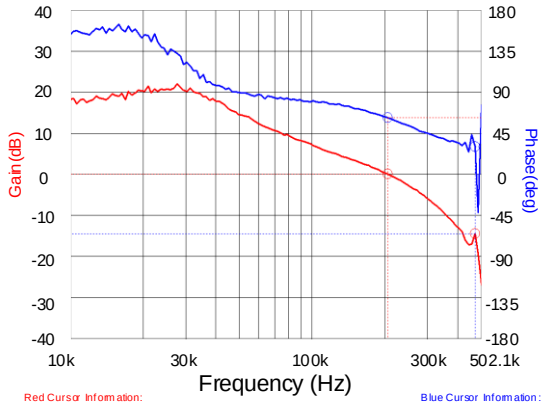
Bode Plot
(SY81102, V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Red Cursor Information:
Band Width: 204.541 kHz
Phase Margin: 60.952 deg

Blue Cursor Information:
Frequency: 502.1 kHz
Gain: -14.237 dB

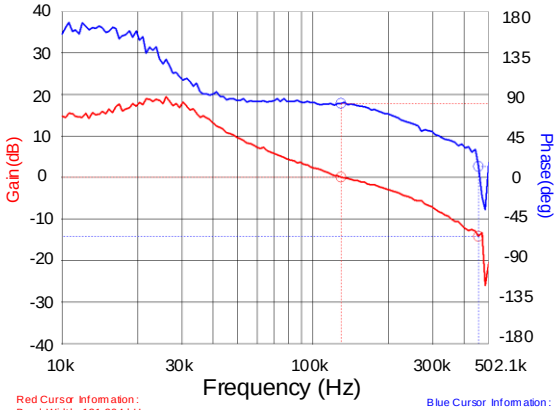
Bode Plot
(SY81102, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A)



Red Cursor Information:
Band Width: 206.330 kHz
Phase Margin: 61.811 deg

Blue Cursor Information:
Frequency: 478.226 kHz
Gain: -16.502 dB

Bode Plot
(SY81102, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2A)



Red Cursor Information:
Band Width: 131.304 kHz
Phase Margin: 80.525 deg

Blue Cursor Information:
Frequency: 462.792 kHz
Gain: -13.915 dB

Detailed Description

General Description

The SY81102x high efficiency synchronous buck converter operate over a wide input voltage range of 4.5V to 18V, and can deliver an output current up to 2A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The high pseudo-constant switching frequency allows small external inductor and capacitor values.

The device also provides cycle-by-cycle current limit protection output under voltage protection and over temperature protection.

Constant On-Time and Ripple-Based Control Strategy

The device uses instant PWM architecture to achieve fast transient response for applications with high step-down ratios, and high efficiency at light loads. It uses a constant on-time and ripple-based control strategy in which a virtual replica of the inductor current signal is synthesized internally and combined with the feedback voltage. When the sum voltage is lower than the reference voltage, the bottom MOSFET turns off and the top MOSFET turns on for a fixed period of time (Constant t_{ON}). t_{ON} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{ON} = \frac{V_{OUT}/V_{IN}}{f_{SW}}$$

The top MOSFET turns off after a period of t_{ON}.

Minimum and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

The device can support a maximum duty cycle of up to 75% across the entire operating temperature range of -40˚C ~ 125˚C.

PFM Light Load Operation

SY81102 and SY81102C use pulse-frequency modulation (PFM) operation mode under light load condition for high efficiency. Under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L}$$

the current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

While in PFM mode, the output of the device doesn't require over voltage protection because the device stops switching as soon as the voltage at the FB node increases above V_{REF}, preventing the output voltage from increasing further.

FCCM Light Load Operation

SY81102E and SY81102B use forced continuous conduction mode (FCCM) under light load condition. Under light load conditions, the bottom MOSFET still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle. The device always operates under continuous conditions mode and keeps fairly constant switching frequency over all the output current range.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection. The device remains in a low current state and all LX node switching actions are inhibited until V_{IN} exceeds its rising threshold. At that time, if EN is enabled, the device will startup. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, the LX node switching actions will again be suppressed.

Precise EN Threshold

The EN pin uses precise rising and falling thresholds to provide programmable ON/OFF control. The device will be turned on when the EN pin voltage exceeds the rising threshold. The device will be turned off while the EN pin voltage falls below the falling threshold. Increasing the input UVLO threshold is possible using an external resistor divider as shown below:

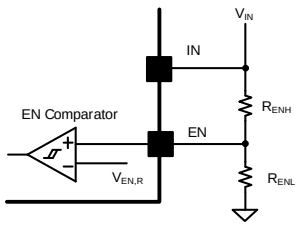


Figure4. EN Control

It is not recommended to connect EN pin to the V_{IN} or another voltage source directly. A resistor with a value between 1kΩ and 1MΩ is recommended if the EN pin is pulled high.

Soft-Start and Startup with Pre-Biased Output

The device incorporates an internal soft-start circuit to ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

External Bootstrap Capacitor

The external bootstrap capacitor provides the gate driver voltage for the N-channel top MOSFET. A 0.1μF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

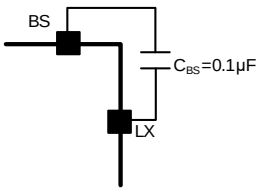


Figure5. Bootstrap Capacitor Connection

Fault Protection Modes

Cycle-by-Cycle Current Limit Protection

If the top MOSFET current exceeds the top current limit threshold, it will turn off and the bottom MOSFET will turn on. If the bottom MOSFET current exceeds the bottom current limit threshold, it will stay on until the current decreases below its current limit threshold. As a result, both inductor peak and valley currents are limited.

Output Under Voltage Protection (UVP)

With output current increasing, as soon as the bottom MOSFET current exceeds its current limit threshold, the top MOSFET will not be allowed to turn on any more. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 33% of the regulated level, the output under voltage protection will be activated and the device will operate in hiccup mode. The hiccup on-time is 1.5ms, and the hiccup off-time is 4.5ms. If the hard short condition is removed, the device will return to normal operation.

Over Temperature Protection (OTP)

The device includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature is reduced by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

Application Information

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. As an example, if V_{OUT} = 3.3V and R_H selected value is 100kΩ, R_L can be calculated as follows:

$$R_L = \frac{0.6}{V_{OUT} - 0.6V} \times R_H$$

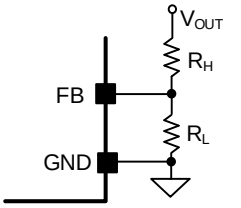


Figure6. Feedback Resistor Divider

With a calculated value of 22.2kΩ for R_L, a standard 1% 22.1kΩ resistor is selected.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 25V rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The device has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) For buck converter using FCCM light load operation mode, make sure the inductance value is high enough to avoid reverse current limit threshold is been triggered just under steady state if the load current is zero.

3) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 50mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use a X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Feedforward Capacitor C_{FF}

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load transient response. It is recommended at least 47pF for most applications. Note that when the output LC parameter is large, the feedforward capacitor can be increased for providing sufficient ripple to FB for small output ripple and good transient behavior.

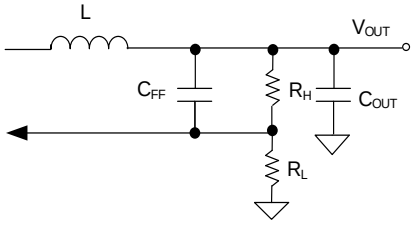


Figure7. Feedforward Network

Application Schematic for SY81102 and SY81102E (V_{OUT} = 3.3V)

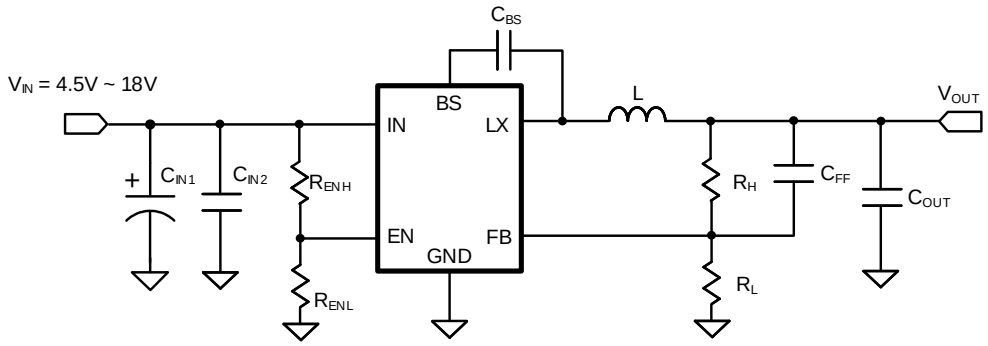


Figure8. Schematic Diagram

BOM List for SY81102 and SY81102E (VOUT = 3.3V)

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47µF/50V Electrolytic Capacitor		
C_{IN2}	10µF/25V/X5R, 1206	GRM319R61E106KA12D	mµRata
C_{OUT}	10µF/16V/X5R, 1206	GRM319R61C106KE15D	mµRata
C_{BS}	0.1µF/50V/X5R, 0603	GRM188R61H104KA93D	mµRata
C_{FF}	47pF/50V/C0G, 0603	GRM1885C1H470JA01D	mµRata
L	4.7µH/inductor, 3.8A	VLS6045EX-4R7M	TDK
R_H	100kΩ, 1%, 0603		
R_L	22.1kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommend Component Values for SY81102 and SY81102E

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	10	3.3µH/VLS6045EX-3R3N	22µF/16V/X5R, 1206
1.8	100	49.9	10	3.3µH/VLS6045EX-3R3N	10µF/16V/X5R, 1206
3.3	100	22.1	47	4.7µH/VLS6045EX-4R7M	10µF/16V/X5R, 1206
5	100	13.7	47	6.8µH/VLS6045EX-6R8M	10µF/16V/X5R, 1206

Application Schematic for SY81102C (V_{OUT} = 3.3V)

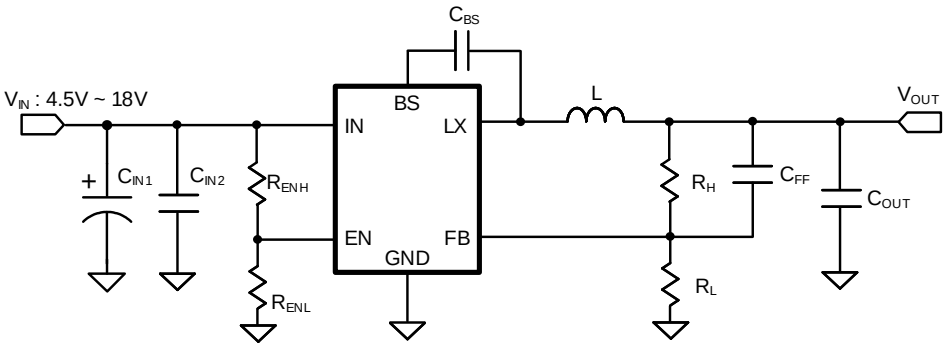


Figure9. Schematic Diagram

BOM List for SY81102C (V_{OUT} = 3.3V)

Reference Designator	Description	Part Number	Manufacturer
C_1	47μF/50V Electrolytic Capacitor		
C_2	10μF/25V/X5R,1206	GRM319R61E106KA12D	mμRata
C_3	10μF/16V/X5R,1206	GRM319R61C106KE15D	mμRata
C_5	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_6	100pF/50V/C0G, 0603	GRM1885C1H101JA01D	mμRata
L_1	3.3μH/4.95A	VLS6045EX-3R3N	TDK
R_1	100kΩ, 1%, 0603		
R_2	22.1kΩ, 1%, 0603		
R_4	10kΩ, 1%, 0603		
R_3	1MΩ, 1%, 0603		

Recommend Component Values for SY81102C

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	220	1.5μH/VLS6045EX-1R5N	10μF/16V/X5R, 1206
1.8	100	49.9	100	2.2μH/VLS6045EX-2R2N	10μF/16V/X5R, 1206
3.3	100	22.1	100	3.3μH/VLS6045EX-3R3N	10μF/16V/X5R, 1206
5	100	13.7	100	3.3μH/VLS6045EX-3R3N	10μF/16V/X5R, 1206

Application Schematic for SY81102B (V_{OUT} = 3.3V)

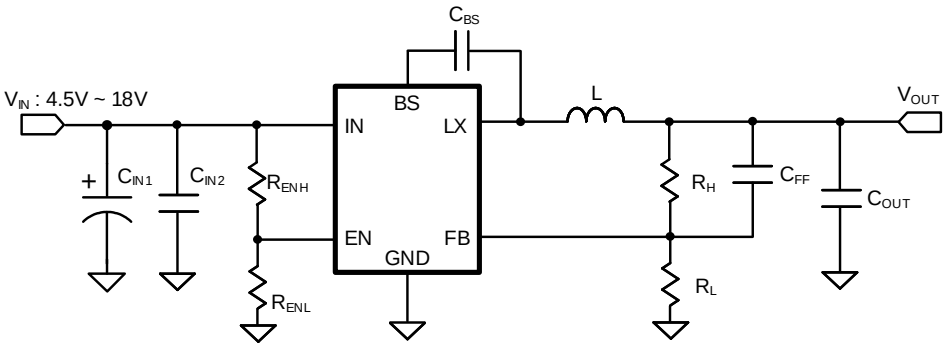


Figure9. Schematic Diagram

BOM List for SY81102B (V_{OUT} = 3.3V)

Reference Designator	Description	Part Number	Manufacturer
C_1	47μF/50V Electrolytic Capacitor		
C_2	10μF/25V/X5R,1206	GRM319R61E106KA12D	mμRata
C_3	10μF/16V/X5R,1206	GRM319R61C106KE15D	mμRata
C_5	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_6	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
L_1	3.3μH/4.95A	VLS6045EX-3R3N	TDK
R_1	100kΩ, 1%, 0603		
R_2	22.1kΩ, 1%, 0603		
R_4	10kΩ, 1%, 0603		
R_3	1MΩ, 1%, 0603		

Recommend Component Values for SY81102B

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
1.2	100	100	47	1.5μH/VLS6045EX-1R5N	10μF/16V/X5R, 1206
1.8	100	49.9	47	1.5μH/VLS6045EX-1R5N	10μF/16V/X5R, 1206
3.3	100	22.1	220	3.3μH/VLS6045EX-3R3N	10μF/16V/X5R, 1206
5	100	13.7	220	4.7μH/VLS6045EX-4R7M	10μF/16V/X5R, 1206

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitors: Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND pins using a wide copper area.

Output Capacitors: Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.

Feedback Network: Place the feedback components (R_H, R_L and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

BS Capacitor: Place the BS capacitor on the **same** layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

EN Signal: It is **not** recommended to connect EN pin directly to V_{IN} or another voltage source. A resistor in a range of 1kΩ to 1MΩ should be used if EN pin is pulled high.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.

PCB Board: To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if possible. Connect the ground pad to a large copper area to enhance thermal performance.

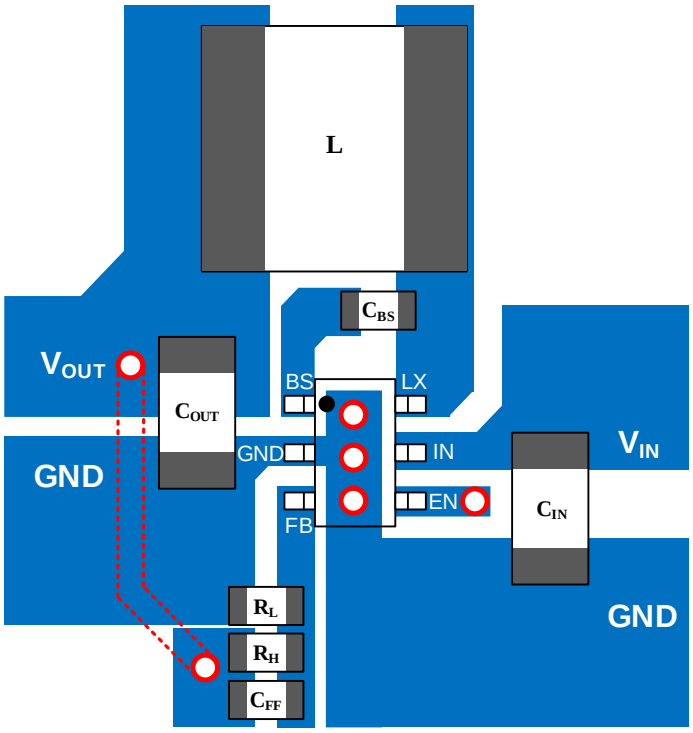
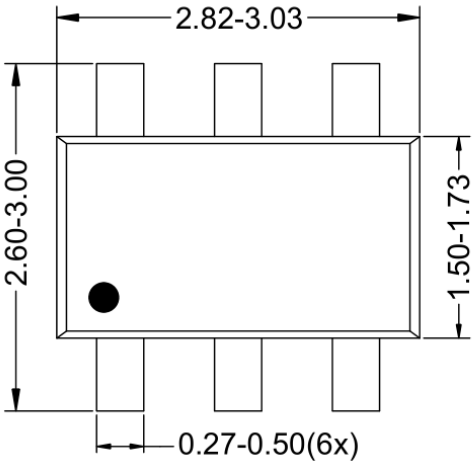
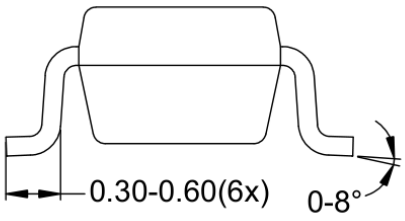


Figure9. Suggested PCB Layout

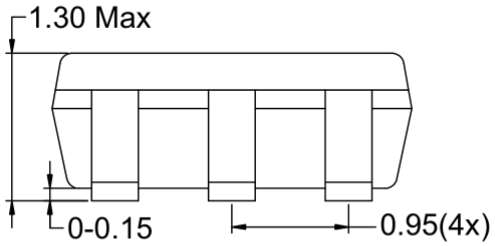
SOT23-6 Package Outline and PCB Layout



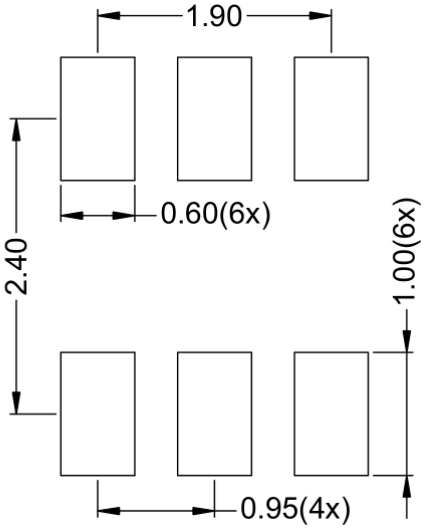
Top View



Side View



Front View



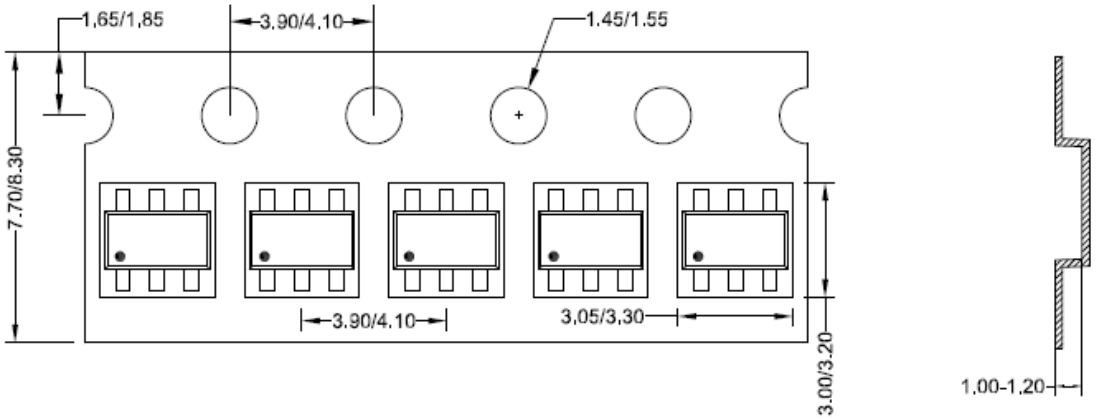
Recommended PCB Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Information

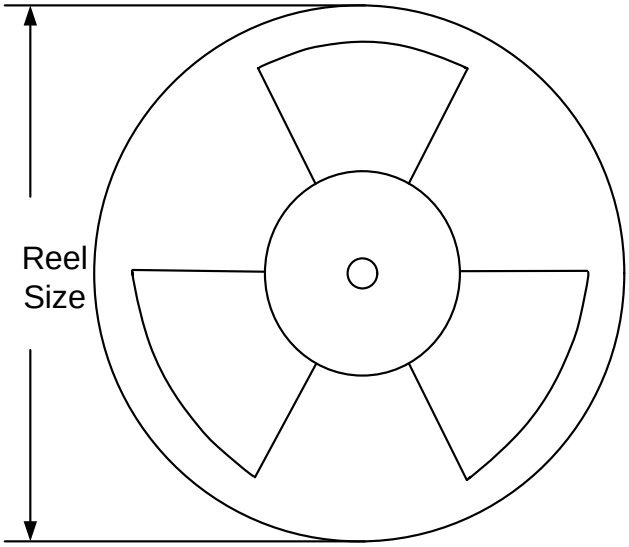
1. Tape dimensions and pin 1 orientation

SOT23-6



Feeding direction ⟶

2. Reel dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7	400	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Jan.21, 2024	1.0	Initial Release	-
July 02, 2024	1.0A	Add SY81102 spec	-
Dec.13, 2024	1.0B	Add SY81102C and SY81102B	-

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