SY26168/SY26169

High Efficiency, 12A, 16V Input Synchronous Step-Down Regulator

General Description

The SY26168 and SY26169 are high efficiency synchronous step-down DC-DC regulators that feature internal power and synchronous rectifier switches, and are capable of delivering 12A continuous output current over a wide input voltage range from 2.7V to 16V. The output voltage is adjustable: SY26168 from 0.9V to 5.5V and SY26169 from 0.6V to 5.5V.

Silergy's proprietary Instant-PWM™ fast-response, constant on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within approximately 100ns while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low ESR ceramic output capacitors.

The stable internal reference (V_{REF}) provides ±1% accuracy over T_J = -40°C to 125°C, and the differential input sense configuration allows the feedback sensing at the most relevant load point.

Internal 13.3mΩ power and 3.8mΩ synchronous rectifier switches provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input undervoltage lockout, internal soft-start, output undervoltage (UVP) and overvoltage (OVP) protection, and thermal shutdown provide safe operation in all operating conditions.

The SY26168 and SY26169 is available in a compact QFN3×4 package.

Features

- Wide Input Voltage Range:
  - 2.7V to 16V if VCC is Supplied by External Source
  - 3.6V to 16V if VCC is Supplied by Internal LDO
- Internal 13.3 mΩ Power Switch and 3.8mΩ Synchronous Rectifier
- Accurate Feedback Setpoint: ±1% from -40°C to 125°C
- Remote Sensing at Point of Load Side
- Ultra-Fast Load Transient Response
- Selectable 600kHz, 800kHz, and 1000kHz Switching Frequency
- Selectable Automatic High Efficiency Discontinuous Operating Mode at Light Loads
- Programmable Valley Current Limit
- Reliable Built-In Protections:
  - Automatic Recovery for Input Undervoltage (UVLO)
  - SY26168 Latch-Off， SY26169 Automatic Recovery for Output Undervoltage (UVP) and Overtemperature (OTP) Conditions
  - SY26168 Latch-Off Mode, SY26169 Hiccup Mode after 32 Consecutive Cycles Valley Current Limit Protection
  - Latch-Off for Output Overvoltage Condition(OVP)
  - Cycle-by-Cycle Reverse, Valley, and Peak Current Limit (OCP)
- Internal and Adjustable Soft-Start to Limit Inrush Current
- Smooth Startup with Pre-Biased VOUT
- Output Voltage Tracking
- Output Sinking Mode
- Power-Good Output Monitor for Undervoltage and Overvoltage

Applications

- Telecom and Networking Systems
- Servers
- High Power Access Points
- Storage Systems
- Cellular Base Station

Typical Application

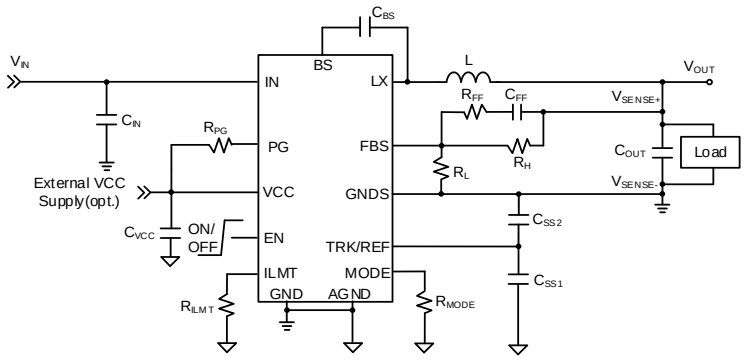


Figure 1. Typical Application Circuit

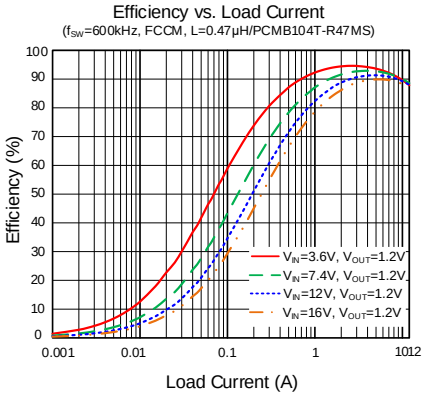


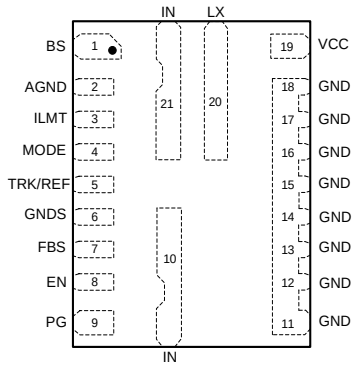
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY26168TXQ	QFN3×4-21 RoHS-Compliant and Halogen-Free	**GBR***xyz*
SY26169TXQ		**GRY***xyz*

x = year code, y = week code, z = lot number code

Pinout (top view)



Device Option

Part Number	V_{REF}	OCP/UVP	OTP	OVP
SY26168TXQ	0.9V	Latch-off	Latch-off	Latch-off
SY26169TXQ	0.6V	Hiccup	Auto-recovery	Latch-off

Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap supply for the high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pins.
2	AGND	Analog ground.
3	ILMT	Synchronous rectifier current limit setting. Connect a resistor to AGND to set the inductor valley current limit value.
4	MODE	Operation mode selection. Program MODE to select FCCM/PFM, and the operating switching frequency. See Table 1.
5	TRK/REF	External tracking voltage input. The FBS voltage tracks this input signal. Optionally adjust the soft-start time by adding an appropriate external capacitor between this pin and the AGND pin, and between this pin and the GNDS pin, respectively.
6	GNDS	Remote ground sense. Connect this pin directly to the negative side of the preferred voltage sense point. Connect to GND if remote sense is not used.
7	FBS	Remote feedback sense. Connect this pin to the center point of the output resistor divider to program the output voltage. See Design Procedure.
8	EN	Enable input. Pull low to disable the device; pull high to enable. Do not leave this pin floating. May be used for increasing startup voltage or sequencing. See Detailed Description.
9	PG	Power-Good indicator. Open-drain output when the output voltage is within 92.5% to 116% of the regulation setpoint.
10, 21	IN	Power input. Decouple this pin to GND pin with at least a 20μF ceramic capacitor.
11, 12, 13, 14, 15, 16, 17, 18	GND	Power ground .
19	VCC	Internal 3V LDO output. Power supply for internal analog circuits and driving circuits. Decouple this pin to GND with at least a 1μF ceramic capacitor. Use short, direct connections and avoid the use of vias. May be driven by an external bias supply. See Detailed Description.
20	LX	Inductor pin. Connect this pin to the switching node of the inductor.

Block Diagram

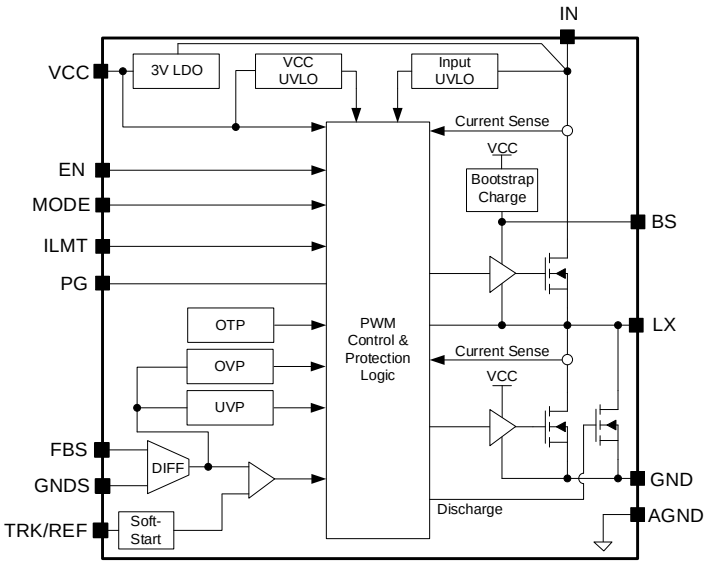


Figure 3. Block Diagram

Absolute Maximum Ratings

Absolute Maximum Ratings (Note 1)	Min	Max	Unit
IN	-0.3	18	V
EN, LX	-0.3	IN + 0.3	
LX, 10ns duration	-5	IN + 5	
BS	LX - 0.3	LX + 4	
FBS, GNDS, AGND, VCC, PG, ILMT, TRK/REF, MODE	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	±2000		V
ESD: CDM (Charged Device Model)	±500		

Thermal Information

Thermal Information (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	25	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5	
P_D Power Dissipation T_A = 25°C	4	W

Recommended Operating Conditions

Recommended Operating Conditions (Note 3)	Min	Max	Unit
IN	2.7	16	V
Output Voltage, SY26168	0.9	5.5	
Output Voltage, SY26169	0.6	5.5	
GNDS, AGND	-0.2	0.2	
VCC External Bias (Note6)	3.13	3.6	
Output Current		12	A
Output Current Limit Setting		14	
Peak Inductor Current		18	
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified (Note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.7		16	V
	UVLO, Rising	$V_{IN,UVLO}$		2.1	2.4	2.7	
	UVLO, Hysteresis	$V_{IN,HYS}$			550		mV
	Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		4	10	µA
	Quiescent Current	I_Q	V_{EN} = 2V, V_{FBS} = 105% V_{REF}, PFM mode, not switching		650		
VCC	UVLO, Rising	$V_{VCC,UVLO}$		2.65	2.8	2.95	V
	UVLO, Hysteresis	$V_{VCC,HYS}$			300		mV
	Output	V_{CC}	I_{VCC} = 0mA	2.88	3	3.12	V
	Load Regulation	$V_{CC,REG}$	I_{VCC} = 25mA		0.5		%
FBS	Reference Voltage	V_{REF}	GNDS = 0V,T_J = -40˚C–125˚C SY26168	0.891	0.900	0.909	V
			GNDS = 0V,T_J = 0˚C–70˚C SY26168	0.895	0.900	0.905	
			GNDS = 0V,T_J = -40˚C–125˚C SY26169	0.594	0.600	0.606	
			GNDS = 0V,T_J = 0˚C–70˚C SY26169	0.597	0.600	0.603	
	Error Amp Offset	V_{OS}		-3	0	3	mV
	Input Current	I_{FBS}	V_{EN} = 2V, V_{FBS} = 1V		50	100	nA
Power Switch	On-Resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3V, T_J = 25°C		13.3		mΩ
	Leakage	$I_{HS,\ LKG}$	V_{EN} = 0V, V_{LX} = 0V		0	10	µA
	Current Limit	$I_{LMT,HS}$		20			A
Synchronous Rectifier	On-Resistance	$R_{DS(ON)LS}$	V_{CC} = 3V, T_J = 25°C		3.8		mΩ
	Leakage	$I_{LS,\ LKG}$	V_{EN} = 0V, V_{LX} = 12V		0	30	µA
	Reverse Current	$I_{LMT,RVS}$			-9		A
I_{LMT} Pin Output Voltage		V_{ILMT}		0.77	0.8	0.83	V
I_{LMT} Ratio		$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ > 5A	12	13.3	14.6	µA/A
Discharge MOSFET Resistance		R_{DIS}			80	180	Ω
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.17	1.22	1.27	V
	Threshold Hysteresis	$V_{EN,HYS}$			0.2		
	Input Current	I_{EN}	V_{EN} = 2V		0		µA
Soft-Start (SS)	Charging Current	I_{SS1}	V_{SS} = 0V		42		
	Discharge Current	I_{SS2}	V_{SS} = 1V		12		
	Minimum Soft-Start Time	$t_{SS,MIN}$	C_{SS} = 1nF, T_J = 25°C (Note 5), SY26168	1	1.5		ms
			C_{SS} = 1nF, T_J = 25°C (Note 5), SY26169	0.75	1		
Overvoltage Protection Threshold		V_{OVP}		112.5	115.5	118.5	%V_{FBS}
Undervoltage Protection	Threshold	V_{UVP}		45	50	55	
	Delay	$t_{UVP,DLY}$	(Note 5)		20		µs
UVP/OCP Hiccup On-Time		$t_{HICCUP,ON}$	C_{SS} = 1nF (Note 5)		3		ms
UVP/OCP Hiccup Off-Time		$t_{HICCUP,OFF}$			11		
Power-Good	Thresholds	V_{PG}	V_{FBS} falling, PG high to low	77	80	83	%V_{FBS}
			V_{FBS} rising, PG low to high	89.5	92.5	95.5	
			V_{FBS} rising, PG high to low	112.5	115.5	118.5	
	Delay	$t_{PG,R}$	Low to high (Note 5)	0.63	0.9	1.17	ms
Power-Good	Delay	$t_{PG,F}$	High to low (Note 5)		20		µs

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Output Low Voltage	$V_{PG,LOW}$	V_{IN} = 0V, 100kΩ from PG to 3.3V		650	800	mV
			V_{IN} = 0V, 10kΩ from PG to 3.3V		750	900	
			V_{EN} = 2V, V_{FBS} = 0V, I_{PG} = 10mA			0.5	V
	Output Low Leakage	$I_{PG,LKG}$	V_{PG} = 3.3V			3	μA
Switching Frequency		f_{SW}	R_{MODE} = 0Ω, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	480	600	720	kHz
			R_{MODE} = 30.1kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	680	800	920	
			R_{MODE} = 60.4kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V, T_J = 25°C	850	1000	1150	
Minimum On-Time		$t_{ON,MIN}$	I_{OUT} = 3A (Note 5)			50	ns
Minimum Off-Time		$t_{OFF,MIN}$	I_{OUT} = 3A (Note 5)			180	
Thermal Shutdown Temperature		T_{SD}	T_J rising (Note 5)		160		˚C
Thermal Shutdown Hysteresis		T_{HYS}	(Note 5)		30		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

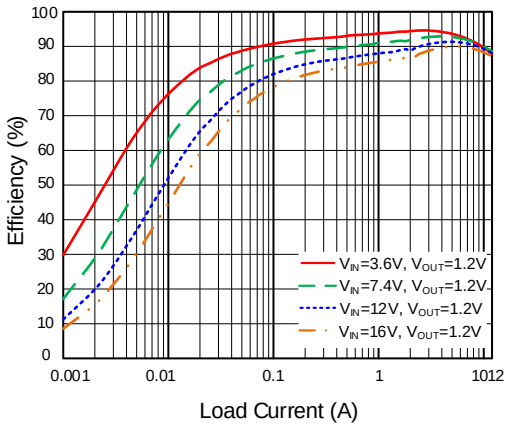
Note 5: Guaranteed by design or statistical correlation.

Note 6: VCC external bias voltage must be higher than VCC regulated voltage if the input voltage operates at 2.7V to 16V.

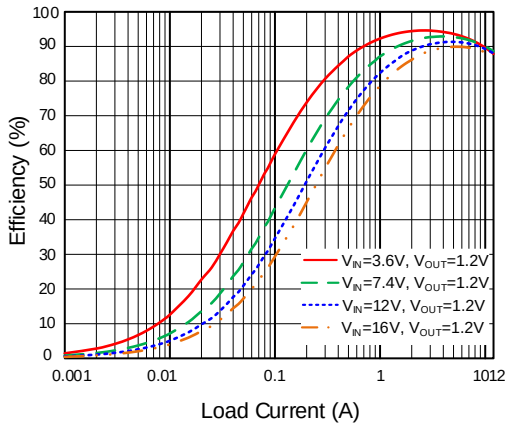
Typical Performance Characteristics

(SY26169, T_A = 25°C, V_{IN} = 12V, V_{OUT} = 1.2V, L = 0.47μH, C_{OUT} = 47μF×3, f_{SW} = 600kHz, R_{ILMT} = 4.5kΩ, C_{SS} = 0.2μF, unless otherwise noted)

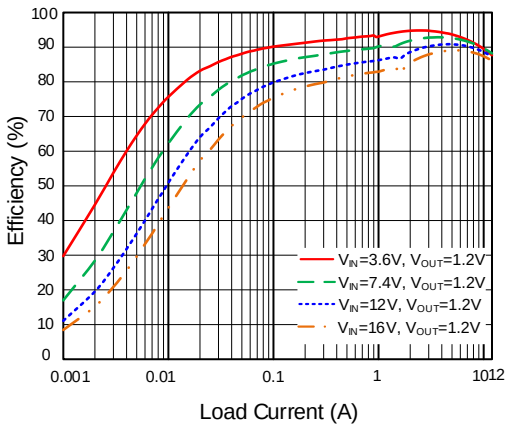
Efficiency vs. Load Current
(f_{SW}=600kHz, PFM, L=0.47μH/PCMB104T-R47MS)



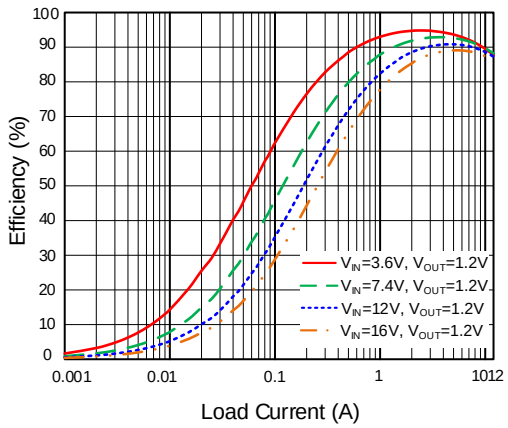
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



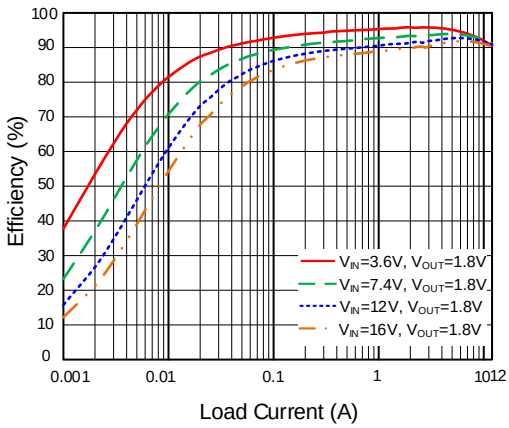
Efficiency vs. Load Current
(f_{SW}=800kHz, PFM, L=0.47μH/PCMB104T-R47MS)



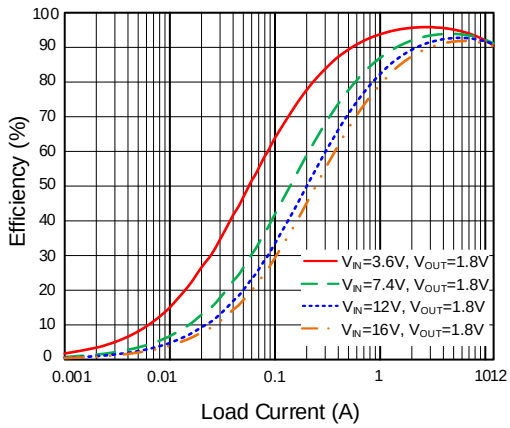
Efficiency vs. Load Current
(f_{SW}=800kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



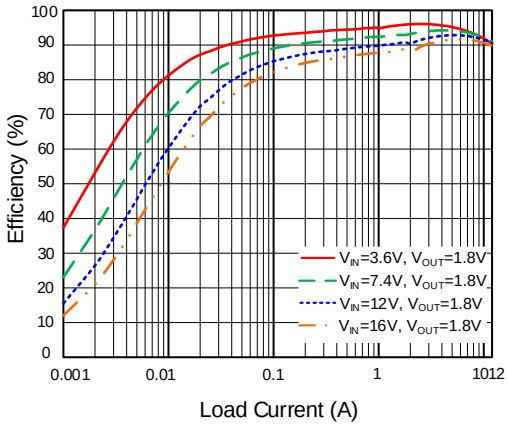
Efficiency vs. Load Current
(f_{SW}=600kHz, PFM, L=0.47μH/PCMB104T-R47MS)



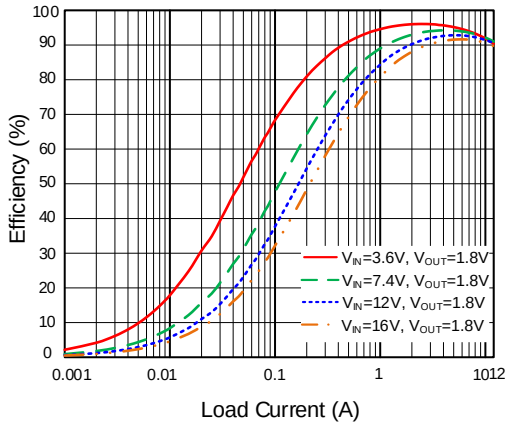
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



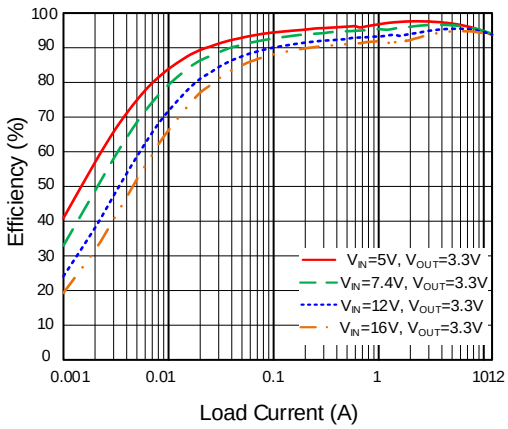
Efficiency vs. Load Current
(f_{SW}=800kHz, PFM, L=0.47μH/PCMB104T-R47MS)



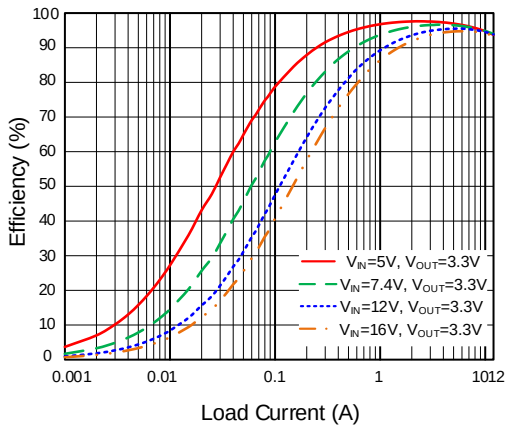
Efficiency vs. Load Current
(f_{SW}=800kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



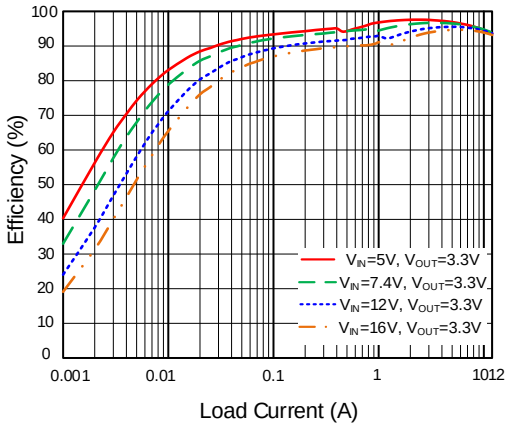
Efficiency vs. Load Current
(f_{SW}=600kHz, PFM, L=1.0μH/PCMB104T-1R0MS)



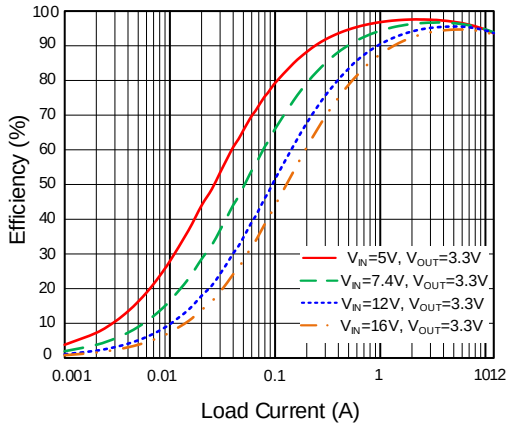
Efficiency vs. Load Current
(f_{SW}=600kHz,FCCM, L=1.0μH/PCMB104T-1R0MS)



Efficiency vs. Load Current
(f_{SW}=800kHz, PFM, L=1.0μH/PCMB104T-1R0MS)



Efficiency vs. Load Current
(f_{SW}=800kHz, FCCM, L=1.0μH/PCMB104T-1R0MS)



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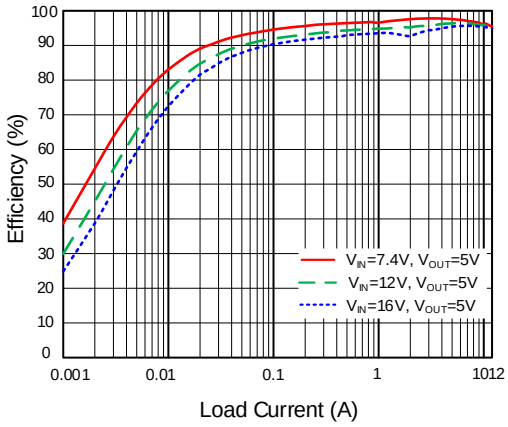
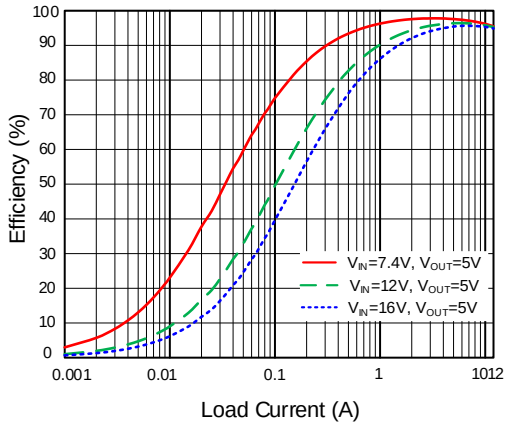
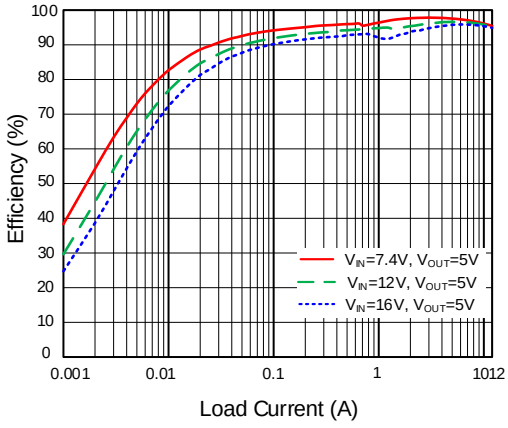
(f_{SW}=600kHz, PFM, L=1.0μH/PCMB104T-1R0MS)



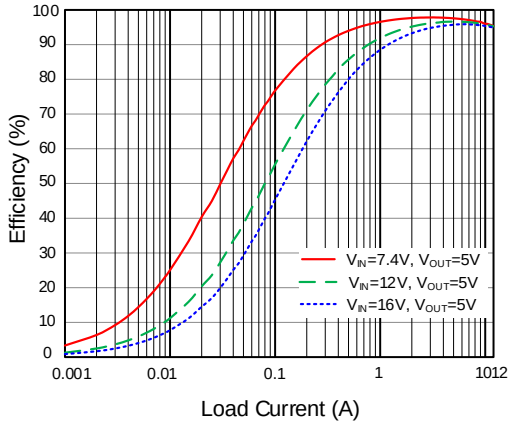
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=1.0μH/PCMB104T-1R0MS)



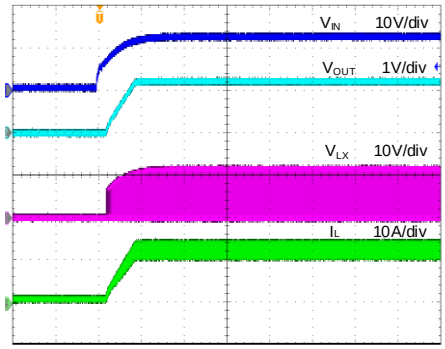
Efficiency vs. Load Current
(f_{SW}=800kHz, PFM, L=1.0μH/PCMB104T-1R0MS)



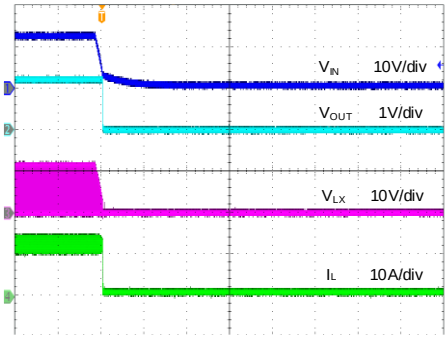
Efficiency vs. Load Current
(f_{SW}=800kHz, FCCM, L=1.0μH/PCMB104T-1R0MS)



Startup from V_{IN}
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)

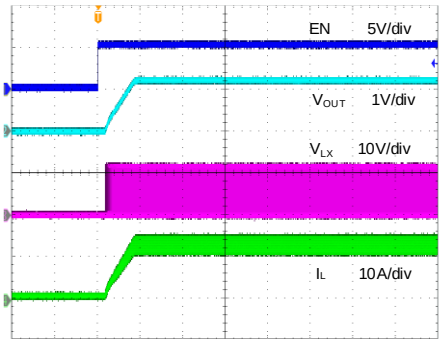


Shutdown from V_{IN}
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)



Startup from EN

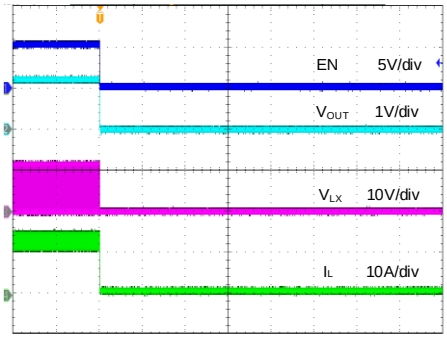
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=12A)



Time (4ms/div)

Shutdown from EN

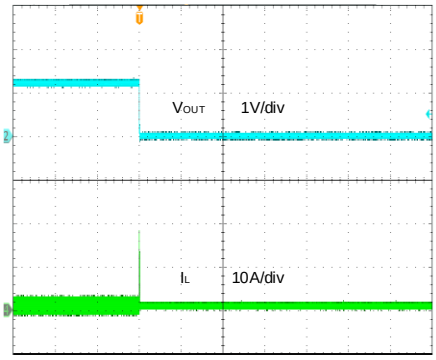
(V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=12A)



Time (4ms/div)

SY26168 Short Circuit Protection

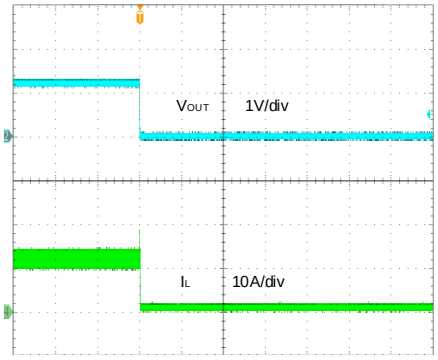
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=4.5kΩ, FCCM)



Time (10ms/div)

SY26168 Short Circuit Protection

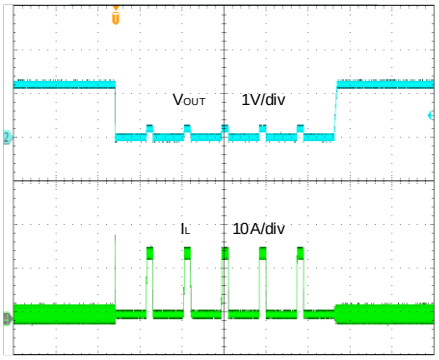
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A~short, R_{ILMT}=4.5kΩ, FCCM)



Time (10ms/div)

SY26169 Short Circuit Protection

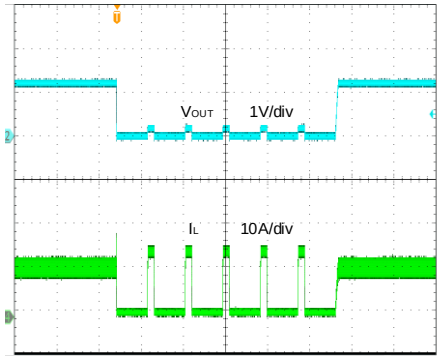
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=4.5kΩ, FCCM)



Time (20ms/div)

SY26169 Short Circuit Protection

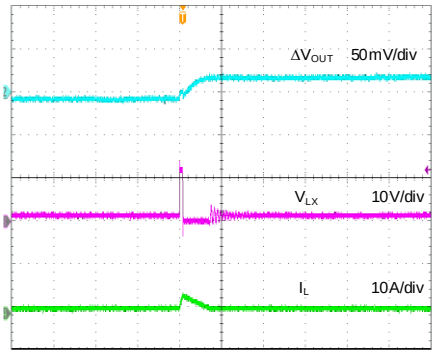
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A~short, R_{ILMT}=4.5kΩ, FCCM)



Time (20ms/div)

Output Ripple

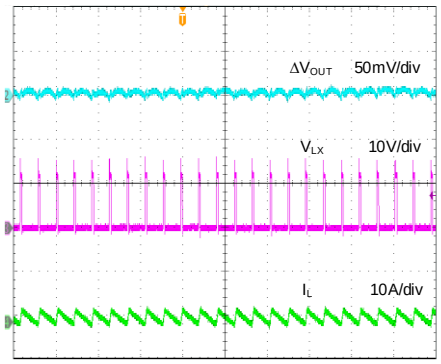
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, PFM)



Time (2μs/div)

Output Ripple

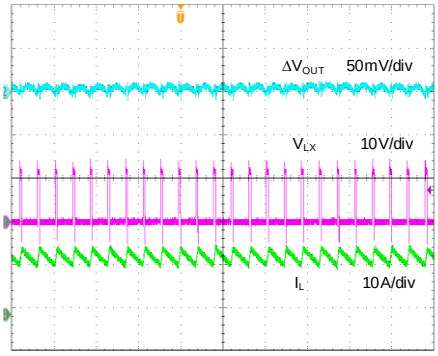
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, FCCM)



Time (4μs/div)

Output Ripple

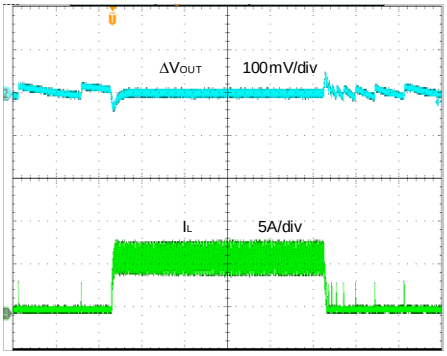
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)



Time (4μs/div)

Load Transient

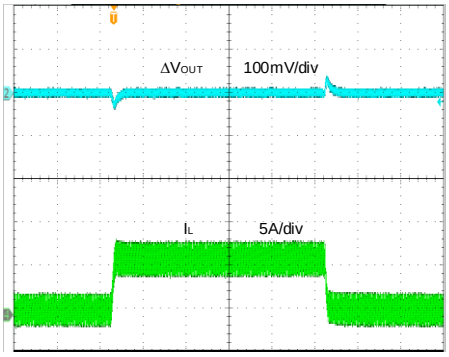
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0~6A, PFM)



Time (100μs/div)

Load Transient

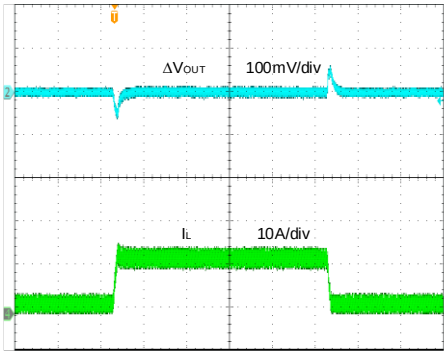
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0~6A, FCCM)



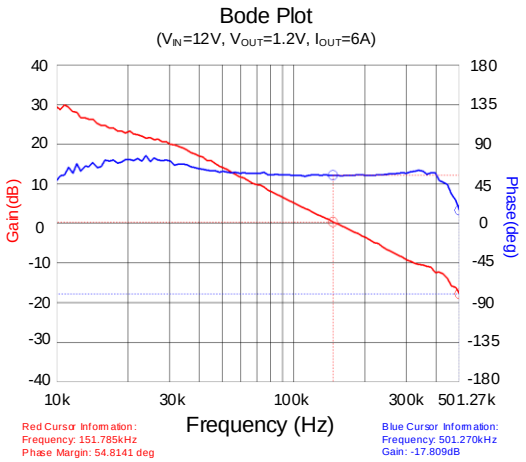
Time (100μs/div)

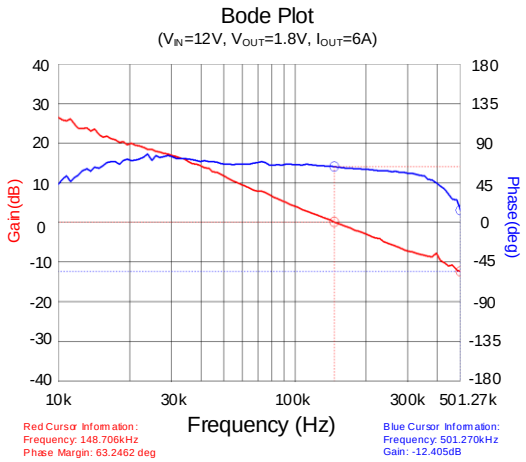
Load Transient

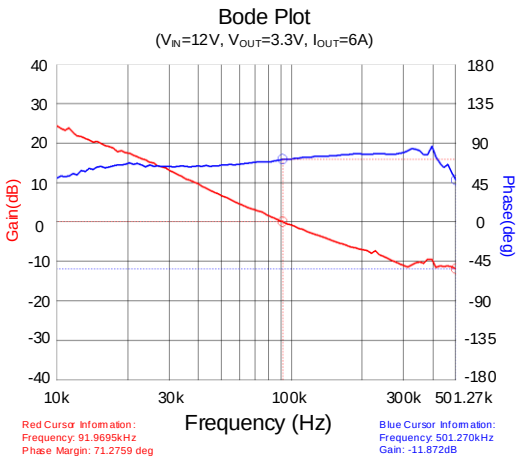
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=1.2~12A, FCCM)

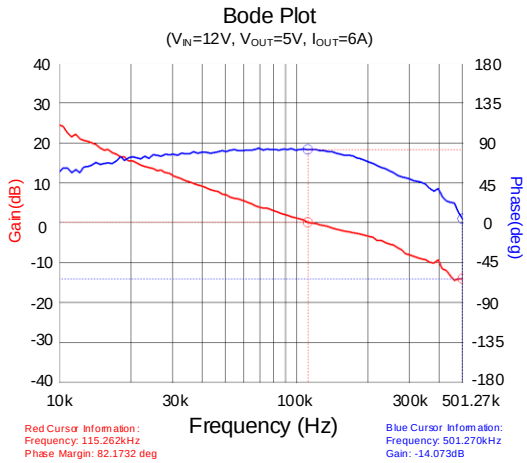


Time (100μs/div)









Detailed Description

Constant On-Time Architecture and Frequency Lock Loop (FLL)

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ratio, $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$. For example, considering that a hypothetical converter targets 1.2V output from a 10V input at 600kHz, the target on-time is (1.2V/10V) × (1/600kHz) = 200ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage measured at the FBS pin drops below the internal voltage reference value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in the COT control loop, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Conventional current-mode or voltage-mode control methods determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier based on current feedback, feedback voltage, internal ramps, and internal compensation signals, so these must all be monitored. These small signals are difficult to observe in a noisy switching environment immediately after switching large currents, which makes such architectures difficult to use.

Once the on-time calculated by the constant on-time architecture deviates from the accurate on-time value, especially in the case of low duty cycle operation, the actual switching frequency will deviate significantly from the setting value. When the load is close to full load, the duty cycle loss will also cause switching frequency deviation. In order to keep the switching frequency relatively constant under different application conditions, the constant on-time architecture needs a frequency lock loop (FLL). In the FLL, the reference frequency is a fixed clock, keeps the same as the setting frequency, and the switching frequency is compared with it cycle by cycle. This loop will adjust the actual on-time, let the switching frequency follow the reference frequency until there is no deviation between them. The FLL function is disabled during soft-start and discontinuous current mode (DCM) condition. Before soft-start is done, the CCM switching frequency is equal to an initial frequency that is slightly lower than the reference frequency.

Instant-PWM Operation

Silergy's Instant-PWM control method adds several proprietary improvements to the traditional COT architecture. First, whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, the Instant-PWM control method derives this signal internally.

Additionally, it optimizes operation with low-ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, Instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current measured flowing through the low-side synchronous rectifier is lower than the bottom FET current limit. When the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. The inductor current then ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on, and the inductor current ramps down linearly.

This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling of the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that transient t_{ON} can be retriggered with minimal delay during high-speed load, allowing the inductor current to ramp quickly and provide sufficient energy to the load.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch turn-off and the low-side synchronous rectifier on-period or the low-side synchronous rectifier turn-off and the high-side power turn-on period.

Light Load Mode and Switching Frequency Selection

In pulse frequency modulation (PFM) or forced continuous conduction mode (FCCM), light load operation mode and switching frequency are both selected by the MODE pin, as shown in Table 1. Once the light load mode and switching frequency are selected after VCC setup, they will be locked until the device shuts down.

Table 1. MODE Configuration

MODE Pin Connection	Light-Load Mode	Switching Frequency
VCC	PFM	600kHz
240kΩ(±20%) to AGND	PFM	800kHz
120kΩ(±20%) to AGND	PFM	1000kHz
AGND	FCCM	600kHz
30kΩ(±20%) to AGND	FCCM	800kHz
60kΩ(±20%) to AGND	FCCM	1000kHz

If PFM light load operation is selected, under light load conditions (typically $I_{OUT} < 0.5 \times \Delta I_L$), the current through the low side synchronous rectifier will ramp to near zero before the next t_{ON} time. When this occurs, the low side synchronous rectifier will turn off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, and the combined feedback and ramp signals remain much greater than the reference voltage, the Instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will correspondingly drop, further enhancing efficiency. The switching frequency can be lower than the audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The device enters CCM once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined as follows:

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_1}$$

If FCCM light load operation is selected, under light load conditions, the low side synchronous rectifier still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle. The device always operates under continuous conduction mode and keeps fairly constant switching frequency over the entire output current range.

Input Undervoltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches can be properly driven, Instant-PWM incorporates input undervoltage lockout protection. The device remains in a low current state and all switching actions are inhibited until V_{IN} exceeds the UVLO (rising) threshold. At that time, if EN is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} falls below $V_{IN,UVLO}$ minus the input UVLO hysteresis, switching actions will again be suppressed.

If the input UVLO threshold is low for some applications with a high input UVLO threshold requirement, use EN and two external divided resistors to adjust the input UVLO, as shown in Figure 4.

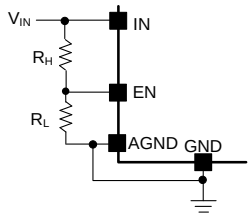


Figure 4. Enable Control

VCC Linear Regulator and VCC UVLO

The SY26168 and SY26169 integrates a high performance, low drop-out linear regulator for 3V VCC, supplied by input voltage, which can power the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 1µF low ESR ceramic capacitor from VCC to GND, as shown in Figure 5.

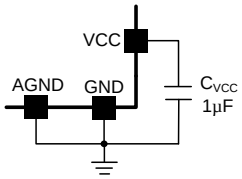


Figure 5. VCC Linear Regulator

Like input UVLO design, VCC also features UVLO protection. When the VCC voltage is lower than the VCC UVLO rising threshold minus VCC UVLO hysteresis, the device will shut down to ensure all internal circuitry logic is correct and the power and synchronous rectifier switches can be properly driven.

V_{CC} may also be used to apply an external 3.3V power source, if available. This external bias will allow device operation with V_{IN} as low as 2.7V.

Enable Control

The EN input is a high voltage capable input with logic-compatible threshold. The comparator design scheme makes the EN rising threshold comparatively accurate. When EN voltage rises to approximately 0.8V, VCC supplies the EN comparator. When EN is driven above 1.22V, normal device operation will be enabled, and the switching node pulse appears. When EN voltage falls below the EN rising threshold minus hysteresis, the switching node pulse is inhibited. When EN voltage is driven lower than 0.4V, the VCC will be shut down,

reducing input current to 4μA typ. (at normal temperature).

It is not recommended to connect EN and IN directly. A resistor of 1kΩ to 1MΩ should be used if EN is pulled high by IN.

Startup and Shutdown

The SY26168 and SY26169 incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately one soft-start time t_{SS}, which avoids high current flow and transients during startup. The startup and shutdown sequences are shown in Figure 6.

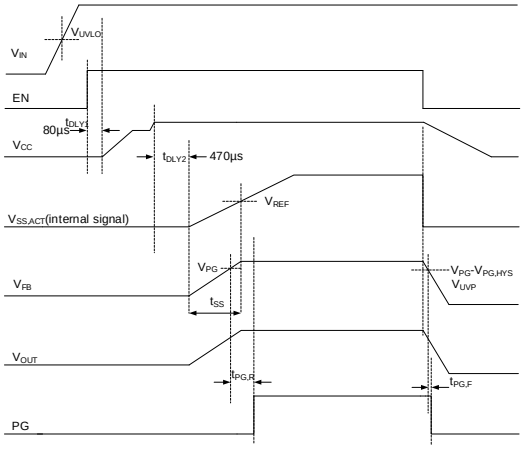


Figure 6. Startup and Shutdown Sequences

After the input voltage exceeds its own UVLO (rising) threshold and EN is enabled for a delay time t_{DLY1}, V_{CC} is turned on. The buck regulator is turned on after another delay time t_{DLY2} after V_{CC} voltage is set up. When the output voltage is 92.5% of the regulation point, PG becomes high impedance after a delay time $t_{PG,R}$.

Programmable Soft-Start Time and On-Time Pre-Bias

The soft-start time t_{SS} can be programmed using the TRK/REF pin. Connect a capacitor between the TRK/REF pin and AGND pins, and between the TRK/REF and GNDS pins to program the soft-start time. The soft-start time can be calculated as follows:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}}{I_{SS}(\mu A)}$$

The typical value of soft-start charging current I_{SS} is 42μA. To guarantee a sufficient programmable soft-start time when using a smaller soft-start capacitor, there is a minimum soft-start time t_{SS_MIN}, as shown in Table 2.

Table 2. Minimum Soft-Start Time

Part Number	Min Soft-Start Time (t_{SS_MIN})
SY26168TXQ	1.5ms
SY26169TXQ	1ms

If the output is pre-biased to a set voltage before start-up, the device disables the switching of both the high side power switch and the low side synchronous rectifier until the internal soft-start circuit voltage exceeds the sensed output voltage at the FBS node. Before the switching node pulse occurs, the switching node voltage is sampled to the internal on-time generator circuit to create on-time pre-bias. This is so that the first on-time will be matched with the current pre-bias output voltage.

Note that in the output voltage pre-biased scenario, if the BS-LX voltage is lower than 1.8V, the low side synchronous rectifier turns on to allow the BS voltage to be charged by VCC. The low side synchronous rectifier turns on for a very narrow pulse, so the drop in the pre-biased output level is negligible.

Output Voltage Tracking and Reference

The SY26168 and SY26169 can also be configured for tracking applications using the TRK/REF pin. When an external voltage signal is connected to TRK/REF, it acts as a reference for the SY26168 and SY26169 output voltage. The FBS voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.2V. During the initial start-up, the TRK/REF needs to exceed 600mV (SY26169) or 900mV (SY26168) initially to ensure proper operation. After that, it can be any value between 0.3V and 1.2V.

Differential Output Voltage Remote Sense Function

The SY26168 and SY26169 supports differential remote output voltage sensing. The dedicated GNDS pin helps provide remote GND voltage sensing, operating in conjunction with remote OUT voltage sensing to limit any decrease in remote load side voltage, even with load current as high as 12A. The remote sense trace pair should be kept at a low impedance to achieve the best performance.

Output Discharge Function

The SY26168 and SY26169 discharges the output voltage when the converter shuts down from V_{IN}, EN, or thermal shutdown so that output voltage can be discharged in minimal time, even if load current is zero. The discharge MOSFET in parallel with the low side synchronous rectifier turns on after the low side synchronous rectifier turns off when shut down logic is

triggered. The output discharge MOSFET $R_{DS(ON)}$ is typically 80Ω at room temperature. Note that the discharge MOSFET is not active beyond these shutdown conditions.

Buck Output Power-Good Indicator

The buck power-good (PG) indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FBS} is greater than $V_{PG,R}$ and less than V_{OVP} for at least the power-good delay time (low to high), PG will be high impedance.

PG should be connected to VCC or another voltage source less than 4V through a resistor (e.g.10kΩ–100kΩ). After V_{IN} exceeds its own UVLO (rising) threshold, the PG MOSFET is turned on so that PG is pulled to GND before the output voltage is ready. After feedback voltage V_{FBS} reaches $V_{PG,R}$, PG is pulled high (after a delay time within 900µs). If V_{FBS} drops to $V_{PG,F}$ or rises to V_{OVP} for an OVP delay time, PG is pulled low (after a delay time within 20µs).

The PG circuit is specifically designed so that when the PG connects to an external power source through 10kΩ–100kΩ, even if the input voltage is zero, the PG voltage maintains an output low voltage level.

External Bootstrap Capacitor Connection

The SY26168 and SY26169 integrates a floating power supply for the gate driver that operates the high side power switch. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the high side N-channel MOSFET power switch.

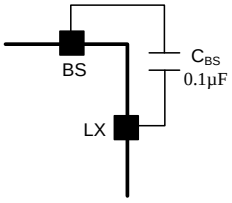


Figure 7. Bootstrap Capacitor Connection

Fault Protection

Programmable Valley Current Limit Protection

Instant-PWM incorporates a cycle-by-cycle "valley" current limit. Inductor current is measured in the low side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the bottom MOSFET current limit, t_{ON} is inhibited until the current returns to safe levels, as shown in Figure 8.

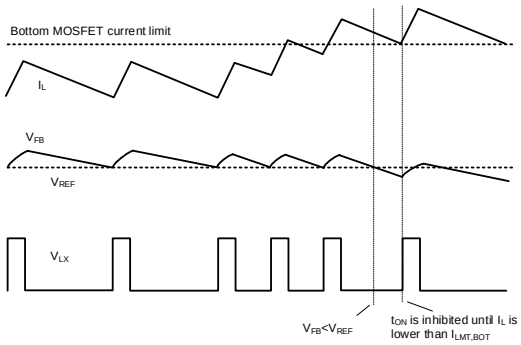


Figure 8. Valley-Current Limit

This limits the inductor current, and because the output current is higher, the output voltage naturally falls. Switching will resume once the inductor current is below the valley current limit.

The valley current limit value can be programmed using the ILMT pin. Connect a resistor between the ILMT and AGND pins to program the valley current limit value. The ILMT output voltage is constant, and the ILMT resistor current is sensed by the device and compared to the low side synchronous rectifier current mirror value. If the mirror current is larger than the ILMT resistor current, the device operates under valley current limit state and t_{ON} is inhibited. The valley current limit value is calculated as follows:

$$I_{LMT,BOT} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}}$$

where ILMT output voltage V_{ILMT} is 0.8V, and the low side synchronous rectifier mirror ratio G_{MIRROR} is 13.3µA/A typically.

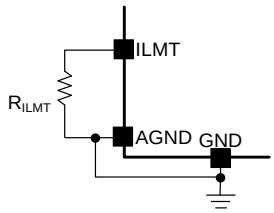


Figure 9. Valley-Current Limit

After startup, if the SY26168 and SY26169 detects 32 consecutive cycles of valley current limit protection, or detects one cycle of valley current limit protection when the FBS voltage drops below the undervoltage threshold, undervoltage protection will be triggered. The undervoltage protection method depends on the SY26168 and SY26169 variant, as follows:

- For the SY26168, the IC will shut down in the latch-off mode.
- For the SY26169, the switching will be disabled for a hiccup off-time. The device will then restart

with a complete soft-start cycle. If the fault condition remains after $t_{HICCUP,ON}$ this 'hiccup' cycle of startup and shutdown will continue unless the junction temperature exceeds T_{SD}. If the fault condition is resolved, the device will resume normal operation.

Peak Current Limit Protection

The device also features cycle-by-cycle "peak" current limit (top MOSFET current limit). During t_{ON} time, the high side power switch current is monitored. If the monitored current exceeds the top MOSFET current limit, the high side power switch is turned off, the low side synchronous rectifier is turned on, and t_{ON} is inhibited. t_{ON} will remain inhibited until the low side synchronous rectifier current is lower than the bottom MOSFET current limit value. Peak current limit protection has a blanking time at the initial on-time, in which the high side power switch current sample is disabled to make sampling noise shielding. Peak current limit protection priority is lower than minimum on-time.

Reverse Current Limit Protection

The SY26168 and SY26169 also features cycle-by-cycle "reverse" current limit. When the current is lower than the reverse current limit (-9A, typ.), the low side synchronous rectifier is turned off, and the high side power switch is turned on. At the initial off-time, low side synchronous rectifier current sample is disabled to make sampling noise shielding.

Output Sink Mode Protection (OSM)

The SY26168 and SY26169 includes output sinking mode. When the FBS voltage becomes higher than 106% of V_{REF}, the high side power switch turns off and the low side synchronous rectifier turns on. The low side synchronous rectifier then turns off and the high side power switch turns on again for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}. The IC repeats this operation until the FBS voltage is pulled lower than 106% of V_{REF}.

Output Undervoltage Protection (UVP)

If V_{OUT} is less than approximately 50% of the output voltage setpoint for approximately 20µs, occurring when the output is short-circuited or the load current is much heavier than the maximum current capacity, the output undervoltage protection (UVP) will be triggered. The undervoltage protection method depends on the SY26168 and SY26169 variant, as follows:

- For the SY26168, the IC will shut down in the latch-off mode.
- For the SY26169, the IC will enter into hiccup protection mode. The hiccup on-time is 3ms, and the hiccup off time is 11ms. If the output fault conditions are removed, the device will resume normal operation in the nearest hiccup on-time.

Output Overvoltage Protection (OVP)

The SY26168 and SY26169 includes overvoltage protection. When the FBS voltage exceeds 115.5% of V_{REF}, overvoltage protection will be triggered. The high side power switch is turned off and the low side synchronous rectifier is turned on until I_L reaches the reverse current limit (-9A). Then, the low side synchronous rectifier is turned off and the high side power switch is turned on again for the on-time determined by V_{IN}, V_{OUT}, and f_{SW}. The IC repeats this operation until the FBS voltage is pulled to less than 50% of V_{REF}, and the IC then shuts down in latch-off protection.

The device is re-enabled when EN or V_{IN} is cycled. When the FBS voltage drops below 50% of V_{REF}, the low side synchronous rectifier is turned off for PFM mode, and remains on for forced CCM operation. If FBS rises to more than 115.5% of V_{REF} again, the IC will repeat overvoltage protection. See the Inductor Selection section to determine proper inductor value. False OVP may occur under FCCM light load conditions if the chosen inductance is insufficient and reverse current limit protection is triggered.

Overtemperature Protection (OTP)

Instant-PWM includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds T_{SD} (160°C typ.), as shown in Figure 10. The overtemperature protection method then depends on the SY26168 and SY26169 variant:

- The SY26168 will remain in latch-off mode.
- The SY26169 will resume normal operation after a complete soft-start cycle, once the junction temperature cools down by the hysteresis value T_{HYS} (30°C typ.)

For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

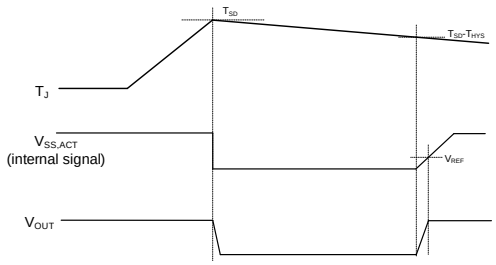


Figure 10. Overtemperature Protection(SY26169)

Application Information

Feedback Resistor Selection

Choose R_1 and R_2 to program the proper output voltage. A value between 1kΩ and 100kΩ is recommended for both resistors to minimize power consumption under light loads.

For SY26168, if V_{SET} is 1.2V and R_1 = 10kΩ, then R_2 can be calculated as 30kΩ using the following equation:

$$R_2 = \frac{0.9V}{V_{SET} - 0.9V} \times R_1$$

For SY26169, If V_{SET} is 1.2V and R_1 = 10kΩ, then R_2 can be calculated as 10kΩ using the following equation:

$$R_2 = \frac{0.6V}{V_{SET} - 0.6V} \times R_1$$

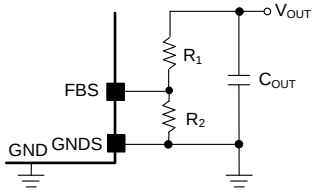


Figure 11. Feedback Resistor-Divider

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply, and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating greater than the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, two 22μF X5R capacitors are sufficient. Place the ceramic input capacitors as close to the device's IN and GND pins as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and will slow the transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$), and estimated ΔI_L as a percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low loss ferrite materials should be considered

Inductor Design Example

Consider a typical design for a device providing 1.2V_{OUT} at 12A from 12V_{IN}, operating at 600kHz and using target inductor ripple current (ΔI_L) of 50%, or 6A. Determine the approximate inductance value first:

$$L_1 = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 6A} = 0.3\mu H$$

Next, select the nearest standard inductance value, in this case 0.33µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 0.33\mu H} = 5.45A$$

$$I_{L,PEAK} = 12A + \frac{5.45A}{2} = 14.725A$$

The resulting 5.45A ripple current is 5.45A/12A, or approximately 45.4%, well within the 20%– 50% target.

$$I_{L,PEAK,RVS} = \frac{5.45A}{2} = 2.725A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 14.725A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). Include both when considering total ripple.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 5.45A using three 47µF ceramic capacitors, each with an ESR of approximately 5mΩ for a parallel total of 141µF and 1.7mΩ ESR.

$$V_{RIPPLE,ESR} = 5.45A \times 1.7m\Omega = 9.3mV$$

$$V_{RIPPLE,CAP} = \frac{5.45A}{8 \times 141\mu F \times 600kHz} = 8.1mV$$

Total ripple = 17.4mV

The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150µF 40mΩ POS capacitor, the result is as follows:

$$V_{RIPPLE,ESR} = 5.45A \times 40m\Omega = 218mV$$

$$V_{RIPPLE,CAP} = \frac{5.45A}{8 \times 150\mu F \times 600kHz} = 7.56mV$$

Total ripple = 225mV

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, but some considerations are still required, especially when using small ceramic capacitors. These capacitors have low capacitance, which results in insufficient stored energy for load transients. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate. ESR undershoot or overshoot may be calculated as V_{ESR} = ΔI_{OUT} × ESR. Using the ceramic capacitor example above and a fast load transient of ±6A,

$$V_{ESR} = \pm 6\text{A} \times 1.7\text{m}\Omega = \pm 10.2\text{mV}$$

The POS capacitor result with the same load transient is

$$V_{ESR} = \pm 6\text{A} \times 40\text{m}\Omega = \pm 240\text{mV}$$

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value, the input-output voltage difference, and the maximum duty factor. During a fast load transient, the maximum duty factor of Instant-PWM is a function of t_{ON} and the minimum t_{OFF}, as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated as

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 6A load increase using the ceramic capacitor case when V_{IN} = 12V. At V_{OUT} = 1.2V, the result is t_{ON} = 167ns, $t_{OFF,MIN}$ = 150ns, D_{MAX} = 167/(167 + 150) = 0.526 and

$$V_{UNDERSHOOT,CAP} = -\frac{0.33\mu H \times (6A)^2}{2 \times 141\mu F \times (12V \times 0.526 - 1.2V)} = -8.2mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{0.33\mu H \times (6A)^2}{2 \times 150\mu F \times (12V \times 0.526 - 1.2V)} = -7.7mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value, and the output voltage:

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 6A load decrease using the ceramic capacitor case above. At V_{OUT} = 1.2V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.33\mu H \times (6A)^2}{2 \times 141\mu F \times 1.2V} = 35.1mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{0.33\mu H \times (6A)^2}{2 \times 150\mu F \times 1.2V} = 33mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load Transient Considerations

The SY26168 and SY26169 uses the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC feed-forward compensation network R_{FF} and C_{FF} may further speed up the load transient responses. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increasing C_{FF} will speed up the load transient response if there is no stability issue.

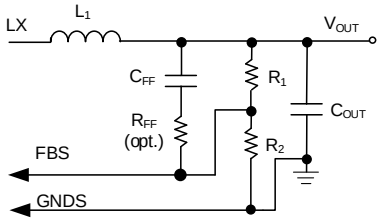


Figure 12. Feed-Forward Network

Note that when C_{OUT} > 500µF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF} > 2.2nF to provide sufficient ripple to FBS for small output ripple and good transient behavior.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as

$$P_{D,MAX} = \frac{(T_{J,MAX} - T_A)}{\theta_{JA}}$$

where $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction-to-ambient thermal resistance θ_{JA} is layout-dependent. For the QFN3×4-21 package, the thermal resistance θ_{JA} is 25°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz copper traces connected to each IC pin and very large, unbroken 1oz internal power and ground planes.

To meet the performance of the standard thermal test board in a typical small evaluation board area, wide copper traces are required to be well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board. A good thermal via from the exposed pad connecting to a wide middle-layer ground plane, and perhaps to an exposed copper area on the board's solder side, is also required.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (125℃ - 25℃)/(25℃/W) = 4W$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 13 to calculate the effect of rising ambient temperature on the maximum power dissipation.

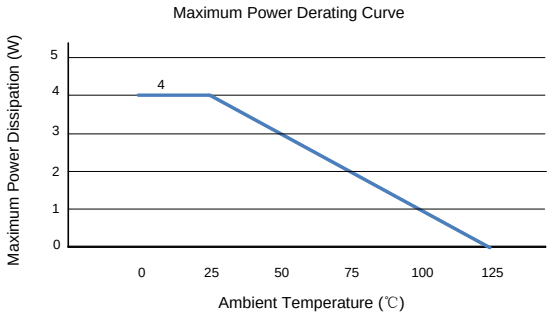


Figure 13. Maximum Power Dissipation

Application Schematic (V_{OUT} = 1.2V）

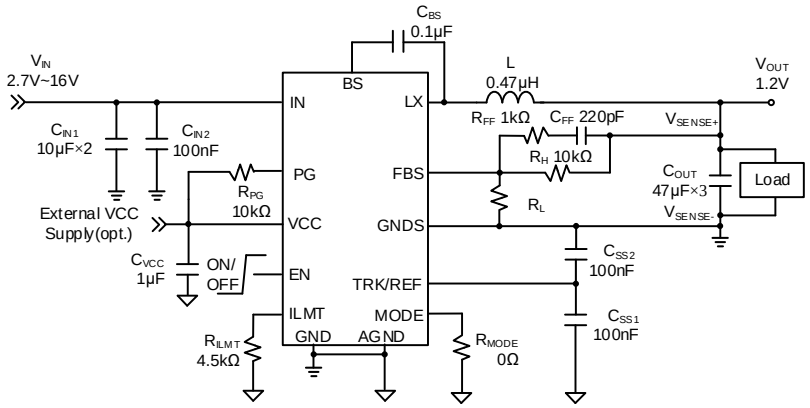


Figure 14. Application Schematic

BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	10μF/25V/X5R, 1206	GRM21BR61E106MA73L	Murata
C_{IN2}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	Murata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	Murata
C_{OUT}	47μF/6.3V/X5R, 1206	GRM31CR60J476KE19L	Murata
C_{SS1}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	Murata
C_{SS2}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	Murata
C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	Murata
C_{VCC}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	Murata
L	0.47μH, inductor	PCMB104T-R47MS	CYNTEC
R_H	10kΩ, 1%, 0603		
R_L,SY26168	30kΩ, 1%, 0603		
R_L,SY26169	10kΩ, 1%, 0603		
R_{PG}	10kΩ, 1%, 0603		
R_{MODE}	0Ω, 1%, 0603		
R_{ILMT}	4.5kΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		

Recommended Components Table for Typical Applications

V_{OUT} (V)	R_{MODE} (kΩ)	Frequency (kHz)	R_H (kΩ)	R_L (kΩ), SY26168	R_L (kΩ), SY26169	C_{FF} (pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	0	600,FCCM	10	30	10	220	0.47μH/(18A/20A)	47μFx3/6.3V/X5R,1206
1.8	0	600,FCCM	10	10	5	220	0.47μH/(18A/20A)	47μFx3/6.3V/X5R,1206
3.3	0	600,FCCM	10	3.75	2.2	220	1.0μH/(18A/20A)	47μFx3/6.3V/X5R,1206
5	0	600,FCCM	10	2.2	1.36	220	1.0μH/(18A/20A)	47μFx3/6.3V/X5R,1206

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

- Place the major MLCC capacitors (C_{IN}, C_{OUT}, C_{VCC}) on the same layer as the device.
- Place the input capacitors as close as possible to the IN and GND pins, minimizing the loop formed by these connections. To reduce parasitic inductance, avoid using direct vias in the power trace between the input capacitors and IN, GND pins.
- Place a smaller package input MLCC capacitor at the reach-out port of Pin 21. This capacitor can be connected with GND by vias.
- Place the VCC capacitor as close as possible to VCC using short, direct connections instead of vias connecting to device GND pins.
- Use a Kelvin connection between AGND and GND at the C_{VCC} negative sides.
- Place the feedback components (R_1, R_2, R_{FF} and C_{FF}) as close to the FBS pin as possible. Avoid routing the remote output sense line and remote GND sense (GNDS) line near LX, BS, or other high frequency signals, as they are noise sensitive.
- Use a Kelvin connection with C_{OUT} for the sampling point, rather than the inductor output terminal.
- Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between them for shielding, to prevent stray capacitive noise pickup.
- Place the BS capacitor on the same layer as the device; keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.
- It is not recommended to connect control signals and IN directly. A resistor of 1kΩ to 1MΩ should be used if they are pulled high by IN.
- Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Connect the exposed GND pad to a large copper area, and place several GND vias on it for heat sinking and to minimize noise.
- A four-layer layout is strongly recommended to achieve better thermal performance. For example, an 8.5cm × 8.5cm four-layer PCB with 2oz copper.
- Keep the high current traces (IN, GND, LX, and OUT trances) as short and wide as possible.
- Utilize the top and bottom layers for power IN and GND, making the copper plane as wide as possible. Dedicate the Middle 1 layer to GND layers for conducting heat and shielding, and the Middle 2 layer to the signal line from top-layer crosstalk. Place signal lines on the Middle 2 layer to prevent separating the top and bottom GND layers.

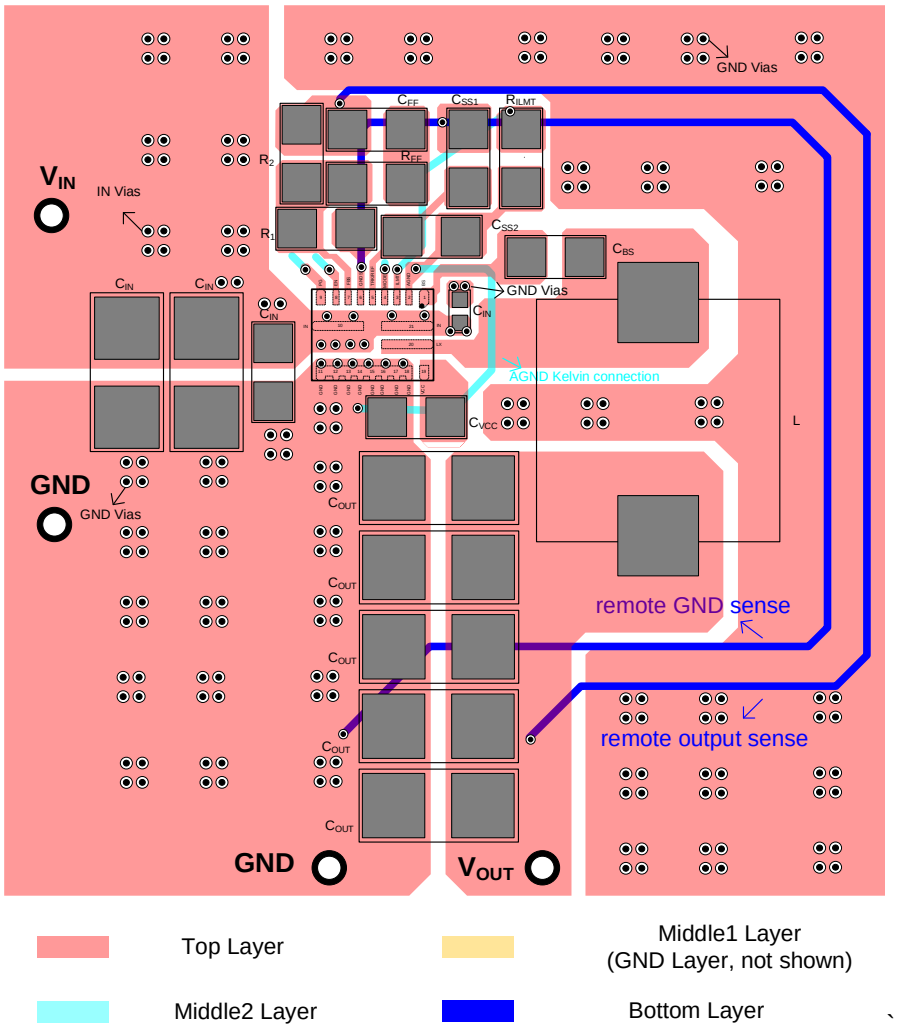
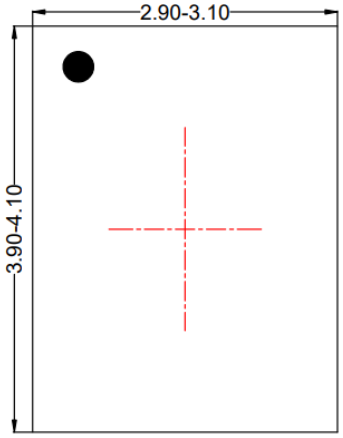
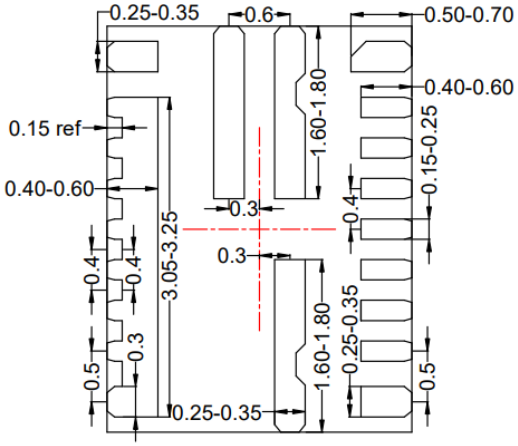


Figure 15. PCB Layout Suggestion

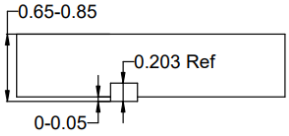
QFN3×4-21 Package Outline Drawing



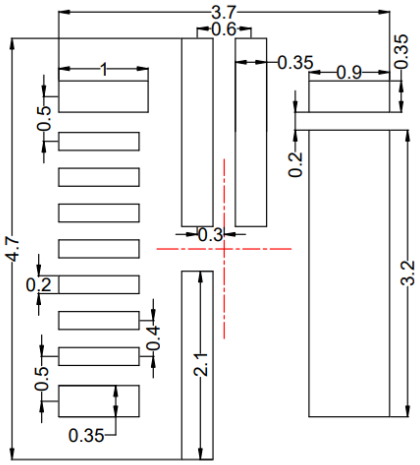
Top View



Bottom View



Front View



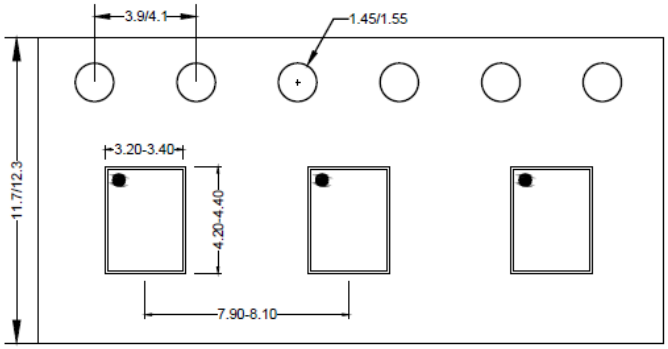
Recommended PCB layout
(Reference only)

Notes:

1. All dimensions are in millimeters and exclude mold flash and metal burr.
2. Center line refers to chip body center.

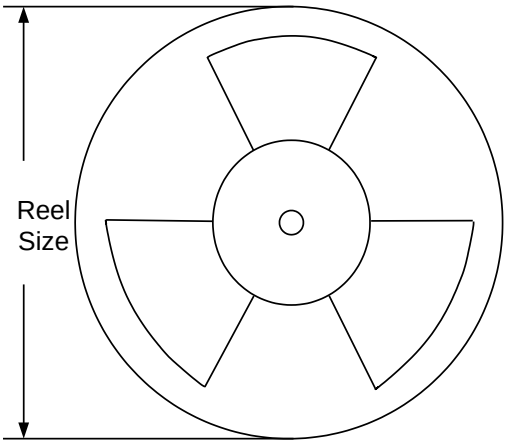
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Direction of feed →

Reel dimensions



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
May 28, 2024	1.0	Initial Release	-

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