SY21232

High Efficiency Fast Response, 98% Duty, 8A, 30V Input Synchronous Buck Converter

General Description

The SY21232 is a high efficiency synchronous buck converter operating over a wide input voltage range of 4.5V to 30V and capable of delivering up to 8A current. It integrates low $R_{DS(ON)}$ top and bottom MOSFETs to minimize the conduction loss. It operates at a pseudo-constant frequency of 500kHz, to enable the use of small size inductor and capacitors. The SY21232 also provides a bypass switch which allows the VCC to be powered by external 3.3V power supply, further reduce the power consumption of the entire system.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY21232 provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection to guarantee safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 20mΩ Top, 10mΩ Bottom
- Wide Input Voltage Range: 4.5V ~ 30V
- Adjustable Output Voltage: 0.6V ~ 24V
- High Duty Cycle Capable using On-Time Stretch
- 8A Continuous Output Current Capability
- 500kHz Pseudo-Constant Frequency
- ±1.5% 0.6V Reference under -40°C ~125°C
- Precise EN Threshold
- Internal 1ms Soft-Start Limits the Inrush Current
- Support Smooth Startup with Pre-Biased Output
- Constant On-time and Ripple-Based Control to Achieve Fast Transient Responses
- Selectable PFM/FCCM Light Load Operation by MODE Pin
- Power Good Indicator
- Optional BYP Input for Power Saving
- Output Auto-Discharge Function
- Selectable Peak and Valley Current Limit Threshold by MODE Pin
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2×3-14

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Monitor
- High Power AP

Typical Application

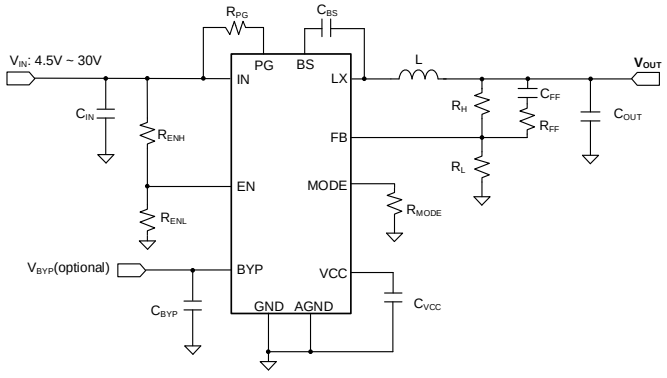


Figure1. Schematic Diagram

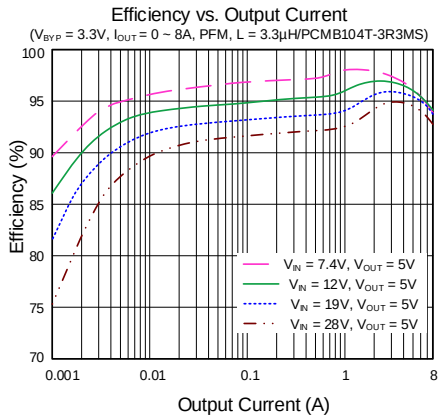


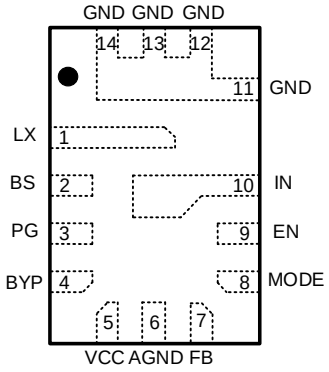
Figure2. Efficiency vs. Output Current

Ordering Information

Ordering Number	Package type	Top Mark
SY21232WYQ	QFN2×3-14 RoHS Compliant and Halogen Free	**FEGxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	LX	Inductor pin. Connect this pin to the switching node of the inductor.
2	BS	Bootstrap Pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
3	PG	Power good indicator pin. PG pin should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
4	BYP	External 3.3V bypass power supply input pin. Decouple this pin to the GND with a 1μF ceramic capacitor. Make one good RC filter for BYP input if the external power rail has significant ripple. Leave this pin floating or connect this pin to the GND if it is not used.
5	VCC	Internal 3.3V LDO output pin. Power supply for internal analog circuits. Decouple this pin to ground with at least a 2.2μF ceramic capacitor.
6	AGND	Analog ground pin.
7	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.
8	MODE	Operation mode selection pin. Program MODE to select FCCM/PFM, and the valley and peak current limit threshold. See table 1.
9	EN	Enable control pin of the device. Pull high to turn on. Pull low to turn off. Do not leave this pin floating.
10	IN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
11, 12, 13, 14	GND	Power ground pin.

MODE Pin Connection	Light Load Mode	Valley Current Limit Threshold	Peak Current Limit Threshold
VCC	PFM	6A	12A
240KΩ±15% to GND	PFM	8A	16A
GND	FCCM	6A	12A
30KΩ±15% to GND	FCCM	8A	16A

Table 1. MODE Selection

Block Diagram

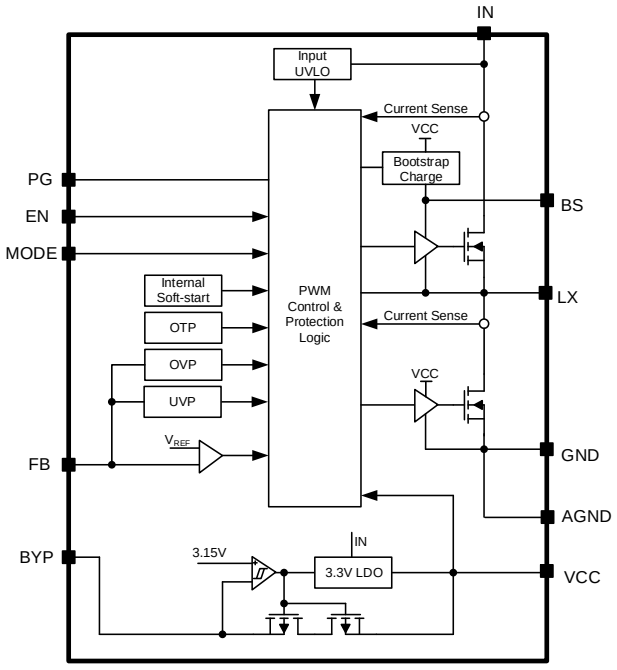


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	31	V
LX, PG, EN, MODE	-0.3	IN + 0.3	
BS-LX, VCC, BYP	-0.3	4	
FB	-0.3	6	
LX, 10ns Duration	GND - 5	IN + 3	
LX, 20ns Duration	GND - 1	IN + 2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	22	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	3	
P_D Power Dissipation T_A=25°C	4.5	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
Input Voltage	4.5	30	V
Output Voltage	0.6	24	
Continuous Output Current		8	A
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

Electrical Characteristics

(T_J = 25°C, V_{IN} = 12V, V_{OUT} = 5V, L = 3.3μH, C_{OUT} = 66μF, I_{OUT} = 1A, unless otherwise specified (Note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		4.5		30	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	V_{IN} rising			4.45	
	UVLO Hysteresis	$V_{IN,HYS}$			0.5		
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{EN} = 3V, V_{FB} = V_{REF} × 105%		120		μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		6	10	
Output	Voltage Range	V_{SET}		0.6		24	V
	Feedback Reference Voltage	V_{REF}	T_J = -40°C ~ 125°C	0.591	0.6	0.609	
	Discharge Current	I_{DIS}	V_{OUT} = 5V		80		mA
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET} (Note5)	0.7	1	1.3	ms
	Maximum Duty Cycle	D_{MAX}	Without inductor	98			%
	FB Input Current	I_{FB}	V_{FB} = 1V	-50		50	nA
	OVP Threshold	V_{OVP}	V_{FB} rising	115	120	125	%V_{REF}
	OVP Hysteresis	$V_{OVP,HYS}$			5		
	OVP Delay Time	$t_{OVP,DLY}$	(Note5)		70		μs
	UVP Threshold	V_{UVP}		45	50	55	%V_{REF}
	UVP Delay Time	$t_{UVP,DLY}$	(Note5)		50		μs
	UVP Hic-Cup On-Time	$t_{HICCUP,ON}$	(Note5)		3		ms
	UVP Hic-Cup Off-Time	$t_{HICCUP,OFF}$	(Note5)		9		
MOSFETs	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			20		mΩ
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			10		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP1}$	V_{MODE} = 0V or V_{CC}		12		A
		$I_{LMT,TOP2}$	R_{MODE} = 30kΩ or 240kΩ		16		
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT1}$	V_{MODE} = 0V or V_{CC}	6			
		$I_{LMT,BOT2}$	R_{MODE} = 30kΩ or 240kΩ	8			
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$		3	4	5	
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
	Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	
Frequency	Switching Frequency	f_{SW}	V_{OUT} = 5V, CCM	425	500	575	kHz
	Minimum On-Time	$t_{ON,MIN}$			50		ns
	Minimum Off-Time	$t_{OFF,MIN}$			100		
Power Good (PG)	Rising Threshold	$V_{PG,R}$	V_{FB} rising (good)	86	90	94	%V_{REF}
	Falling Threshold	$V_{PG,F}$	V_{FB} falling (not good)	81	85	89	
	Delay Time	$t_{PG,R}$	Low to high (Note5)		200		μs
		$t_{PG,F}$	High to low (Note5)		40		
	Low Voltage	$V_{PG,LOW}$	V_{FB} = 0V, I_{PG} = 5mA			0.4	V
VCC	Output Voltage	V_{CC}	VCC adds 1mA load	3.2	3.3	3.4	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
BYP	$R_{DS(ON)}$	$R_{DS(ON),BYP}$			5		Ω
	Turn On Voltage	V_{BYP}		3.05	3.15	3.25	V
	Turn On Hysteresis	$V_{BYP,HYS}$			0.2		
	OVP Voltage	$V_{BYP,OVP}$			120		$\%V_{CC}$
OTP	Temperature	T_{OTP}	(Note5)		150		°C
	Temperature Hysteresis	$T_{OTP,HYS}$	(Note5)		15		

Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

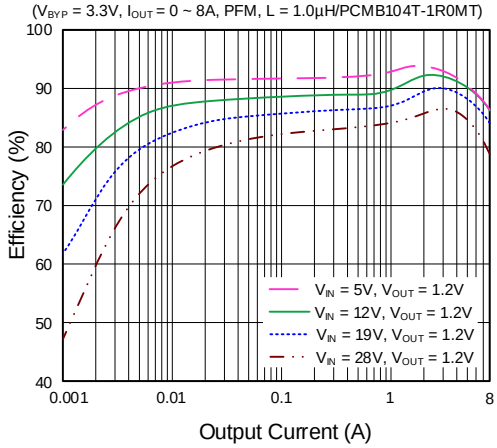
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design.

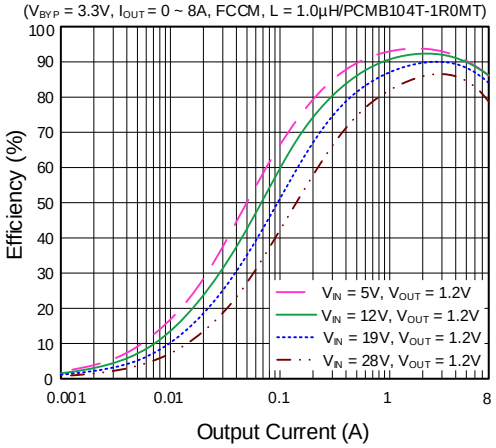
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 5V, L = 3.3µH, C_{OUT} = 66µF, C_{FF} = 220pF, R_{FF} = 1kΩ, unless otherwise noted)

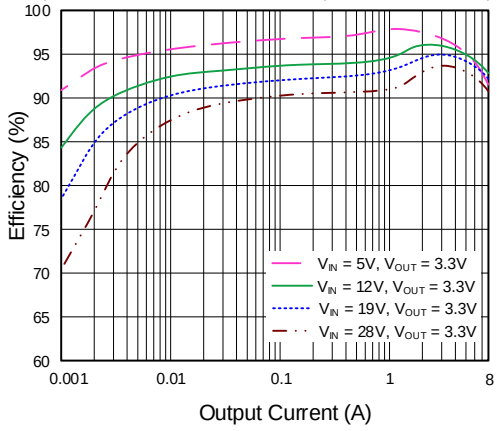
Efficiency vs. Output Current
(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, PFM, L = 1.0µH/PCMB104T-1R0MT)



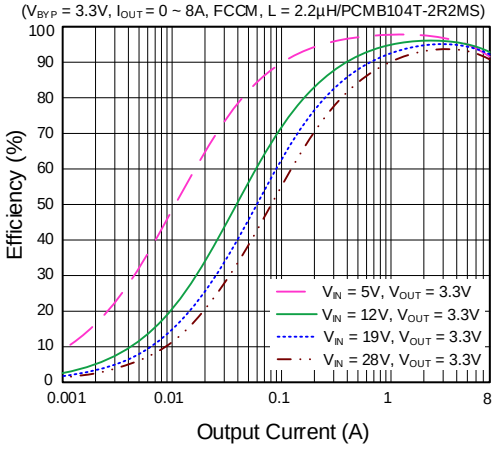
Efficiency vs. Output Current
(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, FCCM, L = 1.0µH/PCMB104T-1R0MT)



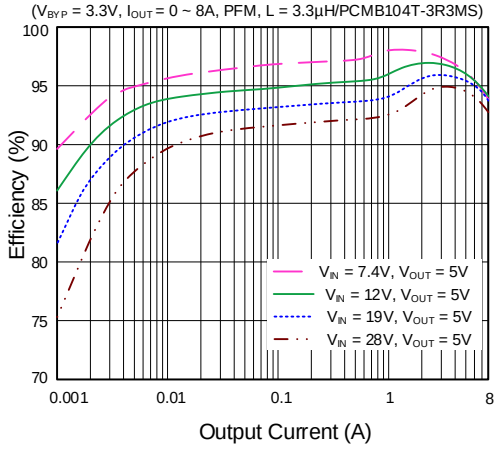
Efficiency vs. Output Current
(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, PFM, L = 2.2µH/PCMB104T-2R2MS)



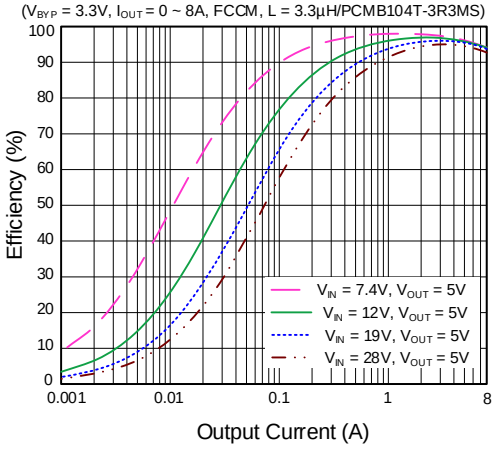
Efficiency vs. Output Current
(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, FCCM, L = 2.2µH/PCMB104T-2R2MS)



Efficiency vs. Output Current
(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, PFM, L = 3.3µH/PCMB104T-3R3MS)

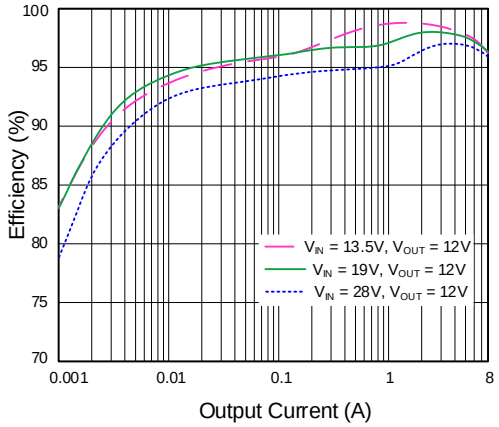


Efficiency vs. Output Current
(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, FCCM, L = 3.3µH/PCMB104T-3R3MS)



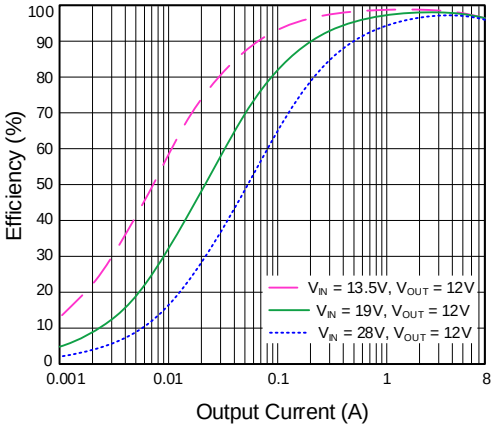
Efficiency vs. Output Current

(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, PFM, L = 4.7µH/PCMB104T-4R7MS)



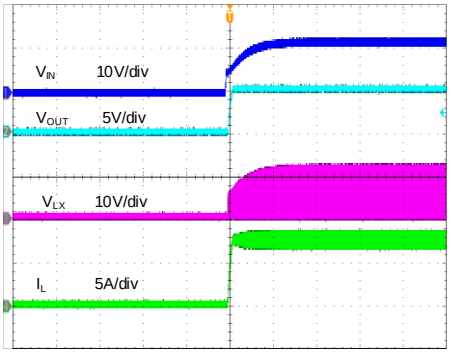
Efficiency vs. Output Current

(V_{BYP} = 3.3V, I_{OUT} = 0 ~ 8A, FCCM, L = 4.7µH/PCMB104T-4R7MS)



Startup from V_{IN}

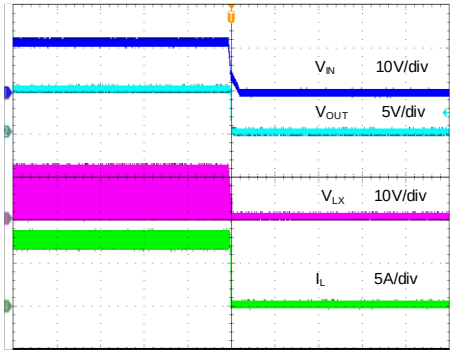
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (10ms/div)

Shutdown from V_{IN}

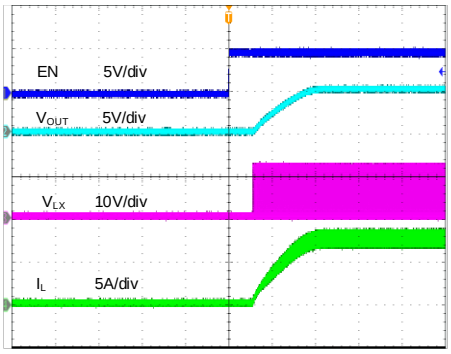
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (10ms/div)

Startup from EN

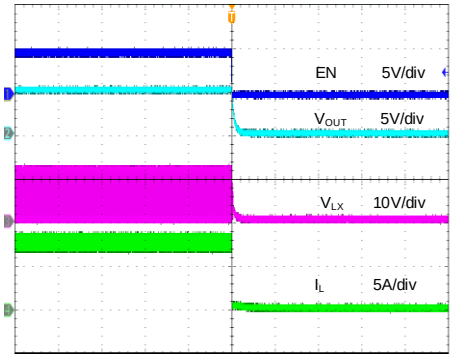
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (800µs/div)

Shutdown from EN

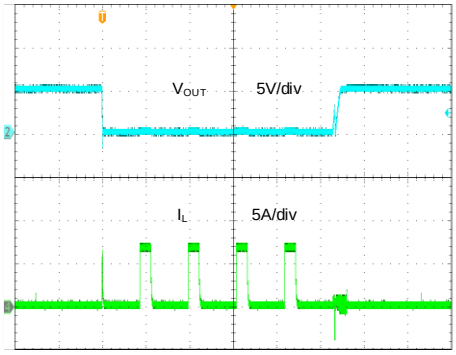
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (800µs/div)

Output Short Circuit Protection

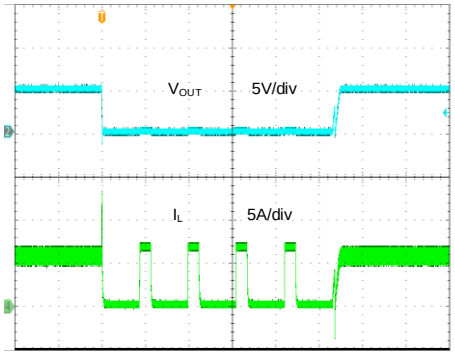
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A ~ Short, V_{MODE} = V_{CC})



Time (10ms/div)

Output Short Circuit Protection

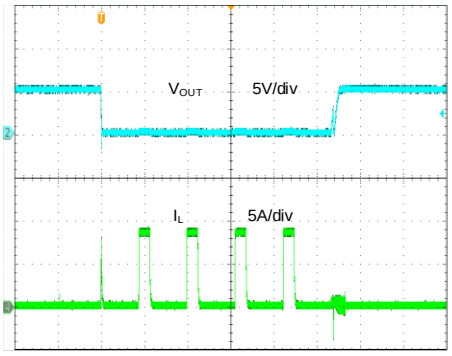
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A ~ Short, V_{MODE} = V_{CC})



Time (10ms/div)

Output Short Circuit Protection

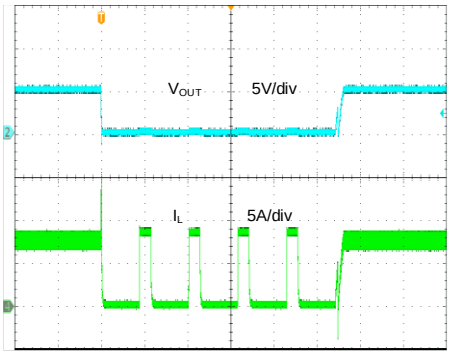
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A ~ Short, R_{MODE} = 240kΩ)



Time (10ms/div)

Output Short Circuit Protection

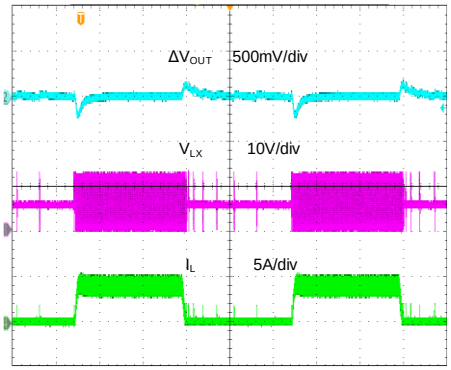
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A ~ Short, R_{MODE} = 240kΩ)



Time (10ms/div)

Load Transient

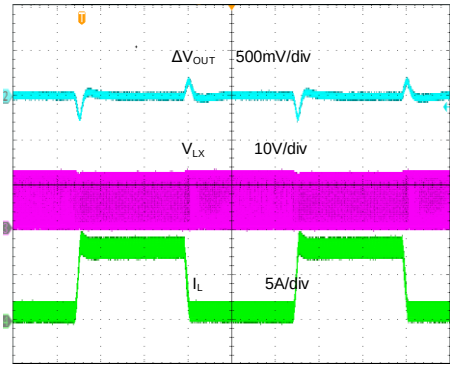
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0 ~ 4A, PFM)



Time (200μs/div)

Load Transient

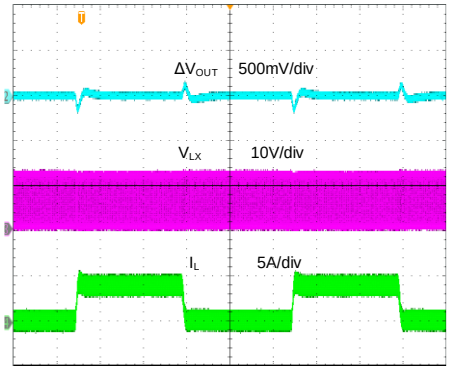
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.8 ~ 8A, PFM)



Time (200μs/div)

Load Transient

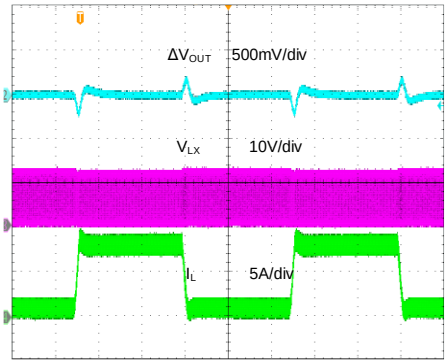
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0 ~ 4A, FCCM)



Time (200μs/div)

Load Transient

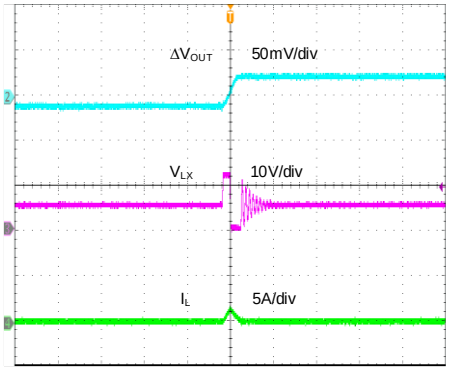
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.8 ~ 8A, FCCM)



Time (200μs/div)

Output Ripple

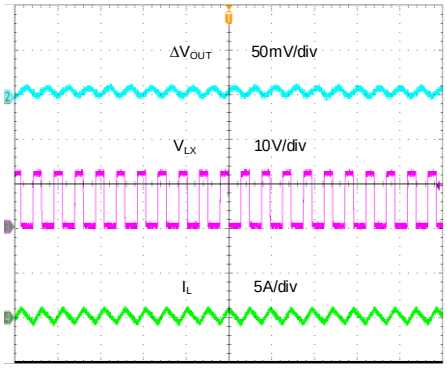
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, PFM)



Time (4μs/div)

Output Ripple

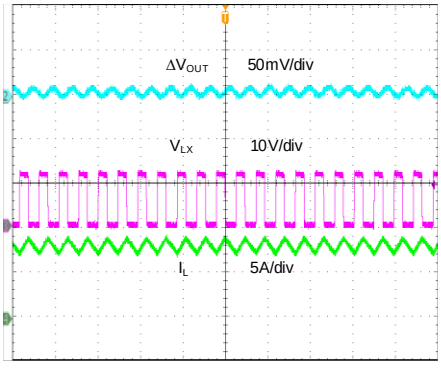
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, FCCM)



Time (4μs/div)

Output Ripple

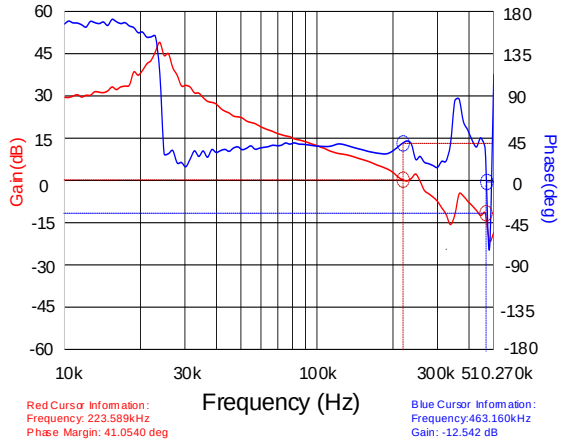
(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A)



Time (4μs/div)

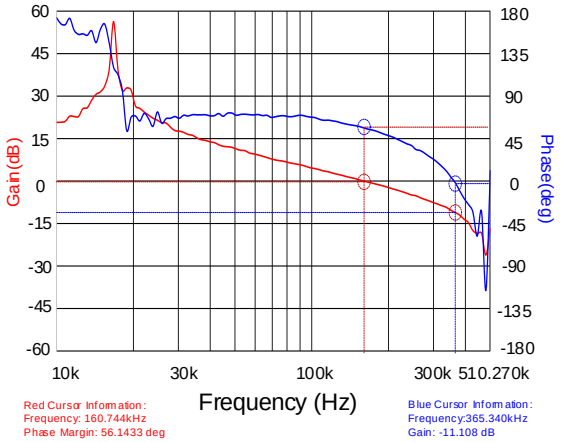
Bode Plot

(V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A, L = 1.0μH, FCCM)



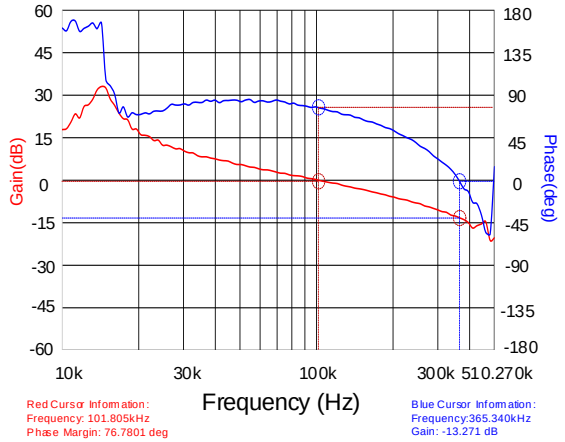
Bode Plot

(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A, L = 2.2μH, FCCM)



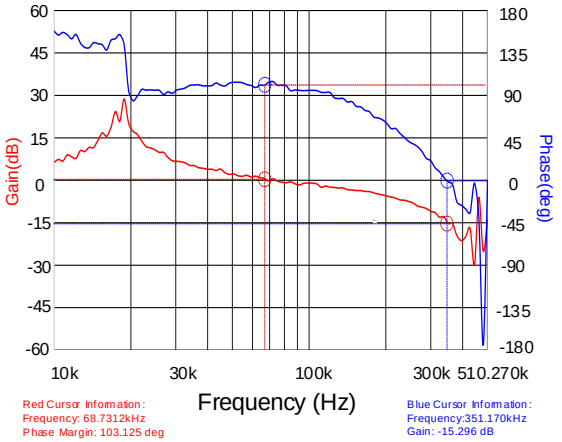
Bode Plot

(V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, L = 3.3μH, FCCM)



Bode Plot

(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 0A, L = 4.7μH, FCCM)



Detailed Description

General Features

Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time (t_{ON}) is a "fixed" voltage ratio,

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

For example, considering that a hypothetical converter targets 5V output from a 28V input at 500kHz, the target on-time is

$$\frac{5V}{28V} \times \frac{1}{500kHz} = 357.14ns$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

In order to convert output voltage under low input voltage operation, the t_{ON} can be stretched to extend the duty cycle as much as it needs. When the device detects feedback voltage is lower than the reference voltage under normal on-time operation and the duty cycle>27%, the t_{ON} will be stretched. The maximum on-time can be limited when the peak current limit actions or high side power switch drive voltage (BS-LX voltage) is below its UVLO voltage (~1.7V). The on-time stretch function is disabled when the duty cycle<20% or the feedback voltage is less than the under voltage protection (UVP) threshold. The device can support 98% open loop duty cycle if not consider duty loss caused by MOSFET $R_{DS(ON)}$ and inductor DCR. The device can also support 100% duty cycle operation if BS-LX voltage adds external >2.1V voltage source.

Instant-PWM Operation

Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the t_{ON} pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients, t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

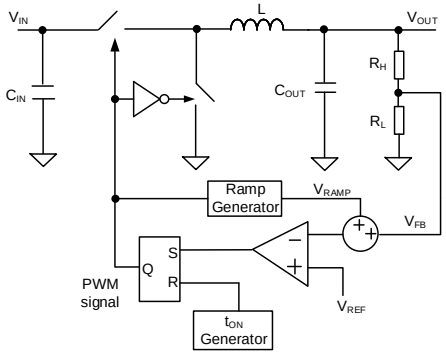


Figure4. Silergy's COT Ripple-based Control Strategy

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as wells as between turning the bottom MOSFET off and the top MOSFET on.

Light Load Operation Mode Selection

PFM or FCCM light load operation is selected using the MODE pin. The detailed MODE pin configuration is shown in the table 1.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \quad (1)$$

The current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

If FCCM light load operation is selected, under light load conditions, the bottom MOSFET still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle appears. The buck converter always operates under continuous conditions mode and keeps fairly constant switching frequency over all the output current range.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input undervoltage lockout protection.

The device remains in a low current state and LX node switching actions are inhibited until V_{IN} exceeds the UVLO rising threshold. At that time, if EN is high, the device is enabled and soft-start ramp is initiated. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX node switching actions will again be suppressed.

Precise EN Threshold

The EN pin uses precise rising and falling thresholds to provide programmable ON/OFF control. The device will be turned on when the EN pin voltage exceeds the rising threshold. The device will be turned off while the EN pin voltage falls below the falling threshold. Increasing the UVLO startup voltage threshold is possible using an external resistor divider as shown below:

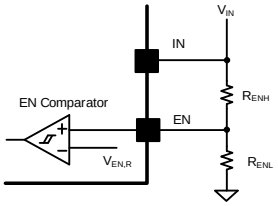


Figure5. Enable Control

It is not recommended to connect EN pin to the V_{IN} or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used for EN pin in this case.

Soft-Start and Startup with Pre-Biased Output

The device incorporates an internal soft-start circuit to ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup. The device operates in FCCM mode during soft-start no matter which mode it selects.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of 200μs (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above V_{OVP} for the OVP delay time, PG is driven low after a delay time of 40μs (typ.).

Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low V_{IN} or EN, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is

enabled. The output discharge current is typically 80mA for V_{OUT} = 5V. The discharge MOSFET is not active outside of these shutdown conditions.

External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a 0.1μF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.

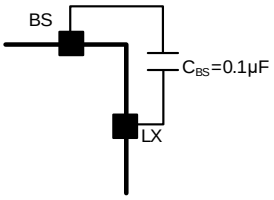


Figure6. Bootstrap Capacitor Connection

VCC Output

The device integrates a high performance, low drop-out linear regulator 3.3V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. Once the input voltage exceeds its own UVLO (rising) threshold, and EN is high, VCC is turned on and supplied power by V_{IN}. After the BYP voltage exceeds BYP turn on voltage, the internal LDO regulator will be turned off and the bypass switch will be turned on so that VCC output can switch to BYP voltage to reduce power consumption. Connect a 2.2μF low ESR ceramic capacitor from VCC to GND. Make sure the loop formed by the VCC capacitor is shorter than the loop for the BYP capacitor, if there is placement conflict between them.

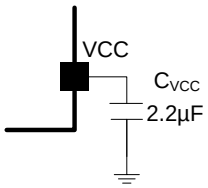


Figure7. VCC Capacitor Connection

BYP Input

When a 3.3V external power supply is connected to the BYP, the internal LDO is automatically turned off. The overall efficiency may be improved by using an external power supply. Connect a 1μF low ESR ceramic capacitor from BYP pin to GND. Using an external low pass filter consisting of a small value resistor R_{BYP} and a ceramic capacitor C_{BYP} is recommended for applications where the external power rail has significant ripple. Connect the pin to GND or leave floating if not used.

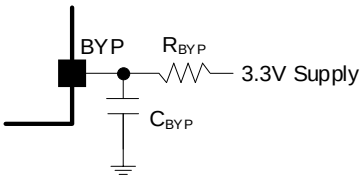


Figure8. BYP Low Pass Filter Connection

Fault Protection Modes

Output Current Limit

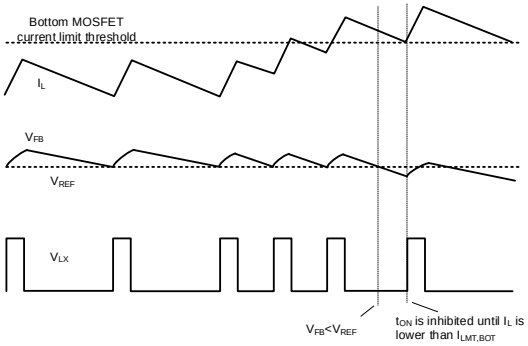


Figure9. Bottom Current Limit Protection

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, t_{ON} is inhibited until the current returns back to below the threshold.

The device supports programmable peak and valley current limit threshold using MODE pin. The detailed MODE pin configuration is shown in the table 1. When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the t_{ON} time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on. t_{ON} can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

Output Under Voltage Protection (UVP)

If V_{OUT} < ~50% of the regulated value for approximately 50μs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will enter into hic-cup protection mode. The hic-cup on time is 3ms, and the hic-cup off time is 9ms. If the output fault conditions are

removed, the buck converter will go back to normal operation in the nearest hic-cup on time.

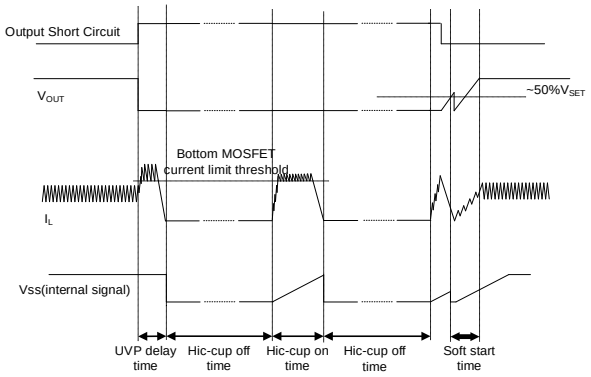


Figure10. Output Under Voltage Protection

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} should be pull low for a while when V_{FB} exceeds UVP threshold if the output fault conditions are removed during hic-cup on time, then the V_{SS} rises smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Over Voltage Protection (OVP)

The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the feedback regulation level, the top MOSFET naturally remains off and different actions are adopted in different operation mode.

When operating in PFM light load mode, if the output voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage.

When operating in FCCM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold for the OVP delay time, the protection will be triggered, and LX node switching actions will be suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. False OVP triggers may happen under FCCM light load condition, if the inductance value is chosen too low.

Over Temperature Protection (OTP)

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects the junction temperature exceeds 150°C, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled, once the junction temperature cools down by approximately 15°C, the buck converter will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

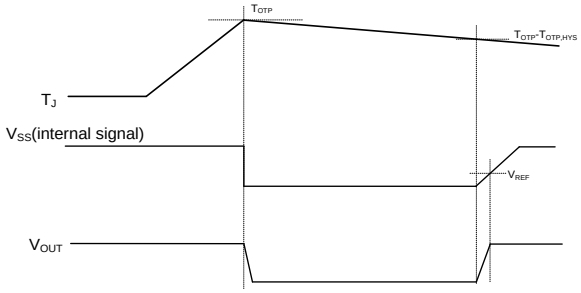


Figure11. Over Temperature Protection

Design Procedure

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 1kΩ and 1MΩ is recommended for both resistors. As an example, if V_{SET} = 5V and R_H selected value is 100kΩ, R_L can be calculated as follows:

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_H$$

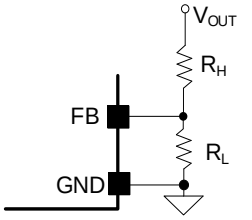


Figure12. Feedback Resistor Divider

With a calculated value of 13.7kΩ for R_L, a standard 1% 13.7kΩ resistor is selected.

Input Capacitor C_{IN}

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most

often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10μF X5R capacitor is sufficient. Place the ceramic input capacitor as close to the device's IN and GND pin as possible.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The device has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) Make sure the inductance value is high enough to avoid reverse current limit threshold is been triggered just under steady state if the load current is zero.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L,PEAK,RVS} = \frac{\Delta I_L}{2} < I_{LMT,RVS}$$

3) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use a X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Feedforward Capacitor C_{FF}

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load transient response. It is recommended 220pF for most applications. Note that when the output LC parameter is large, the feedforward capacitor can be increased for provide sufficient ripple to FB for small output ripple and good transient behavior.

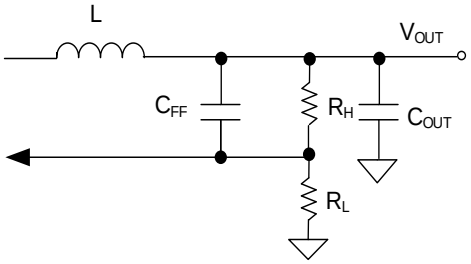


Figure13. Feedforward Network

Note: For C_{OUT} > 500μF and when the minimum load current is low, use feedforward values of R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FB node for low output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2×3-14 package the thermal resistance θ_{JA} is 22°C/W when measured on a standard Silergy 8.5cm×8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz copper traces connected to each device pin and very large, unbroken 1-oz internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated by the following formula:

$$P_{D,MAX} = \frac{125℃ - 25℃}{22℃/W} = 4.55W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

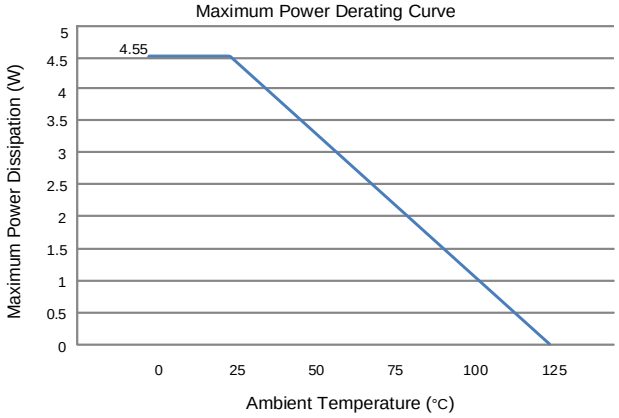


Figure14. Maximum Power Derating Curve

Application Schematic (V_{OUT} = 5V）

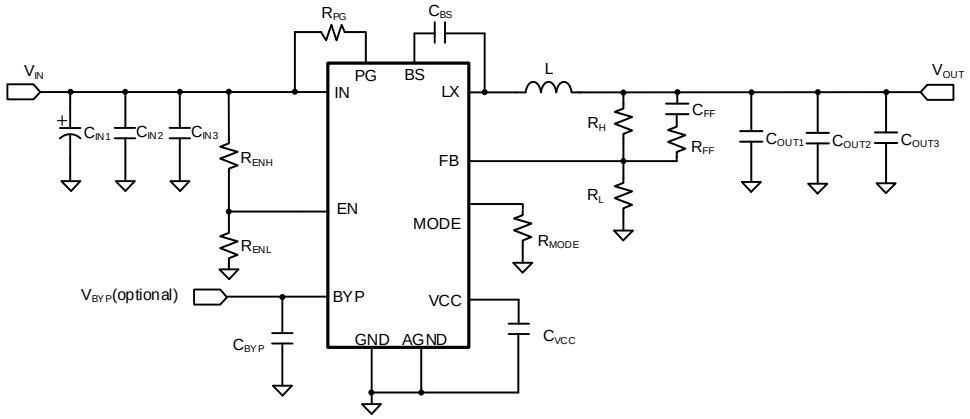


Figure15. Schematic Diagram

BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V, Electrolytic Capacitor		
C_{IN2}	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C_{IN3}, C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{OUT1}, C_{OUT2}, C_{OUT3}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C_{VCC}	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mμRata
C_{BYP}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	mμRata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
L	3.3μH/10.0A, inductor	PCMB104T-3R3MS	CYNTEC
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		
R_H, R_{PG}	100kΩ, 1%, 0603		
R_L	13.7kΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		
R_{MODE}	240kΩ, 1%, 0603		

Recommend Components Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number
1.2	100	100	220	1.0μH/PCMB104T-1R0MT
3.3	100	22.1	220	2.2μH/PCMB104T-2R2MS
5	100	13.7	220	3.3μH/PCMB104T-3R3MS
12	100	5.26	220	4.7μH/PCMB104T-4R7MS

Recommend Components Values

V_{OUT}(V)	L(μH)	$C_{OUT(Range)}$(μF)	R_{FF}(kΩ)	C_{FF}(pF)
1.2	0.68	66-500	1	220
1.2	1.0	66-500	1	220
1.2	1.5	66-500	1	220
3.3	1.5	66-500	1	220
3.3	2.2	66-300	1	220
3.3	2.2	300-500	1	470
3.3	3.3	66-180	1	220
3.3	3.3	180-500	1	470
5	2.2	66-200	1	220
5	2.2	200-500	1	470
5	3.3	66-120	1	220
5	3.3	120-500	1	470
5	4.7	66-120	1	220
5	4.7	120-500	1	680
12	3.3	66-120	1	220
12	3.3	120-500	1	470
12	4.7	66-88	1	220
12	4.7	88-150	1	680
12	5.6	66-220	1	680
12	5.6	220-500	1	1000

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor close to IN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the IN and GND using a wide copper pour. A 0.1μF input ceramic capacitor is recommended to reduce the high-frequency noise.

Output Capacitors: Ensure that the C_{OUT} negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC Capacitor: Place the VCC capacitor close to VCC pin using a short, direct copper trace to the nearest AGND pin (pin 6). Make one Kelvin connection between AGND and GND at the C_{VCC} negative side by multiple vias.

BYP Capacitor: Place the BYP capacitor close to BYP using short, direct copper trace to one nearest AGND pin (pin 6) if bypass function is used. It is recommended to make one good RC filter for BYP input if the 3.3V external power ripple is large.

Feedback Network: Place the feedback components (R_H, R_L, R_{FF} and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Use a Kelvin connection for the feedback sampling point at C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

EN Signal: It is not recommended to connect EN pin directly to V_{IN} or another voltage source. A resistor in a range of 1kΩ to 1MΩ should be used if EN pin is pulled high.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper area as wide as possible. Middle1 layer should be used as a GND layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

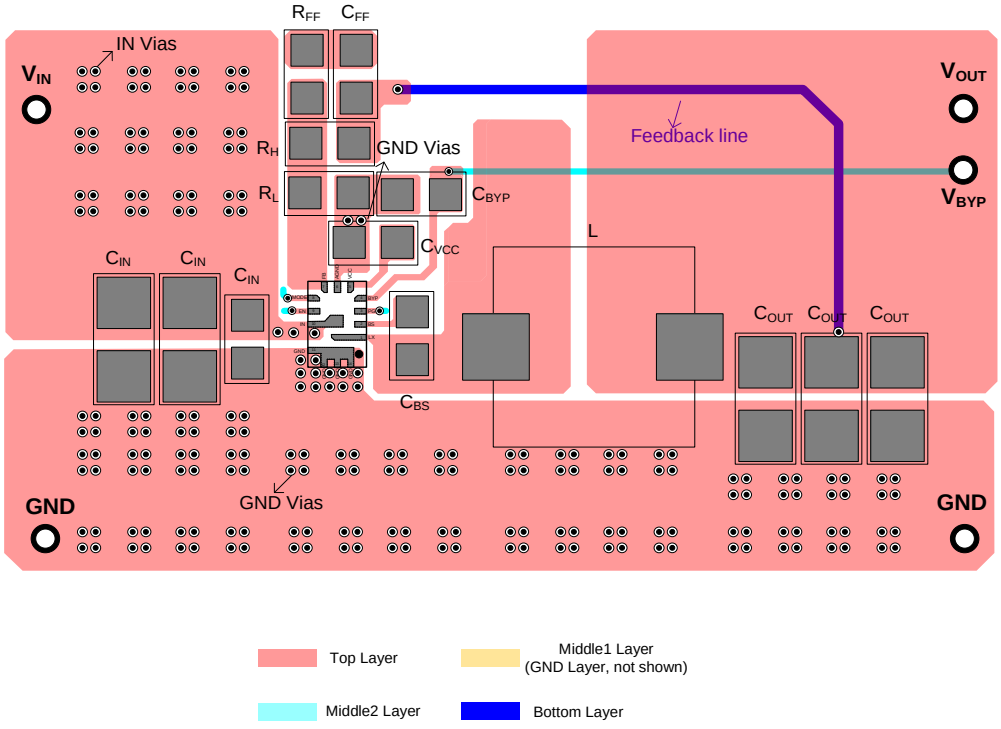
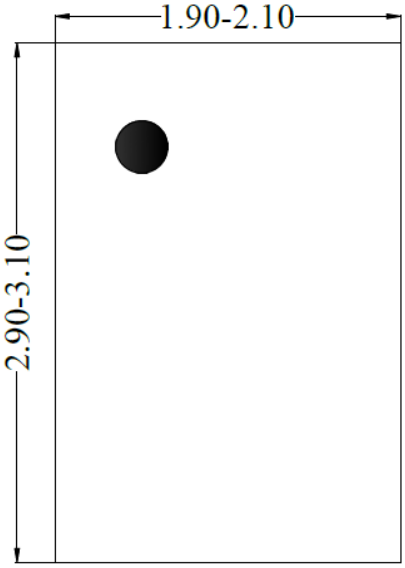
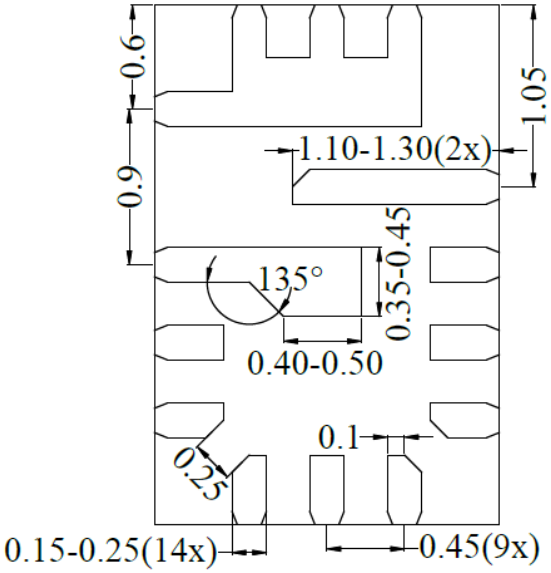


Figure16. PCB Layout Suggestion

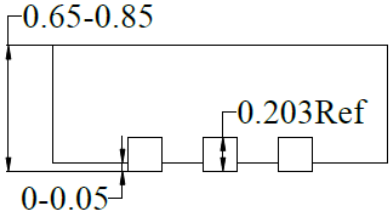
QFN2x3-14 Package Outline Drawing



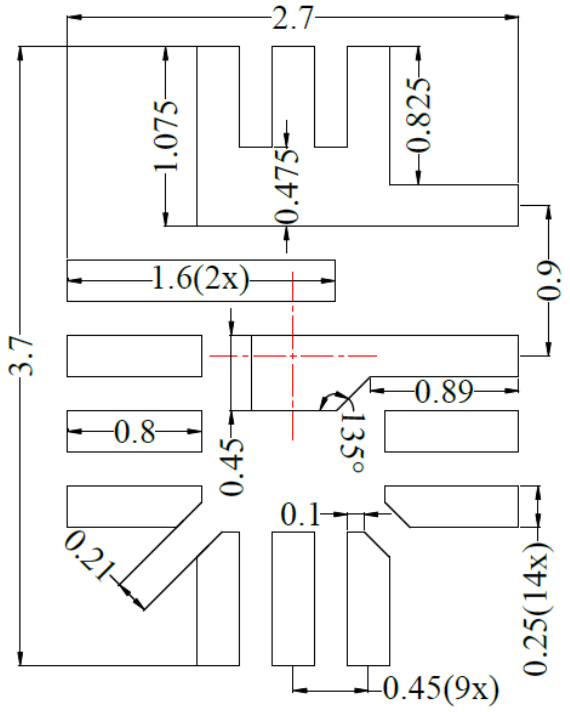
Top View



Bottom view



Front View



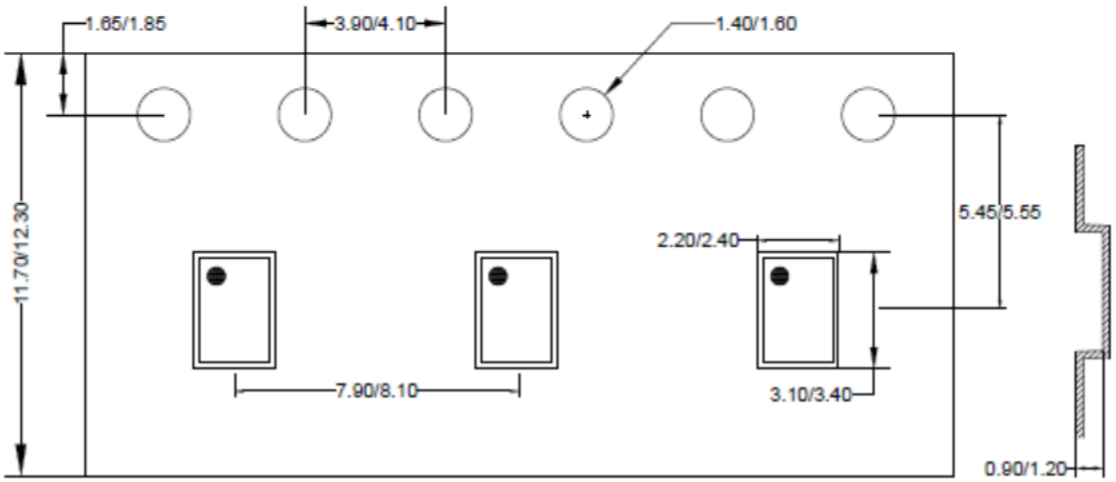
Recommended PCB layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Information

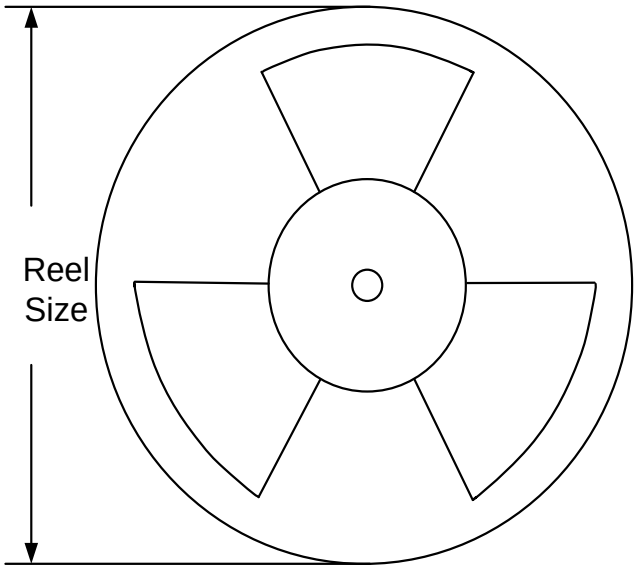
1. Tape Dimensions and Pin 1 Orientation

QFN2×3-14



Direction of Feed ⟶

2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN2×3-14	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sep. 24, 2024	Revision 1.0	Initial Release

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