

General Description

The SA33103 is a synchronous step-down controller capable of generating output voltages from 0.7V to 15V by driving external high and low side NMOS transistors. The user can adjust the switching frequency from 200kHz to 1.0MHz via an external resistor, and synchronization with an external clock is supported. The device offers three operating modes: PWM, PLL PWM, and PFM, selectable via the MODE pin. The automatic PFM mode enhances efficiency under light load conditions.

The SA33103 includes protection functions such as cycle-by-cycle current limit, Under Voltage Detection (UVD), Over Voltage Detection (OVD), Over Voltage Protection (OVP), Short Circuit Protection (SCP), and thermal shutdown. Additionally, the PGOOD (Power Good) pin indicates the output status.

The CLKOUT pin of the SA33103 features a 180° phase shift function to support multiphase applications. For EMI reduction, a spread-spectrum clock generator is available to diffuse the oscillation frequency during PWM operation.

The SA33103 is available in a QFN4×4-24 package.

Features

- Wide Input Voltage Range: 4.0V to 60V
- Start-Up Input Voltage: 4.5V
- Output Voltage Range: 0.7V to 15V
- Fold Back Reference Voltage: 640mV±1%
- Adjustable Switching Frequency: 200kHz to 1MHz
- Spread Frequency Function
- Adjustable Soft-Start Time
- Pre-Bias Start-Up
- Output Voltage Abnormal Detection (UVD/OVD), indicated on the PGOOD pin
- Cycle by Cycle Current Limit Protection
- AEC-Q100-Grade 1: -40°C ~ 125°C
- Thermal Shutdown When $T_J > 160^\circ\text{C}$
- Reliable Protection Features: SOP, UVD, OVD, OVP, and OTP
- Package: QFN4×4-24

Applications

- DC/DC Converter
- Power Module
- Automotive Power Supply Unit
- Power Source for Control Units, Including Electric Vehicles
- Inverter and Charge Controller

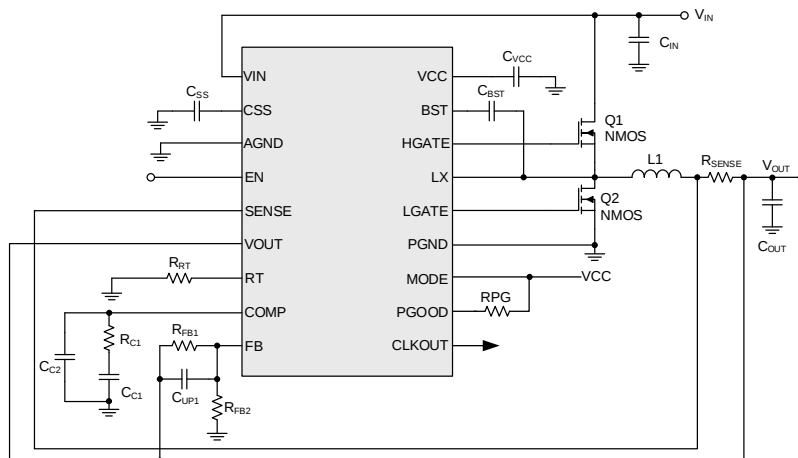


Figure 1. Typical Application Circuit (Buck Topology)

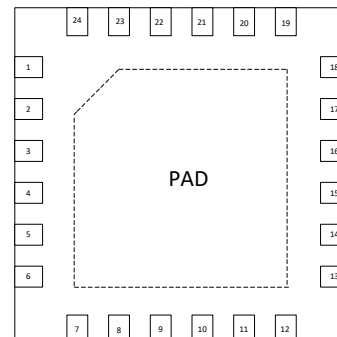
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA33103QCQ	QFN4×4-24 RoHS-Compliant and Halogen-Free	AADBxyz

Device code: AADB

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	CSS	Soft-start programming pin. An external capacitor is connected from the CSS pin to the AGND pin to begin programming the soft-start time.
2	AGND	Analog GND pin.
3	EN	Chip enable pin, logic high enable.
4	SENSE	Positive input to the inductor current sense amplifier.
5,10,15,20,22,23	NC	No connect.
6	VOUT	Negative input to the inductor current sense amplifier.
7	RT	Switching frequency adjustment pin. $RRT(k\Omega) = 41993 \times fsw(kHz)^{-1.039}$
8	COMP	Output of the error amplifier. An external RC network between COMP and AGND compensates for the regulator feedback loop.
9	FB	Feedback pin for output voltage regulation. The value of V_{OUT} can be calculated by $V_{OUT} = 0.64(R_{top} + R_{bot}) / R_{bot}$.
11	CLKOUT	Clock output pin.
12	PGOOD	Power good open drain output.
13	MODE	Mode set pin.
14	PGND	Power ground pin.
16	LGATE	Output of the Low side gate driver. Connect directly to the gate of the low side MOSFET.
17	LX	Switching node pin.
18	HGATE	Output of the high side driver. Connect directly to the gate of the high side MOSFET.
19	BST	Bootstrap pin.
21	VCC	Internal LDO output. Connect a capacitor to the ground.
24	VIN	Power supply pin.
Exposed pad		Exposed pad. The exposed pad is on the bottom side of the device. It is not electrically connected to SGND or PGND. Connect the exposed pad to SGND and PGND during PCB layout for better thermal performance.

Block Diagram

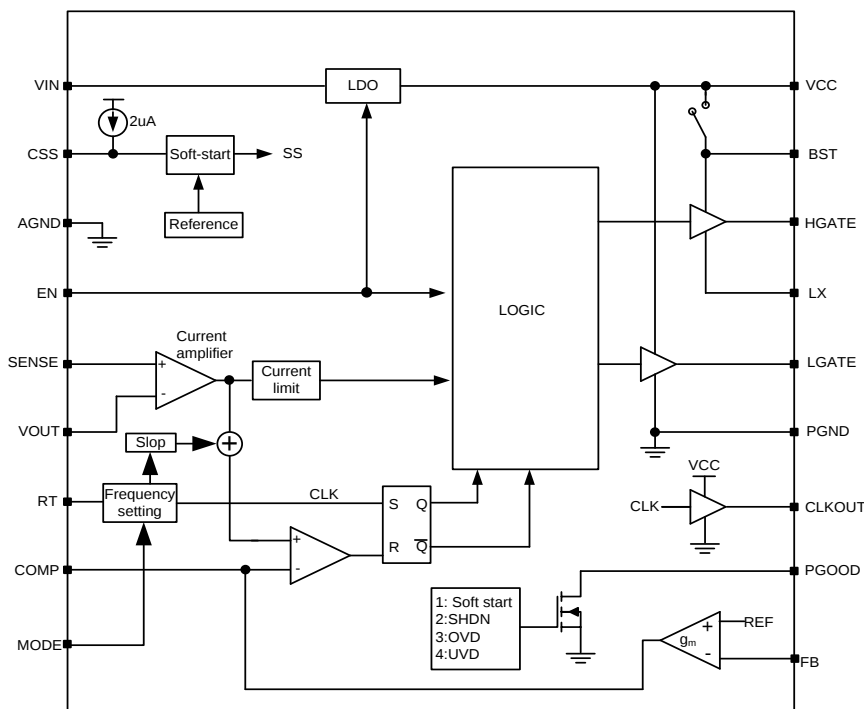


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)		Min	Max	Unit
VIN, EN, LX, VOUT, SENSE, CSS, FB		-0.3	66	V
COMP, MODE, PGOOD, CLKOUT, VCC, VBST-VLX, LGATE		-0.3	6	
RT		0.3	10	
HGATE		LX-0.3	BST	
Dynamic LX to GND Voltage in 20ns Duration		5	66	V
Junction Temperature, Operating		-40	150	°C
Lead Temperature (Soldering, 10s)			260	
Storage Temperature Range		-55	150	
VESD Electrostatic Discharge	Human Body Mode (HBM)		±2000	V
	Charge Device Mode Corner PIN (1, 9, 10, and 18) (CDM)		±750	
	Charge Device Mode Other PIN (CDM)		±500	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Case Thermal Resistance		50	°C/W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	4	60	V
VOUT	0.7	15	
Ambient Temperature Range	-40	125	°C

Electrical Characteristics

($V_{IN} = 13V$ (Note 3), $T_A = 25^\circ C$ unless otherwise specified (Note4))

	Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Input & VCC Supply	Start-Up Voltage	V _{START}			4	4.5	V
	VCC Regulate Voltage	V _{CC}	V _{FB} =0.672V	4.9	5.1	5.3	V
	Standby Current	I _{STANDBY}	V _{IN} =12V, EN=0		3	20	μA
	VIN Supply Current at PWM Without Switching	I _{VIN1}	V _{FB} =0.672V, MODE=5V, V _{OUT} =SENSE=LX=5V		2.7	3.5	mA
	VIN Supply Current at PFM Without Switching	I _{VIN2}	V _{FB} =0.672V, MODE=0V, V _{OUT} =SENSE=LX=5V		192	280	μA
	VCC UVLO Threshold	V _{UVLO2}	V _{CC} Rising	3.8	4	4.2	V
		V _{UVLO1}	V _{CC} Falling	3.1	3.3	3.5	V
Fold Back	FB Reference	V _{FB}	T _A =25°C	0.6336	0.64	0.6464	V
			-40°C≤T _A ≤125°C	0.6272		0.6528	V
	FB Pin OVD Threshold	V _{FBOVD1}	V _{FB} Rising	0.66	0.694	0.72	V
		V _{FBOVD2}	V _{FB} Falling	V _{FB} +0.005	0.664	0.7	V
	FB Pin UVD Threshold	V _{FBUVD1}	V _{FB} Rising	0.58	0.613	0.634	V
		V _{FBUVD2}	V _{FB} Falling	0.55	0.578	0.6	V
	FB Pin Current	I _{FBH}	V _{FB} =0.64V	-0.1		0.1	μA
		I _{FBL}	V _{FB} =0V	-0.25		0	μA
Switching Frequency/T _{on_min} /T _{off_min}	Oscillation Frequency	f _{OSC0}	RT=135kΩ	218	250	282	kHz
		f _{OSC1}	RT=32kΩ	945	1080	1215	kHz
	Minimum T _{off}	T _{off_min}	From falling edge of HGATE to falling edge of LGATE	130		242	ns
	Minimum T _{on}	T _{on_min}			100	135	nS
	Synchronizing Frequency	F _{SYNC}	250kHz low clamp	80	250*0.5	180	kHz
			250kHz high clamp	250	250*1.5	600	kHz
			1000kHz low clamp	400	1000*0.5	700	kHz
1000kHz high clamp			1100	1000*1.5	2200	kHz	
Soft Start	Soft-Start Time	T _{SS1}	CSS OPEN	0.35		1.0	ms
		T _{SS2}	Css=4.7nF	1.3		2.3	ms
	Charge Current for SS	I _{TSS}	CSS=0V	1.6	2	2.4	μA
	CSS Voltage at The End of Soft Start	V _{SSEND}		0.62		0.72	V
	Discharge Resistance Integrate in CSS Pin	R _{DIS_CSS}	V _{IN} =12V, EN=0V, CSS=3V	2	4.2	5.5	kΩ
Internal GATE Driver MOS	On Resistance of HGATE Pull Up	R _{UPHGATE}	BST-LX=5V, I _{HGATE} =-100mA		2.5	5	Ω
	On Resistance of HGATE Pull Low	R _{DOWNHGATE}	BST-LX=5V, I _{HGATE} =100mA		1.5	3.5	Ω
	On Resistance of LGATE Pull Up	R _{UPLGATE}	VCC-PGND=5V, I _{LGATE} =-100mA		4	7	Ω

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	On Resistance of LGATE Pull Low	$R_{DOWNLGATE}$	$V_{CC-PGND}=5V$, $I_{LGATE}=100mA$		1.5	3.5	Ω
Current Limit	Current Limit Threshold	V_{LIMIT}	SENSE-VOUT (VOUT>0.5V)	58	70	82	mV
	Reverse Current Limit Threshold	$V_{IREVLIMIT}$	SENSE-VOUT (VOUT>0.5V)	-47	-35	-23	mV
MOS Fault Protection	LX Short to GND Protection Threshold	$V_{LXSHORTL}$	LX short to GND	1		2	V
	LX Short to VIN Protection Threshold	$V_{LXSHORTH}$	LX short to VIN	1		2	V
EN/MODE/CLKOUT/PGOOD Threshold	EN High Threshold	V_{ENH}				1.3	V
	EN Low Threshold	V_{ENL}		0.9			V
	EN High Input Current	I_{ENH}	EN=44V	0.2		5	μA
	EN Low Input Current	I_{ENL}	EN=0V	-1	0	1	μA
	Highest MODE High Threshold	V_{MODEH}	Mode high voltage range	0.5		1.1	V
	MODE Hysteresis Voltage	V_{MODEL}	Hysteresis voltage of V_{MODEH} and V_{MODEL}	10	56	110	mV
	MODE High Input Current	I_{MODEH}	MODE=6V	1		6.6	μA
	MODE Low Input Current	I_{MODEL}	MODE=0V	-1	0	1	μA
	CLKOUT High Voltage	$V_{CLKOUTH}$	CLKOUT	4.7		VCC	V
	CLKOUT Low Voltage	$V_{CLKOUTL}$	CLKOUT	0		0.1	V
	PGOOD Pin Off Voltage	V_{PGOFF}	VIN=4V, PG=1mA		0.26	0.54	V
	PGOOD Pin Off Current	I_{PGOFF}	VIN=12V, EN=0, PG=6V	-0.1	0	0.1	μA
Loop Amplify	Loop Amplify	gm (EA)	COMP=1.5V	0.5	1	1.55	ms
Protection	Thermal Shut Down	T_{TSD}	T_A Rising	150	160		$^{\circ}C$
	Thermal Shut Down Recovery	T_{TSR}	T_A Falling	125	140		$^{\circ}C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

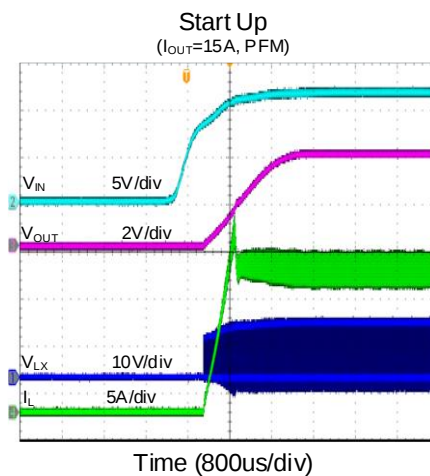
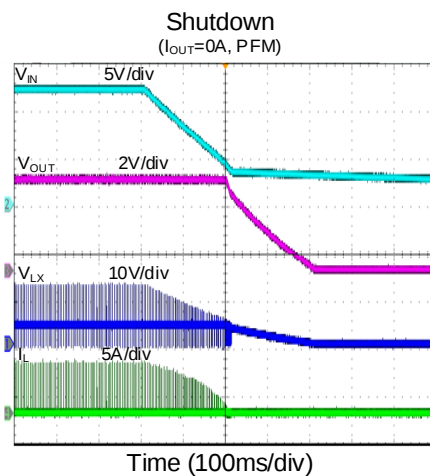
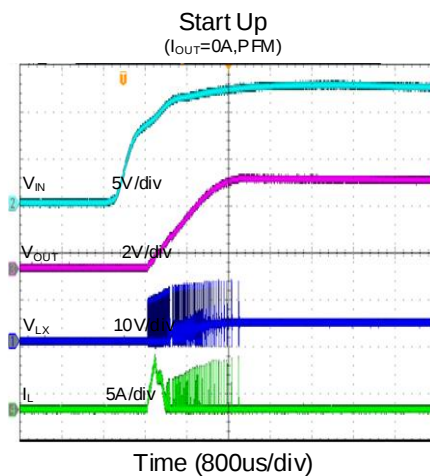
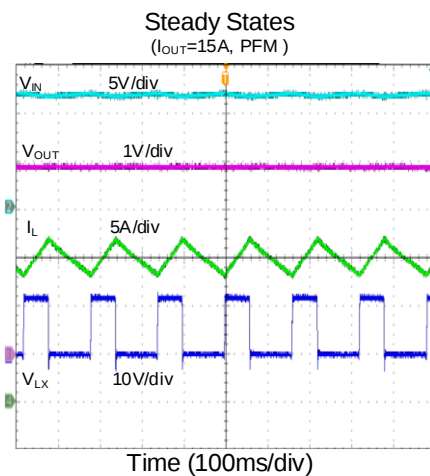
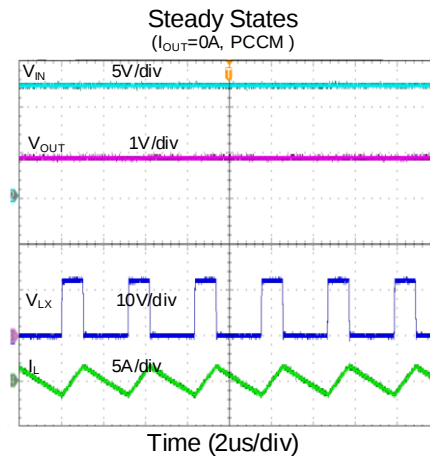
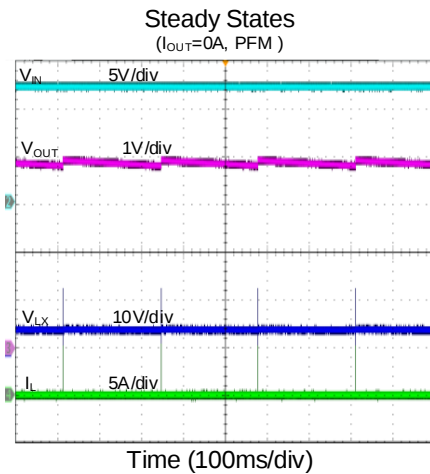
Note 2: θ_{JA} is measured with natural convection at $T_A = 25^{\circ}C$ on a 2oz two-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin 4. [Use the actual condition provided by package engineering.]

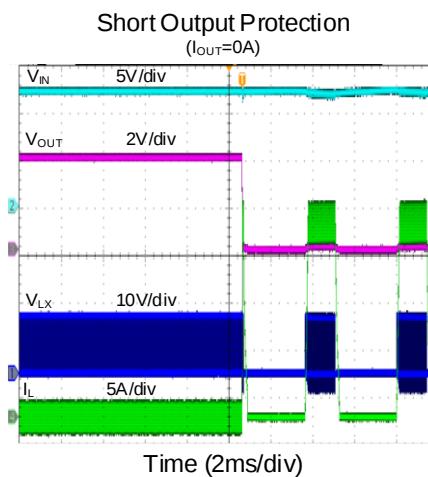
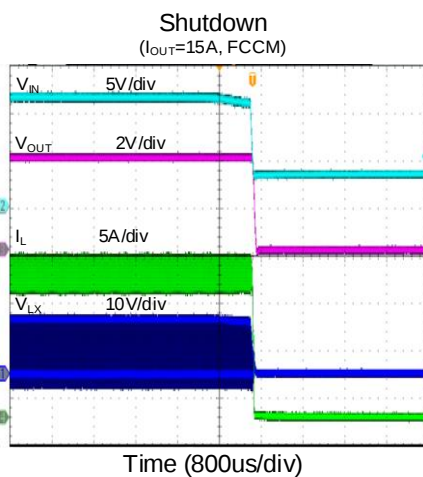
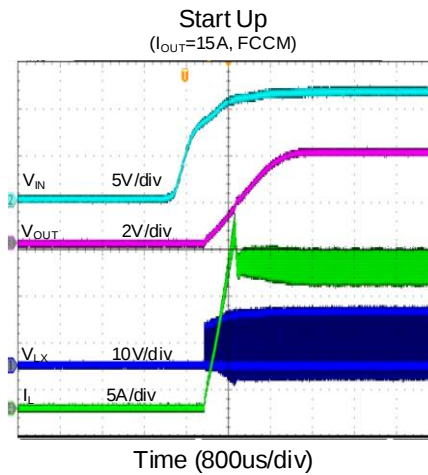
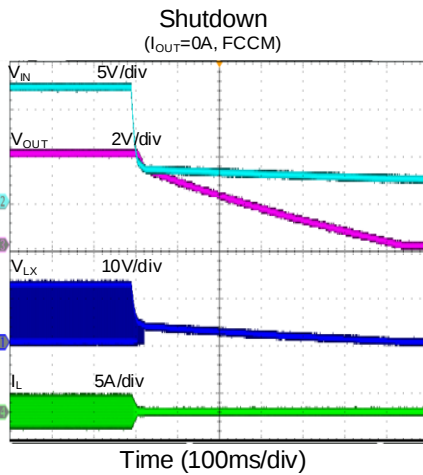
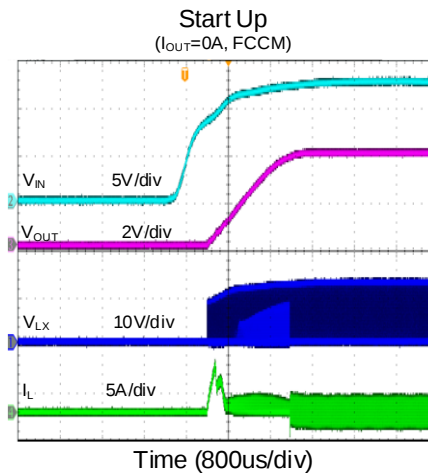
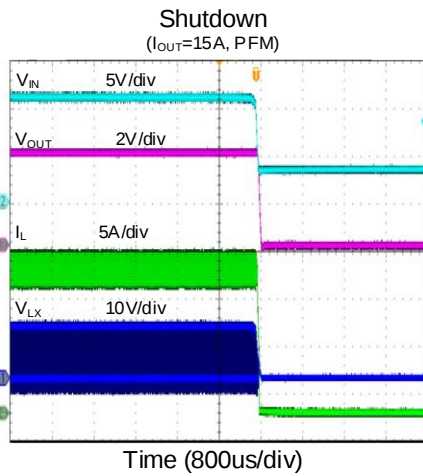
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^{\circ}C$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

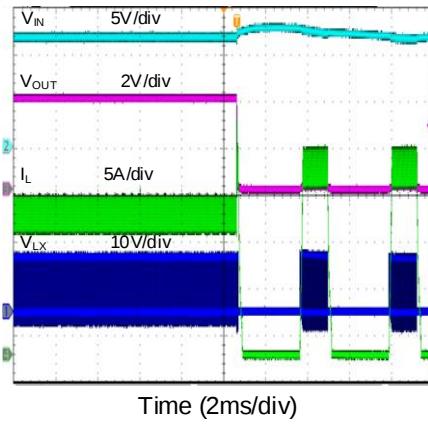
Typical Performance Characteristics

($V_{IN}=12V$, $V_{OUT}=3.8V$, $L=2.2\mu H$, $C_{OUT}=200\mu F$)

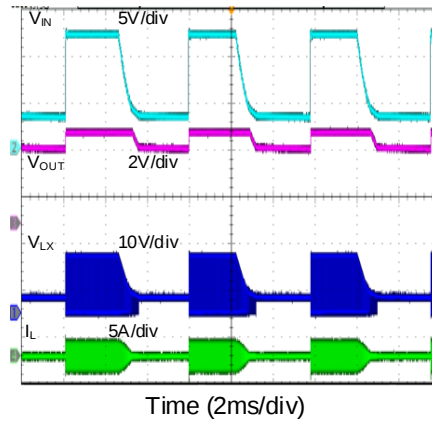




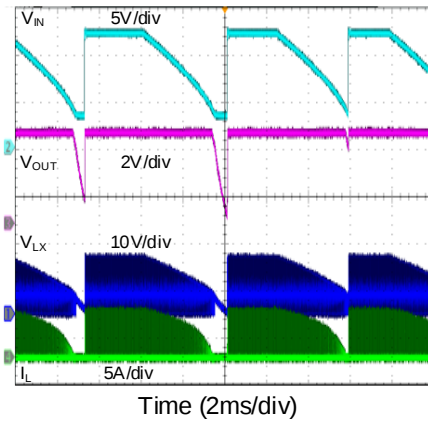
Short Output Protection
($I_{OUT}=15A$)



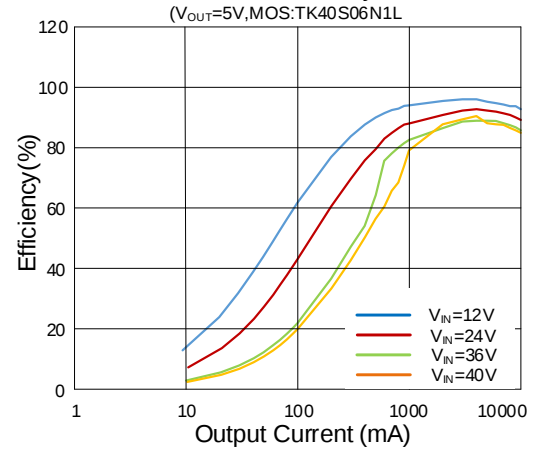
Pre-bias Function
($I_{OUT}=0A, FCCM$)



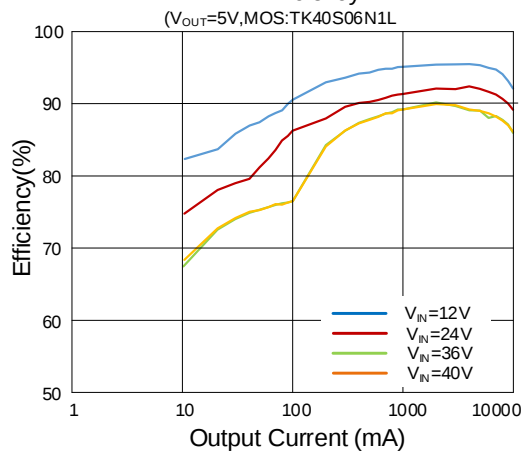
Pre-bias Function
($I_{OUT}=3A, FCCM$)



FCCM Efficiency



PFM Efficiency



Detailed Description

Operation Principle

The SA33103 is a fixed frequency and current mode controller for Buck topology.

Mode PIN Function

The operation mode of the SA33103 can be changed among PLL, PWM, and PFM modes by applying different signals to the MODE pin:

- Connecting MODE below MODEL sets the device to operate in PFM mode.
- Connecting MODE above MODEH sets the device to operate in PWM mode.
- Connecting a clock to the MODE pin sets the device to operate in PLL mode, with the switching frequency following the external clock frequency.

PLL Mode:

When an external clock is added to the MODE pin, the device will operate in PLL mode with an average switching frequency equal to the frequency of the external clock. The spread frequency function is also enabled to improve EMC. When the external clock is too high or too low, the SA33103 will set the clamp switch frequency based on the RT setting. It is recommended that the external clock be set between $0.5 \times F_{RT}$ and $1.5 \times F_{RT}$.

PWM Mode:

When the connection mode is higher than MODEH, select PWM mode. In PWM mode, the switching frequency is determined only by the RT resistance, and even at light load, the output voltage ripple is reduced.

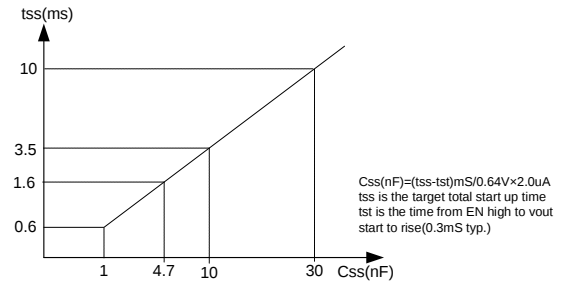
PFM Mode:

When the MODE pin is connected below MODEL, PFM mode is selected. In PFM mode, the SA33103 operates in Continuous Conduction Mode (CCM) under heavy loads and Discontinuous Conduction Mode (DCM) under light loads. The transition between CCM and DCM depends on the inductor current. When the inductor current (IL) decreases to zero, the device enters DCM. If IL is greater than zero, it operates in CCM. In DCM, if the inductor current remains zero for an extended period, the SA33103 enters standby mode to reduce its operating current.

CSS PIN Function

Connect an external CSS ceramic capacitor between the CSS pin and the AGND pin to adjust the soft-start time. The SA33103 includes a built-in minimum soft-start time of $630\mu s$ (typ). This minimum time will be applied if the soft-start time set by the external ceramic capacitor is

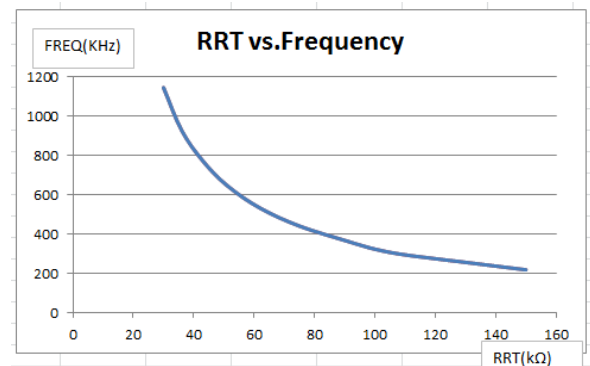
shorter than $630\mu s$ to prevent overshoot. The output current from the CSS pin is $2\mu A$ (typ). Different capacitors can be selected to change the soft-start time. The relationship between CSS and TSS is shown in the following curve:



RT Pin Function

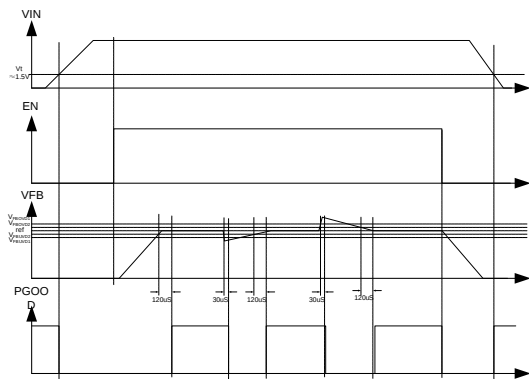
The RT pin is used for setting the SA33103 switching frequency. Choosing a different RT resistor allows control of the switching frequency from 200kHz to 1.2MHz. The EC table guarantees the switching frequency when R_{RT} ranges from $135k\Omega$ to $32k\Omega$. The relationship between the switching frequency and R_{RT} is shown in the equation and curve below:

$$R_{RT} [k\Omega] = 41993 \times f_{OSC} [kHz]^{-1.039}$$



PGOOD Pin Function

The PGOOD pin indicates the output voltage status after a soft start. When VOUT is lowered or raised, PGOOD is pulled down by an internal drain MOSFET. When VOUT returns to a normal voltage, PGOOD is pulled up by an external resistor connected to the VCC or other voltage source.

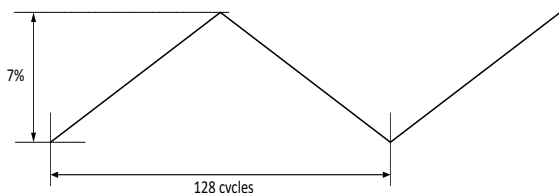


CLKOUT PIN Function

The CLKOUT pin provides a 180° phase-shifted clock output relative to the internal oscillator. This is beneficial for cascaded power supplies or multichannel power supplies, as it helps reduce current ripple at the input capacitor and the size of the EMI filter. The CLKOUT signal has a 50% duty cycle. When the first SA33103 operates in frequency decrease mode, the CLKOUT will become asynchronous to the internal oscillator.

Spread Frequency Function

The spread frequency function works for EMC reduction. The SA33103 changes the switching frequency every 128 cycles, and the range is $\pm 3.5\%$.



Pre-Bias Function

The SA33103 incorporates pre-bias to provide a smooth output voltage when a cold crank or constant start causes the output voltage to drop.

Current Limit Function

The SA33103 provides a cycle-by-cycle current limit function. When the SENSE-VOUT voltage exceeds VLIMIT, the HGATE turns off, and the LGATE turns on. When the SENSE-VOUT voltage drops below VIREVLIMIT, the LGATE turns off, and the HGATE turns on.

Under Voltage Detection

Under voltage detection monitors the voltage from the FB pin. When VFB drops below V_FBUVD2 for longer than 30µs, the SA33103 will pull down the PGOOD voltage. When the voltage on the FB pin rises above V_FBUVD1 for longer than 120µs, PGOOD is pulled high again.

Over Voltage Detection

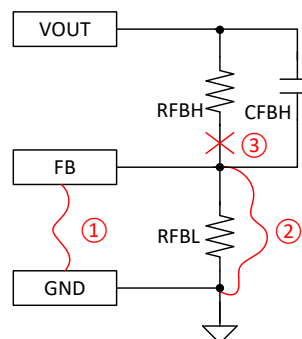
Over voltage detection monitors the voltage on the FB pin. When VFB rises above V_FBOVD1 for longer than 30µs, the SA33103 will pull down PGOOD. When the voltage on the FB pin drops below V_FBOVD2 for longer than 120µs, PGOOD is pulled high again.

Output Over Voltage Protection

When the output voltage reaches VOUT_OV (typically 18V), the SA33103 will monitor the output voltage from the VOUT pin and enter hiccup mode.

FB Abnormal Detection

The SA33103 combines the signals detected by the FB pin and the VOUT pin to detect FB anomalies. When $V_{OUT} > 6.0V$ and $V_{FB} < 180mV$ an FB abnormality is detected, causing the device to enter hiccup mode. Possible causes for this condition include the FB pin being shorted to GND, RFBH being open, or RFBL being shorted to GND. If CFBH is used, VFB will be coupled by CFBH, causing VFB to exceed 15mV, and VOUT may rise to VOUT_OV.



- ① FB pin short to GND
- ② RFBL short to GND
- ③ RFBH open

LX Short to VIN or LX Short to GND Protection

Abnormal current will occur in the high side MOSFET or low side MOSFET in the following cases:

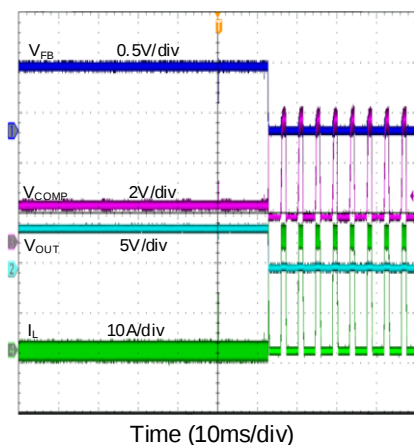
1. High side MOSFET DS short/open
2. Low side MOSFET DS short/open
3. Inductor short
4. HGATE open
5. LGATE open

Detect VIN-VLX when HGATE is on. If VIN-VLX is higher than VLXSHORTH, the device will stop PWM and enter hiccup mode. Detect VLX when LGATE is on. If VLX is higher than VLXSHORTL, the device will stop PWM and enter hiccup mode.

Over Current Protection

After the SA33103 completes the soft start, the inductive current is detected from the RSENSE cycle by cycle. If

V_{RSENSE} exceeds V_{LIMIT} for 128 consecutive cycles, the device will enter burp rising mode.



Hiccup Mode

In hiccup mode, the SA33103 stops HGATE and LGATE, discharges the CSS and COMP, and attempts to restart after a delay of 3ms.

Thermal Shut Protection

The SA33103 integrates an internal junction temperature monitor. If the temperature exceeds T_{TSD} , the device will shut down until the junction temperature drops below T_{TSR} . During thermal shutdown, the device will turn off the power supply from VIN to VCC, disable both the high side and low side MOSFETs, and discharge the CSS and COMP.

Layout Design

For optimal performance of the SA33103, the following guidelines must be followed:

1. A ceramic capacitor should be connected from the COMP pin to AGND to avoid noise disturbance.
2. The Kelvin sampling loop from the sensing resistor to the device should be as small as possible to ensure accurate current sensing (Sense pin and VOUT pin to current sense resistor).
3. AGND/PGND and VIN/VOUT GND should be properly connected in the PCB.

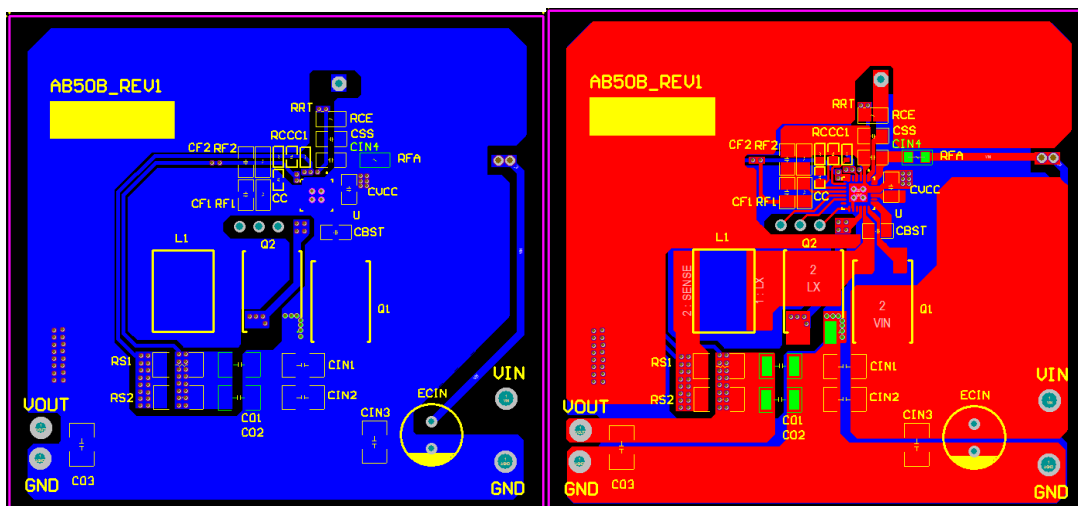


Figure 3. PCB Layout Suggestion

Application Example

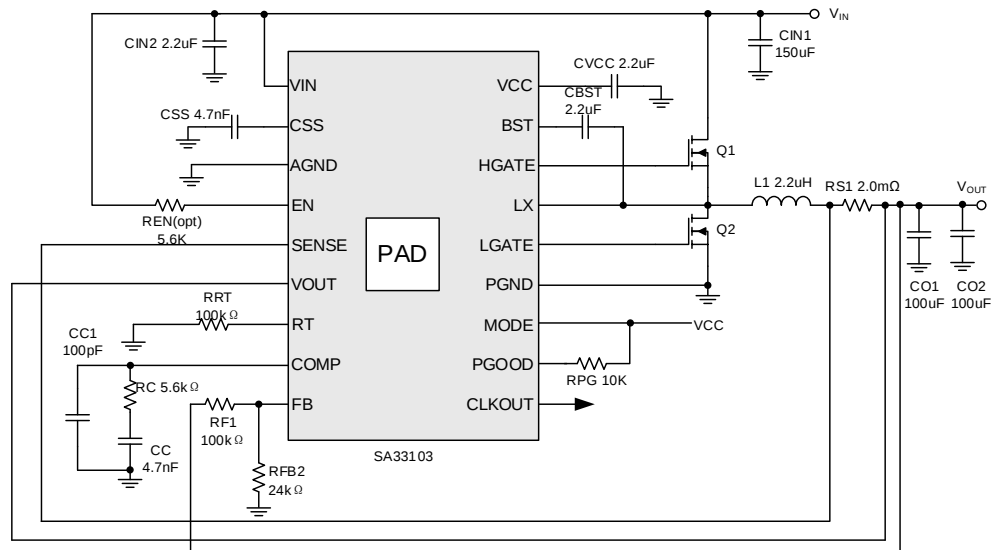
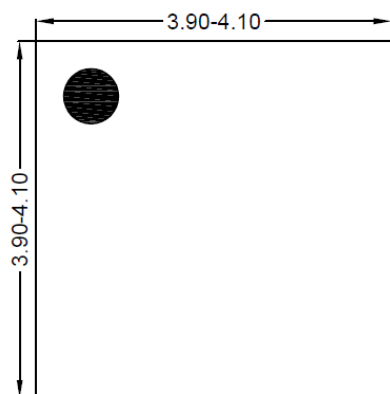
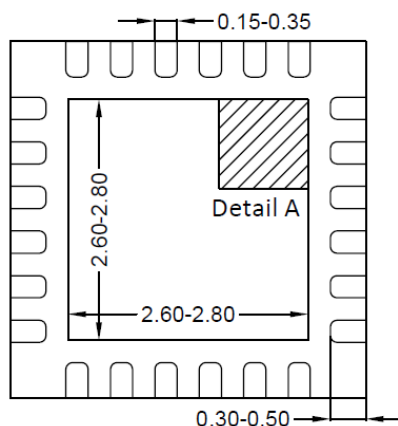


Figure 4. Schematic Diagram ($V_{OUT}=3.3V$, $I_{LOAD}=15A$, $F_{SW}=300KHz$)

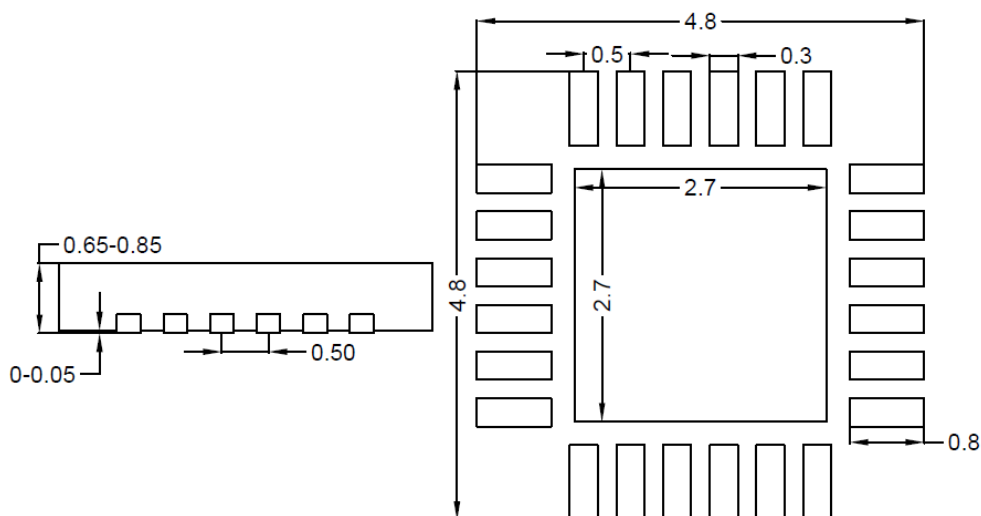
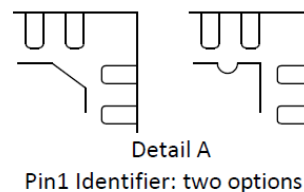
QFN4x4-24 Package Outline & PCB Layout



Top View



Bottom View



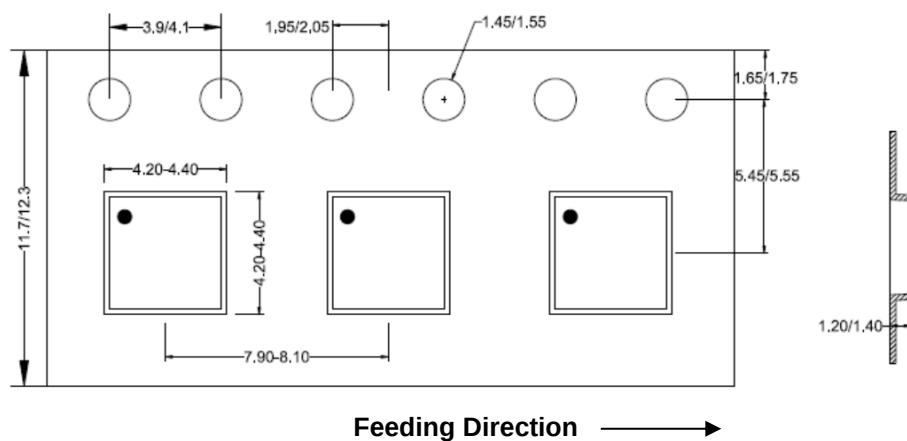
Front View

PCB Layout (Recommended)

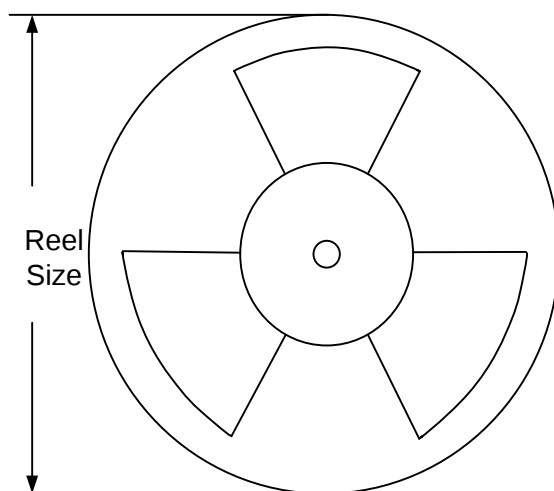
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

QFN4x4 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel (pcs)
QFN4×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 17, 2024	Revision 1.0	Initial Release

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