SY26670NGG

16V/70A DrMOS

General Description

Power Stage SY26670NGG is a monolithic power stage integrating a dedicated half bridge gate driver and both high side and low side MOSFETs to achieve high power density and high efficiency. Optimized switching edge, best in-class MOSFET and comprehensive protection logic make it suitable for CPU, GPU and POL power designs.

The SY26670NGG operates with VDRV/VCC from 3.0V to 3.6V and 3.3V PWM input signal, available for the switching frequency up to 2.0MHz. Tri-state PWM input is achieved for power-saving operation mode. Dead time and propagation delay time are optimized for high efficiency and reliable operation. Switching edge is tuned carefully for better efficiency and EMI performance. SY26670NGG provides low voltage spike and switching loss with embedded driving capacitor and input voltage capacitor.

The SY26670NGG integrates an on-chip temperature monitor to report the real-time junction temperature via TMON/FLT pin, this pin can also be pulled up or down as the fault flag together with IMON/FLT pin. The SY26670NGG provides a current reporting function via IMON/FLT pin, which achieves ±5% accuracy over temperature range. Cycle-by-cycle peak and valley current limit threshold can be programed by external resistor to protect the MOSFET.

Features

- 70A Output Current Capability
- Integrated Driver, Power MOSFET and Decoupling Capacitors
- VDRV/VCC/BST/VIN UVLO
- Support Switching Frequency up to 2.0MHz
- 3.3V PWM Input Compatible with Tri-state Logic
- Integrated 5μA/A Current Sensing and Accurate Inductor Current Report
- Integrated 8mV/°C Temperature Monitor and Report
- Provide OTP with Fault Flag
- Cycle-by-cycle Peak Current Protection with Fault Flag and Negative Over Current Protection
- Programmable Threshold for Peak Current and Valley Current Protection
- Auto Refresh for V_{BST} Power Supply in Tri-state
- Common Footprint Package: LGA5×6-41

Applications

- Multiphase Synchronous Buck Converters
- High Current CPU, GPU, ASIC and AI Power Supply
- Telecom and Server Power

Typical Applications

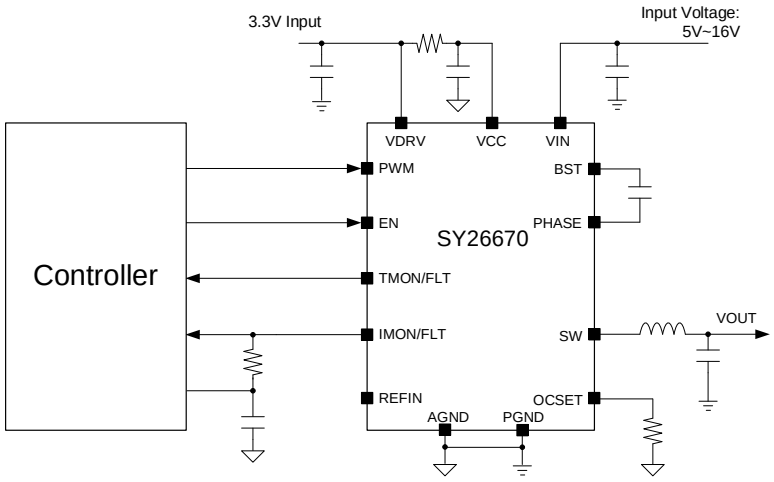


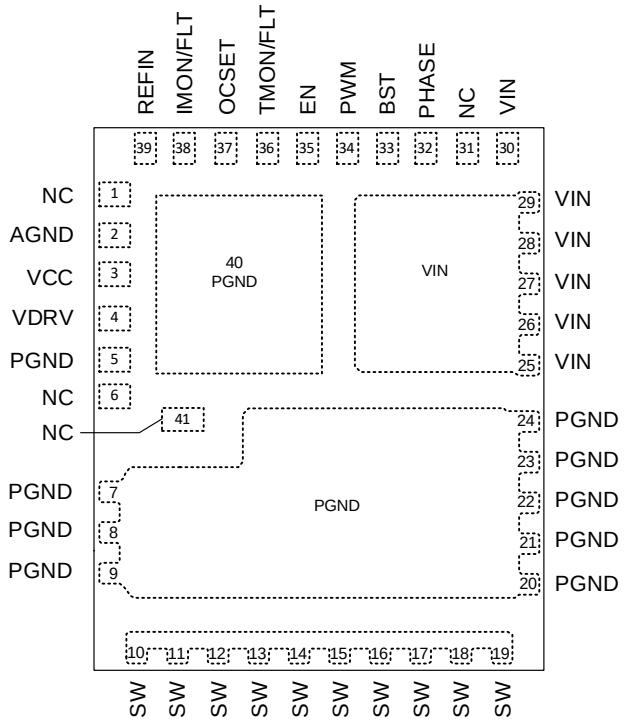
Figure1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY26670NGG	LGA5×6-41 RoHS Compliant and Halogen Free	**FYE*xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Pin Description
NC	1, 6, 31, 41	No connection.
AGND	2	Analog Signal Ground.
VCC	3	Internal analog power supply pin. Connect a RC filter from VDRV to this pin. Higher than 1μF to AGND is recommended.
VDRV	4	3.3V for gate drivers. This pin should be bypassed to GND.
PGND	5, 7-9, 20-24, 40	Power Ground.
SW	10-19	Switching point, connected to the inductor.
VIN	25-30	Input pin. Decouple this pin to the PGND pin as close as possible.
PHASE	32	Phase node.
BST	33	Bootstrap capacitor connection. Connect a ceramic capacitor from this pin to the PHASE pin.
PWM	34	3.3V PWM input pin. Logic high sets control FET gate high only, logic low sets synchronous FET gate high only. Both MOSFET gates are set low if PWM stays in Hi-Z for longer than the tri-state hold off time.
EN	35	Enable input. Pull low to disable the device and pull high to enable. Do not leave this pin floating.
TMON/FLT	36	Temperature monitor and FAULT flag pin. This pin provides temperature report function with a slope of 8 mV/°C. In the event of a FAULT, this pin is pulled HIGH to VCC, and pulled down to 0V when EN OFF or VCC/VDRV UVLO.
OCSET	37	Peak/valley current protection set pin. A resistor to AGND to program the peak/valley current protection threshold.
IMON/FLT	38	Current sensing output with a mirrored current of inductor current with 5μA/A gain.
REFIN	39	External reference voltage input for current sensing bias. This pin can be left floating.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	18	V
SW-GND 10ns Duration	-8	25	
SW- DC	-0.3	V_{IN}+0.3	
VIN-SW 10ns Duration	-8	28	
VIN-SW DC	-0.3	V_{IN}+0.3	
BST-PHASE 3ns Duration		6.9	
BST-PHASE 10ns Duration		5	
BST-PHASE DC		4	
VCC, VDRV, PWM, EN, TMON/FLT, IMON/FLT, OCSET, REFIN	-0.3	4	
Instantaneous Current		70	A
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	16.3	°C/W
$\theta_{JC(Top)}$ Junction-to-Case (Top) Thermal Resistance	3.5	
$\theta_{JC(Bottom)}$ Junction-to-Case (Bottom) Thermal Resistance	1.1	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	5	16	V
Control and Driver Voltage V_{VCC}, V_{VDRV}	3	3.6	
Switching Frequency	200	2000	kHz
Junction Temperature, Operating	-40	125	°C

Electrical Characteristics

(V_{IN}=12V, V_{CC}= V_{DRV}=3.3V, TJ = -40°C~125°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN UVLO Rising Threshold	$V_{IN,UVLO}$			4.5	4.9	V
VIN UVLO Hysteresis	$V_{IN,UVLO\_HYS}$			0.7		V
VCC UVLO Threshold	$V_{UVLO,VCC}$		2.5	2.7	2.9	V
VCC UVLO Hysteresis	$V_{HYS,VCC}$			0.2		V
VCC Supply Current in Standby Mode	$I_{VCC,ENL}$	EN=Low		50		μA
VCC Supply Current in Active Mode		EN=High, PWM=Low		13		mA
VDRV UVLO Threshold	$V_{UVLO,VDRV}$		2.7	2.9	3.1	V
VDRV UVLO Hysteresis	$V_{HYS,VDRV}$			0.2		V
VDRV Supply Current in Standby Mode		EN=Low			1	mA
VDRV Supply Current in Active Mode		EN=High, PWM=Low			2	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM High Level Input Voltage	$V_{PWM,H}$		2.6			V
PWM Tri-state Voltage	$V_{PWM,TRI}$		1.4		1.9	V
PWM Low Level Input Voltage	$V_{PWM,L}$				0.7	V
PWM Floating Output Pull up Impedance	$R_{PWM,PU}$			10		kΩ
PWM Floating Output Pulldown Impedance	$R_{PWM,PD}$			10		kΩ
PWM Input Frequency Range	F_{PWM}		200		2000	kHz
Entering Tri-state Delay Time (Note 4)		Input Logic going tri-state to both MOSFETs OFF		50		ns
Exiting Tri-state Propagation Delay (Note 4)				20		ns
PWM Propagation Delay (Note 4)	$t_{PWM,DLY}$	From PWM High to LS MOSFET OFF		25		ns
Minimum ON Time (Note 4)	$t_{ON,MIN}$			35		ns
Minimum OFF Time (Note 4)	$t_{OFF,MIN}$			100		ns
Dead Time from LS FET OFF to HS FET ON (Note 4)	$t_{DT,L2H}$			3		ns
Dead Time from HS FET OFF to LS FET ON (Note 4)	$t_{DT,H2L,POS}$	Positive Inductor Current		6		ns
	$t_{DT,H2L,NEG}$	Negative Inductor Current		10		ns
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$	V_{BS-LX}=3.3V, T_J=25°C		3.7		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$	V_{DRV}=3.3V, T_J=25°C		1.12		mΩ
EN High Level Threshold	$V_{EN,H}$		1.5			V
EN Low Level Threshold	$V_{EN,L}$				0.5	V
EN ON Delay Time	$t_{ENON,DLY}$			50		μs
EN OFF Delay Time	$t_{ENOFF,DLY}$			500		ns
Temp Monitor Voltage	V_{TMON}	T_J =25°C		800		mV
Temp Monitor Voltage Slope	k_{TMON}			8		mV/°C
TMON Output Source Current	$I_{TMON,SRC}$			7		mA
TMON Pulldown Resistance	R_{TMON}			20		kΩ
IMON Output Range	$V_{IMON,RNG}$		0.8		1.85	V
IMON Gain (Note 4)	G_{CS}	V_{IN}=12V, V_{OUT}=1V, f_{PWM}=500kHz, 0A<I_{OUT}≤70A		5		μA/A
IMON Offset		I_{OUT}=0A, PWM=LOW, Low side ON, REFIN Range=1.0V-1.4V, T_j=25℃	-5		5	μA
IMON Overall Accuracy (Note4)		V_{IN}=12V, V_{OUT}=1V, f_{PWM}=500kHz, 0A<I_{OUT}≤30A	-1.5		1.5	A
		V_{IN}=12V, V_{OUT}=1V, f_{PWM}=500kHz, 30A<I_{OUT}≤70A	-5		5	%
Fault Report						
TMON/FLT Active High Logic for Fault Report	$V_{FLT,H}$			Vcc-0.1		V
TMON/FLT Active Low Logic for Fault Report	$V_{FLT,L}$				0.1	V
Fault Report Source Current	$I_{FLT,SRC}$		20			mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IMON/FLT Report Voltage	$V_{IMON/FLT,OCP}$	OCP	2.1	2.2	2.3	V
	$V_{IMON/FLT,OTP}$	OTP	0.5	0.6	0.7	V
	$V_{IMON/FLT,UVLO}$	VIN UVLO			0.3	V
Over Temperature Protection Threshold (Note 4)	T_{OTP}			150		°C
Over Temperature Hysteresis (Note 4)	$T_{OTP,HYS}$			20		°C
Peak Current Limit Max Programmable Threshold	$I_{PK,MAX}$	OCSET pin floating or connected to VCC		80		A
Peak Current Limit Min Programmable Threshold	$I_{PK,MIN}$	R_{OCSET}=151.7kΩ		20		A
Peak Current Limit Threshold Program Gain		$R_{OCSET}×I_{PK}$		3035		kΩ×A
Peak Current Limit Flag Trigger Counter				10		times
Valley Current Limit Threshold	$I_{VLY,LMT}$			87.5%		Peak OCP
Low Side FET Negative Current Protection				-40		A

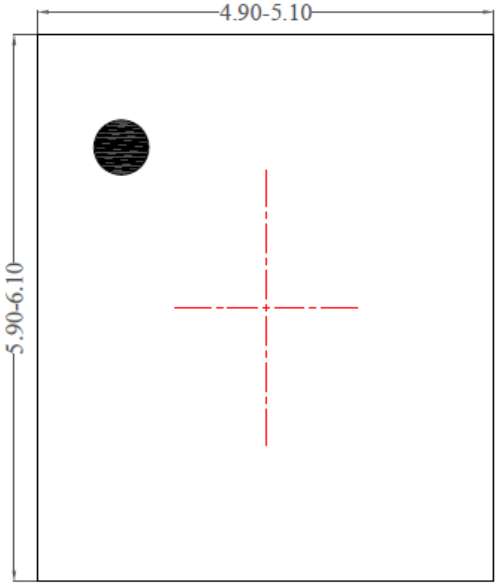
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A=25°C on an 8.1cm×11.7cm size six-layer Silergy Evaluation Board.

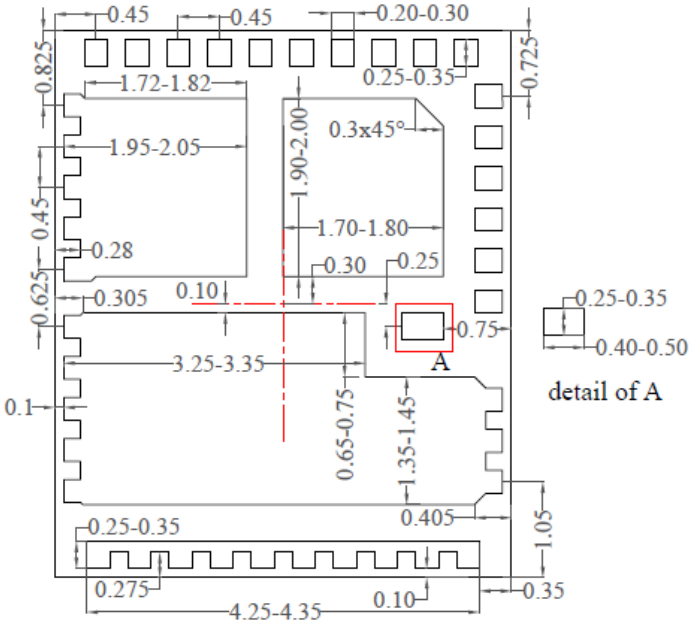
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

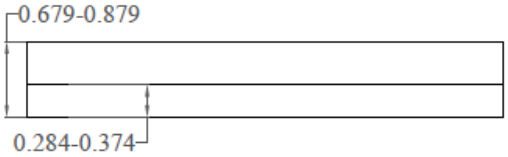
LGA5×6-41 Package Outline Drawing



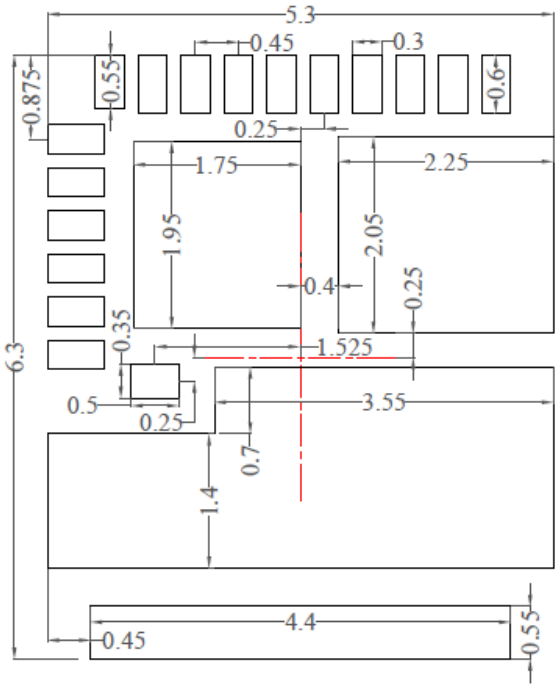
Top View



Bottom view



Front View

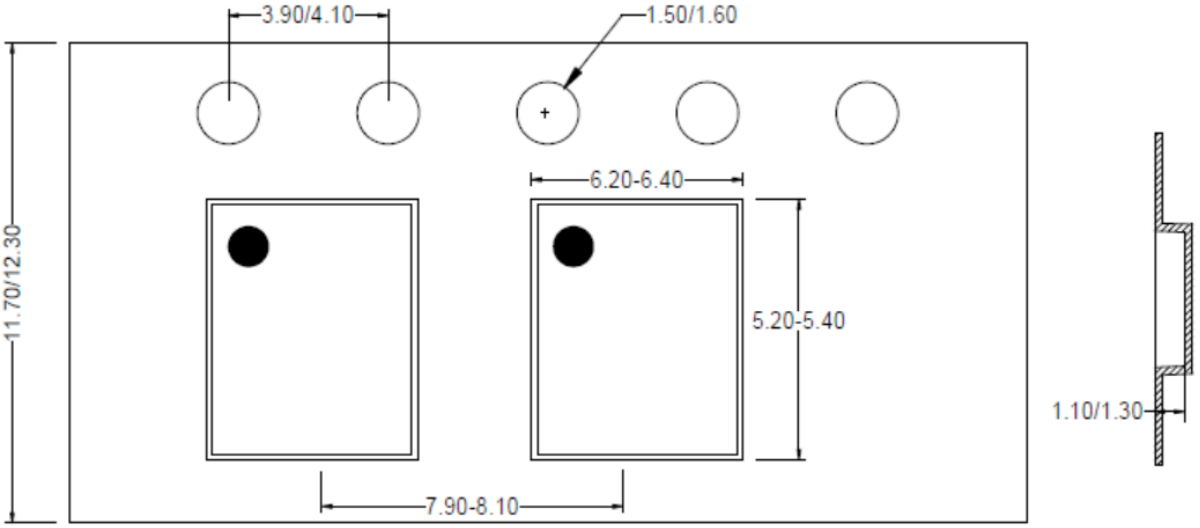


Recommended PCB layout
(only for reference)

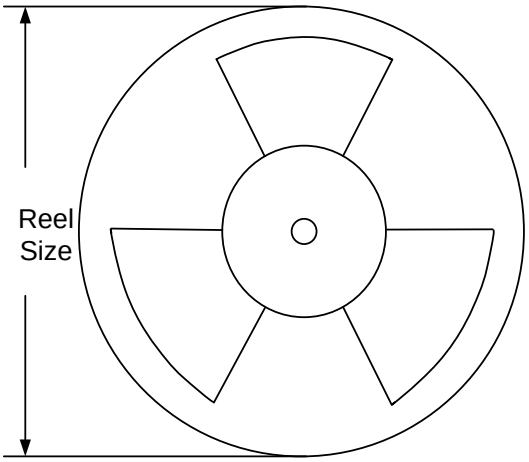
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. LGA5×6 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
LGA5×6	12	8	13"	400	400	5000

3. Others: NA

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