



General Description

The SQ33020Z is a high frequency quasi-resonant (QR) flyback controller designed for power delivery (PD) capable adapters and quick chargers. It can drive enhancement GaN FETs directly, and can deliver 240W output power. The 25kHz–300kHz switching frequency allows for reduced transformer and capacitor sizes.

The SQ33020Z operates using peak current control. It provides a QR mode in which the GaN FET can be turned on at a valley point to reduce switching loss, especially under high input voltages.

In conventional QR flyback solutions, the valley number always varies between 1 and 2 or 3 and 5, which increases V_o ripple and creates audible noise. The SQ33020Z uses a proprietary circuit to lock the valley number between 1 and 6, for improved stability compared with other conventional QR solutions.

If the load decreases, the SQ33020Z will enter discontinuous conduction mode (DCM) to reduce the switching frequency for higher efficiency. If the load is very light, the SQ33020Z will enter burst mode to further reduce power loss.

The SQ33020Z provides comprehensive functions to ensure reliable operation, including: HV startup, X capacitor discharge, output and VCC overvoltage protection (OVP), AC input OVP, output undervoltage protection (UVP), internal and external overtemperature protection (OTP), and open-loop protection (OLP).

It is recommended to use the SQ33239 as a secondary side Synchronous Rectifier (SR) controller in conjunction with the SQ33020Z so that Zero Voltage Switching (ZVS) operation can be achieved for higher efficiency.

The SQ33020Z is available in a compact SSOP9 package.

Features

- DCM+QR Combined Operating Mode
- Direct Enhancement-Mode (E-Mode) GaN FET Driver
- Programmable Gate Driver Current
- Switching Frequency Range: 25kHz–300kHz
- Automatic Valley Lockout from 1 to 6 cycles
- Low Frequency Burst (1kHz)
- Frequency Modulation to Reduce EMI Noise (Configurable using ZCS Resistor)
- Internal Soft-Start
- Integrated 700V HV Startup Circuit
- X Capacitor Discharge Protection
- AC Input OVP
- Programmable Output OVP and UVP
- Current Sense Resistor Short Protection
- Internal and External OTP
- MSL3
- Compact Package: SSOP9

Applications

- AC/DC Adapters
- PD Adapters
- Quick Chargers

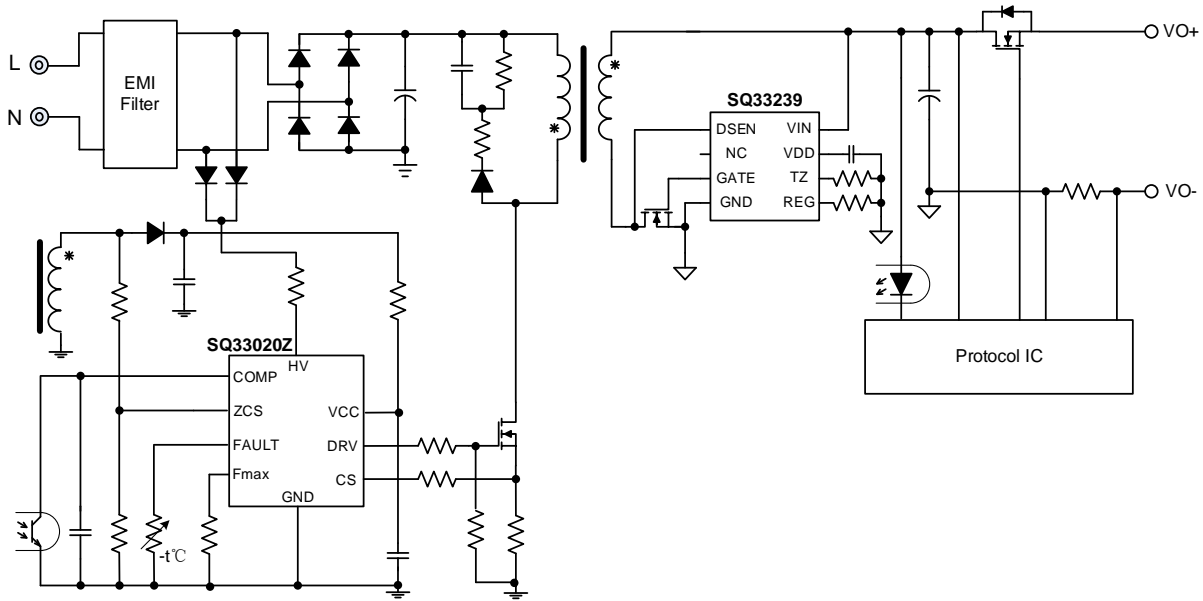


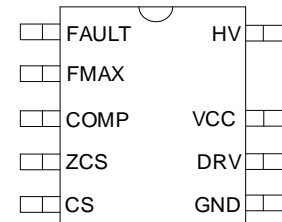
Figure 1. Typical Application Circuit using Synchronous Rectification (SR)

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ33020ZFVP	SSOP9 RoHS-Compliant and Halogen-Free	AATNxyz

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	FAULT	External OTP and V_{OUT} OVP pin
2	FMAX	Maximum frequency (f_{MAX}) set pin with an external resistor to GND
3	COMP	Compensation voltage of secondary side, connected to an optocoupler
4	ZCS	Output voltage, input voltage, and QR valley detection pin
5	CS	Transformer current sensing pin
6	GND	Ground pin
7	DRV	Programmable GaN gate drive pin
8	VCC	Power supply pin
9	HV	HV startup, X capacitor discharge detection pin

Block Diagram

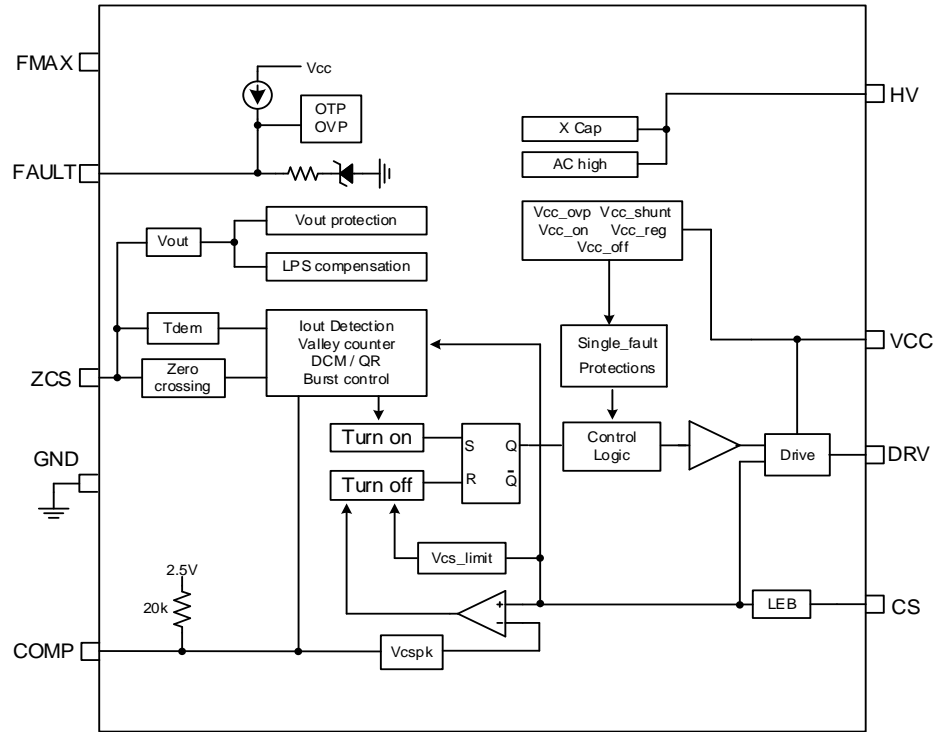


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
HV	-0.3	700	V
VCC	-0.3	30	
DRV	-0.3	8	
CS, COMP, FMAX, FAULT	-0.3	4	
ZCS	-1 (Note 1)	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-60	150	
Note1, Dynamic ZCS Negative Voltage in 50µs Duration		-1	V
Note1, Dynamic ZCS Negative Current in 50µs Duration		-2	mA
Human Body Model ESD (HV Pin) per ESDA/JEDEC JS-001-2017 (Note 6)		±1	kV
Human Body Model ESD (All Pins Except HV Pin) per ESDA/JEDEC JS-001-2017 (Note 6)		±2	kV
Charged Device Model ESD per JS-002-2018 (Note 6)		±500	V
Latch-Up Test per JEDEC78E (Note 6)		±100	mA
MSL Rating		3	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		158	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		30	
PD Power Dissipation $T_A = 25^\circ\text{C}$		0.79	W

Recommended Operating Conditions

Parameter	Min	Max	Unit
VCC	8	25	V
Junction Temperature Range	-40	125	°C

Electrical Characteristics

($V_{VCC} = 13\text{V}$ (Note 7), $T_J = -40^\circ\text{C} \sim 125^\circ\text{C}$ unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
HV	HV Current to Charge VCC	$I_{HV_CHARGE1}$	$V_{HV} = 100V_{DC}$, $V_{CC} = 0V$	0.15	0.3	0.55	mA
			$V_{HV} = 100V_{DC}$, $V_{CC} = 3V$	2.6	4.0	5.4	mA
	Current to Discharge X Capacitor (Note 4)	I_{HV_XCAP}			2.0		mA
	High or Low Voltage Detection (Note 4)	$HV_{TH_AC_HIGH}$		200	218	236	V
	AC Low Debounce Time	$t_{AC_LOW_DBC}$			40		ms
	Debounce Time to Detect AC Unplug	t_{UNPLUG_DBC}			100		ms
	Input OVP	HV_{TH_OVP}		426	446	468	V
Input OVP Debounce Cycles	N_{HV_OVP}			4			
VCC	VCC Turn-On Threshold	V_{CC_ON}	V_{CC} rising	18	20	22	V
	VCC Turn-Off Threshold	V_{CC_OFF}	V_{CC} falling	6.5	7.0	7.5	V
	VCC Short Threshold	$V_{CC_SHORT_TH}$		0.5	0.7	0.8	V
	VCC Regulation Threshold	V_{CC_REG}		10	11	12	V
	VCC Regulation Hysteresis (Note 4)	V_{CC_REGHYS}			2.0		V
	Protection Timer after Error Trigger	t_{ERROR}			1.0		s
	VCC OVP Threshold	V_{CC_OVP}	V_{VCC} rising	26.4	28.0	29.6	V
	VCC OVP Debounce Cycles	N_{VCCOVP_DBC}			4		
	VCC Shunt Threshold	V_{CC_SHUNT}		25	27	29	V
	VCC Shunt Current Capability	I_{VCC_SHUNT}	$V_{CC} > V_{CC_SHUNT}$		10		mA
	Normal Operation Current Consumption	$I_{CC_OPERATING}$	$C_L = \text{open}$, $f_{SW} = 50\text{kHz}$		1.2		mA
	Standby Current Consumption	$I_{CC_STANDBY}$	$V_{COMP} < V_{TH_SLEEP_IN}$	280	400	520	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
FMAX	Frequency Set	f _{MAX}	R > 260kΩ		60		kHz
			R = 100kΩ		156		
			R < 52kΩ or Floating	270	300	320	
CS	Maximum Peak Current Limit Threshold if Secondary Side Short	V _{CS_MAX}		685	720	755	mV
	Leading Edge Blanking for V _{CS_MAX}	t _{CS_LEB1}			150		ns
	Delay Time from V _{CS_MAX} to PWM Off	t _{CSMAX_DELAY}			30		ns
	V _{CS_MAX} Debounce Cycles	N _{VCSMAX_DBC}			4		
	VCS Limit	V _{CS_LIMIT1}	AC Low	475	500	525	mV
	VCS Limit	V _{CS_LIMIT2}	AC High	425	450	475	mV
	Leading Edge Blanking Time for V _{PK} Control and V _{CS_LIMIT}	t _{CS_LEB2}			250		ns
	Delay Time from V _{CS_LIMIT} to DRV Falling (Note 4)	t _{CS_DELAY2}			30		ns
	Delay Time from V _{PK} Control to DRV Falling	t _{CS_DELAY3}			30		ns
	VCS Minimum in DCM Mode	V _{CSMIN_DCM}		85	100	115	mV
	Soft-Start (Note 8)	t _{SST}			10		ms
	QR Mode Frequency of Modulation (Note 8)	f _{MODULATION_QR}			4		kHz
	V _{CSPK} Modulation Amplitude in QR Mode (Note 8)	V _{QR_MODULATION1}	Valley = 1–3		20		mV
			Valley = 4–6		30		mV
CS Short-Circuit Protection in Soft Start (Note 4)	V _{CS_SHORT}	t _{ON} = 6.2μs		60		mV	
ZCS	OVP Threshold Voltage	V _{ZCS_OVP}		2.36	2.50	2.64	V
	OVP Threshold Voltage Debounce Cycles	N _{ZCSOVP_DBC}			4		
	UVP Threshold Voltage of V _{OUT}	V _{ZCS_UVP}			150		mV
	UVP Threshold Voltage Debounce Time	t _{VOUTUVP_DBC}			20		ms
	Maximum Value of Off Blanking Time	t _{ZCSLEB_MAX}		1.65	2.3	2.95	μs
	Minimum Value of Off Blanking Time	t _{ZCSLEB_MIN}		0.65	0.9	1.3	μs
	Maximum Off-Time	t _{OFF_MAX}		90	120	150	μs
	Zero-Cross Point Detect	V _{ZCS_ZERO}			0		mV
	QR Turn-On Delay Time (Note 4)	t _{ZCS_ONDELAY}			100		ns

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Fault	Current Source for OTP Detection	I _{OTP}		42.5	45	47.5	μA
	OTP Threshold	V _{OTP_TH}		0.37	0.4	0.43	V
	OTP Exit Threshold (Note 4)	V _{OTPEXIT_TH}			0.43		V
	Clamp Diode for OVP	V _{OVDPDIODE}		1.00	1.20	1.40	V
	Capability of Clamp Diode for OVP (Note 8)	I _{RFAULTOVP}			1		mA
	OVP Threshold	V _{OVP_TH}			2.5		V
	Debounce Time to Trigger OTP/OVP	t _{FAULTOTP/OVP_DBC}	V _{FAULT} < V _{OTP_TH} V _{FAULT} > V _{OVP_TH}		200		μs
COMP	Internal Pullup Voltage Source	V _{COMP_PULLUP}		2.2	2.5	2.8	V
	Internal Pullup Resistor	R _{COMP_PULLUP}			20		kΩ
	V _{CS_LIMIT} Point (Note 4)	V _{COMP_LIMIT}			1.9		V
	QR Mode to DCM Change Threshold	V _{COMP_{TH}_DCM}			1.0		V
	Hysteresis of QR Mode to DCM	V _{COMP_{TH}_DCMHYS}			0.1		V
	Minimum Switching Frequency Threshold	V _{COMP_FMIN}		0.55	0.7	0.85	V
	Enter Burst Mode Threshold	V _{COMP_BURSTIN}	V _{COMP} falling	0.19	0.25	0.31	V
	Exit Burst Mode Threshold (Note 8)	V _{COMP_BURSTOUT}	V _{COMP} increasing		0.45		V
	Start PWM Threshold in Burst Mode	V _{COMP_BURSTSTART}	V _{COMP} increasing		0.35		V
	Burst Frequency	V _{COMP_BURSTFREQ}			1		kHz
	OLP Threshold	V _{COMP_OLP}	V _{COMP} rising	1.95	2.2	2.45	V
DRV	High Voltage Clamp	V _{DRV-CS_CLAMP}		6.0	6.3	6.6	V
	Programmable Driver Current	I _{DRV}	DVR-GND: 43kΩ		5		mA
			DVR-GND: 22kΩ		10		mA
			DVR-GND: 10kΩ		20		mA
			DVR-GND: < 2kΩ		Not supported		
	Sink Current (Note 4)	I _{DRV_SINK}			600		mA
	t _{ON_MAX}	t _{ON_MAX}		14	20	26	μs
Frequency Limit in DCM Mode	f _{LIMIT_DCM}			75		kHz	
Frequency Minimum in DCM Mode	f _{MIN_DCM}		20	25	32	kHz	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	DCM Mode Modulation Frequency	f _{MODULATION_DCM}			250		Hz
	Minimum Valley Number in QR Mode	VALLEY _{NUMBER}	HV < 218V	1		6	
			HV > 218V	1		6	
Internal OTP	OTP Threshold (Note 5)	T _{OVP_SHUTDOWN}			150		°C
	Recovery Threshold (Note 5)	T _{OVP_RECOVERY}			130		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A = T_J = 25^\circ\text{C}$. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: Meets ESDA/JEDEC JS-001-2017 and JEDEC78E.

Note 7: Increase VCC pin voltage gradually higher than V_{CC_ON} voltage, then reduce it to 13V.

Note 8: Application test result.

Detailed Description

HV Startup and Power Supply

The HV pin charges the VCC capacitor at AC power-on. When VCC voltage rises above V_{CC_ON} , the HV circuit will be turned off to reduce power loss.

HV will charge the VCC pins together during AC power-on. The suggested values for the VCC capacitors are 10 μ F and 1 μ F, respectively, which enable a small total solution size.

In situations when the device enters protection mode, the PWM operation is stopped for a t_{ERROR} time. Because of the power consumption during t_{ERROR} , the VCC capacitor voltages will drop. When VCC falls below V_{CC_REG} , HV circuitry is enabled again to charge the capacitors until $V_{CC} > (V_{CC_REG} + V_{CC_REGHYS})$. After t_{ERROR} , the internal logic will be reset, and a restart sequence is initiated.

QR Mode (Automatically Selected Valley Number between 1 and 6)

In QR mode, PWM turns on at the valley point of the GaN FET drain voltage. This improves EMI and efficiency. V_{CSPK} is controlled by V_{COMP} , and the valley number is controlled by the output load. When V_{COMP} is higher than $(V_{COMP_THDCM} + V_{COMP_THDCMHYS})$, QR mode is enabled and set to operate on the 6th voltage valley. As the load increases, the valley number decreases in one-step increments until it reaches the minimum value.

Valley Detect

The waveform in Figure 3 shows the valley detection method. When the falling edge of the zero-crossing voltage appears at the ZCS pin, the SQ33020Z will turn on the GaN FET after a delay.

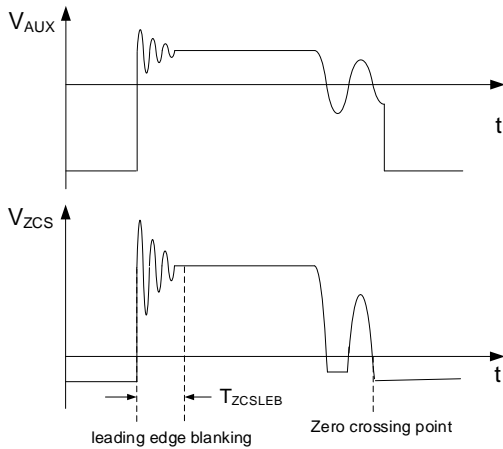


Figure 3. Valley Detection

Noise is present at the ZCS pin when the GaN FET turns off, which may affect valley detection. The SQ33020Z uses a blanking time to avoid noise interference, which is described in the Output OVP and UVP section.

DCM Mode

When V_{COMP} is lower than $V_{COMP_TH_DCM}$, discontinuous conduction mode (DCM) is enabled. In DCM, V_{CSPK} and the switching frequency are controlled by V_{COMP} . PWM turns on instantly at f_{SW} and does not wait for the valley point. As load decreases, frequency first decreases from f_{LIMIT_DCM} to f_{MIN_DCM} , and the device operates in Pulse Frequency Modulation (PFM) mode to maintain high efficiency. When the frequency has decreased to f_{MIN_DCM} and load continues decreasing, V_{CSPK} begins decreasing to keep constant output voltage.

Burst Mode

When frequency and V_{CSPK} have all decreased to respective minimum values, if the output load continues decreasing, V_{COMP} will be lower than $V_{COMP_BURSTIN}$. In this case the device starts operating in Burst mode. PWM will start when V_{COMP} is higher than $V_{COMP_BURSTSTART}$. The PWM number of switching cycles is controlled by t_{BURST} in order to keep burst frequency lower than the set value. PWM operation will continue until the set number of cycles are completed. PWM then stops and waits for the next rising edge of $V_{COMP_BURSTSTART}$. With this method, the burst frequency is low, and audible noise is reduced.

When V_{COMP} is higher than $V_{COMP_BURSTOUT}$, the SQ33020Z will enter DCM mode.

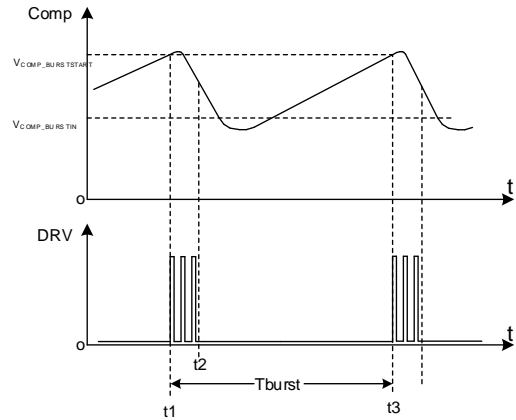


Figure 4. Quiet Burst

VCC Power Supply

Figure 5 shows a typical VCC supply circuit. During the X capacitor discharge process, C11 voltage will be charged to V_{CC_SHUNT} . In this case, a 35V capacitor voltage rating is recommended.

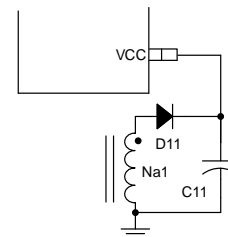


Figure 5. Typical Circuit for One-Winding Application

X Capacitor and Frequency Modulation Configuration using the ZCS Resistor

The frequency modulation and X capacitor discharge functions can be selected using the ZCS resistor. When the X capacitor is enabled, HV should be connected to the AC line via two diodes. When the X capacitor is disabled, HV can be connected to V_{BUS} to eliminate the diodes and reduce solution cost.

Table 1. ZCS Resistors Configuration

ZCS Pulldown (R8)	X Capacitor Function	Frequency Modulation
15-16kΩ ±1%	Disabled	Disabled
8.2kΩ ±1%	Enabled	Disabled
4.3kΩ ±1%	Disabled	Enabled
2.0-2.2kΩ ±1%	Enabled	Enabled

The ZCS_OVP threshold is 2.50V. With R8 selected, R7 can be calculated according to V_{OUT_OVP} and N_a/N_s . The resistor R4, in series with CS should be adjusted as well. If I_{OUT_OLP} (application dependent) increases when V_{AC} is rising, the value of R4 should be increased for more compensation.

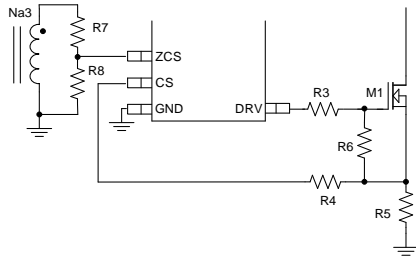


Figure 6. X Capacitor and Frequency Modulation using ZCS Resistor

Programmable Drive Current

During turn-on, the SQ33020Z uses constant current to charge the input M1 capacitance C_{GS} and improve EMI performance. During turn-off, the DRV pin will be pulled down quickly to reduce turn-off loss. Traditional drive resistors and diodes are not required. R3 is used to make slight adjustments to the turn-off speed. The recommended value of R3 is 5Ω–20Ω.

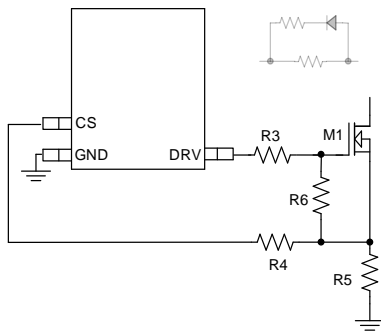


Figure 7. Drive Circuit of GaN FET

At turn-on, the constant current value can be selected using R6 based on the Table 2.

Table 2. Constant Current Value

R6	Constant Current
10kΩ	20mA
22kΩ	10mA
43kΩ	5mA
<2kΩ	Not Supported

The device enters protection mode for R6 values below 2kΩ where PWM switching is disabled.

Using a lower current, the GaN turn-on speed will be slower and EMI performance will be better. R6 value is measured during startup, and the current value is fixed until the following startup.

Frequency Limit Curve

For QR mode operation, when load decreases, switching frequency will increase. This will also increase switching loss, so the FMAX pin can be used to limit the maximum frequency. The relationship between frequency limit and the FMAX pin resistor is shown in Figure 8.

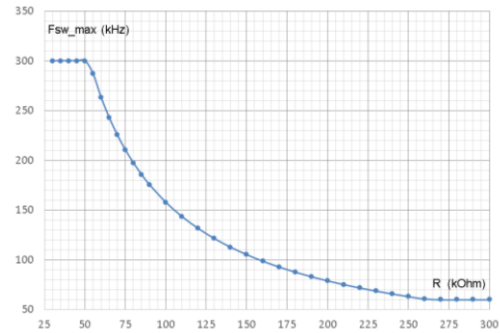


Figure 8. Frequency Limitation Curve

When the FMAX pin is floating, or if the resistor is lower than 30kΩ, the frequency limit is 300kHz. When frequency limit is triggered, PWM will turn on at the next valley.

Frequency Modulation

In QR mode, the SQ33020Z adds a triangle voltage on V_{CS} for frequency modulation. If the valley number is between 1 and 3, the modulation amplitude is set to 20mV. If the valley number is between 4 and 6, the modulation amplitude is set to 30mV in order to obtain an effective range of frequency modulation.

Soft-Start

At startup, when V_{COMP} rises to $V_{COMP_BURSTSTART}$, PWM operation starts and V_{CS} increases from the minimum value linearly. Under heavy load or V_{OUT} short conditions, soft-start will terminate after t_{SST} . Under light load or no-load conditions, when the V_{CS} value determined by V_{COMP} is lower than the value determined by soft-start, soft-start will terminate and V_{COMP} will control V_{CS} .

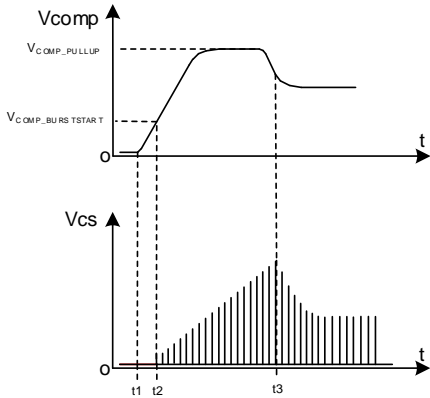


Figure 9. Soft-Start Process

Under startup or V_{OUT} short conditions, V_{OUT} and ZCS are very low. If ZCS cannot detect an effective valley signal, t_{OFF_MAX} will be enabled. This is helpful to reduce deep CCM switching and reduce the V_{DS} on the SR MOSFET.

V_{CS_LIMIT}

After t_{CS_LEB2} during every cycle, when V_{CS} is higher than V_{CS_LIMIT} , PWM will turn off immediately. The decision is made cycle by cycle and will not affect the next cycle's PWM on-time.

V_{CS_MAX}

Under normal operating conditions, V_{CS_LIMIT} can limit GaN peak current and provide sufficient protection. When the transformer winding or the secondary diode short circuits, the current slope is very high and the transformer will enter saturation. The current can rise to a much higher level during t_{CS_LEB2} .

The SQ33020Z can detect V_{CS} after t_{CS_LEB1} , which is shorter than t_{CS_LEB2} . If V_{CS} is higher than V_{CS_MAX} for four consecutive cycles, PWM operation stops and the timer starts. After t_{ERROR} , the logic is reset and a restart is triggered, with HV charging VCC to V_{CC_ON} .

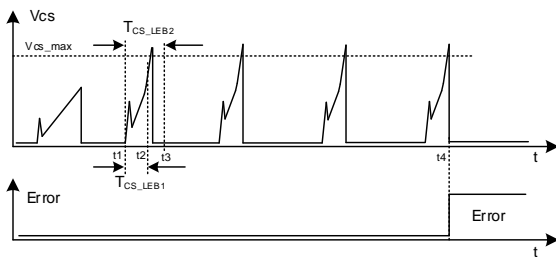


Figure 10. V_{CS_MAX} Process

X Capacitor Discharge

Under light load, when the charger is unplugged from the AC source, there may be remaining high voltage on the input terminals, which can represent a safety concern.

The SQ33020Z uses the HV pin to discharge the X capacitor. HV is connected to the AC side through R1, D1, and D3. The recommended R1 value is 5k Ω –10k Ω , which protects against surge voltages on the AC line.

If there is no HV rising edge for the duration of t_{UNPLUG_DBC} , an AC unplug condition is detected and PWM stops. HV sources an I_{HV_XCAP} current to the VCC pin. As a result, VCC rises to V_{CC_SHUNT} and HV falls linearly. When VCC becomes lower than V_{CC_OFF} , the discharge stops.

The voltage rating of the VCC capacitor should be higher than V_{CC_SHUNT} . A 35V voltage rating is recommended.

During X capacitor discharge, when a rising edge on HV (indicating AC re-plug) is detected, the discharge is terminated immediately. The t_{ERROR} timer continues. During t_{ERROR} , HV keeps VCC between V_{CC_REG} and $(V_{CC_REG} + V_{CC_REGHYS})$. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

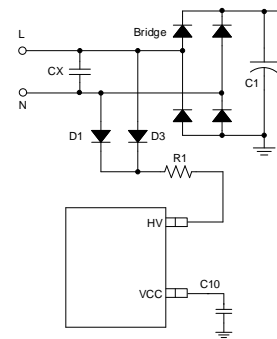


Figure 11. X Capacitor Discharge Circuit

Figure 12 shows the discharge waveforms:

- At t_1 , AC unplug occurs.
- At t_2 , AC unplug is confirmed. PWM stops and HV sources current to VCC.
- At t_3 , VCC rises to V_{CC_SHUNT} .
- At t_4 , X capacitor discharge current is lower than VCC dissipation and VCC begins falling.
- At t_5 , VCC is lower than V_{CC_OFF} and the discharge stops.

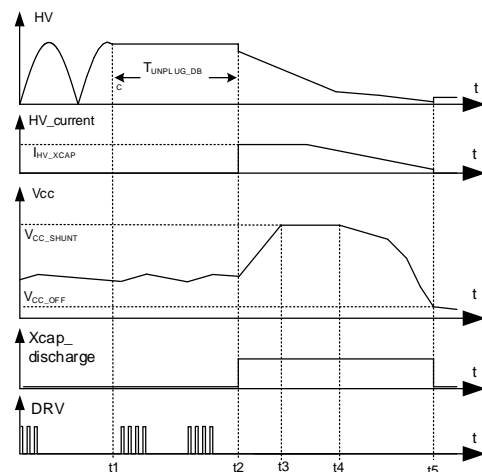


Figure 12. X Capacitor Discharge Waveforms

Output OVP and UVP

The SQ33020Z detects the output voltage through the ZCS pin and provides output overvoltage protection (OVP) and undervoltage protection (UVP). When the primary GaN FET turns off, there is a parasitic resonance on AUX winding. The SQ33020Z uses blanking time to avoid false triggering. Blanking time is adaptive according to V_{CSPK} . When V_{CSPK} is below 200mV, primary current is low and energy stored in leakage inductance is also low. Parasitic resonance on auxiliary winding will be shorter, and blanking time is also shorter. Blanking time increases to the maximum value as V_{CSPK} rises to 500mV.

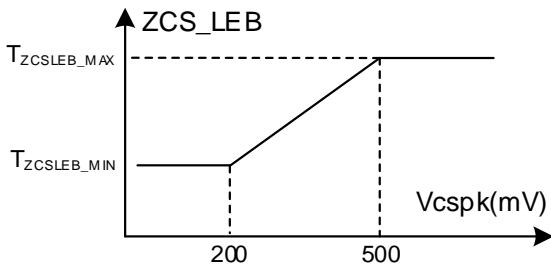


Figure 13. ZCS Blanking Time

When ZCS voltage is higher than V_{ZCS_OVP} for N_{ZCSOVP_DBC} cycles, ZCS_OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

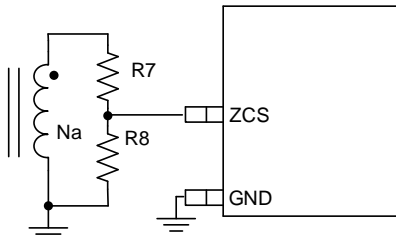


Figure 14. ZCS OVP Setting

Output OVP threshold is calculated as follows:

$$V_{OUT_OVP} = V_{ZCS_OVP} \times \frac{R7 + R8}{R8} \times \frac{N_s}{N_a}$$

When ZCS voltage is lower than V_{ZCS_UVP} continuously for a $t_{VOUTUVP_DBC}$ period, ZCS_UVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

Note: The pulldown resistor R8 value should be selected first, based on use of the X capacitor and frequency modulation settings. Then, R7 should be calculated according to the above equation. UVP is used to avoid continuous operation under V_{OUT} short-circuit conditions and is not mandatory for the design.

VCC OVP

The SQ33020Z provides VCC overvoltage protection (OVP) to protect the IC from abnormal high voltage caused by an open feedback loop or improper N_A winding. When VCC rises to V_{CC_SHUNT} and external power current capability is higher than the shunt ability, VCC can continue rising.

VCC is continuously monitored. If VCC is higher than V_{CC_OVP} for four continuous cycles, VCC OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

If the error condition still exists after restart, the IC will operate in hiccup mode.

Open-Loop Protection

If the output is short-circuited, the optocoupler circuit is open, or the load increases too much, V_{COMP} will increase. When V_{COMP} is higher than V_{COMP_OLP} and lasts for t_{OLP_DBC} , open-loop protection (OLP) is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

FAULT OTP and OVP

The FAULT pin can be used to detect OVP and overtemperature protection (OTP) conditions. During normal operation, the current of I_{OTP} is clamped by D12. D12's clamp voltage is selected to be between the OTP threshold and OVP threshold. Therefore, neither protection is triggered.

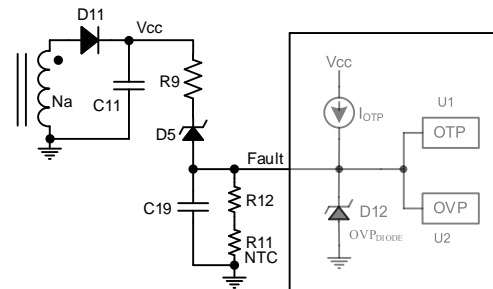


Figure 15. Fault OTP and OVP

Under fault conditions, VCC or VCCH will rise. In this case if D5 also fails, the pullup current might be higher than D12's clamp ability and the FAULT pin voltage will increase. When the voltage becomes higher than V_{OVP_TH} and lasts for $t_{FAULTOTP/OVP_DBC}$, FAULT OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

R11 is a negative temperature coefficient (NTC) resistor. As temperature rises, R11 resistance falls. When R11 resistance is low enough, there will be no current flowing into D12 and the I_{OTP} current will flow into R11. As I_{OTP}

does not change, FAULT voltage will fall along with R11 resistance. When FAULT voltage is lower than V_{OTP_TH} , FAULT OTP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} . After restart, the FAULT pin is monitored, and PWM will not begin until FAULT voltage is higher than $V_{OTPEXIT_TH}$.

R9 is used to limit the current flowing into the FAULT pin. The OVP threshold is primarily decided by D5 breakdown voltage. R12 is used to adjust the OTP threshold. C19 is used to filter noise, with a recommended value of 100pF.

CS Pin Short-Circuit in Soft-Start

In the soft-start process, during t_{ON} of every PWM cycle, V_{CS} is sampled every $4\mu s$ and compared with V_{CS_SHORT} . If $V_{CS} < V_{CS_SHORT}$, short-circuit protection is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

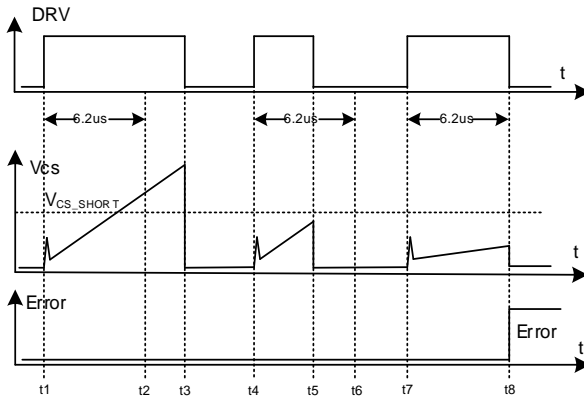


Figure 16. CS Short Protection

Figure 16 shows the short-protection logic:

- At t_2 , V_{CS} is higher than V_{CS_SHORT} . No protection.
- At t_5 , the $6.2\mu s$ timer has not expired. No comparison is needed. No protection.
- At t_8 , V_{CS} is lower than V_{CS_SHORT} at $6.2\mu s$ mark. Protection is triggered.

Input OVP Function

When HV is greater than HV_{TH_OVP} for N_{HV_OVP} cycles plus a set delay, Input OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

Internal OTP

The SQ33020Z continuously monitors the die temperature during normal operation. When the die temperature rises above the OTP threshold, PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON} .

Design Guide

BUS Capacitor Calculation

Generally, bulk capacitor C_{BUS} is selected according to the following rules:

- No PFC: 1.5–1.8 μF per watt (output power).
- With PFC: 0.5–0.8 μF per watt (output power).

Minimum BUS Voltage Calculation

Minimum BUS voltage appears when input voltage V_{AC} is lowest and output current reaches its rated value. When there is no power factor correction (PFC) circuit before the flyback, minimum BUS voltage is calculated as follows:

$$V_{BUS_MIN} = \sqrt{2V_{IN_MIN}^2 - \frac{P_o(1-K_{CH})}{\eta C_{BUS} f_o}}$$

where K_{CH} is the BUS capacitor charge coefficient (generally K_{CH} is set to 0.2–0.3), η is conversion efficiency, and f_o is the AC input frequency.

When selecting the necessary capacitors, the following aspects must be considered: The actual capacitance for aluminum capacitors is only 85-90% of nominal value and component tolerance must be considered.

The following examples are helpful for fast selection and can be used as a reference.

For a 30W solution with no boost PFC circuit, bus nominal capacitance is 27 + 27 μF . V_{BUS_MIN} is as follows:

Output Power	30W	35W	40W	45W
AC90V 50Hz	86V	80V	75V	68V
AC90V 60Hz	93V	87V	83V	78V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

For a 66W solution with no boost PFC circuit, under full load (20V, 3.3A) V_{BUS_MIN} is as follows:

Bus Nominal Capacitance	82 + 22 μF	82 + 10 μF	82 μF	68 μF
AC90V 50Hz	82V	78V	72V	60V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

For a 140W solution with boost plus flyback topology, output is 28V, 5A. Bus nominal capacitance is 39+39 μF .

At 90VAC, 50Hz, boost PFC outputs 240VDC. V_{BUS} is 222V (min) to 253V (max). Ripple is 31V.

At 176VAC, 50Hz, boost PFC outputs 350VDC. V_{BUS} is 338V (min) to 362V (max). Ripple is 24V.

Transformer Parameters Calculation

1. Primary/secondary turns ratio: N_{PS}

N_{PS} is limited by voltage stress on the primary GaN FET:

$$N_{PS} \leq \frac{V_{MOS_BR} K_{DR} - \sqrt{2} V_{IN_MAX} - \Delta V_{SN}}{V_O + V_{D_F}}$$

where V_{MOS_BR} is the breakdown voltage of the primary GaN FET; K_{DR} is the V_{DS} de-rating factor of the power MOS; V_{IN_MAX} is always 264VAC; V_{D_F} is the forward voltage of the secondary rectification diode (if SR is used on the secondary side, use $V_{D_F} = 0$); ΔV_{SN} is the voltage spike at primary GaN turn-off. A starting value of 50V can be used for the calculation.

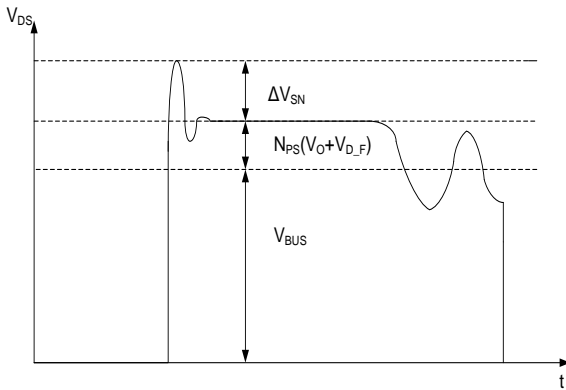


Figure 17. Primary V_{DS} Waveform

After N_{PS} is determined, the reflected voltage can be calculated as follows:

$$V_{OR} = N_{PS} \times (V_O + V_{D_F})$$

2. Primary Inductance: L_P

The SQ33020Z operates in QR and DCM modes (The device doesn't support CCM operation). The transformer primary inductance is mainly related to switching frequency. With V_{BUS} at its minimum value, L_P can be calculated as follows:

$$L_P = \frac{1}{2 \times f_{SW_MIN} \times V_O \times I_O} \times \left(\frac{V_{BUS_MIN} \times V_{OR}}{V_{BUS_MIN} + V_{OR}} \right)^2$$

where V_O is the output voltage and the unit is V; N_{PS} is the primary/secondary turns ratio; V_{BUS_MIN} is the minimum voltage after the bridge (V); f_{SW_MIN} is the frequency at V_{BUS_MIN} (kHz); I_O is the output current (A); L_P is the primary inductance (mH).

The parameters, V_O , N_{PS} , V_{BUS_MIN} and I_O have been determined. Only f_{SW_MIN} needs to be selected. When

f_{SW_MIN} is higher, L_P will be lower. The frequency for 230VAC designs will also be higher.

For a typical application, f_{SW_MIN} is approximately 100kHz-130kHz, at V_{BUS_MIN} (usually 80V-90V). Then, frequency at V_{BUS_MAX} (370V) is approximately 160kHz-220kHz.

3. Turns of primary winding: N_P

- Select the magnetic core, confirm the effective core area (AE)
- Select B_{MAX} for the magnetic core (0.32T-0.36T)
- Calculate primary R_{CS} (preliminary):

$$R_{CS} = \frac{V_{CS_LIMIT} \times N_{PS} \times V_{BUS_MIN}}{2 \times I_{OUT_OLP} \times (V_{OR} + V_{BUS_MIN})}$$

where V_{CS_LIMIT} is 0.5V and I_{OUT_OLP} is the overload protection threshold, which is selected based on the maximum current that the converter needs to deliver. For example, when the maximum current required is 3A, a value of 3.5A can be used for I_{OUT_OLP} .

- Calculate maximum primary peak current

$$I_{PPK_MAX} = \frac{V_{CS_LIMIT}}{R_{CS}}$$

- Calculate primary turns: N_P

$$N_P = \frac{L_P \times I_{PPK_MAX}}{B_{MAX} \times A_E}$$

4. Turns of secondary winding: N_S

$$N_S = \frac{N_P}{N_{PS}}$$

In the actual design, f_{SW_MIN} is difficult to determine. If a random value is selected, later calculations may be difficult and might lead to selecting an unsuitable transformer bobbin. The following flow is suggested, for reduced number of iterations and predictable results:

- Select transformer and AE
- Determine winding width of the bobbin
- Select N_S wire gauge
- Determine N_S
- Determine V_{OR} and N_{PS}
- Calculate N_P
- Select N_P wire gauge
- Calculate R_{CS}

9. Calculate I_{PPK_MAX}
10. Determine B_{MAX}
11. Calculate L_P

With this procedure, f_{SW_MIN} is not an input parameter. When L_P is calculated, the switching frequency f_{SW} is determined as well. This will always lead to a satisfactory design, and efficiency will always be close to optimal for a given transformer.

5) Turns of auxiliary winding: N_A

For fast charge applications, V_{OUT} range is wide. Turns of AUX winding should take V_{OUT_MAX} and V_{OUT_MIN} into consideration.

Increasing efficiency is possible by using two AUX windings if a slight increase in BOM cost is acceptable.

- AUXL can supply V_{CC} at V_{OUT_MAX} .
- $18V < \frac{V_{OUT_MAX}}{N_S} \times N_{AUXL} < 22V$
- AUXH can supply V_{CC} at V_{OUT_MIN} .
- $10V < \frac{V_{OUT_MIN}}{N_S} \times N_{AUXH} < 14V$

In low-cost applications, one winding (AUXH) is sufficient. The number of turns for the AUXH winding is the same as N_{AUXH} in the above formula.

Secondary Rectifier MOSFET Selection

Under the conditions of V_{BUS_MAX} and V_{OUT_OVP} , the reverse voltage of the secondary rectification MOSFET will reach its maximum level. The maximum voltage (ignoring the voltage spike when the primary MOSFET is turned on) is calculated as follows:

$$V_{D_R_MAX} = \frac{\sqrt{2}V_{IN_MAX}}{N_{PS}} + V_{O_OVP}$$

Maximum instantaneous forward current is calculated as follows:

$$I_{SPK_MAX} = I_{PPK_MAX} \times N_{PS}$$

For a 66W (20V, 3.3A) solution, BSC098N10NS5 is recommended, which has a rating of 100V, 8.2mΩ ($V_{GS} = 10V$).

For a 90W (20V, 4.5A) solution, BSC0805LS is recommended, which has a rating of 100V, 6.0mΩ ($V_{GS} = 10V$).

For a 120W (20V, 6.0A) solution, two MOSFETs in parallel are recommended, primarily for heat dissipation. Two BSC098N10NS5 MOSFETs are recommended, which have a rating of 100V, 8.2mΩ ($V_{GS} = 10V$).

Ensure that the MOSFET selected can handle the dissipated heat without exceeding the target acceptable temperature increase. Validate the design performing temperature measurements under worst-case load and ambient temperature conditions.

Layout Considerations

Follow these PCB layout guidelines for optimal performance and EMI considerations:

- Signals are grouped into two categories: switching nodes and important signal nodes:
 - Switching nodes: primary drain/AUX/core; secondary drain/AUX/core.
 - Important signal nodes (sensitive):
 - Primary: V_{CS} , FAULT, comp, ZCS, f_{MAX} , etc.
 - Secondary: REG, TZ (TZ pin of SQ33239), feedback loop, etc.
- To guarantee normal operation, important signal nodes should be far away from switching nodes. If PCB routing is difficult, static nodes should be used as shielding between switching and signal nodes. Static nodes can be V_{BUS} , GND, VCC, V_{OUT} , SGND, etc.
- In order to optimize EMI performance, switching nodes loops on the PCB layout should be as small as possible. Switching nodes should not be selected for heat sinking, such as GaN drain.
- In order to obtain good EMI performance, the main current loop should be as small as possible.
 - Current path during t_{ON} : bus capacitor → transformer → GaN → R_{CS} → GND → bus capacitor
 - Current path during t_{OFF} time: transformer → SR_MOS → C_{OUT} → GND → transformer
 - Current in leakage inductance and snubber circuit
 - Drive loop of primary and secondary MOSFETs
- Place these components near SQ33020Z:
 - Fault capacitor, comp capacitor, f_{MAX} resistor, CS resistor (in series), VCC

capacitor.

- ZCS pullup resistor should be placed near the AUX pin of the transformer, and pulldown resistor should be near the ZCS pin.
1. The REG and TZ resistors, V_{DD} and V_{IN} capacitors should be close to SQ33239.
- GND routing is as follows:
 - SQ33020Z GND should be connected to

RCS_GND in order to get accurate V_{CS} signal.

- Because $V_{GS(TH)}$ of the GaN FET may be as low as 1.2V, it can be falsely triggered by noise. To reduce noise interference use the following rules:
 - Connect IC_GND to RCS_GND directly.
 - Keep the drive loop as small as possible.

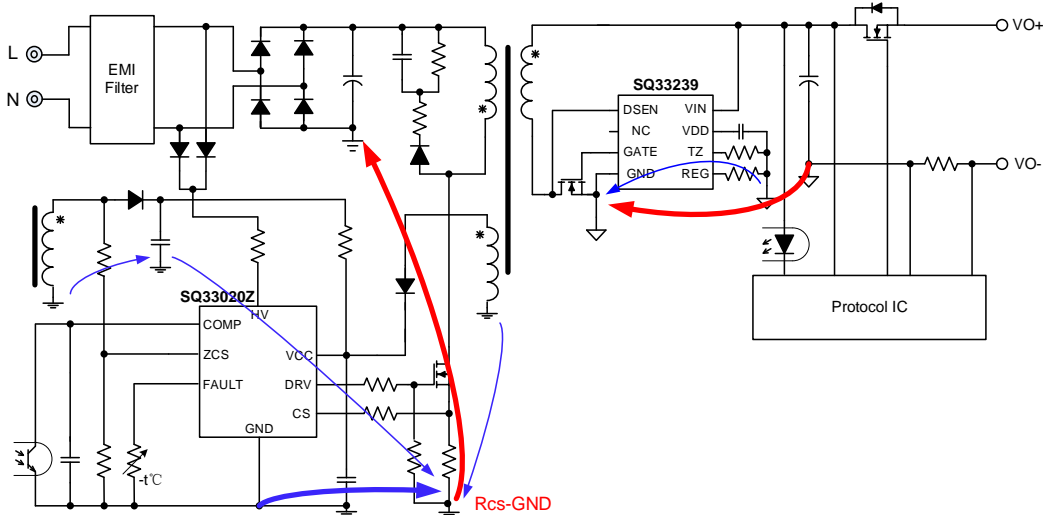


Figure 18. Recommended PCB Layout

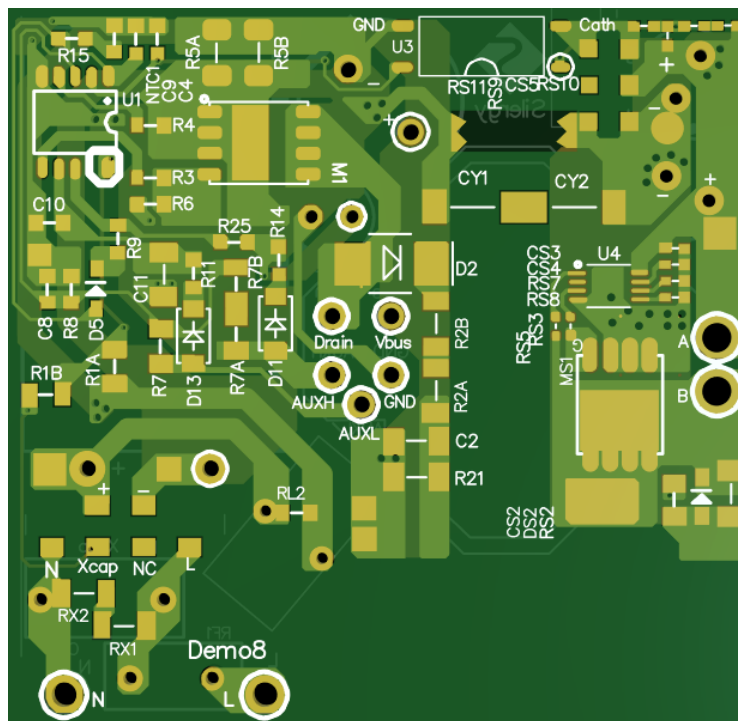


Figure 19. Bottom Layer of Recommend PCB Layout

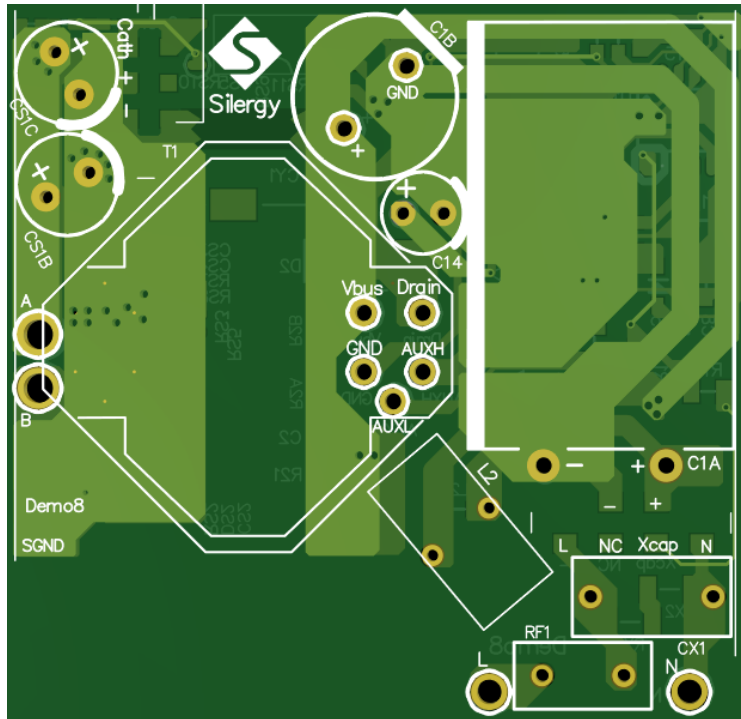


Figure 20. Top Layer of Recommend PCB Layout

Design Example

This section provides a step-by-step design example of a typical application.

Input/Output Specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	90V–264V
Rated output power	P_O	66W
Rated output voltage	V_O	5V–20V
Output OVP level	V_{O_OVP}	24V
Rated output current	I_O	3.3A
OLP	I_{OLP}	4.04A
Efficiency	η	93%

Design Parameters

Parameter	Symbol	Value
Breakdown voltage of power MOS	V_{MOS_BR}	650V
V_{DS} de-rating factor of power MOS	K_{DR}	90%
Spike on V_{DS} at power MOS turn-off	ΔV_{SN}	70V
BUS capacitor charge coefficient	K_{CH}	0.2
Secondary diode forward voltage drop	V_{D_R}	0V (SR)
Transformer effective A_e (RM8)	A_E	62 mm ²

1. BUS capacitor selection

Select BUS capacitor: $C_{BUS} = 104\mu F$ (1.57 $\mu F/W$)

2. Minimum BUS voltage calculation

BUS capacitor charge coefficient: $K_{CH} = 0.2$

$$V_{BUS_MIN} = \sqrt{2V_{IN_MIN}^2 - \frac{P_o(1-K_{CH})}{\eta C_{BUS} f_o}} = \sqrt{2 \times 90^2 - \frac{66 \times (1-0.2)}{93\% \times 104 \mu \times 60}} = 84V$$

3. Transformer design

a. Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS} \leq \frac{V_{MOS_BR} K_{DR} - \sqrt{2} V_{IN_MAX} - \Delta V_{SN}}{V_o + V_{D_F}} = \frac{650 \times 0.9 - \sqrt{2} \times 264 - 70}{20 + 0} = 7.1$$

N_{PS} is selected as: $N_{PS} = 6.25$, Reflected voltage $V_{OR} = 6.25 \times 20V = 125V$.

b. Calculate L_P of the transformer: Select $f_{SW_MIN} = 110kHz$

$$L_P = \frac{1}{2 \times f_{SW_MIN} \times V_o \times I_o} \times \left(\frac{V_{BUS_MIN} \times V_{OR}}{V_{BUS_MIN} + V_{OR}} \right)^2 = \frac{1}{2 \times 110kHz \times 20V \times 3.3A} \times \left(\frac{84 \times 125}{84 + 125} \right)^2 = 0.174mH$$

c. Calculate R_{CS} : In normal operation.

$$R_{CS} = \frac{V_{CS_LIMIT} \times N_{PS} \times V_{BUS_MIN}}{2 \times I_{OUT_OLP} \times (V_{OR} + V_{BUS_MIN})} = \frac{0.5 \times 6.25 \times 84}{2 \times 4.04 \times (125 + 84)} = 0.155ohm$$

d. Calculate maximum primary peak current:

$$I_{PPK_MAX} = \frac{V_{CS_LIMITL}}{R_{CS}} = \frac{0.50}{0.155} = 3.23A$$

e. Calculate primary winding turns N_P : $B_{MAX} = 0.354T$

$$N_P = \frac{L_P \times I_{PPK_MAX}}{B_{MAX} \times A_E} = \frac{170\mu H \times 3.23A}{0.354T \times 62mm^2} = 25ts$$

f. Calculate secondary winding turns N_S :

$$N_S = \frac{N_P}{N_{PS}} = \frac{25}{6.25} = 4$$

g. Calculate auxiliary winding turns $N_{AUXL} = 4ts$: $V_{OUT_MAX} = 20V$

$$18V < \frac{V_{OUT_MAX}}{N_S} \times N_{AUXL} < 22V, \quad 3.6 < N_{AUXL} < 4.4$$

h. Calculate auxiliary winding turns $N_{AUXH} = 10ts$: $V_{OUT_MIN} = 5V$

$$10V < \frac{V_{OUT_MIN}}{N_S} \times N_{AUXL} < 14V, \quad 8 < N_{AUXH} < 11.2$$

4. Secondary diode selection

a. Maximum reverse voltage calculation:

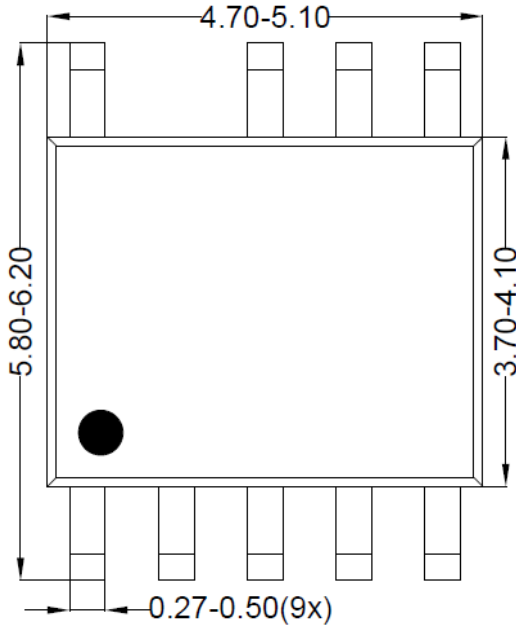
$$V_{D_R_MAX} = \frac{\sqrt{2} V_{IN_MAX}}{N_{PS}} + V_{O_OVP} = \frac{\sqrt{2} \times 264}{6.25} + 24 = 84V$$

Considering the voltage spike, reverse voltage rating is recommended to be 100V–120V.

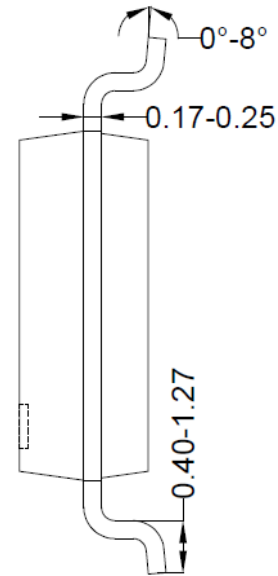
b. Maximum instantaneous forward current:

$$I_{SPK_MAX} = I_{PPK_MAX} \times N_{PS} = 2.45A \times 6.25 = 15.3A$$

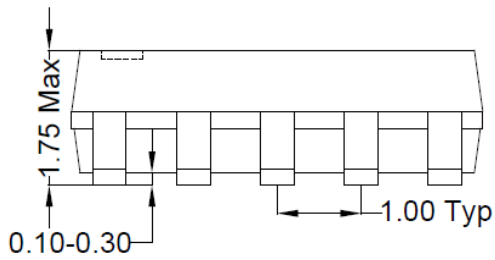
SSOP9 Package Outline Drawing



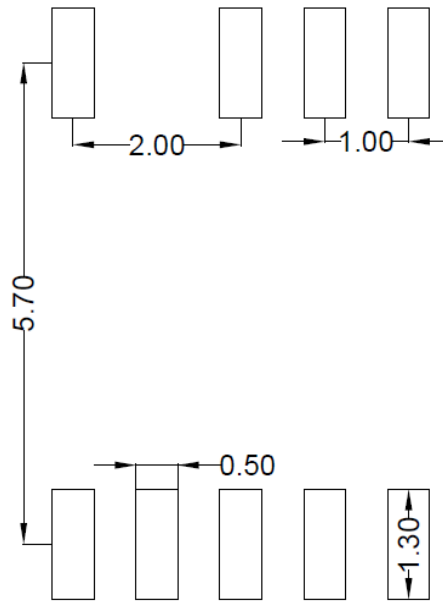
Top view



Side view



Front view

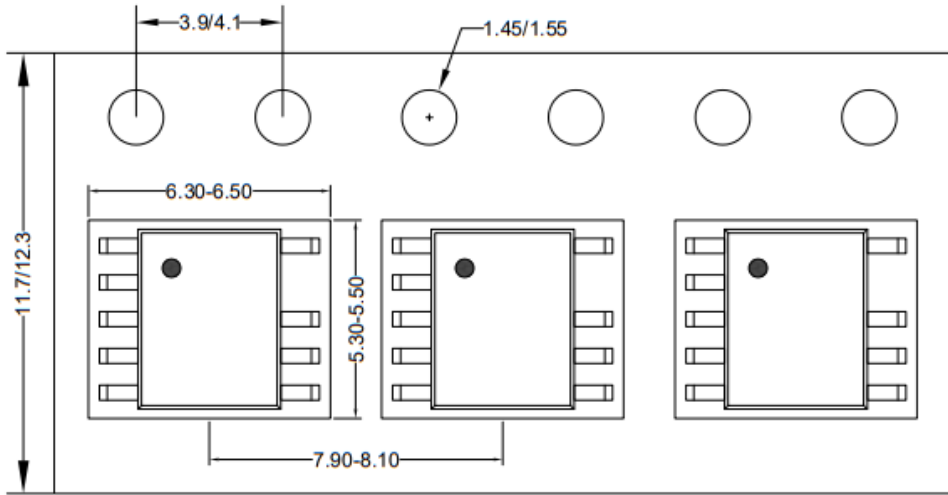


**Recommended PCB layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

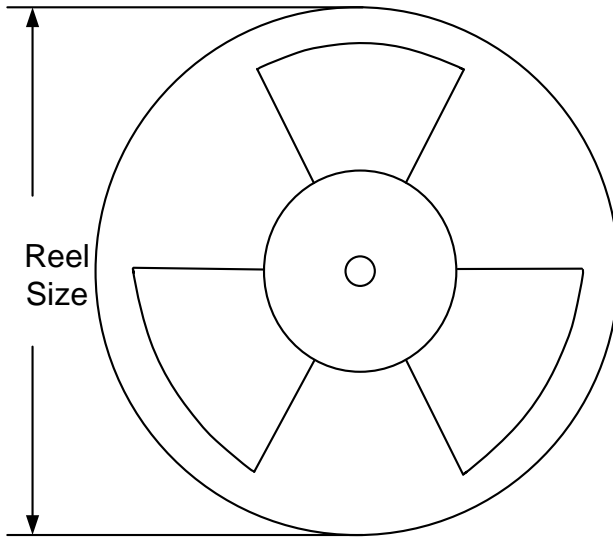
Tape and Reel Specification

Tape Orientation



Feeding Direction →

Reel Specification for packages



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
SSOP9	12	8	13"	400	400	4000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
April 21, 2025	Revision 1.0	Initial Release

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