SY5236/SY5236A

ZVS Flyback SR Controller

General Description

SY5236/A is a Flyback synchronous rectifier (SR) controller with high performance capabilities. It is suitable for continuous conduction mode (CCM), discontinuous conduction mode (DCM) and quasi-resonant (QR) mode Flyback converter.

The SY5236/A adopts proprietary operation mode to achieve Flyback zero voltage switching (ZVS) turn-on, which can greatly improve Flyback efficiency and power density. The SY5236/A also adopts the adaptive gate voltage control for safe operation.

SY5236/A uses DRAIN sense (DSEN) voltage falling slope rate detection to avoid SR MOSFET false turn on caused by parasitic ringing in DCM or QR mode.

During light load conditions, the controller enters power saving mode to improve light load efficiency.

The SY5236/A is available in a SOT23-6 package.

Features

- Suitable for CCM, DCM and QR Mode Flyback Converter
- Proprietary Operation Mode for Flyback ZVS
- DSEN Pin Sensing up to 200V
- DSEN Falling Slope Rate Detection to Avoid False Turn on of SR MOSFET by Parasitic Ring
- DSEN High Voltage Blanking Time Detecting to Enhance System ESD Performance
- Dual Power Supply Channels for 3V to 30V Output Systems
- Power Saving Mode to Improve Light Load Efficiency
- Up to 500kHz Switching Frequency
- 10ns Typical Turn off Propagation Delay
- 2A Sink, 0.5A Source Gate Driver Capability
- Compact Package: SOT23-6

Applications

- Smart Phone Fast Chargers
- AC/DC Adapters and Auxiliary Power Supplies

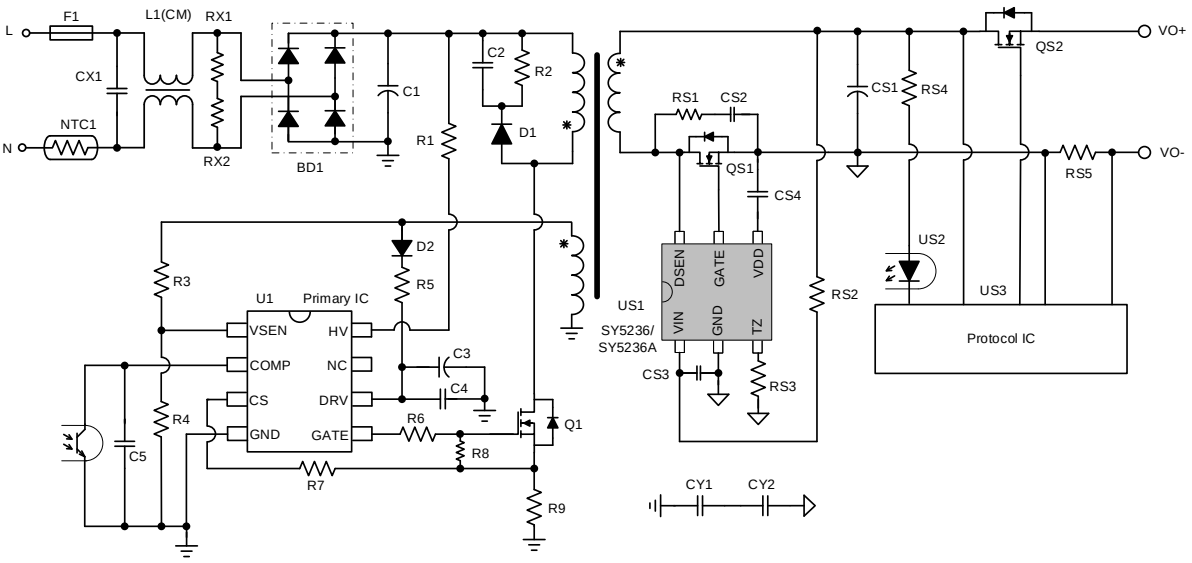


Fig. 1(a) Typical Application Circuit (SR MOSFET Location: Low Side)

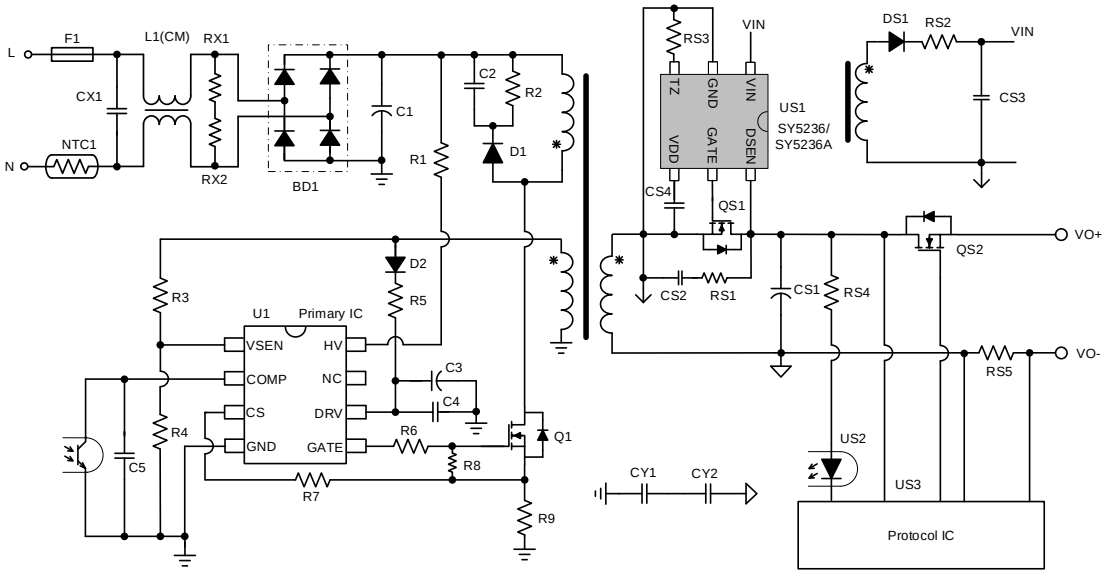


Fig. 1(b) Typical Application Circuit (SR MOSFET location: High Side)

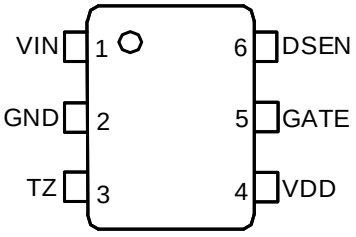
Fig. 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Output Voltage	Package type	Top Mark
SY5236ABT	3V~12V	SOT23-6 RoHS-Compliant and Halogen-Free	**HNE*xyz***
SY5236AABT	3V~30V		**KTQ*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	VIN	Power supply pin, connect it to the output of converter when a low-side SR MOSFET is used.
2	GND	Connect this pin to SR MOSFET Source terminal.
3	TZ	Connect a resistor to setting ZVS on time.
4	VDD	Output of internal LDO, power supply for control unit and gate drive circuit, It is recommend to connect a 1μF ceramic capacitor between the VDD and GND pins.
5	GATE	Connect this pin to the Gate terminal of the SR MOSFET.
6	DSEN	This pin should be connected to the DRAIN of SR MOSFET for voltage sensing. This pin is also used as a power supply option.

Block Diagram

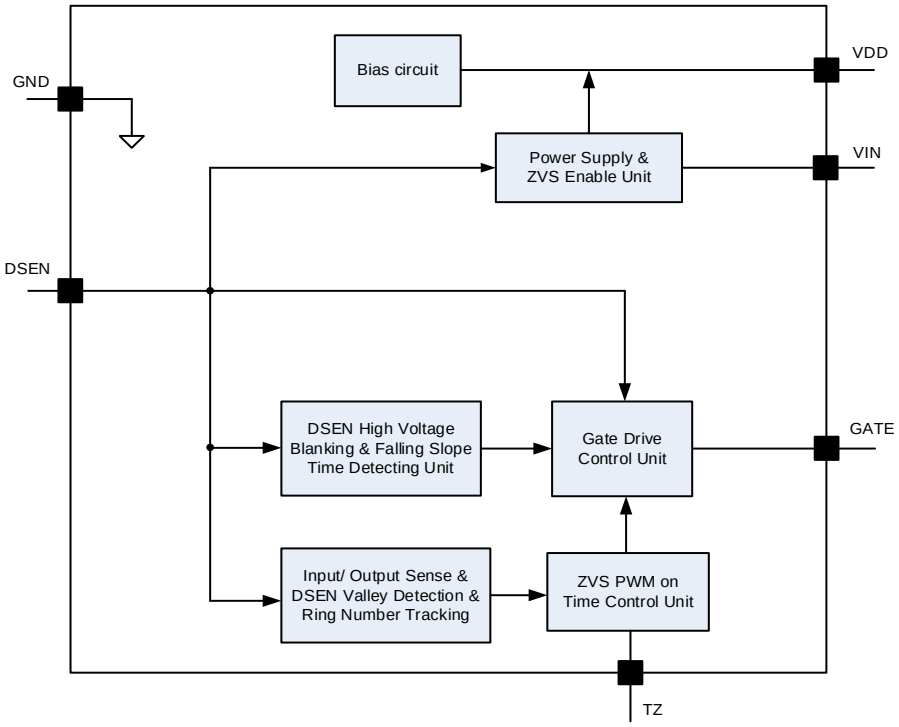


Fig.2 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	38	V
TZ	-0.3	5	
VDD, GATE	-0.3	16	
DSEN	-1	200	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		170	°C/W
θ_{JC} Junction-to-case Thermal Resistance		130	
P_D Power Dissipation T_A = 25°C		0.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	2.8	30	V
DSEN	-1	150	
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{VDD}=9V, T_J=25℃, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Pin	VIN Power Supply Channel and ZVS Enable Threshold	V_{VIN_VINSPY}	V_{VIN} is rising	4.35	4.65	4.9	V
	DSEN Power Supply Channel and ZVS Disable Threshold	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.25	4.55	4.8	V
VDD Pin	VDD ON Threshold	V_{VDD_ON}		3.45	3.65	3.85	V
	UVLO Hysteresis	V_{VDD_HYS}		150	250	350	mV
	VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8	8.75	9.5	V
	VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		6.3	6.8	7.3	V
	Operating Current	I_{VDD_OP}	V_{VDD}=9V,C_{GATE}=2.2nF , F_{SW}=100kHz		2.5	3.2	mA
	Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHG\_MAX}$	VIN pin is active to charge VDD capacitor	30	40		mA
			DSEN pin is active to charge VDD capacitor	40	50		mA
	Quiescent Current	I_Q	Under Sleep Mode		85	110	μA
DSEN Pin	Low Level Threshold to Enable Slope Detection(Note5)	V_{DSEN_LTH}	V_{DSEN} is falling	-20	0	20	mV
	V_{DS} Regulation Voltage	V_{DS_REG}	SR MOSFET is conducting	-55	-40	-25	mV
	SR Turn off Threshold	V_{OFF_TH}	V_{DSEN} is rising	-15	0	15	mV
	Force Turn off Threshold	V_{FORCE_TH}	V_{DSEN} is rising	40	57	75	mV
	Enter Sleep Mode Time Threshold	t_{SLP_TH}		60	80	100	μs
TZ Pin	ZVS on Time Program Coefficient	k_{TZ}	SY5236		6		10^{-12}
			SY5236A		4.5		10^{-12}
	ZVS V_{BULK} Enable Threshold	$V_{BULK\_EN\_TH}$	V_{BULK} is rising, SY5236	22	24	26	V
			V_{BULK} is rising, SY5236A	34.5	38	41.5	V
	ZVS V_{BULK} Disable Debounce Time	t_{DIS_DBC}	V_{BULK} is falling	13.5	20	26.5	ms
GATE Pin	GATE Pin Clamped Current before VDD ON	I_{CLP}	Vgs=1V	160	200		mA
	Max. Source Current	I_{SOURCE_MAX}	V_{VDD}=9V, C_{LOAD}=2.2nF, Vgs from 1V to 6V	0.375	0.5		A
	Max. Sink Current	I_{SINK_MAX}	V_{VDD}=9V, C_{LOAD}=2.2nF, Vgs from 6V to 1V	1.5	2		A
	Minimum ON Time	t_{ON_MIN}		750	1000	1250	ns
	Minimum OFF Time	t_{OFF_MIN}		300	450	600	ns
	Turn on propagation Delay Time(Note5)	t_{DLY_ON}	C_{GATE}=2.2nF		30	50	ns

	Turn off propagation Delay Time(Note5)	t_{DLY_OFF}	C_{GATE}=2.2nF		10	20	ns
OTP	Thermal Shutdown Temperature (Note5)	T_{SD}			165		°C
	Hysteresis to Resume Operating (Note5)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz two-layer JEDEC standard board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested. [Note 5 may be omitted if all EC parameters are tested in production.]

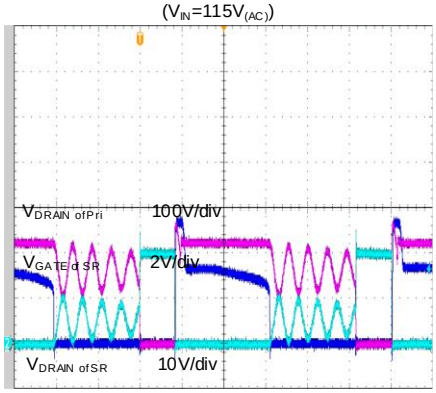
Typical Performance Characteristics

(Test condition: input voltage: 90Vac~264Vac; output spec: 5Vdc_3A, 11Vdc_5A/7.3A; Includes SR controller SY5236ABT; Ambient temperature: 25±5℃; Ambient humidity: 65±25%.)

5Vdc_3A Output

Steady States

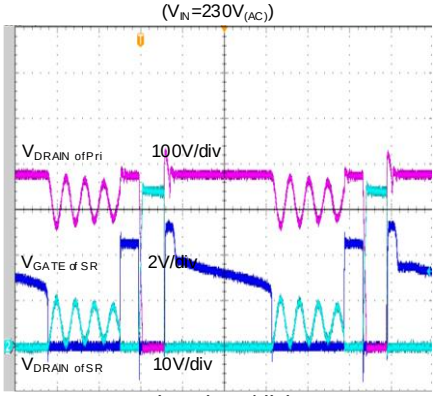
(V_{IN}=115$V_{(AC)}$)



Time (4μs/div)

Steady States

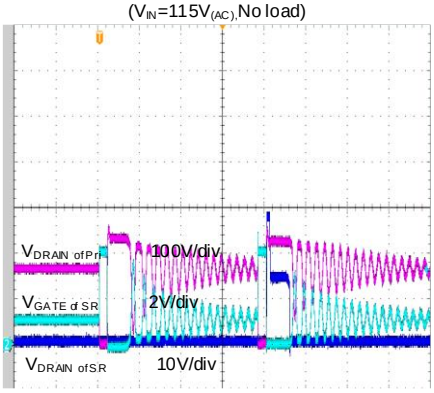
(V_{IN}=230$V_{(AC)}$)



Time (4μs/div)

Steady States

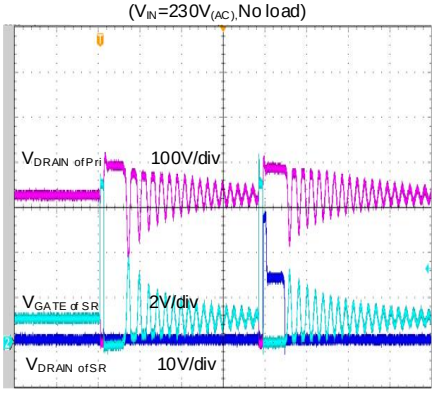
(V_{IN}=115$V_{(AC)}$,No load)



Time (10μs/div)

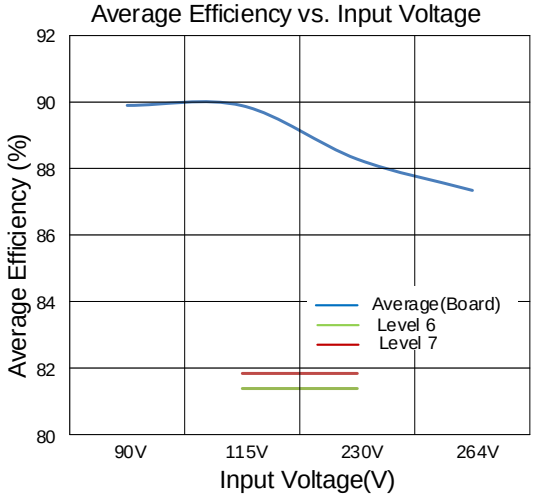
Steady States

(V_{IN}=230$V_{(AC)}$,No load)



Time (10μs/div)

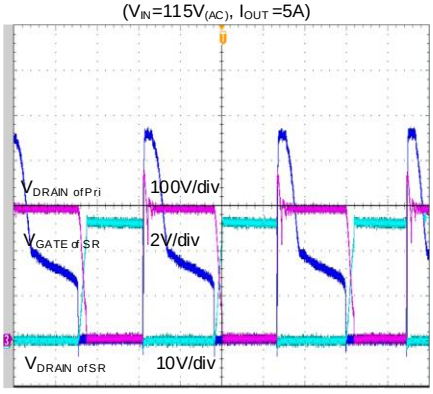
Average Efficiency vs. Input Voltage



11Vdc_5A/7.3A Output

Steady States

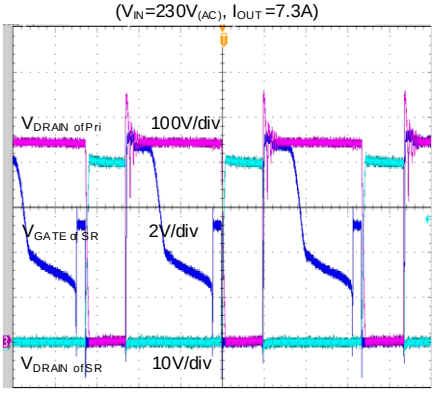
(V_{IN}=115$V_{(AC)}$, I_{OUT} =5A)



Time (4µs/div)

Steady States

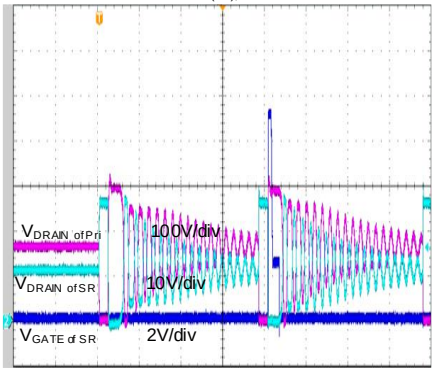
(V_{IN}=230$V_{(AC)}$, I_{OUT} =7.3A)



Time (4µs/div)

Steady States

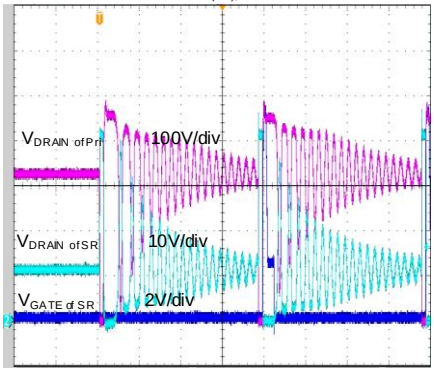
(V_{IN}=115$V_{(AC)}$,No load)



Time (10µs/div)

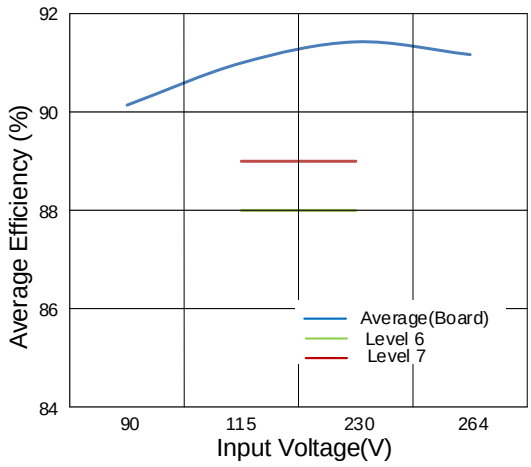
Steady States

(V_{IN}=230$V_{(AC)}$,No load)



Time (10µs/div)

Average Efficiency vs. Input Voltage



Detailed Description

Introduction

The SY5236/A is a Flyback SR controller with high performance capabilities. During high line input, the device compatible with QR mode converters for ZVS operation, it is suitable for the primary side PWM converters operating in QR and valley lock mode, where the valley lock number is between 1 and 6.

Using a proprietary architecture, the SY5236/A supports Flyback ZVS turn on, which can greatly improve the solution efficiency and increase power density, while using adaptive gate voltage control to ensure system reliability.

The SY5236/A can achieve ZVS function by SR MOSFET turned on twice in a switching cycle. After the secondary side continuous current is completed, ZVS PWM is turned on at the last ring valley, generating negative current to achieve the primary side ZVS.

To ensure safe operation, SR control functions include turn on/off control, V_{DS} regulation and slope programming. The ZVS function helps the primary side MOSFET to turn on at a low DRAIN voltage to reduce the switching losses, thereby increasing system efficiency and power density.

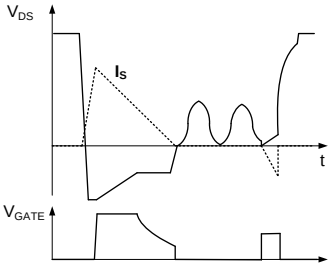


Fig. 3 SR Operation Diagram

GATE Drive

For proper operation, while $V_{VDD}<V_{VDD\_ON}$ the SR MOSFET gate is pulled down. The circuit in the diagram below is used for this purpose:

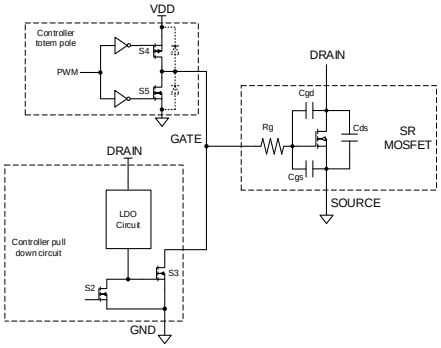


Fig. 4 Circuit Used for SR MOSFET Control during Start-up

When $V_{VDD}<V_{VDD\_ON}$, switch S2 is open and the DRAIN voltage will charge the Cgs capacitance for the S3 switch. When S3 turns ON, it will pull down the gate of the SR MOSFET. The pull down current of S3 is 200mA (@Vgs=1V for the POWER MOSFET) to optimize the performance.

While $V_{VDD}>V_{VDD\_ON}$, the S2 switch is closed, leading to S3 being turned OFF (switch open). The GATE pin will be controlled only by the driver circuit consisting of S4 and S5, as shown in Fig.4 & Fig.5.

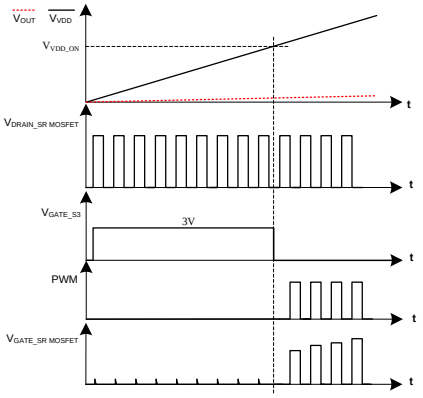


Fig. 5 GATE Pin Timing Diagram

SR Turn on

The traditional method of turning ON the SR MOSFET is to use a set turn-on threshold V_{ON_TH}.

When the DRAIN voltage falls and reaches V_{ON_TH}, the SR MOSFET is turned ON after a short delay.

While in DCM or QR operating modes, a resonant waveform may appear after the transformer secondary current decreases to zero. Sometimes, the amplitude of this resonant waveform can be large enough to cause the DRAIN voltage to drop below the turn-on threshold V_{ON_TH}, which may lead to the false turn-on of the SR MOSFET. To address this issue, a circuit to detect the falling slope rate of V_{DSEN} is used.

When the primary MOSFET is turned off, the V_{DRAIN} falling slope rate is very high, and the SR MOSFET will turn on. During the resonant phase, the V_{DSEN} falling slope rate is relatively low, and the SR MOSFET will not turn on. The SY5236/A uses a resistor divider circuit to sense the DRAIN voltage, where V_{PVS} is 0.02 x V_{DSEN}.

Two thresholds are set to sense the V_{PVS} falling slope rate. $\triangle t$ is the time duration measured when V_{PVS} is falling between the high-level threshold V_{PVS_HTH} and the low-level threshold V_{DSEN_LTH} (0mV). $\triangle t$ is compared with a falling slope reference time t_{REF} using a counter.

A blanking period is used to prevent external noise (such as ESD noise) from falsely turning on the SR MOSFET.

If V_{PVS} is above V_{PVS_HTH}, lasts for t_{PVS_BLK} (200ns) and the falling slope time $\triangle t < t_{REF}$, the IC considers this action as

a primary MOSFET turn-off event, and will turn ON the SR MOSFET after a short delay. In all other cases the SR MOSFET will not be turned ON.

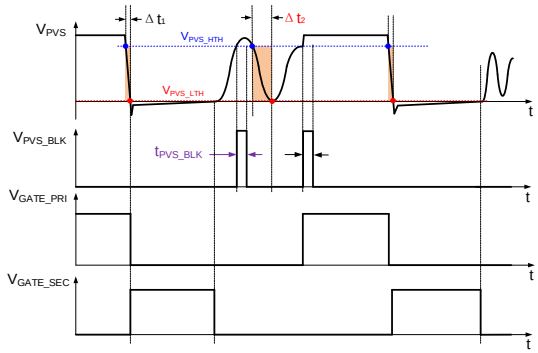


Fig. 6 SR MOSFET Turn ON Time Diagram

V_{PVS_HTH} is a dynamically adjusted value, and it has a value of 0.85 x V_{DSEN}. The falling slope ref time threshold t_{REF} is 95ns (typical value).

SR Gate Control

In DCM mode, the current through the SR MOSFET will decrease before the primary MOSFET is turned on. The closed-loop V_{DS} regulation circuit will gradually reduce V_{GATE} once V_{DS} is above the V_{DS_REG} (-40mV) level. As the current through the SR MOSFET decreases, V_{GATE} drops close to the turn off threshold of the SR MOSFET. At this point, the product of the (I_D x R_{DSON}) can no longer be regulated to V_{DS_REG}, causing V_{DS} to increase beyond V_{OFF_TH}. After a short time delay (t_{OFF_DLY}), a large sink current will pull down the gate voltage to zero to turn OFF the SR MOSFET.

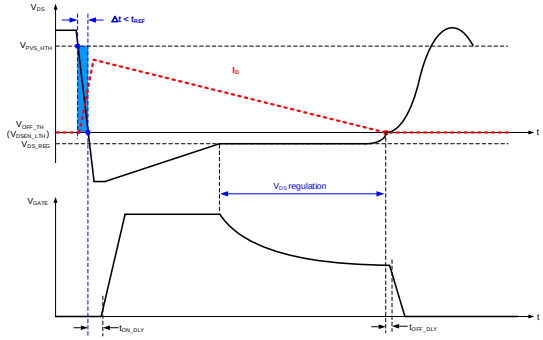


Fig. 7 SR MOSFET Control in DCM Mode

During the CCM mode, the primary MOSFET will be turned ON before secondary current decreases to ZERO, and V_{DS} will rapidly increase. The device will compare V_{DS} with another threshold V_{OFF_TH}, and once V_{DS} is rising and crossing V_{OFF_TH}, after a short delay time t_{OFF_DLY}, the gate voltage will be pulled down by a large sink current to achieve fast turn off. The turn off delay time t_{OFF_DLY} is designed to be very short to minimize the power loss caused by primary and secondary MOSFET overlap.

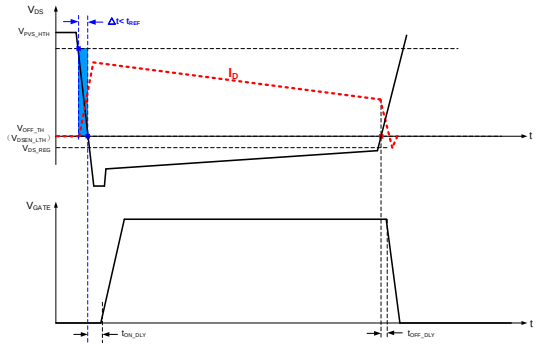


Fig. 8 SR MOSFET in CCM Mode

Dual Channel Power Supply

The device optimizes the overall efficiency by using two possible power sources during normal operation.

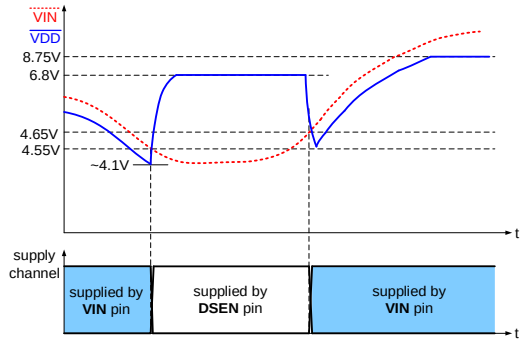


Fig. 9 Timing Diagram of Dual Channel Supply

Before VDD voltage reaches the V_{VDD_ON} threshold, the voltage is supplied by DSEN pin. When the voltage exceeds the V_{VIN_VINSPY} threshold, the VIN pin will be used instead.

As VIN increases, VDD will follow VIN (with about 0.5V voltage drop). When the voltage goes above 8.75V, the rail is regulated internally to this value.

When VIN is decreasing and crossing $V_{VIN\_DSENSPY}$, the device will switch to using the DSEN pin, and VDD will be regulated to 6.8V. The timing diagram is shown in Fig. 9.

Min ON Time & Min OFF Time

When the primary MOSFET is turned off, the DRAIN voltage of the secondary SR MOSFET will drop rapidly to about -700mV, due to the circuit parasitic resonance. To avoid false turn-off of the SR MOSFET, a blanking time t_{ON_MIN} is applied after the SR MOSFET is turned ON. During this blanking time, the GATE pin output is latched off.

After SR MOSFET is turned OFF, a ringing will appear on DRAIN voltage waveform. To avoid the internal logic circuit false trigger, a blanking time t_{OFF_MIN} used.

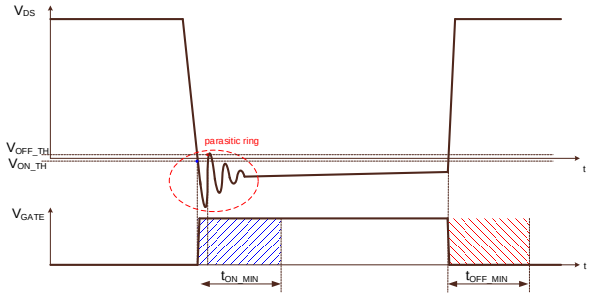


Fig. 10 Timing Diagram of Min ON/OFF Time

ZVS Operation

The key function of the SY5236/A is to achieve primary MOSFET ZVS turn on for high efficiency and high power density. The SY5236/A is compatible with primary side QR mode which has valley number lock operation mode to achieve this function.

The SY5236/A adopts a proprietary drive method to increase the resonant magnitude of switching node, which pulls primary DRAIN voltage (V_{DRAIN_PRI}) to approximately 50V to achieve primary side MOSFET ZVS conduction. The ZVS PWM is only activated in QR mode within 1~6 valleys. Beyond this range, ZVS is disabled.

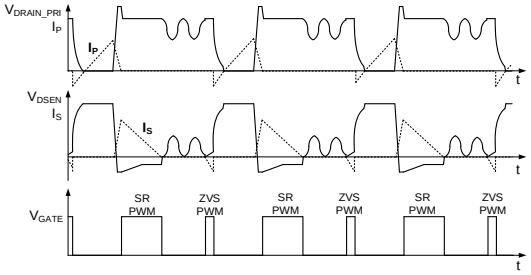


Fig. 11 ZVS Control Diagram

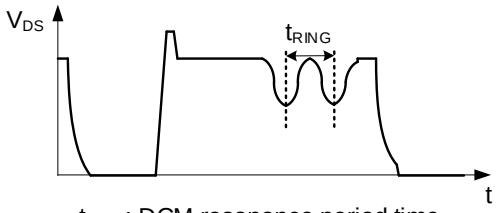
ZVS Coefficient TZ Resistor Setting

The ZVS performance is affected by transformer's magnetizing inductance (L_M) and the total equivalent capacitance (C_{SW}) of the switching node. For best efficiency, the resistor value connected between TZ and GND pins can be adjusted.

Method 1: Calculate the coefficient based on magnetizing inductance and equivalent switching node capacitance.

The resistor sets ZVS PWM turn on time. The value can be calculated using the following equation:

$$R_{TZ} = \frac{\sqrt{C_{SW} \cdot L_M}}{k_{TZ}} (\Omega)$$



t_{RING}: DCM resonance period time

Method 2: Calculate the coefficient based on DCM resonance time period.

$$R_{TZ} = \frac{t_{RING}}{2 \cdot \pi} \cdot \frac{1}{k_{TZ}} (\Omega)$$

The R_{TZ} should be adjusted slightly around the calculated value. The R_{TZ} value between 20kΩ and 82kΩ is recommended.

ZVS Enable

1. Power supply: when the VIN supply is active, ZVS will be enabled. When the DSEN supply is active, the ZVS will be disabled (the supply power loss is much higher when DSEN pin is used and the driving loss may be greater than ZVS effect).

2. Input voltage (V_{BULK}) condition: at low line input voltage, the efficiency is not significantly improved by using ZVS. To optimize operation, the input voltage range is limited to maximize ZVS effect. The input voltage range calculation is shown below:

ZVS enable: $V_{BULK} > N_{PS} \cdot V_{BULK\_EN\_TH}$ lasting for 120us

ZVS disable: $V_{BULK} < N_{PS} \cdot V_{BULK\_EN\_TH}$ lasting for 20ms

CCM+ZVS Application

During low line input, the primary side PWM converter may work in CCM state, SY5236/A disables ZVS function; During high line input, the primary side PWM converter disables CCM state and operates in the QR mode, when the ring number is between 1~6, SY5236/A enables ZVS turn on; when the ring number is larger than 6, SY5236/A disables ZVS turn on. To achieve better system reliability, it is recommended that the maximum CCM operating voltage below minimum ZVS operating voltage, leaving enough voltage gap to ensure that ZVS is enabled and CCM is disabled.

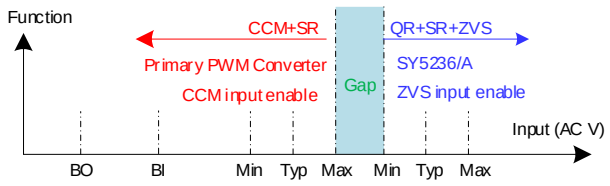


Fig. 11 ZVS Input Enable Diagram

The recommended ZVS minimum input voltage is shown below:

Part Number	N_{PS}	V_{BULK_MIN} with ZVS (N_{PS}*$V_{BULK\_EN\_TH\_MIN}$)
SY5236	$7 \le N_{PS} \le 12$	N_{PS}*22
SY5236A	$3 \le N_{PS} < 7$	N_{PS}*34.5

Therefore, the CCM maximum input voltage should be less than the minimum ZVS enable voltage with leaving enough voltage gap.

ZVS Protection

To guarantee operation of the ZVS function, the force turn off (V_{FORCE_TH}) and maximum on time (t_{ZVS_MAX}, 3.3us) during ZVS PWM is strictly limited to guarantee safety operation.

In external noise (for example: ESD noise), when the primary-secondary side is common, to prevent excessive ZVS current, the secondary side current will be limited during ZVS with force turn off, plus max on time.

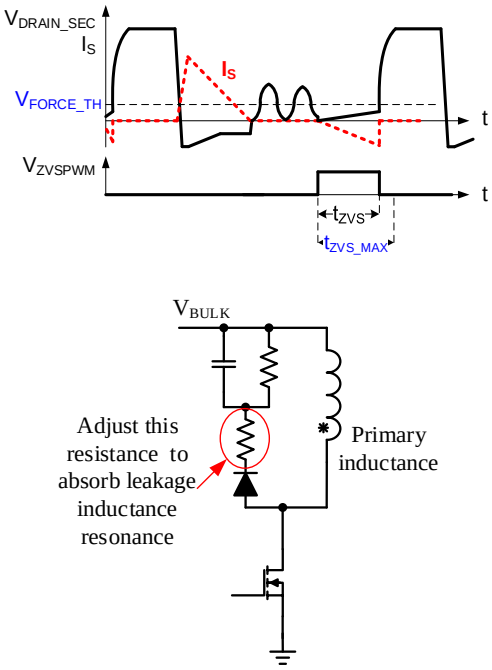


Fig. 12 ZVS Limit Protection

To prevent excessive ZVS current or primary side false turn on, the secondary current is limited during ZVS conduction. However, the primary leakage inductance resonance may false trigger the ZVS force turn off and cause the ZVS PWM early turned off. To avoid this situation, it is recommended to add a primary inductance resonance absorption resistor.

Power Saving Mode

Under light load conditions, the device will enter power saving mode to improve light load efficiency.

During the switching cycle, a timer will start to count after SR MOSFET is turned off. If the timer counts to 80us before next SR turn on, the device will enter power saving mode to reduce the overall power consumption. The device exits power saving mode on the next SR MOSFET turn on time.

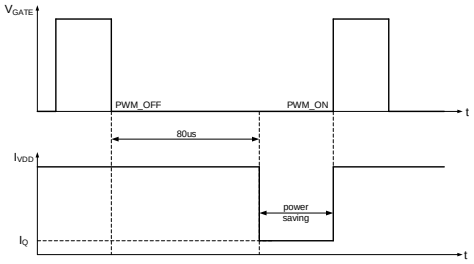


Fig. 13 Power Saving Mode Timing Diagram

OTP

The internal die temperature is continuously monitored. If the die temperature rises above 165℃, the device stops switching the SR MOSFET and keep gate voltage to 0V. When the die temperature drops below 145℃, it resumes normal operation.

Typical Application Schematic

Typical application circuit information is displayed in an 80W (11V7.3A output) PD Flyback design. The PD charger circuit includes SR controller (SY5236ABT).

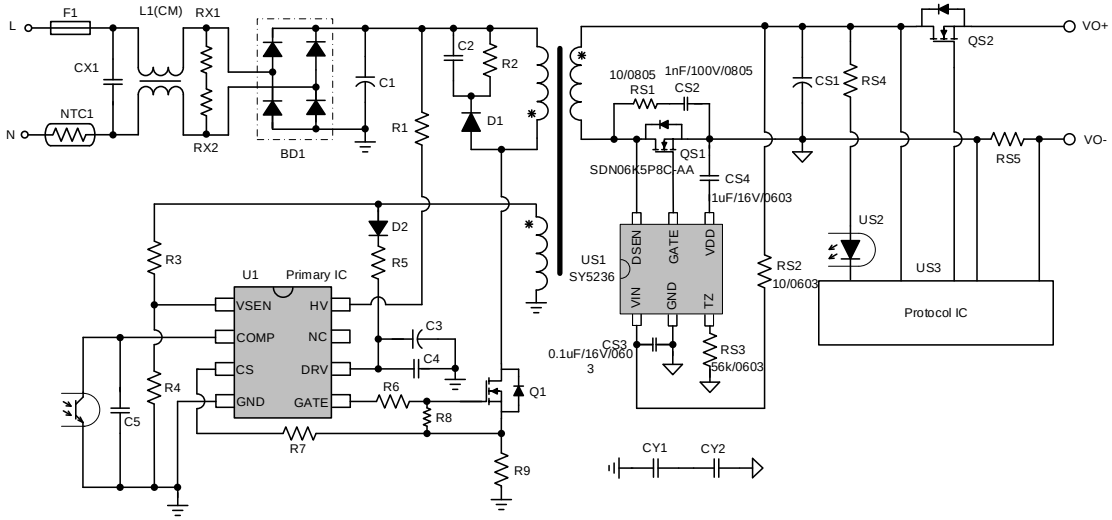


Fig. 14 80W PD Typical Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
RS1	10Ω/0805	0805W8F100JT5E	UNI-ROYAL
RS2	10Ω/0603	0603WAF100JT5E	UNI-ROYAL
RS3	56kΩ/0603	0603WAF4702T5E	UNI-ROYAL
CS2	1nF/100V/X7R, 0805	CC0805KRX7R0BB102	YAGEO
CS3	0.1uF/16V/X7R, 0603	CC0603KRX7R8BB104	YAGEO
CS4	1uF/16V/X7R, 0603	CC0603KRX7R0BB105	YAGEO
QS1	4.8mΩ/60V	SDN06K5P8C-AA	Silicon Magic
US1	SR Controller	SY5236ABT	Silergy

Design Procedure

SR MOSFET Selection

The MOSFET selection is based on optimizing the R_{DSON} verus Gate Charge losses.

Below a certain level, the R_{DSON} of the MOSFET doesn't directly reduce the conduction loss, because SY5236 uses a loop that regulates the voltage drop in the forward direction to around 40 mV across the drain-source terminals.

For optimal performance consider a minimum of 30% SR MSOFET conduction period at maximum load for optimal performance.

For example, for an 80W converter, the peak current of the SR MOSFET should be about 29A for 7.3A load current. To achieve a control time corresponding to 30% duty cycle, the R_{DSON} should be selected using the formula:

$$R_{DSON} \geq \frac{V_{DS\_REG}}{I_{PK\_SR} \times 0.3} = \frac{40mV}{8.7A} \approx 4.6m$$

For the MOSFET voltage rating, the maximum V_{DS} should be lower than breakdown derated voltage. For example, for the 80W converter example, the transformer turn ratio is 11 and the design the derating coefficient $K_{Derating}$ is 0.9.

The breakdown voltage of the MOSFET should be higher than the value calculated using the formula below:

$$V_{DS(BR)} \geq \frac{V_{DS\_MAX}}{K_{Derating}} = \frac{\frac{V_{BULK}}{N_{PS}} + V_{OUT} + \Delta V_{Spike}}{K_{Derating}} = \frac{\frac{373}{11}V + 11V + 10V}{0.9} = 57V$$

A 60V/4.8mΩ MOSFET is recommended for the above requirements.

Other considerations for selecting the right MOSFET are: overall efficiency, thermal performance, and cost.

Snubber Selection

The Snubber components RS1 and CS1 are used to damp the switching ringing caused by stray inductance L_{Stray} and equivalent capacitance C_{EQ} in the secondary switching loop.

The L_{Stray} can be tested using a LCR meter. The C_{EQ} can be calculated considering the switching ringing period, based on the formula:

$$C_{EQ} = \frac{T_r^2}{(2\pi)^2 \times L_{Stray}} = \frac{50ns^2}{(6.28)^2 * 100nH} = 634pF$$

Considering the Q of the circuit equal to 1, the snubber resistor RS1 can be calculated using the formula:

$$R_{RS1} = \frac{1}{Q}\sqrt{\frac{L_{stray}}{C_{EQ}}} = \sqrt{\frac{100nH}{634pF}} = 12.56\Omega$$

A value of 10 Ω can be selected in this case.

C_{CS1} will influence the spike of V_{DS} and thermal performance, C_{CS1} is set to 1nF after trade-off.

External Components Selection

When used in low-side configuration, the SY5236 uses two power inputs. VIN pin is one of the supply channels, and a reservoir capacitor, CS3, has to be connected close to this pin.

The recommended value and voltage rating for CS3 are:

0.1 μF/25V.

The recommended value for RS2 is 10 Ω.

The recommended value and voltage rating for CS4 in most applications are: 1uF/16V.

Layout Design

Follow the following PCB layout guidelines for optimal performance and thermal dissipation:

- Minimize the size of the switching loops: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.
- To achieve better EMI and Efficiency performance, use a decoupling capacitor between the output connector and the SR MOSFET output.
- To reduce ringing the parasitic inductance should be reduced by optimizing the layout, and/or increasing the RC snubber.

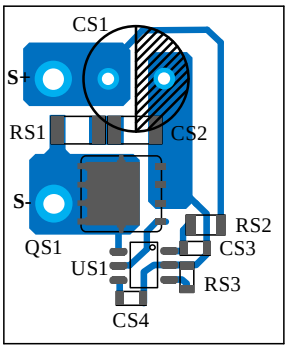
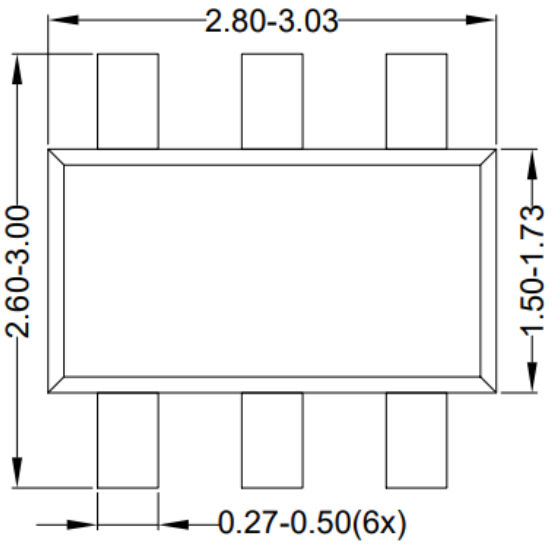


Fig.15 PCB Layout suggestion

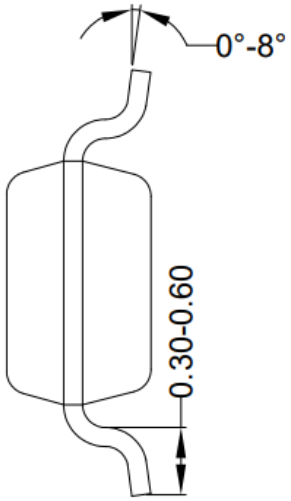
Design Notes:

1. To improve the system ESD performance, a 10Ω~51Ω resistor should be used in series between VIN pin and output terminal, and at least 100nF cap should be used in parallel between VIN pin and GND pin.
2. To achieve better system reliability, it is recommended that the maximum CCM operating voltage below minimum ZVS operating voltage, leaving enough voltage gap to ensure that ZVS is enabled and CCM is disabled.

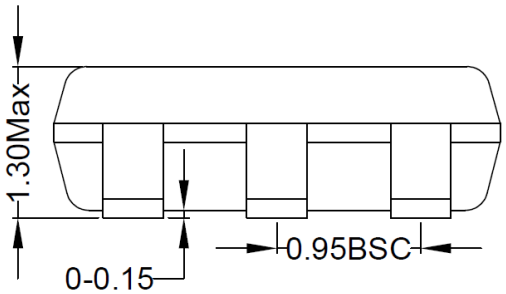
SOT23-6 Package Outline & PCB layout



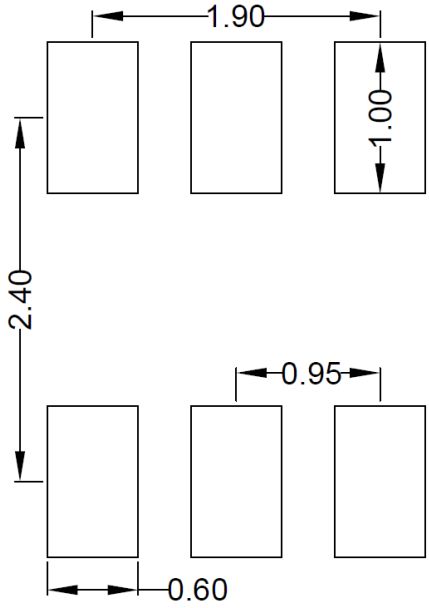
Top View



Side View



Front View

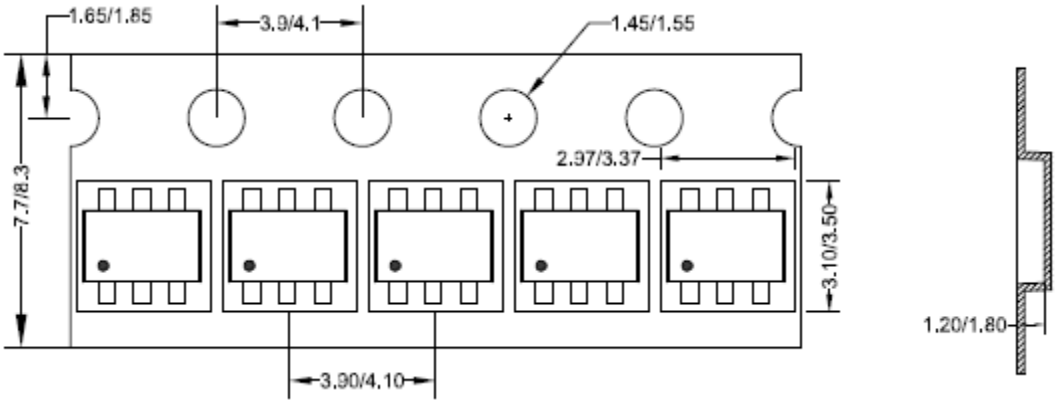


Recommended PCB Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

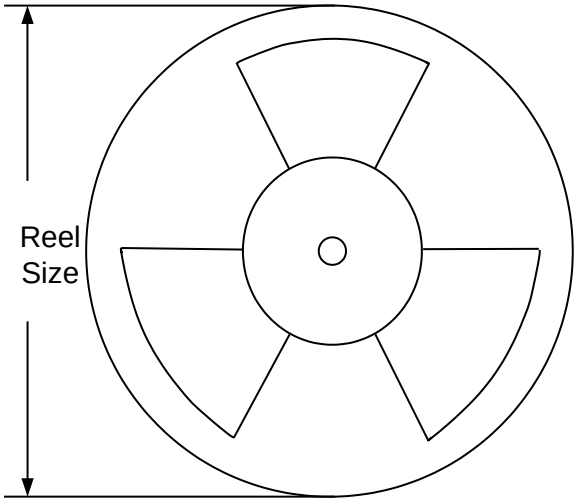
Taping & Reel Specification

1. Taping orientation for packages（SOT23-6）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
April 14, 2025	Revision 1.0	Initial Release
August 11,2025	Revision 1.0A	Update the EC table
May 22, 2026	Revision 1.0A1	Modify the CCM+ZVS application description

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