SQ33261

Dual-Channel LLC Synchronous Rectification Controller

General Description

The SQ33261 is a dual-channel synchronous rectification (SR) controller for LLC resonant converters.

The SQ33261 has extremely fast turn-off and high sink current capability, suitable for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The SQ33261 also integrates a dual-channel interlock function to prevent short circuits between the two channels and improve system reliability.

Under light load conditions, the SQ33261 will enter green mode, in which the gate driver is latched off to reduce driver loss and improve efficiency.

The SQ33261 is available in a compact SO8 package.

Features

- Dual-Channel SR Controller for LLC Resonant Converters
- Supports CCM, DCM Operation
- DA/DB Pins sensing up to 200V
- Wide 4.2V to 38V Power Supply Range
- 110µA Low Quiescent Current in Green Mode
- Dual-Channel Interlock to Prevent Short Circuit between Channels
- 15ns Fast Turn-Off Propagation Delay
- 1.7A Sink, 0.3A Source Gate Driver Capability
- Compact Package: SO8

Applications

- Gaming Adapters
- Desktop, All-in-One PCs
- AC/DC Adapters

Typical Application

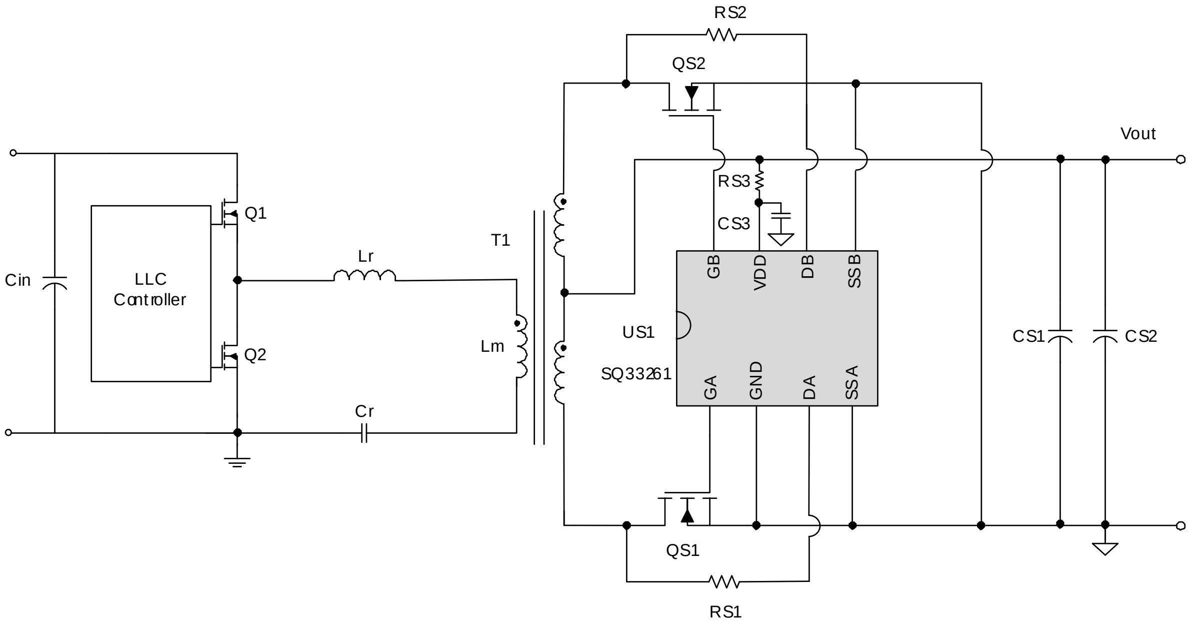


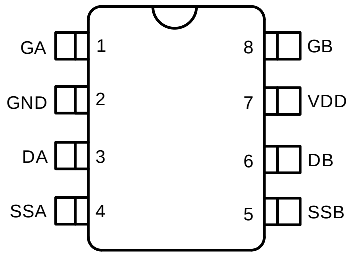
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ33261FAP	SO8 RoHS-Compliant and Halogen-Free	**AAGG*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	GA	Channel A gate driver pin
2	GND	Power ground
3	DA	Channel A drain voltage sense pin
4	SSA	MOSFET A source sense pin.
5	SSB	MOSFET B source sense pin.
6	DB	Channel B drain voltage sense pin
7	VDD	Power supply pin
8	GB	Channel B gate driver pin

Block Diagram

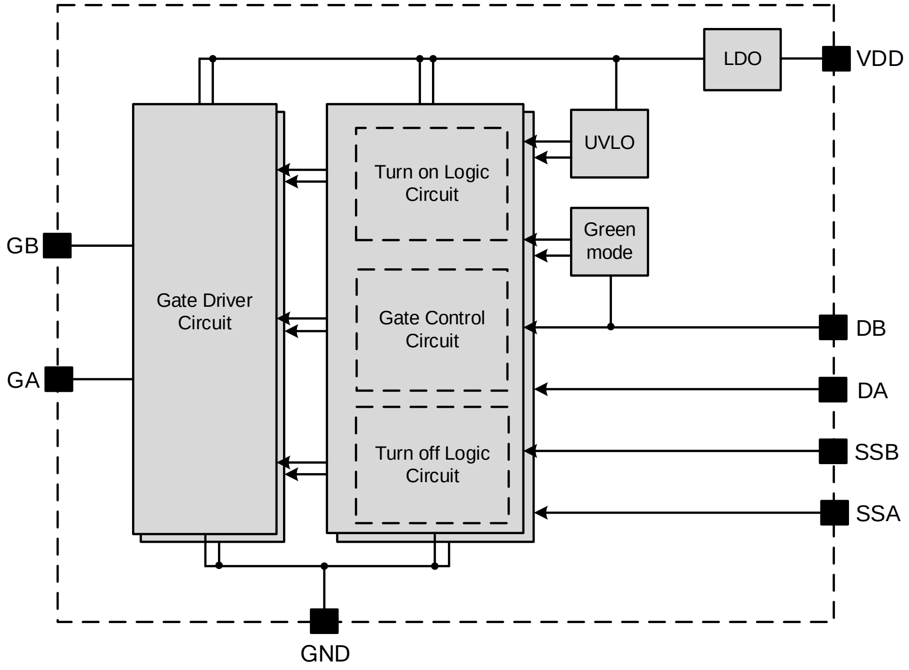


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
DA/DB	-1.5	200	V
GA/GB	-0.3	16	
VDD	-0.3	40	
SSA/SSB	-0.3	1	
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		150	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		60	
PD Power Dissipation T_A = 25°C		1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
DA/DB	-1	180	V
VDD	4.2	38	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

(V_{VDD} = 12V, T_J = -40°C–125°C, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VDD	VDD UVLO ON	V_{VDD_ON}		3.45	3.7	3.95	V
	VDD UVLO Hysteresis	V_{VDD_HYS}		150	200	250	mV
	Operating Current	I_{VDD_OP}	V_{VDD} = 12V, C_{LOAD}= 4.7nF, f_{SW} = 100kHz		17		mA
	Quiescent Current	I_{VDD_STB}	DA/DB no switching	80	110	140	µA
DA/DB/VSS	Turn-On Threshold	V_{TH_ON}		-240	-195	-150	mV
	Gate Pulldown Regulation Threshold	$V_{DS\_REG\_DN}$		-42	-27	-12	mV
	Difference Value between Gate Pulldown and Pullup Regulation Threshold	$V_{DS\_DIFF\_DN\_UP}$			16		mV
	Logic Turn-Off Threshold	$V_{TH\_LOG\_OFF}$		20	40	60	mV
GA/GB	GATE Pulldown Current before VDD UVLO On	I_{CLP}	V_{GA}, V_{GB} = 1V, V_{DA}, V_{DB} = 12V		200		mA
	Maximum Source Current (Note 5)	I_{SOURCE_MAX}	C_{LOAD} = 4.7nF, V_{GA}, V_{GB} from 1V to 6V		0.3		A
	Maximum Sink Current (Note 5)	I_{SINK_MAX}	C_{LOAD} = 4.7nF, V_{GA}, V_{GB} from 6V to 1V		1.7		A
	Maximum Gate Value		V_{VDD} = 5 V	4.85	4.95	5	V
			V_{VDD} = 12 V	9	10.2	11.3	V
	Minimum On-Time	t_{ON_MIN}		65	100	135	ns
	Minimum Off-Time	t_{OFF_MIN}		920	1200	1430	ns
	Turn-On Propagation Delay (Note 5)	t_{DLY_ON}			20		ns
	Gate Fast Shunt Propagation Delay (Note 5)	t_{DLY_SHUNT}			15		ns
	Time Threshold to Enter Green Mode	t_{MOD_DLY}		55	80	105	µs
OTP	Thermal Shutdown Temperature (Note 5)	T_{SD}			165		°C
	Hysteresis to Resume Operating (Note 5)	T_{OTP_HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

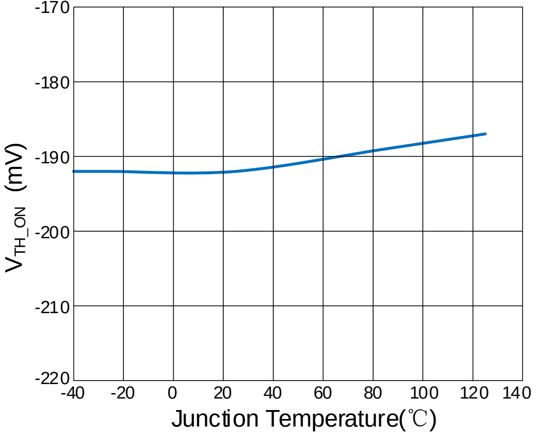
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz two-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin 4.

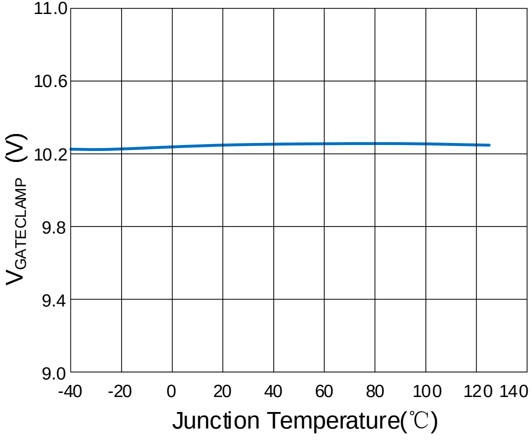
Note 3: The device is not guaranteed to function outside its operating conditions.

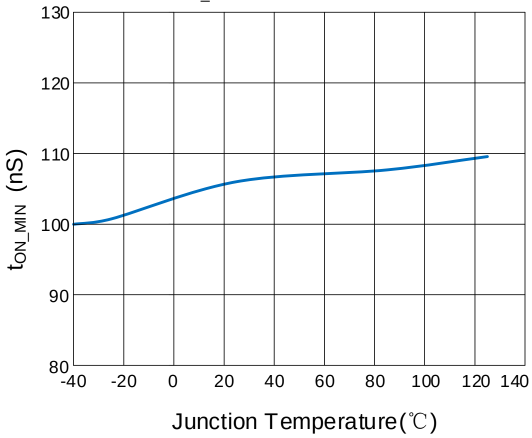
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = -40°C –125°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

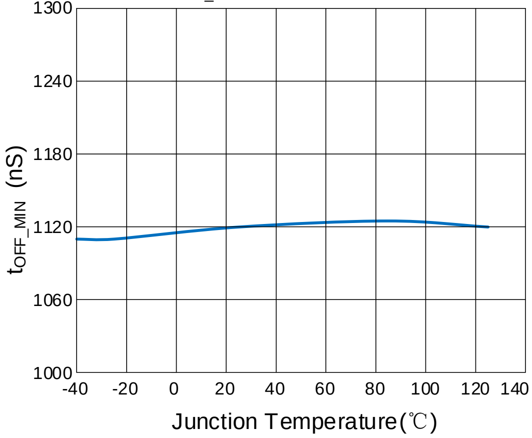
Note 5: Guaranteed by design or statistical correlation and not production tested.

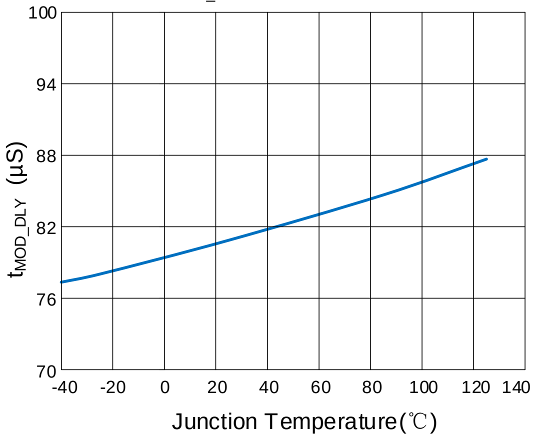
Typical Performance Characteristics

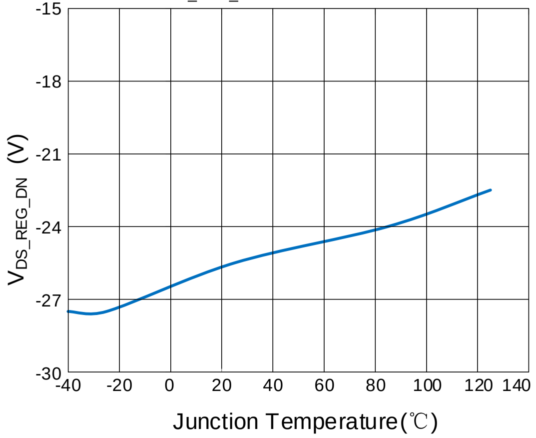

V_{TH_ON} VS. Temperature


$V_{GATECLAMP}$ VS. Temperature

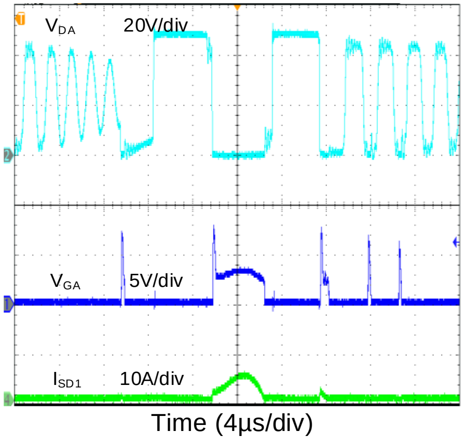

t_{ON_MIN} VS. Temperature


t_{OFF_MIN} VS. Temperature

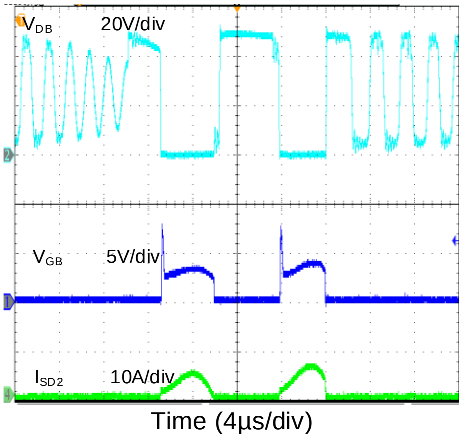

t_{MOD_DLY} VS. Temperature


$V_{DS\_REG\_DN}$ VS. Temperature

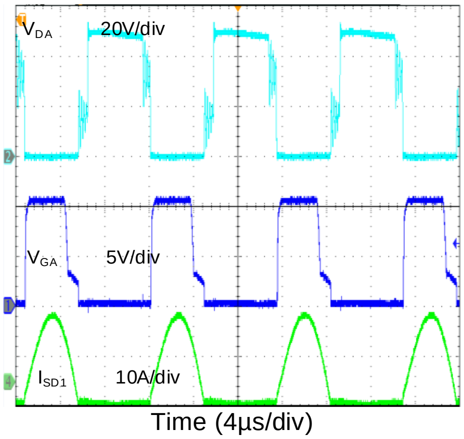
Steady State
(V_{IN}=230Vac, V_{OUT}=24V,I_{OUT}=0.5A)



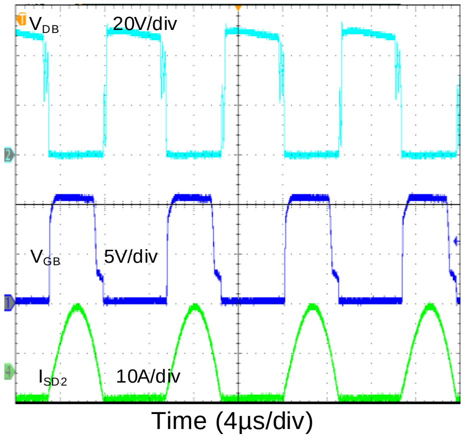
Steady State
(V_{IN}=230Vac, V_{OUT}=24V,I_{OUT}=0.5A)



Steady State
(V_{IN}=230Vac, V_{OUT}=24V,I_{OUT}=10A)



Steady State
(V_{IN}=230Vac, V_{OUT}=24V,I_{OUT}=10A)



Detailed Description

Gate Pin Pulldown before VDD ON

In the LLC converter, the primary side switch operates before the SQ33261 begins operating, then the drain-to-source voltage (V_{DS}) of the SR MOSFET is rapidly increasing as soon as the primary switch starts operating. If the C_{GD} of the SR MOSFET is large, the gate voltage of the SR MOSFET will be pulled up, resulting in false turn-on.

To resolve this problem, the SQ33261 provides a gate pulldown function. As shown in Figure 3, the gate voltage of SR MOSFET will be pulled down when the VDD voltage is less than V_{VDD_ON}.

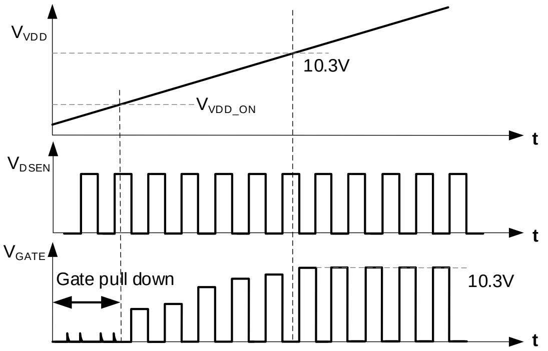


Figure 3. Timing Diagram of SR Gate Waveform

Power Supply and Driver

The internal logic circuit is powered by the VDD pin. When the VDD voltage is greater than V_{VDD_ON}, the SQ33261 starts operation, and the driver amplitude follows the VDD voltage. The device clamps the gate driver voltage to a maximum level of 10.3V to achieve low driving loss and compatibility with different MOSFETs, as shown in Figure 3.

Turn-On

As shown in Figure 4, at t = t_0, V_{DS} is lower than V_{TH_ON} and the SR MOSFET will be turned on after a short delay time (t_{DLY_ON}).

Gate Amplitude Control

In normal applications, gate voltage should be high to obtain a lower $R_{DS(ON)}$ and increase efficiency. However, the high level gate voltage at turn-on is not ideal in an LLC SR circuit, because it cannot achieve accurate zero-crossing current. SQ33261 uses smart gate regulation control method, as shown in Figure 4:

- t_1–t_2: Gate voltage is pulled up by a maximum 300mA charge current.
- t_2–t_3: Gate amplitude remains at the maximum value.
- t_3–t_4: Gate amplitude is pulled down to slow the rise of V_{DS}.

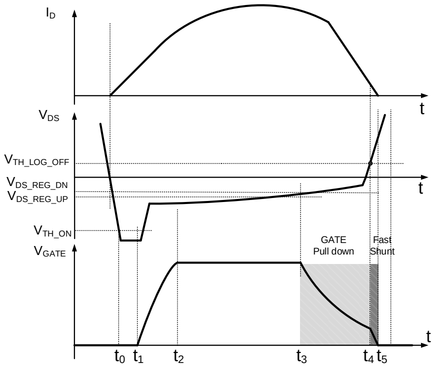


Figure 4. Waveform of Operating in Heavy Load

Turn-Off

As shown in Figure 4, at t = t_4, V_{DS} crosses the turn-off threshold ($V_{TH\_LOG\_OFF}$) and the gate voltage is pulled down to 0 and locked after a short delay time(t_{DLY_SHUNT}).

Green Mode

During light loads, the gate driver of the SQ33261 is latched off to reduce driver loss and improve efficiency

During each switching cycle, after SR MOSFET of B channel is turned off, a timer will start to count, if the timer has counted to 80us before next SR turn on instant, IC will enter green mode, and reduce the power consumption. IC will exit green mode by SR MOSFET of B channel turn on event.

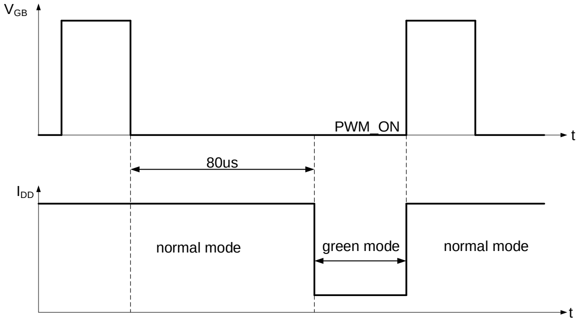


Figure 5. Enter Green Mode

Dual-Channel Gate Interlock

In order to prevent short circuits between the two channels, the SQ33261 provides a dual-channel interlock function. When the SR MOSFET of Channel A turns on, the SQ33261 disables the SR MOSFET gate driver of Channel B, until the SR MOSFET of Channel A turns off and the V_{DS} of Channel A is greater than 2V, as shown in Figure 6.

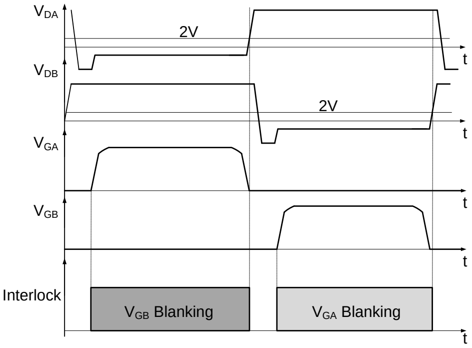


Figure 6. Channel Interlock Waveform

Overtemperature Protection (OTP)

If the IC die temperature rises above 165°C, the SQ33261 will stop driving the SR MOSFET and keep gate voltage to 0V. When the die temperature drops below 150°C, the IC will resume normal operation.

Typical Application

Figure 7 shows a typical application circuit for a 24V/10A LLC converter. The circuit includes a primary-side controller and an SR controller (SQ33261).

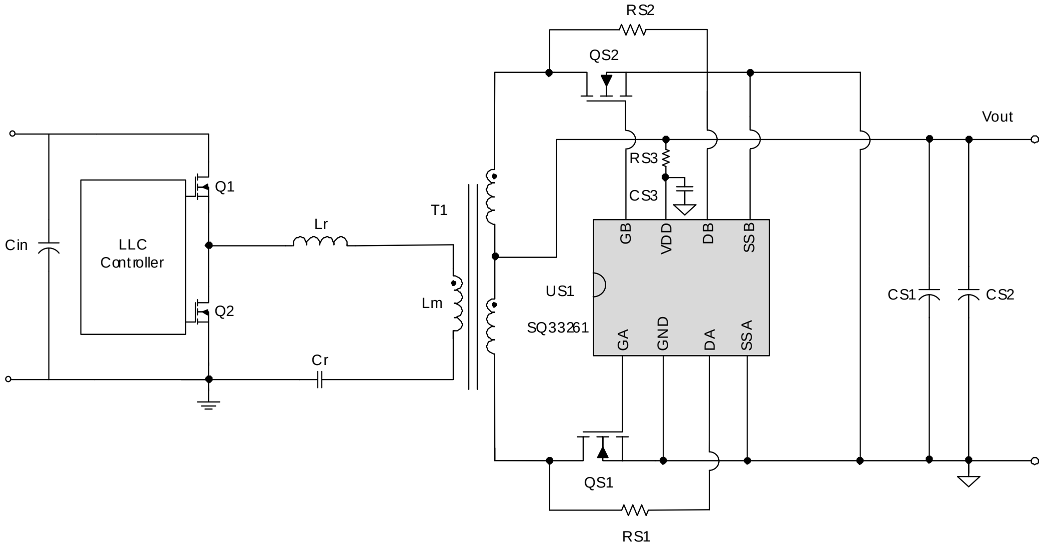


Figure 7. Typical Application Circuit

BOM List (SR Part)

Designator	Description	Part Number	Manufacturer
QS1,QS2	60V/6.2mΩ/DFN5*6	AON6262E	ALPHA&OMEGA
RS1,RS2	1kΩ/0805	0805W8F1001T5E	UNI-ROYAL
RS3	10Ω/0805	0805W8F100JT5E	UNI-ROYAL
CS3	1µF/50V/X7R, 0805	CC0805KKX7R9BB105	YAGEO

Design Procedure and Example

SR MOSFET Selection

Generally, the conduction loss will be reduced by using a lower $R_{DS(ON)}$ MOSFET, but the switching losses have to also be considered. To reduce total loss, $R_{DS(ON)}$ should be selected considering the efficiency, thermal performance, and MOSFET cost. MOSFET $R_{DS(ON)}$ should be no less than $V_{DS\_REG\_UP}$(-45mV)/I_{OUT}. For example, in an LLC converter with 10A output, $R_{DS(ON)}$ can be calculated as follows:

$$R_{DS(ON)} \geq \frac{-V_{DS\_REG\_UP}}{I_{OUT}} \approx 4.5m\Omega$$

When selecting the MOSFET, the maximum V_{DS} should be lower than the breakdown derated voltage. For example, in an LLC converter with 24V output and a derating coefficient of 0.9, the MOSFET breakdown voltage can be calculated as follows:

$$V_{DS(BR)} \geq \frac{V_{DS\_MAX}}{K_{Derating}} = \frac{2(Vo+V_{spike})}{K_{Derating}} = \frac{2\times(24+2)}{0.9} = 57.7V$$

A 60V/6.2mΩ MOSFET is uesd as the SR MOSFET in the 24V/10A LLC converter.

External Components Selection

Consider the following when selecting external components:

- The SQ33261 is powered directly by the VDD pin. To enhance system ESD performance, the recommended value of RS3 is 10Ω and the recommended value of CS3 is 0.1μF.
- In order to reduce the influence of negative voltages, a 1kΩ resistor should be used in series with the DA/DB pins.

Layout Design

Follow these PCB layout guidelines for optimal performance:

- Keep the circuit loop of all switching circuits small: secondary power loop, secondary RC snubber circuit loop, and IC power supply loop.
- The SSA pin and SSB pin should be as symmetrical as possible to reduce the difference in drive waveforms between two channels.
- The coupling capacitance between the DSEN and the drive signal should be reduced as much as possible to prevent noise from interfering with the drive signal.

Bottom View

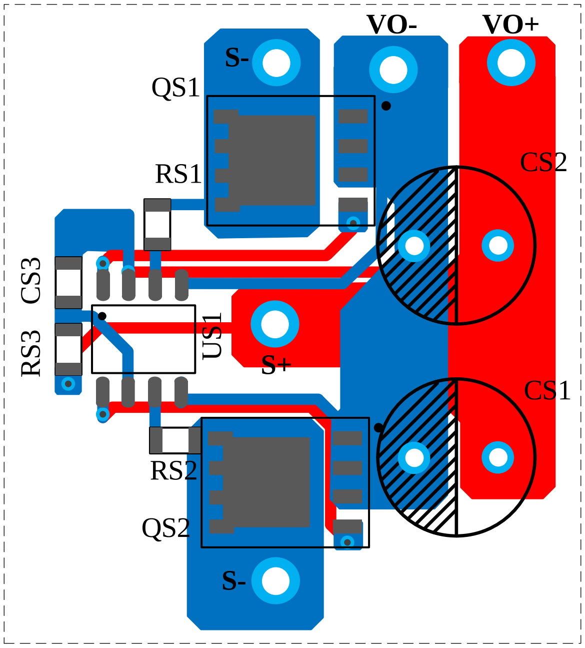
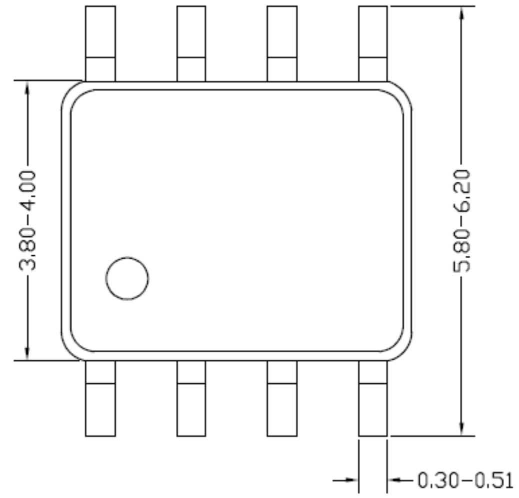
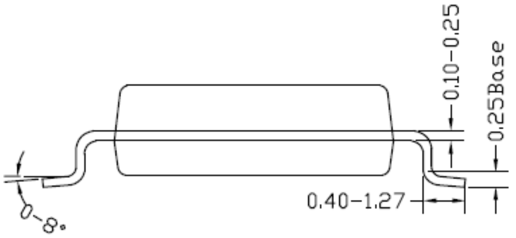


Figure 8. Suggested PCB Layout

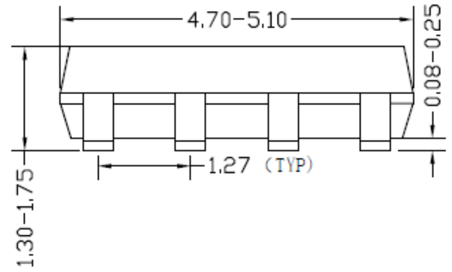
SO8 Package outline



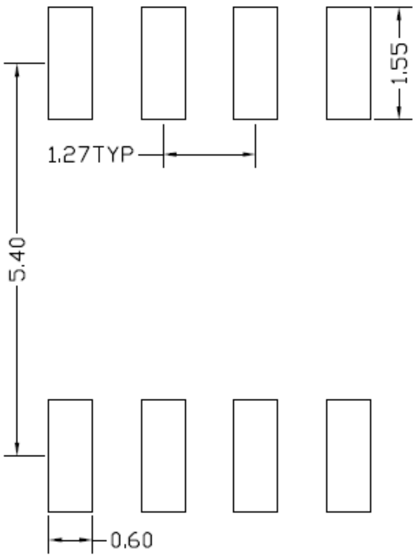
Top view



Side view



Front view



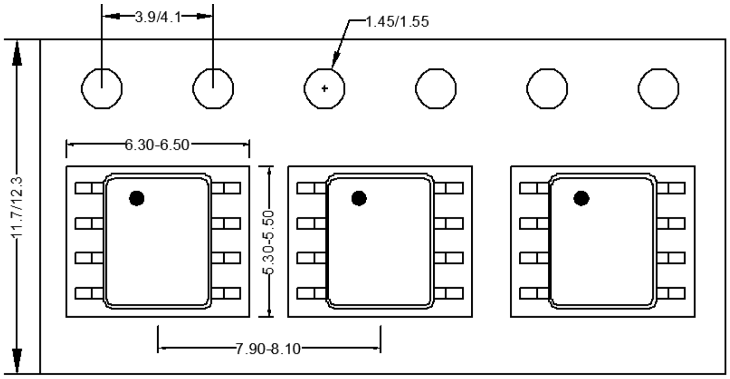
Recommended Pad Layout

(Reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

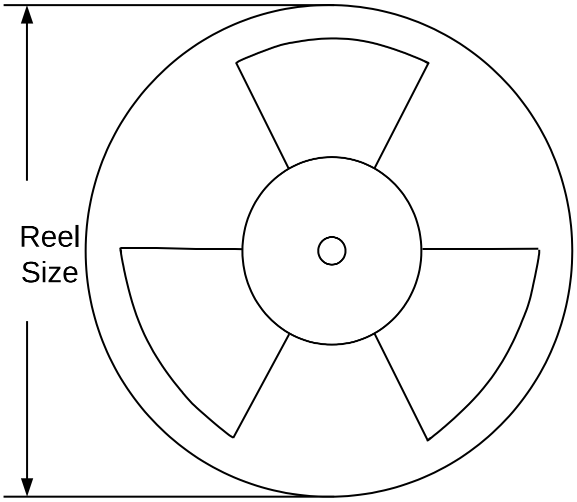
Tape and Reel Specification

Tape dimensions (SO8)



Feeding direction →

Reel dimensions



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
SO8	**12**	**8**	**13"**	**400**	**400**	**2500**

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
October 29, 2024	Revision 1.0	Initial Release

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