SQ55800/SQ55801

Isolated Dual-channel 5A/8A Gate Driver

General Description

The SQ55800/SQ55801 is an isolated dual-channel gate driver for Si MOSFETs, SiC MOSFETs and IGBTs with a propagation delay of only 32ns. Each channel has at least 5A source and 8A sink ability, which can drive a power transistor up to 2MHz. It can be used as two low-side drivers, two high-side drivers, or as a half-bridge driver with programmable dead time.

The SQ55800 has reinforced isolation ability (5700Vrms input-to-output per UL1577 and 1850V channel-to-channel) in SOP14W package, and the SQ55801 has basic isolation abitlity (2500Vrms input-to-output per UL1577 and 700V channel-to-channel) in DFN5*5-13 package. Robust operation is guaranteed by a minimum of 150V/ns Common-Mode Transient Immunity (CMTI) capability.

The SQ55800/SQ55801 has a wide power supply range to meet different application requirements. The input side supports 3-18V power supply, and the output side supports up to 25V bias voltage. Both power supplies have UVLO protection.

Features

- Insulation voltage: (SQ55800)
  - 5700Vrms input-to-output Per UL1577
  - ±1850V channel-to-channel
- Insulation voltage: (SQ55801)
  - 2500Vrms input-to-output Per UL1577
  - ±700V channel-to-channel
- CMTI Higher Than ±150V/ns
- Switching Parameters:
  - 32ns Typical Propagation Delay
  - 10ns Minimum Pulse Width
  - 5ns Maximum Delay Matching
  - 6ns Maximum Pulse-Width Distortion
- 5A Peak Source, 8A Peak Sink Output
- 3V to 18V Input Power Supply Range
- Up to 25V Output Power Supply
- Programmable Dead Time
- Isolation Barrier Life >40 Years
- Operating Temperature Range: –40°C to +125°C
- Package: SOP14W (SQ55800), DFN5*5-13 (SQ55801)

Applications

- Isolated AC/DC and DC/DC Converters
- EV Chargers
- Server Power Supplies
- Motor Drivers
- Solar Inverters
- UPS and Battery Chargers

Typical Application

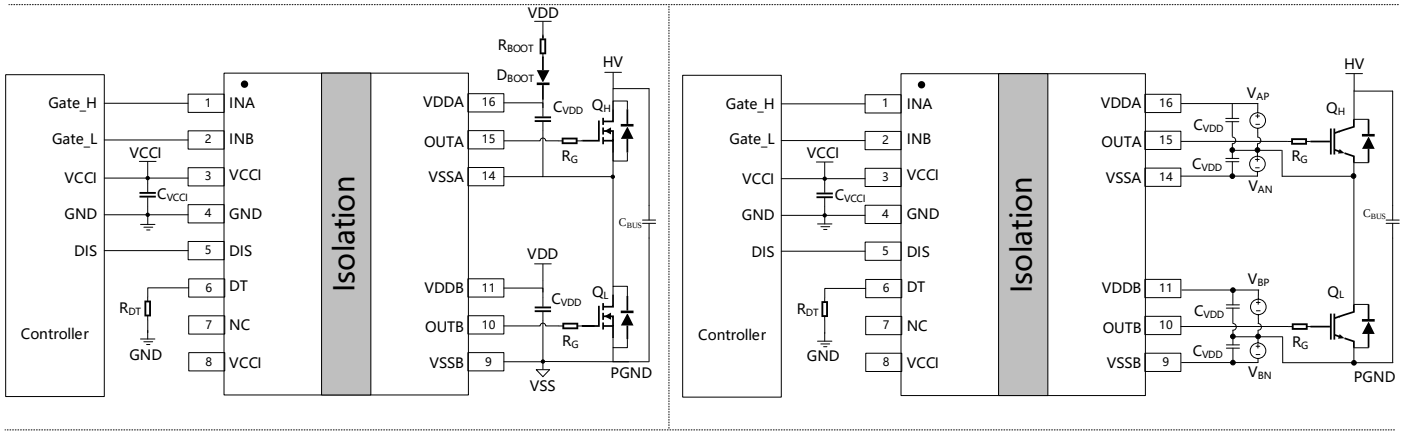


Figure 1. Typical Application Circuit (MOSFET / IGBT Half-bridge)

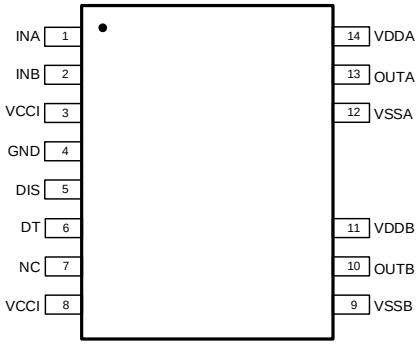
Ordering Information

Ordering Part Number	Package Type	VDDA/B UVLO	Top Mark
SQ55800AHWP	SOP14W	8V	AADQxyz
SQ55800BHWP*	SOP14W	6V	AADRxyz
SQ55800HWP*	SOP14W	13V	GTLxyz
SQ55801ATYD*	DFN5*5-13	8V	AADWxyz
SQ55801BTYD	DFN5*5-13	6V	AADYxyz
SQ55801TYD*	DFN5*5-13	13V	AADTxyz

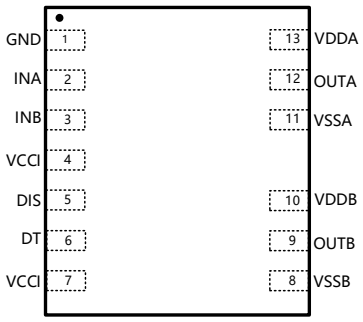
x = year code, y = week code, z = lot number code

* Future product. Specifications subject to change.

Pinout (top view)



(SOP14W-SQ55800)



(DFN5*5-13-SQ55801)

Pin Description

Pin No		Pin Name	Pin Description
SQ55800	SQ55801		
1	2	INA	Channel A input signal with a TTL/CMOS compatible input threshold. This pin is internally pulled down. If not used, it is recommended to connect this pin to GND.
2	3	INB	Channel B input signal with a TTL/CMOS compatible input threshold. This pin is internally pulled down. If not used, it is recommended to connect this pin to GND.
3, 8	4, 7	VCCI	Power supply for input side.
4	1	GND	Ground for input side.
5	5	DIS	Disables both driver outputs when asserted high, enables if set low or left open. If not used, it is recommended to connect to GND.
6	6	DT	DT pin is a multi-function pin: 1. When connected to VCCI, deadtime is disabled and overlap of OUTA and OUTB is allowed. 2. Connect a resistor ($1k\Omega \le R_{DT} \le 200k\Omega$) between DT and GND to adjusts dead time according to the equation: t_{DT} (in ns) = 10 × R_{DT} (in kΩ). It is recommended to parallel a low ESR capacitor between this pin to GND.
7	/	NC	Not connected.
9	8	VSSB	Ground for output-side channel B.
10	9	OUTB	Driver output of channel B. Connect this pin to the gate of MOSFET or IGBT.

11	10	VDDB	Power supply for output-side channel B.
12	11	VSSA	Ground for output-side channel A.
13	12	OUTA	Driver output of channel A. Connect this pin to the gate of MOSFET or IGBT.
14	13	VDDA	Power supply for output-side channel A.

Block Diagram

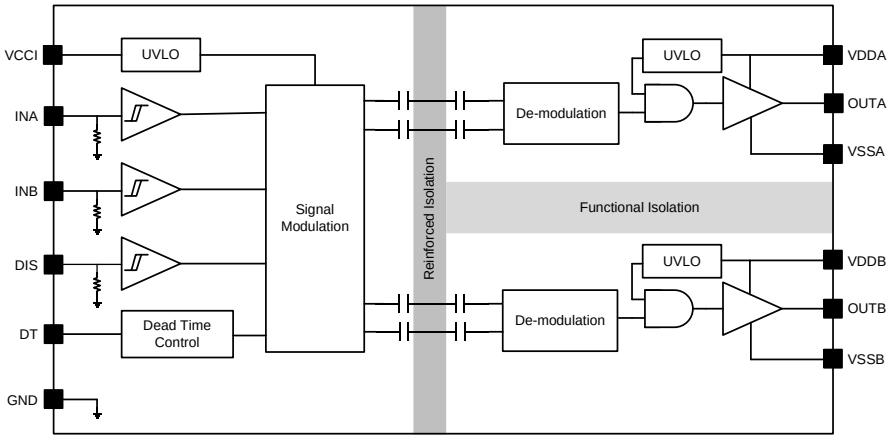


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCCI to GND	-0.3	20	V
INA/INB/DIS/DT to GND	-0.3	V_{VCCI}+0.3	
INA/INB (Transient for 200ns) to GND	-2	V_{VCCI}+0.3	
VDDA to VSSA	-0.3	30	
OUTA to VSSA	-0.3	V_{VDDA}+0.3	
OUTA (Transient for 200ns) to VSSA	-2	V_{VDDA}+0.3	
VDDB to VSSB	-0.3	30	
OUTB to VSSB	-0.3	V_{VDDB}+0.3	
OUTB (Transient for 200ns) to VSSB	-2	V_{VDDB}+0.3	
VSSA-VSSB (for SQ55800)	-1850	1850	
VSSA-VSSB (for SQ55801)	-700	700	
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	SQ55800	SQ55801	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	100.5	186	°C/W
θ_{JC} Junction-to-Case Thermal Resistance (Junction to top)	22.8	36	
PD Power Dissipation T_A = 25°C	1.24	0.67	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCCI to GND	3	18	V
VDDA to VSSA, VDDB to VSSB (for SQ55800AHWP)	9.2	25	V
VDDA to VSSA, VDDB to VSSB (for SQ55801BTYD)	6.5	25	V
Ambient Temperature	-40	125	°C
Junction Temperature	-40	130	°C

Insulation Specifications

Parameter	Symbol	Test conditions	Value		Unit
			SQ55800	SQ55801	
Clearance Distance	CLR	Shortest insulation distance through air	> 8	> 3.5	mm
Creepage Distance	CPG	Shortest insulation distance through package surface	> 8	> 3.5	mm
Distance Through Insulation	DTI		>32		μm
Comparative Tracking Index	CTI	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600		V
Material Group		Per IEC 60664-1	I		
Overvoltage Category per IEC 60664-1		Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-II	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	/	
DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01 (Note 5)					
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	AC voltage (bipolar)	2121	792	V_{PK}
Maximum Working Isolation Voltage	V_{IOWM}	AC voltage (sin wave); time dependent dielectric breakdown (TDDB) test	1500	560	V_{RMS}
		DC voltage	2121	792	V_{DC}
Maximum Transient Isolation Voltage	V_{IOTM}	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	8000	3535	V_{PK}
Maximum Surge Isolation Voltage	V_{IOSM}	Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	/	V_{PK}
		Test method per IEC 62368-1, 1.2/50 μs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	/	3500	V_{PK}
Apparent Charge (Method b1)	q_{pd}	Method b1; routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	<5	/	pC
		Method b1; routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	/	<5	pC

Apparent Charge (Method a, subgroup1)	q_{pd}	Method a, after environmental tests subgroup 1. $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	<5	/	Pc
		Method a, after environmental tests subgroup 1. $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	/	<5	pC
Apparent Charge (Method a, subgroup2/3)	q_{pd}	Method a, after Input/Output safety test subgroup 2/3. $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	<5		pC
Total Input to Output Capacitance	C_{IO}	V_{IO} = 0.4 sin (2πft), f =1 MHz	1.2		pF
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V at T_A = 25°C	> 10^{12}		Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}		Ω
		V_{IO} = 500 V at T_S =150°C	> 10^{9}		Ω
Pollution Degree			2		
Climatic Category			40/125/21		
UL 1577 (Note 5)					
Withstand Isolation Voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60s. (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5700	2500	V_{RMS}

Electrical Characteristics

(V_{VCCI} = 3.3 V or 5 V, 0.1μF capacitor from VCCI to GND, $V_{VDDA} = V_{VDDB}$ = 15V, 1μF capacitor from VDDA and VDDB to VSSA and VSSB, DT pin tied to VCCI, C_L = 0 pF, T_A = –40°C to +125°C, unless otherwise specified (Note 4))

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
VCCI to GND UVLO Thresholds						
VCCI UVLO Rising Threshold	V_{VCCI_ON}		2.55	2.7	2.85	V
VCCI UVLO Falling Threshold	V_{VCCI_OFF}		2.35	2.5	2.65	V
UVLO Threshold Hysteresis	V_{VCCI_HYS}			0.2		V
VDD to VSS UVLO Thresholds (SQ55800AHWP)						
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}		8.3	8.7	9.2	V
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF} V_{VDDB_OFF}		7.8	8.2	8.7	V
VDDA/B UVLO Threshold Hysteresis	V_{VDDA_HYS} V_{VDDB_HYS}			0.5		V
VDD to VSS UVLO Thresholds (SQ55801BTYD)						
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}		5.7	6	6.3	V
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF} V_{VDDB_OFF}		5.4	5.7	6	V
VDDA/B UVLO Threshold Hysteresis	V_{VDDA_HYS} V_{VDDB_HYS}			0.3		V
Supply Currents						
VCCI Quiescent Current	I_{VCCIQ}	V_{INA} = 0V, V_{INB} = 0V		2.3	2.8	mA
VCCI Operating Current	I_{VCCI}	(f = 500kHz) current per channel		7.3		mA
VDDA and VDDB Quiescent Current	I_{VDDAQ}, I_{VDDBQ}	V_{INA} = 0V, V_{INB} = 0V		4	5.1	mA
VDDA and VDDB Operating Current	I_{VDDA}, I_{VDDB}	(f = 500kHz) current per channel, C_{OUT} = 100pF		7.2		mA

INA and INB and DIS						
Input High Threshold Voltage	V_{INAH}, V_{INBH}, V_{DISH}		1.6	1.8	2	V
Input Low Threshold Voltage	V_{INAL}, V_{INBL}, V_{DISL}		0.7	0.9	1.1	V
Input Threshold Hysteresis	V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}			0.9		V
Input Pin Pull Down Resistance (INA/B, DIS)	R_{INA_PD}, R_{INB_PD}, R_{DIS_PD}			100		kΩ
Output						
Output Peak Source Current (Note 6)	I_{OA+}, I_{OB+}	C_{VDD} = 10μF, C_{LOAD} = 0.18 μF, f = 1kHz,		5		A
Output Peak Sink Current (Note 6)	I_{OA-}, I_{OB-}	C_{VDD} = 10μF, C_{LOAD} = 0.18 μF, f = 1kHz,		8		A
High State Output Resistance	R_{OHA}, R_{OHB}	I_{OUT} = 100mA, T_A = 25°C, $R_{OHA}=(V_{DDA}-V_{OUTA}) / I_{OUT}$ $R_{OHB}=(V_{DDB}-V_{OUTB}) / I_{OUT}$		1		Ω
Low State Output Resistance	R_{OLA}, R_{OLB}	I_{OUT} = -100 mA, T_A = 25°C $R_{OLA} = V_{OUTA} / I_{OUT}$ $R_{OLB} = V_{OUTB} / I_{OUT}$		0.43		Ω
Deadtime Programming						
Dead Time	t_{DT}	DT open		8		ns
Dead Time	t_{DT}	R_{DT} = 20kΩ	160	200	240	ns
Switching Characteristics						
Minimum Pulse Width	t_{PWmin}	Output off for less than minimum, C_{OUT} = 0pF			20	ns
Rising Edge Propagation Delay from INA/B to OUTA/B	t_{PDLH}			32	42	ns
Falling Edge Propagation Delay from INA/B to OUTA/B	t_{PDHL}			32	42	ns
Pulse Width Distortion	t_{PWD}	$\lvert t_{PDLH} - t_{PDHL} \rvert$			6	ns
Channel-to-channel Mismatch	t_{DM}				5	ns
Output Rise Time (20% to 80%)	t_R	C_{OUT}=1.8nF		6		ns
Output Fall Time (90% to 10%)	t_F	C_{OUT}=1.8nF		7		ns
Shutdown Time from Disable True	t_{DIS}			33	50	ns
Recovery Time from Disable False	t_{EN}			33	50	ns
VCCI Power-up Delay Time:	$t_{VCCI+ \text{ to OUT}}$	INA or INB tied to VCCI		50		μs
VDDA/B Power-up Delay Time	$t_{VDD+ \text{ to OUT}}$	INA or INB tied to VCCI		26		μs
Common-mode Transient Immunity						
High-state Common-mode Transient Immunity (Note 6)	$CMTI_H$	INA and INB both are tied to VCCI; V_{CM} = 1500V (bench test only)		±150		V/ns
Low-state Common-mode Transient Immunity (Note 6)	$CMTI_L$	INA and INB both are tied to GND; V_{CM} = 1500V (bench test only)		±150		V/ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in natural convection at T_A = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2x2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25℃. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Certification planned.

Note 6: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

(Test conditions: VCCI=3.3V; VDDA/B=15V; Ambient temperature: -40-125 ℃; No load unless otherwise noted.)

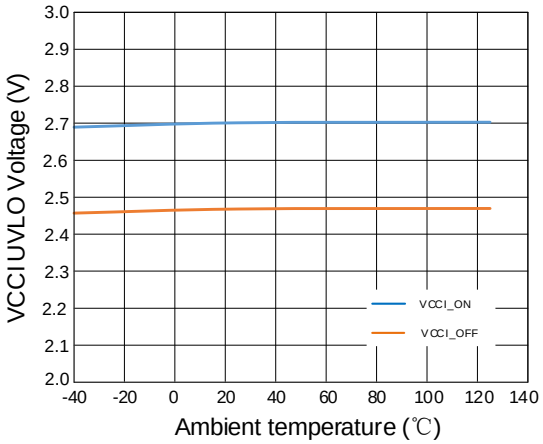


Figure 3-1. VCCI UVLO threshold vs temperature

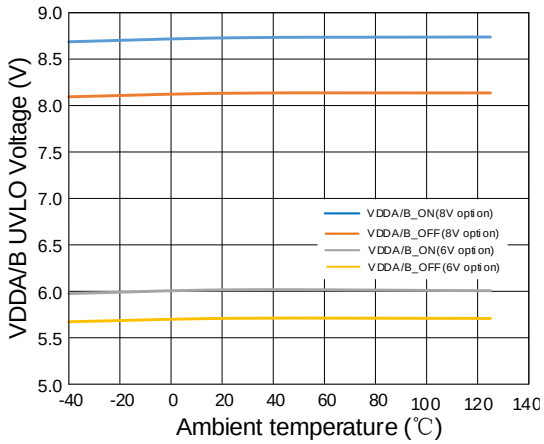


Figure 3-2. VDDA/B UVLO threshold vs temperature

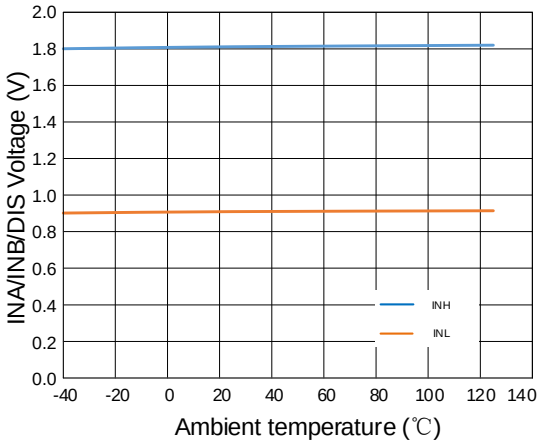


Figure 3-3. INA/INB/DIS threshold vs temperature

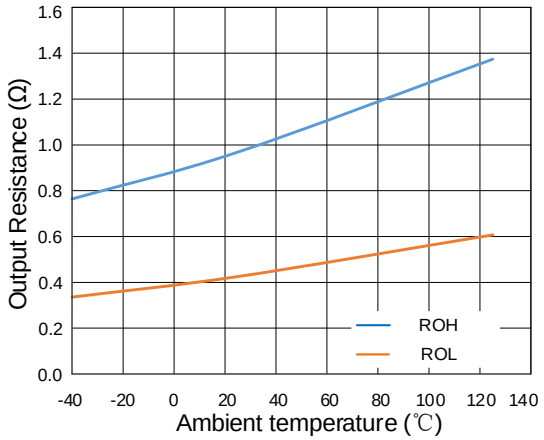


Figure 3-4. Output resistance vs temperature

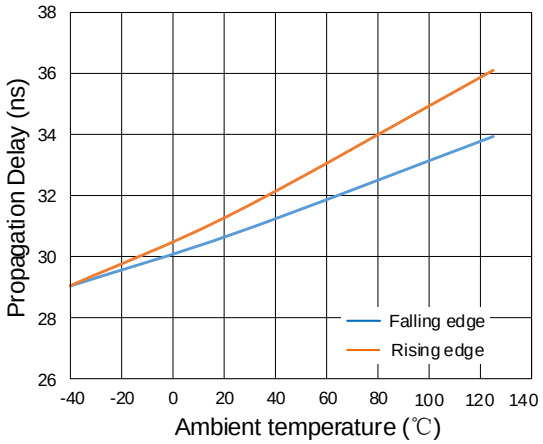


Figure 3-5. Propagation delay vs temperature

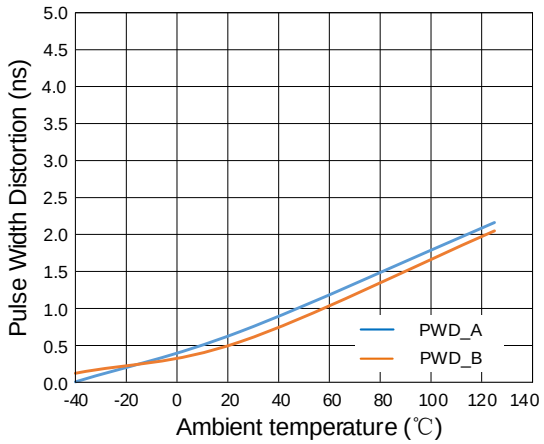


Figure 3-6. Pulse width distortion vs temperature

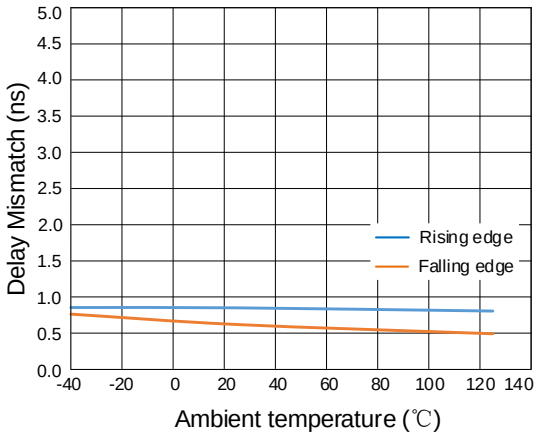


Figure 3-7. Propagation delay mismatch vs temperature

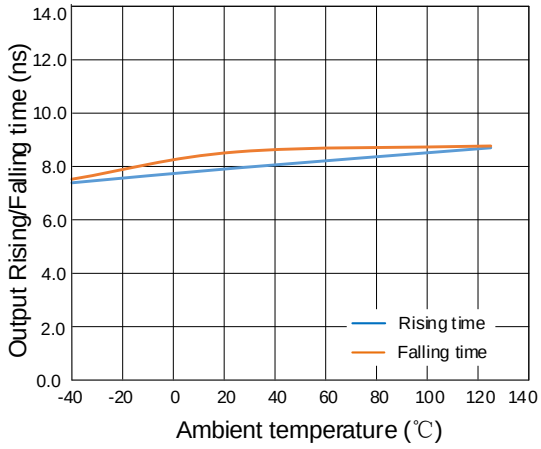


Figure 3-8. Output rising/falling time vs temperature

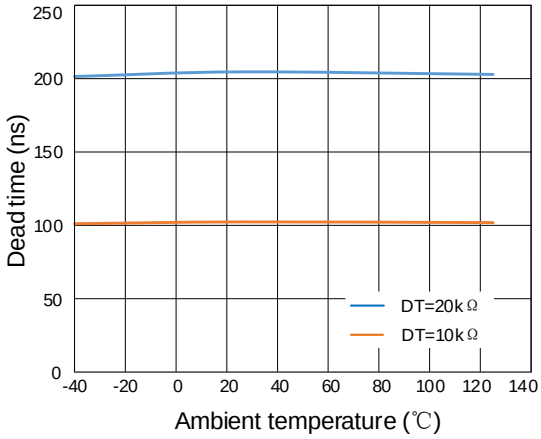


Figure 3-9. Dead time vs temperature

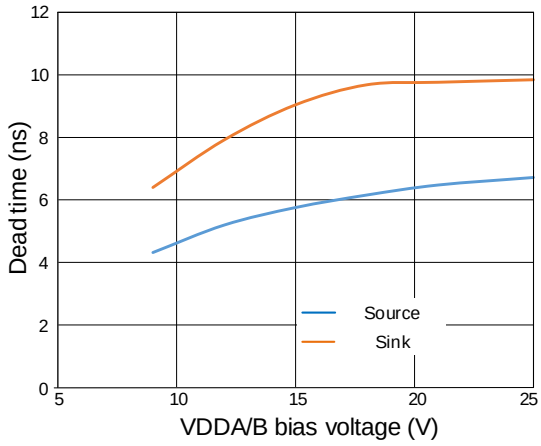


Figure 3-10. Output peak current vs VDDA/B bias voltage

Parameter Measurement Information

(a) Propagation Delay and Delay Mismatch

Figure 4-1 shows how to measure propagation delay (t_{PD}) and delay mismatch (t_{DM}). To measure these two parameters, INA and INB are shorted together, and DT is tied to VCCI to disable dead time function.

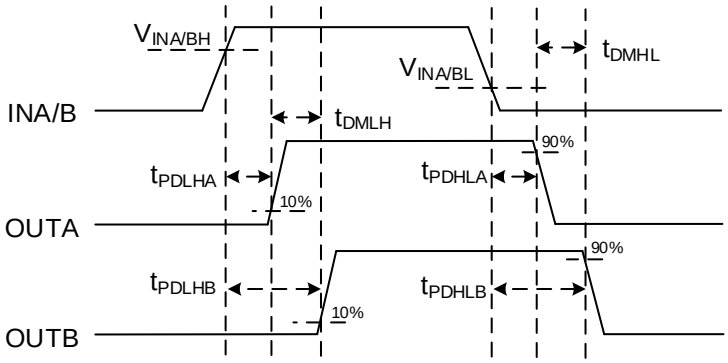


Figure 4-1. Propagation delay and delay mismatch measurement waveforms

(b) Rising and Falling Time

Figure 4-2 shows the method to measure OUTA/B rising time (t_R) and falling time (t_F). In this measurement, a capacitor of 1.8nF is connected between OUTA/B and VSSA/B.

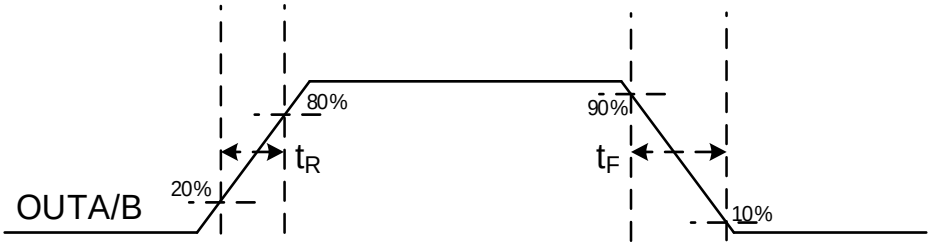


Figure 4-2. OUTA/B rising and falling time measurement waveforms

(c) Disable Response Time

Figure 4-3 shows the method to measure time delay for disabling the device (t_{DIS}) and the recovery time delay (t_{EN}). When there is a long distance between the DIS pin and controller, it is recommended to use an RC filter to enhance noise immunity. When the DIS pin is not used, it is recommended to connect it to GND.

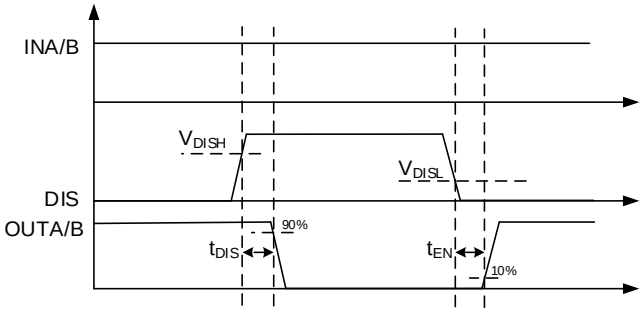


Figure 4-3. Disable function timing diagram

(d) Dead time measurement

If the DT Pin is open or tied to GND through a proper resistor (R_{DT}), the dead time function is enabled. Figure 4-4 shows the dead time logic. If the dead time of INA and INB is shorter than the dead time set by R_{DT}, the dead time (t_{DT1}) is set by the resistor R_{DT}. If the dead time of INA and INB is longer than the dead time set by R_{DT}, the output dead time (t_{DT2}) is determined by input signals.

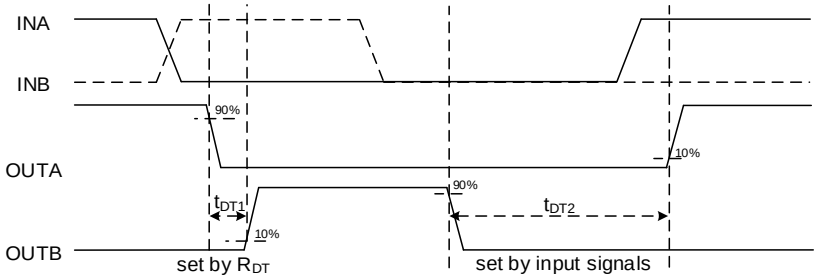


Figure 4-4. Dead time measurement

(e) Power-up and shut-down delay

After the power supply voltage goes above the UVLO rising threshold, there is a time delay before the device is ready to deliver a signal cross isolation barrier. The time delay is defined as $t_{VCCI+\ to\ OUT}$ for VCCI and $t_{VDD+\ to\ OUT}$ for VDDA/B. After the power supply is ready, it is recommended to leave enough time margin before driving a PWM signal. If the time margin is not enough, the output will stay low until the required power-up delay is completed.

Figure 4-5 shows the measurement method of the power-up delay time for VCCI and VDDA/B. In this measurement, INA/B are tied to VCCI.

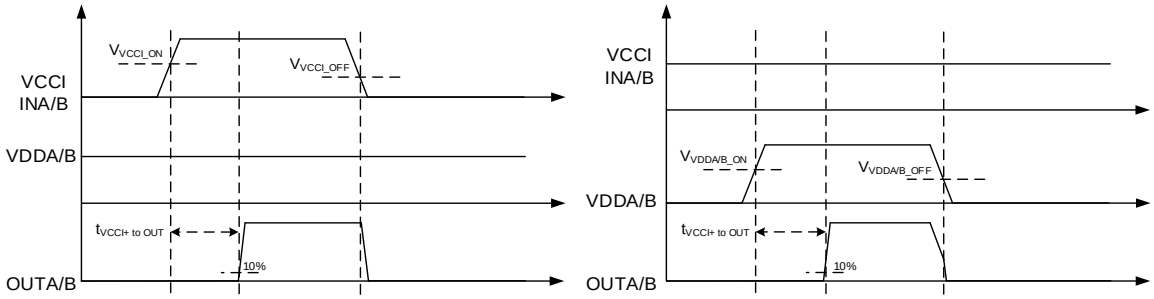


Figure 4-5. VCCI and VDDA/B power-up delay

(f) CMTI Test

Figure 4-6 is a simplified schematic of CMTI test setup. In bench test, both positive and negative slew rates have been tested under the conditions of INA/B=0 and INA/B=1.

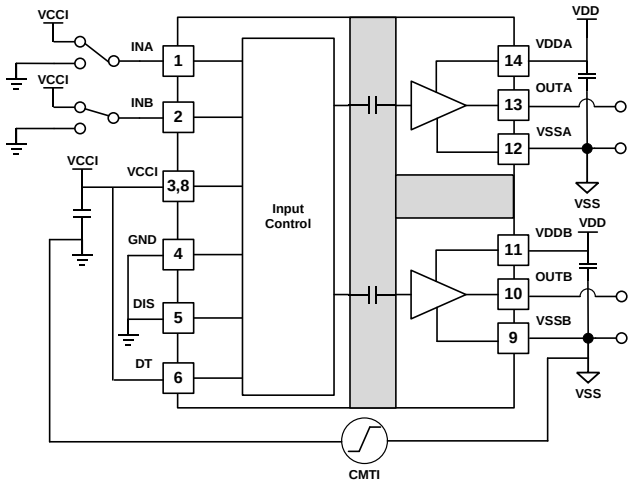


Figure 4-6. CMTI test schematic

Detailed Description

Overview

The SQ55800/SQ55801 is a dual-channel isolated gate driver, and it can safely drive SiCs and MOSFETs in dual low-side, dual high-side, and half bridge configurations.

The input pins are CMOS/TTL compatible, allowing this chip to be directly connected to most controllers, such as MCUs/DSPs/FPGAs. The disable and dead time functions can be enabled or disabled to suit most applications.

The SQ55800/SQ55801 has 5A/8A drive ability, and it can directly drive most SiCs and MOSFETs quickly. At least 150V/ns CMTI capability guarantees robust operation in high-voltage half-bridge circuits.

Power supply Under Voltage Lock Out (UVLO)

The SQ55800/SQ55801 has an internal under voltage lock out (UVLO) protection feature on both the input and output side power supplies. During UVLO Protection, OUTA/B are actively pulled-down regardless of the status of INA/B. Hysteresis (V_{VCCI_HYS} and V_{VDDA/B_HYS}) is used to avoid noise on power supply. The detailed UVLO Logic is listed in Table 1.

Table 1. Power supply UVLO Protection Logic

Condition	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} before start-up	X	X	L	L
VCCI-GND < V_{VCCI_OFF} after start-up	X	X	L	L
VDDA-VSSA < V_{VDDA_ON} before start-up	X		L	
VDDA-VSSA < V_{VDDA_OFF} after start-up	X		L	
VDDB-VSSB < V_{VDDB_ON} before start-up		X		X
VDDB-VSSB < V_{VDDB_OFF} after start-up		X		X

Input and output logic table

When VCCI, VDDA, and VDDB are powered up, INA, INB, DIS, and DT will determine the output state. The detailed input and output logic is listed in Table 2.

Table 2. INPUT/OUTPUT Logic Table

INPUTS			OUTPUTS		NOTE
DIS	INA	INB	OUTA	OUTB	
L or Float	L or Float	L or Float	L	L	
L or Float	L or Float	H	L	H	If Dead Time is enabled, the output rising edge occurs after the dead time expires.
L or Float	H	L or Float	H	L	
L or Float	H	H	L	L	DT is floating or programmed with R_{DT}
L or Float	H	H	H	H	DT pin is pulled-up to VCCI
H	X	X	L	L	

Input and Output Structures

The input pins (INA, INB, and DIS) of SQ55800/SQ55801 are TTL and CMOS compatible, with a 1.8V high threshold, and 0.9V low threshold. Although a wide hysteresis of 0.9V can guarantee good noise immunity and stable operation in most applications, it is still recommended to use an RC filter on INA/INB/DIS pins. When left open, the input pins are pulled down internally by a 100 kΩ resistor, but it is recommended to ground the input by a low resistance path when it is not used.

The OUTA/B pins of SQ55800/SQ55801 are pulled up using a PMOS and pulled down using an NMOS (as shown in Figure 5). Both OUTA and OUTB have active clamp functions. If VDDA/B is unpowered, when the voltage of OUTA/B rises above 1.5V, the pull-down NMOS is turned-on by the resistor R_{CLAMP}. Thus, OUTA/B are clamped below 1.5V.

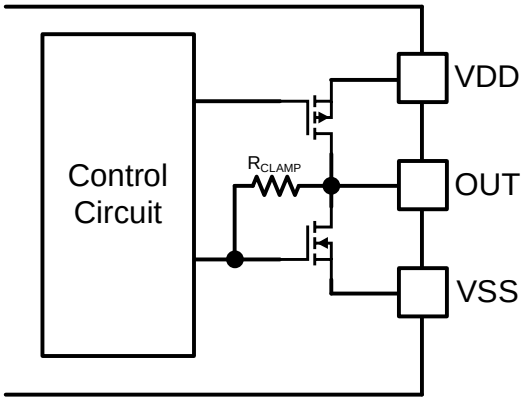


Figure 5. Output Structure

Programmable Dead Time

The dead time function is designed to avoid falsely turning on OUTA and OUTB simultaneously. OUTA/B are pulled-down immediately after INA/B are pulled-down. However, one channel can be pulled-up, only if the other channel is pulled-down for a period of time.

The DT pin is a multi-use pin and has 3 functions:

(1) DT pin pulled-up to VCCI: the dead time function is disabled, and outputs completely match inputs. This mode allows OUTA and OUTB to overlap. When operating in this mode, it is recommended to pull-up the DT pin through a resistor to VCCI.

(2) DT Pin floating: When the DT pin is open, the default dead time (typical 8ns) is enabled.

(3) DT Pin connected through a programming resistor to GND pin: when placing a resistor ($1k\Omega \le R_{DT} \le 200k\Omega$) between DT and GND, the dead time is determined by the equation: $t_{DT} \approx 10 \times R_{DT}$, where t_{DT} is the programmed dead time, in nanoseconds, and R_{DT} is the resistance between DT pin and GND, in kilo-ohms. A dead time between 10ns to 2us can be programmed. A capacitor larger than 2.2nF is recommended to be paralleled with R_{DT} to reduce noise.

8 combinations (A~H) of INA and INB are listed in Figure 6 and Table 3 to provide dead time logic details.

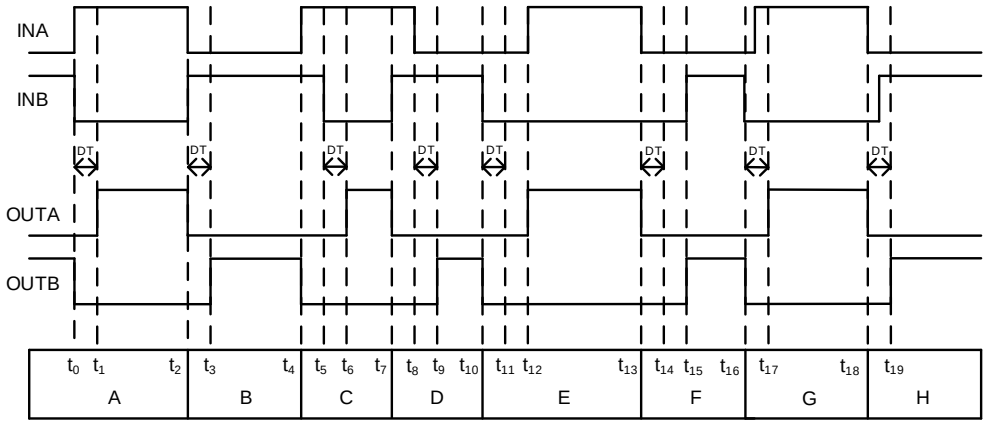


Figure 6. Dead time waveforms

Table 3. Dead Time Logic Table

	Condition	Result
A	INA's rising edge and INB's falling edge occur at the same time.	OUTB follows INB and goes low immediately at t_1. After OUTB stays low for the dead time, OUTA goes high at t_1.
B	INB's rising edge and INA's falling edge occur at the same time.	OUTA follows INA and goes low immediately at t_2. After OUTA stays low for the dead time, OUTB goes high at t_3.
C	INA's rising edge happens before INB's falling edge.	In overlap time (t_4- t_5), OUTA and OUTB are low. At t_5, overlap ends and the dead-timer is triggered. After OUTB stays low for the dead time, OUTA goes high at t_6.
D	INB's rising edge happens before INA's falling edge.	In overlap time (t_7- t_8), OUTA and OUTB are low. At t_8, overlap ends and dead-timer is triggered. After OUTA stays low for the dead time, OUTB goes high at t_9.
E	INA's rising edge happens after INB's falling edge, and the time delay is larger than dead time.	OUTB follows INB and goes low immediately at t_{10}. At t_{12}, OUTB already stays low for more than dead time. Thus, OUTA follows INA and goes high immediately.
F	INB's rising edge happens after INA's falling edge, and the time delay is larger than dead time.	OUTA follows INA and goes low immediately at t_{13}. At t_{15}, OUTA already stays low for more than dead time. Thus, OUTB follows INB and goes high immediately.
G	INA's rising edge happens after INB's falling edge, but the time delay is smaller than dead time.	OUTB follows INB and goes low immediately at t_{16}. At INA's rising edge, the low-time of OUTB is shorter than dead time, and OUTA stays low. After OUTB stays low for the dead time at t_{17}, OUTA goes high.
H	INB's rising edge happens after INA's falling edge, but the time delay is smaller than dead time.	OUTA follows INA and goes low immediately at t_{18}. At INB's rising edge, the low-time of OUTA is shorter than dead time, and OUTB stays low. After OUTA stays low for the dead time at t_{19}, OUTB goes high.

Typical Application Schematic

Before driving the power MOSFETs ON/OFF, the device must be powered. VCCI can share the same power supply with the MCU, while the VDDA/B rail is usually powered by an isolated supply, such as a flyback or push-pull circuit. The BOM for the circuits shown in this section is listed below:

Table 4. BOM list of application circuit

Designator	Description	Part Number	Manufacturer
U1	SQ55800AHWP/SOP14W or SQ55801BTYD/DFN5*5-13	SQ55800AHWP or SQ55801BTYD	SILERGY
C_{VCCI}	1μF/25V/X7R/0805	GRM21BR71E105KA99L	muRata
C_{BOOT}, C_{VDD}, C_Z	10μF/50V/X7R/0805	GRM21BR61H106KE43L	muRata
C_{IN}	100pF/25V/X7R/0805	CC0805KRX7R8BB101	YAGEO

C_{DIS}, C_{DT}	10nF/25V/X7R/0805	CC0805KRX7R8BB103	YAGEO
C_{GS}	470pF/50V/X7R/0805	CC0805KRX7R9BB471	YAGEO
C_{BUS}	10uF/1200V/P=37.5mm	MKP1848H61012JP2	VISHAY
R_{IN}	100Ω/±1%/0805	RC0805FR-07100RL	YAGEO
R_{DT}	20kΩ/±1%/0805	RC0805FR-0720KL	YAGEO
R_{BOOT}, R_{ON}	10Ω/±1%/0805	RC0805FR-0710RL	YAGEO
R_{OFF}	5.1Ω/±1%/0805	RC0805FR-075R1L	YAGEO
R_{GS}, R_Z	10kΩ/±1%/0805	RC0805FR-0710KL	YAGEO
D_{BOOT}	1200V/TO252-2	ASD10120D	AnBon
D_{OFF}	40V/SOD-123FL	SS1040FL	PANJIT
D_Z	3V Zener/SOD-123	MMSZ4683-E3-08	VISHAY
Q_H, Q_L	NTH4L014N120M3P/TO-247-4	NTH4L014N120M3P	ONSEMI

Bootstrap power supply

If a power transistor can be safely turned off with 0V gate-to-source voltage, the bootstrap power supply can be used. It is simple and low-cost, but a high-side transistor cannot operate with a duty-cycle ratio very close to 100%. If the on-time of low-side transistor Q_L is not sufficient, VDDA cannot be powered up using this method.

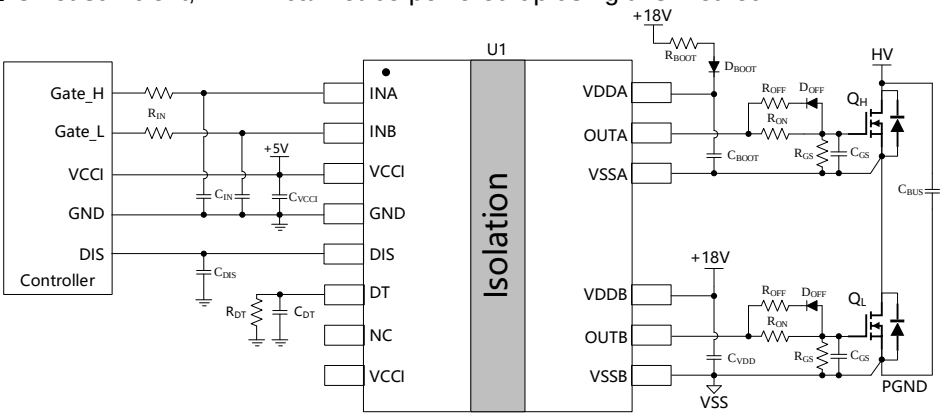


Figure 7. Typical application schematic with bootstrap power supply

The bypass capacitors for VCCI, VDDA, and VDDB are important for optimal operation. Surface-mount multi-layer ceramic capacitors (MLCC) are recommended due to their low ESR and ESL.

It is recommended to use input filters (R_{IN} and C_{IN}) to enhance input noise immunity when the input PCB traces are long, at the expense of a slight increase in propagation delay. A trade-off should be made between noise immunity and propagation delay based on the application requirements. Commonly used values: R_{IN} =100Ω and C_{IN} =100pF.

When using a bootstrap circuit, the low-side transistor Q_L needs to turn on for enough time to charge capacitor C_{BOOT} before delivering the PWM signal. For the bootstrap diode (D_{BOOT}), it is recommended to use a high-voltage fast-recovery diode or a SiC Schottky diode with a low forward voltage drop and low junction capacitance to minimize the power losses (e.g. C4D02120E). A bootstrap resistor (R_{BOOT}) should be used to limit the inrush current and overshoot on VDDA, in order to keep the voltage of VDDA below absolute maximum ratings.

The external gate driver resistors (R_{ON} and R_{OFF}) are used to limit ringing caused by parasitic parameters, high slew rate, and body diode reverse recovery. A gate-source resistor R_{GS} is recommended to pull down gate voltage when the driver is unpowered. Additionally, the gate-source resistor C_{GS} can absorb miller current caused by high dv/dt and ensure safe operation.

Power supply with negative bias

Because of non-ideal PCB layout and long package leads (TO-220 and TO-247), some parasitic inductance and capacitance is inevitably introduced, causing ringing on the gate voltage, especially in high power applications. The ringing increases the risk of false turn-on and shoot-through, and applying a negative bias voltage is a popular way to solve this problem.

The first example (shown in Figure 8) uses a Zener diode to produce negative bias. The negative bias is determined by Zener diode voltage. This configuration needs two isolated power supplies (VDDA and VDDB) on the output side.

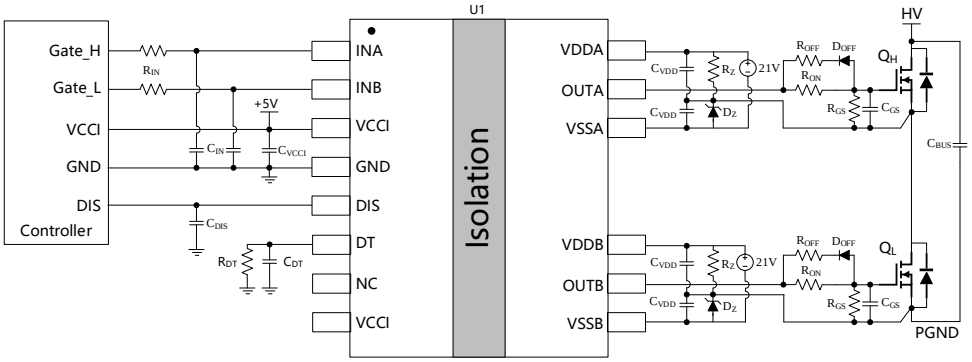


Figure 8. Typical application schematic of negative bias with Zener diode

The second example (shown in Figure 9) uses two isolated dual-output power supplies to produce negative bias voltages for VDDA and VDDB. This solution has more flexibility to set positive and negative bias, however, it uses four power supplies.

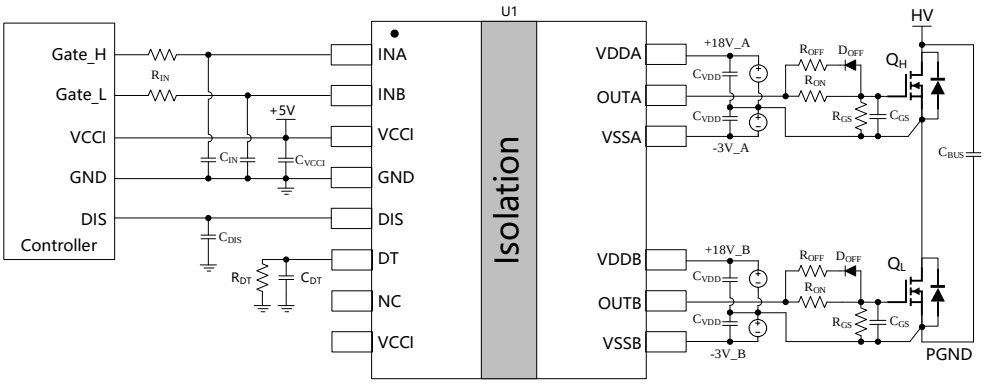


Figure 9. Typical application schematic of negative bias with double output power supply

The last example (shown in Figure 10) only uses one power supply to produce negative bias for VDDA and VDDB.

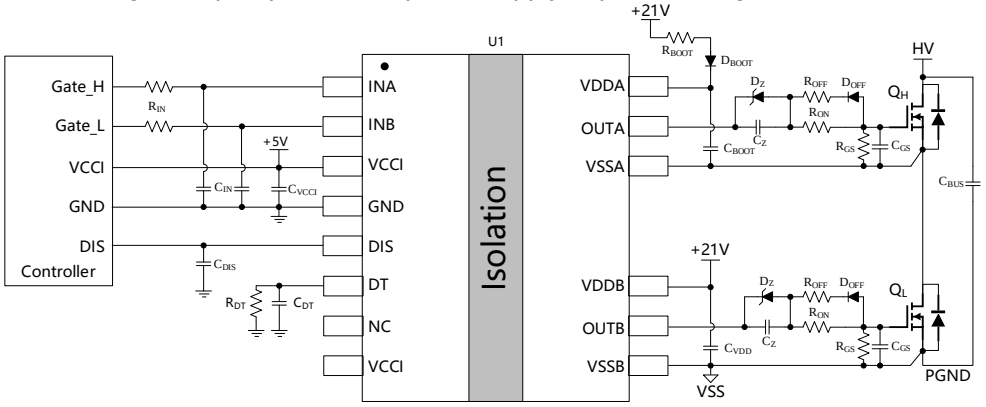


Figure 10. Typical application schematic of negative bias with only one power supply

This solution has minimum and maximum duty-cycle limitations. To guarantee a stable negative bias voltage set by the Zener diode, the duty-cycle ratios of OUTA and OUTB cannot be too small. The minimum duty ratio is

$$\text{duty ratio}_{A/B} \geq \frac{V_Z}{V_{DD} - V_F} \times 100\%$$

For a half-bridge working in symmetrical mode, the PWM signal of OUTA and OUTB is symmetrical, which means the duty ratio cannot be too large. The duty ratio of symmetrical half-bridge should stay in the range of

$$\frac{V_Z}{V_{DD}-V_F}\times 100\% \le \text{duty ratio}_{A/B} \le (1-\frac{V_Z}{V_{DD}-V_F})\times 100\%$$

This circuit is suitable for converters working with fixed duty-cycle ratio (close to 50%), such as variable frequency resonant converters and phase shift converters.

Design Layout

A good PCB layout is important for the performance. The key points are listed below:

(a) Low ESR and low ESL capacitors should be connected between VCCI and GND, VDDA/B and VSSA/B as close as possible.

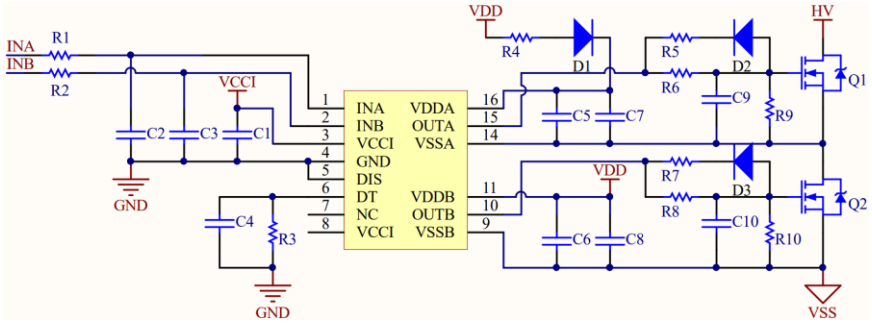
(b) Dead time resistor (R_{DT}) and capacitor (C_{DT}) should be placed close to DT Pin to provide better noise immunity.

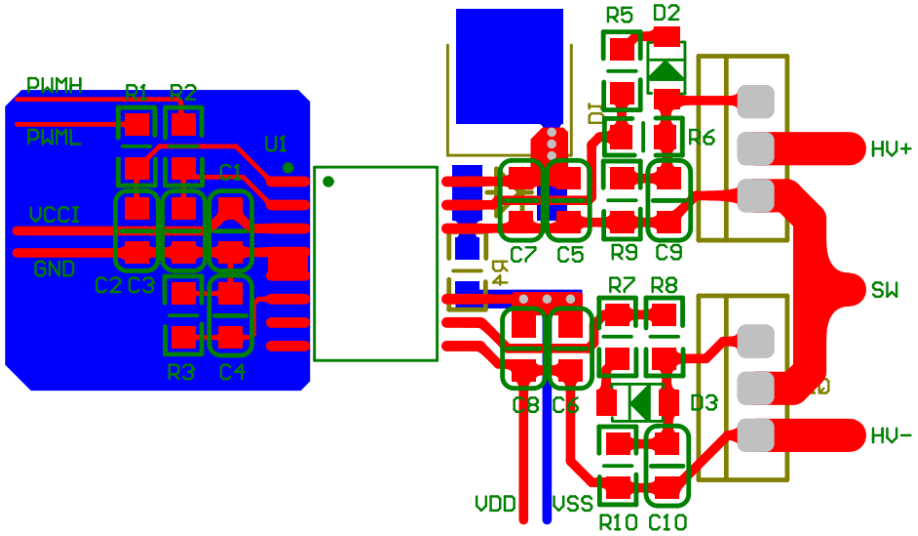
(c) Minimizing the gate source/sink current loop can reduce loop inductance and produce less noise. Thus, the driver should be close to the power transistor.

(d) To ensure adequate isolation between the input and output sides, traces and copper should not be placed in the area below the chip. For SQ55800, it is recommended to use a PCB cutout below the chip. For SQ55801, PCB cutout is not recommended.

(e) For high-voltage half-bridge applications, channel A and channel B of the output side will operate with DC-link voltage. Thus, all PCB components connected to channel A should have some distance from the components connected to channel B.

For SQ55800, a schematic and a layout example are shown in Figure 11, with TO-220 MOSFETs as an example.





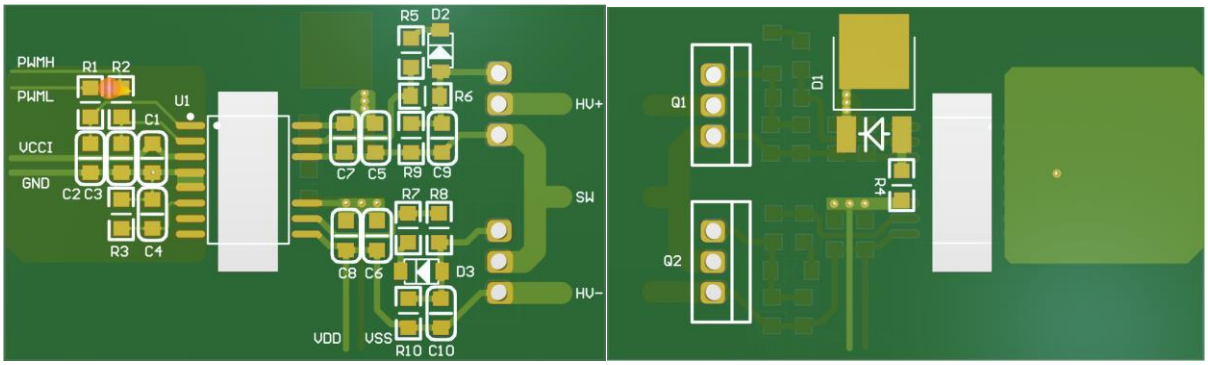


Figure 11. SQ55800 PCB Layout Suggestion

For SQ55801, a schematic and a layout example are shown in Figure 12, with TO-220 MOSFETs as an example.

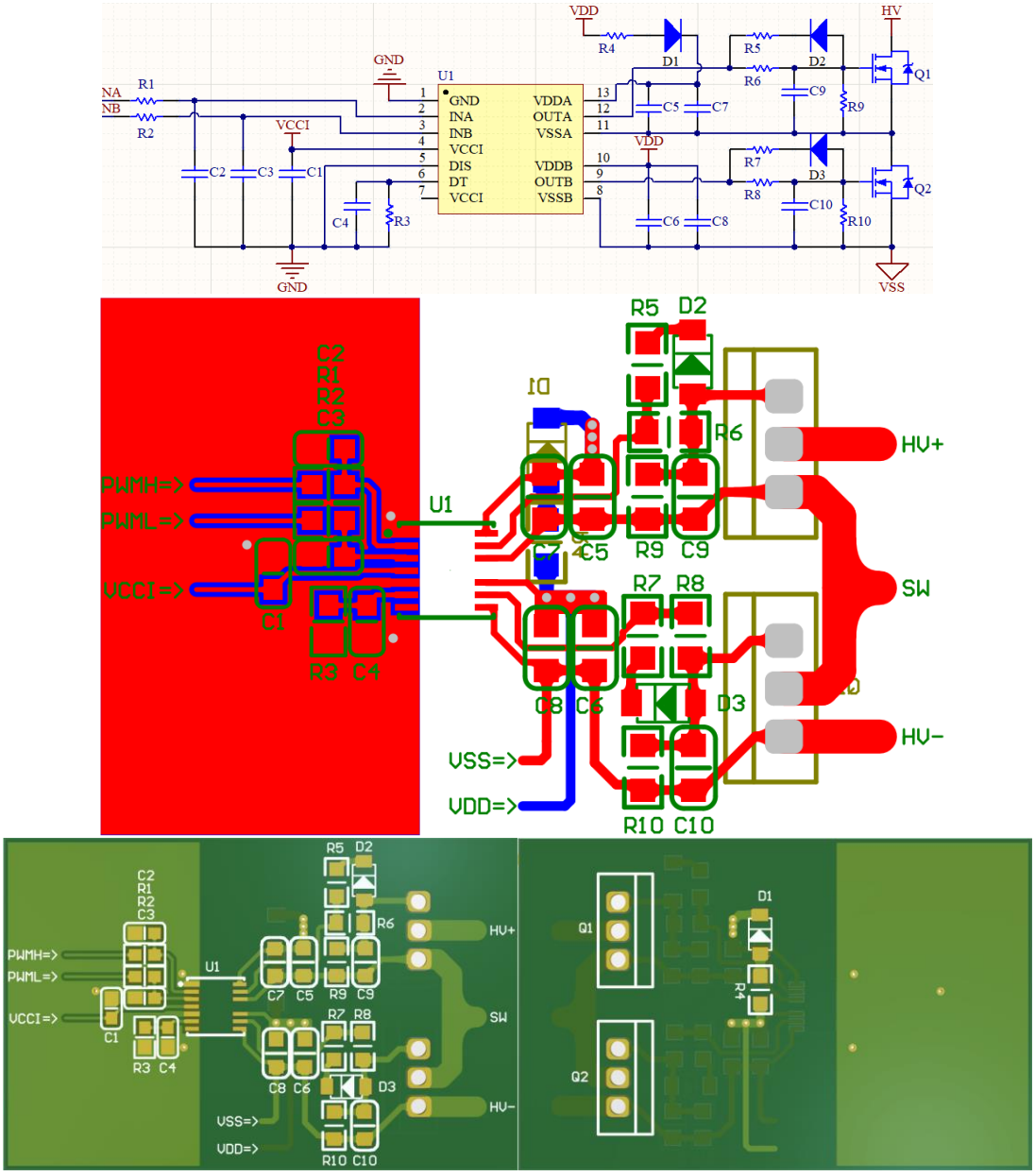
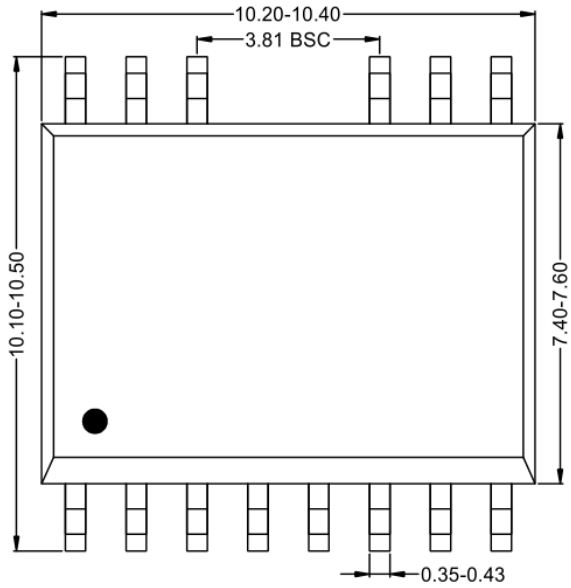
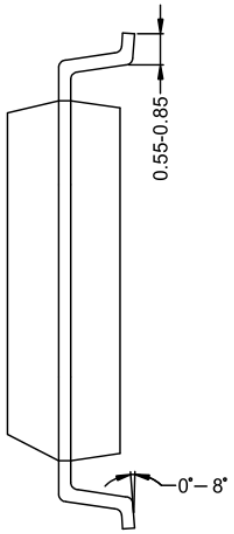


Figure 12. SQ55801 PCB Layout Suggestion

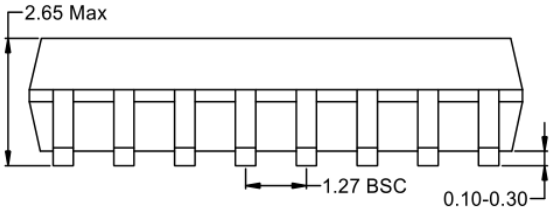
SOP14W Package Outline & PCB Layout



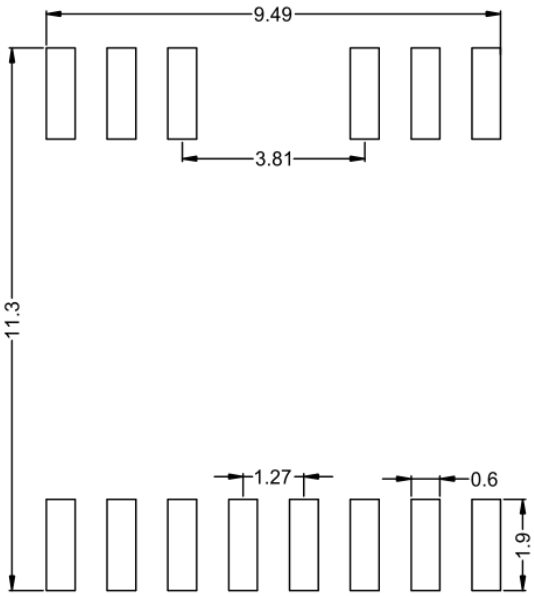
Top View



Side View



Front View

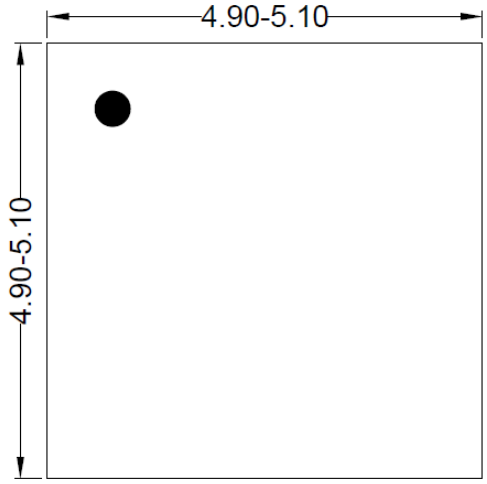


Recommended PCB Layout

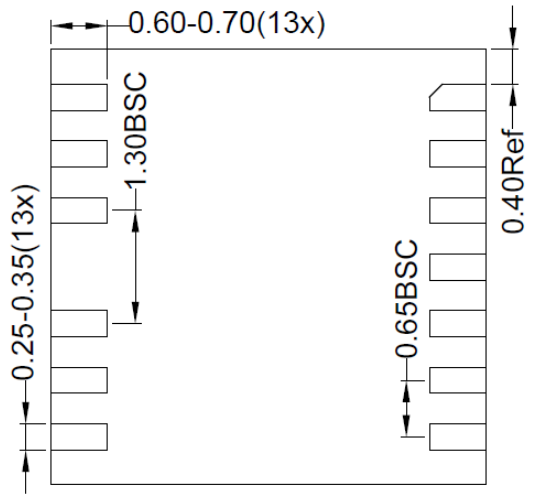
(reference only)

Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

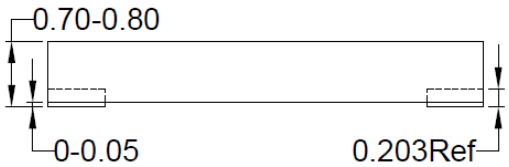
DFN5x5-13 Package Outline & PCB Layout



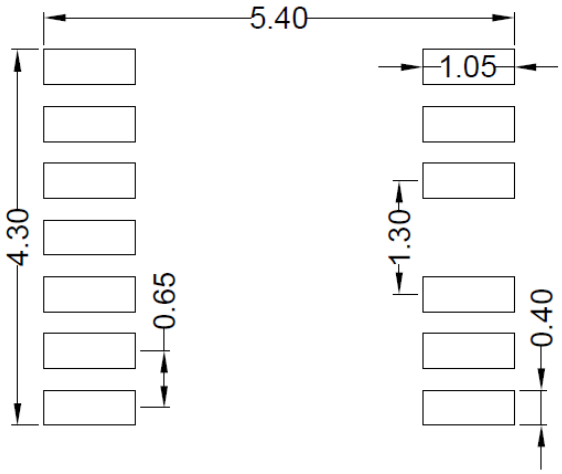
Top View



Bottom View



Front View

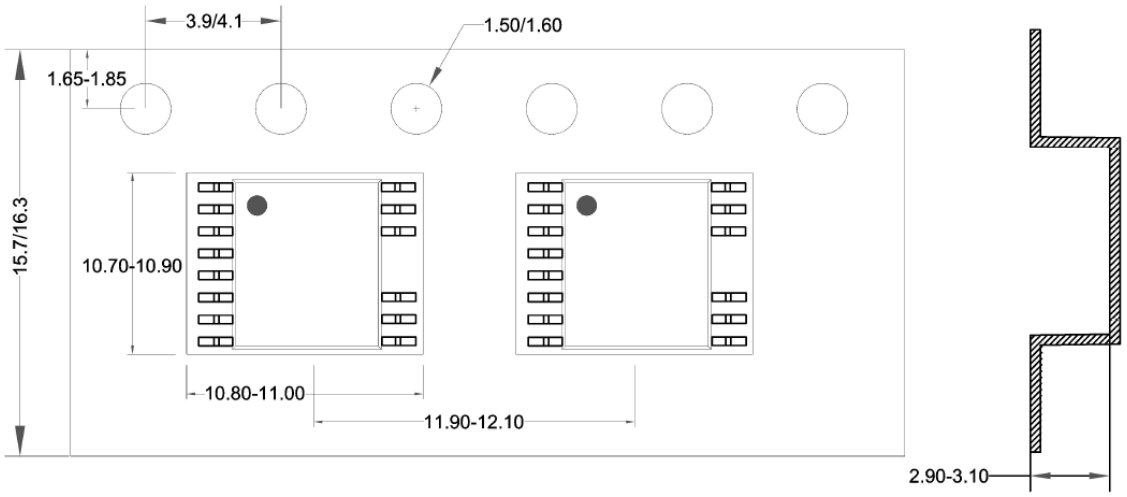


Recommended PCB layout
(Reference only)

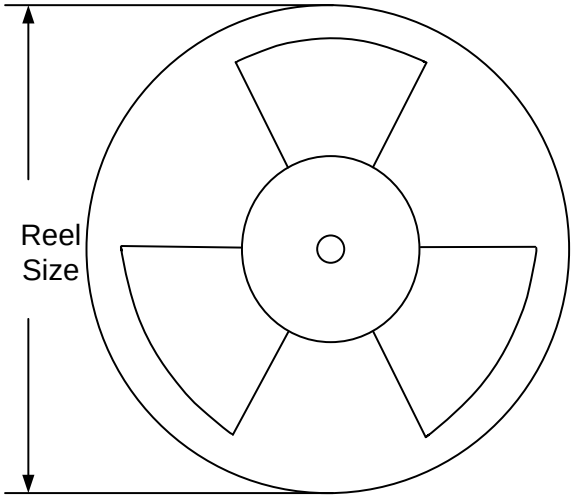
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Specifications (SQ55800)

1. SOP14W Tape Orientation



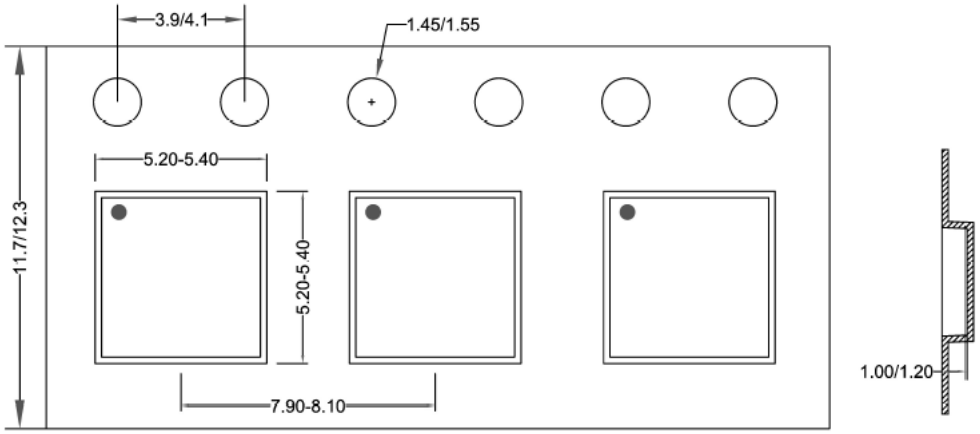
2. Carrier Reel Specification



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SOP14W	16	12	13"	400	400	1500

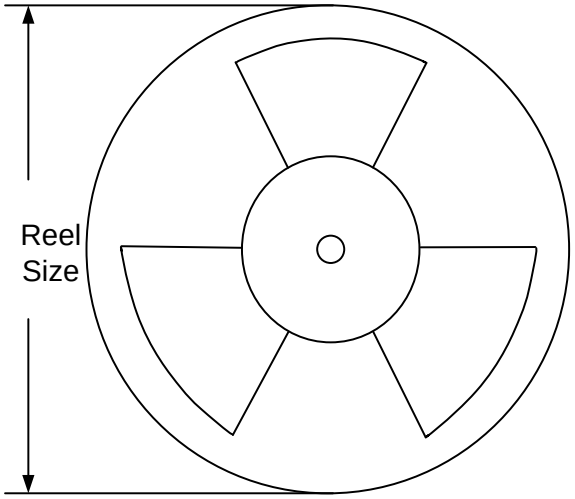
Tape and Reel Specifications (SQ55801)

1. DFN5*5-13 Tape Orientation



Feeding Direction ⟶

2. Carrier Reel Specification



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
DFN5*5-13	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please ensure that you have the latest revision.

Date	Revision	Change
November 12, 2024	Revision 1.0	Initial Release

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