SA63000B

SPI Communication Transceiver for Automotive Battery Management System

1. General Description

The SA63000B is a communication transceiver that combines SPI and a daisy-chain UART interface, specially designed for Silergy's automotive battery management devices. These interfaces enable the SA63000B to function as a bridge device, facilitating communication between the host and Silergy's automotive battery management devices.

The SA63000B integrates a 32-byte RX buffer and a 256-byte TX buffer to efficiently manage the communication rate gap between the 2MHz-6MHz SPI and the 0.95Mbps(typ) daisy-chain UART interface.

The SA63000B supports reverse wake-up of the host via the INH pin, which alerts the SBC module when a fault is detected during sleep mode.

2. Features

- Support Power Supply from 4.75V to 24V
- Sleep Mode: Support Reverse Wake-up of the Host with 5μA Quiescent Current
- Active Mode: Support Ring Architecture Communication and Fault Indication
- SPI (2MHz-6MHz): Compatible with 3.3V/5V Logic
- Transformer/Capacitor Isolated Differential Daisy-chain UART Interface
- Support Silergy's Automotive Battery Management Devices
- ASIL-D Functional Safety-Capable
- AEC-Q100 Grade1: -40°C to +125°C
- Package Info: TSSOP16E
- MSL1

3. Applications

- Battery Management Systems (BMS)
- Electric and Hybrid Vehicles (EV/HEV)
- Fuel Cell
- Energy Storage

4. Typical Application Circuit

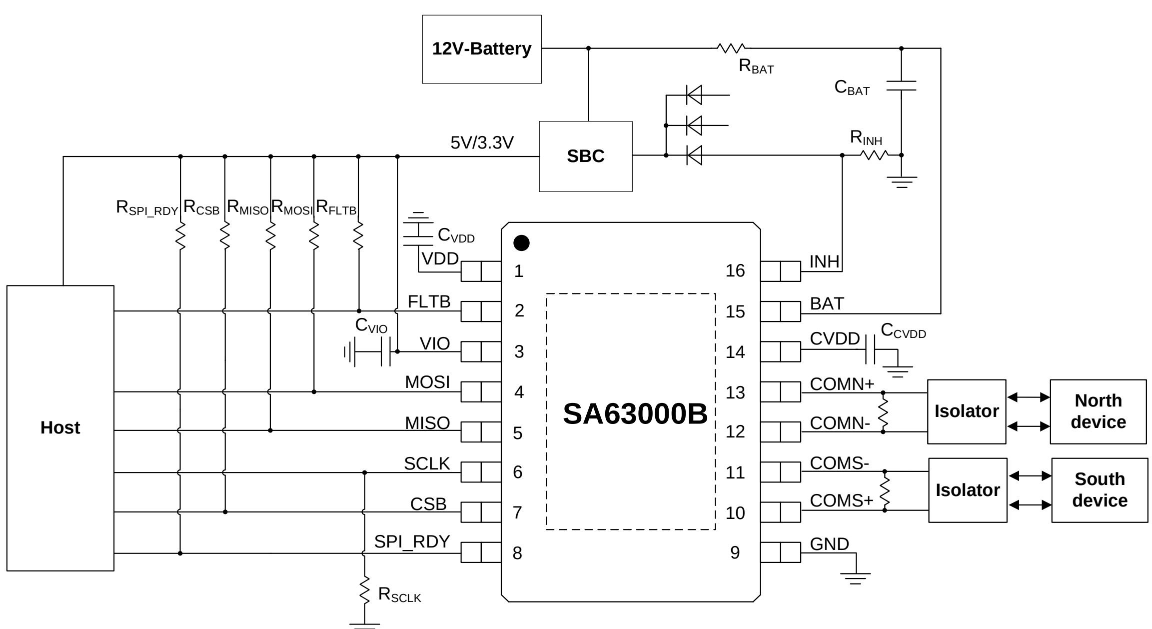

Figure 4-1. Schematic Diagram

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5. Block Diagram

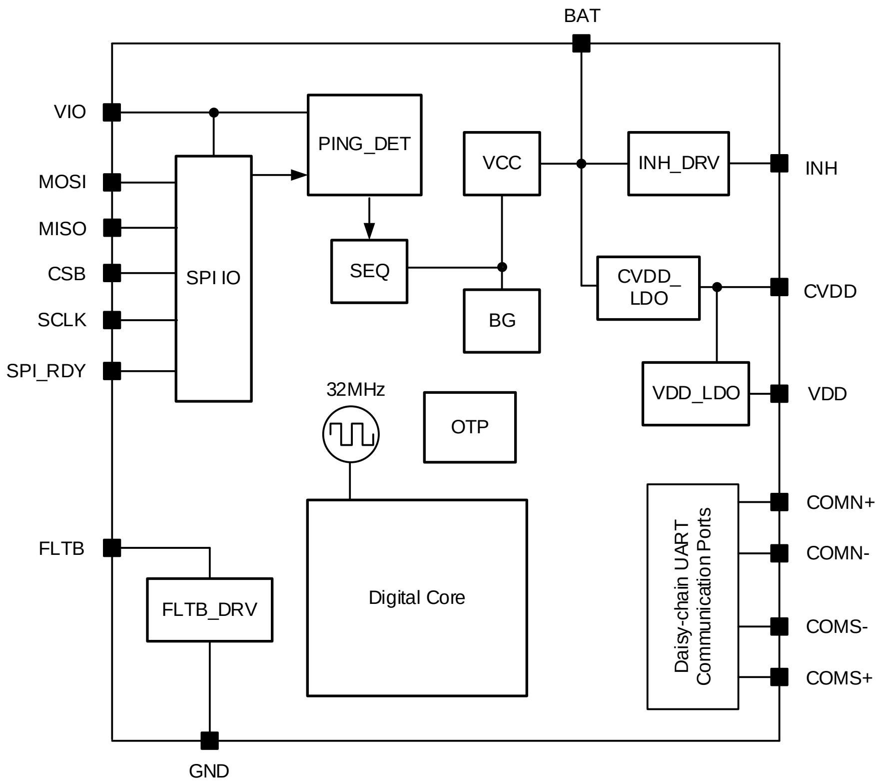


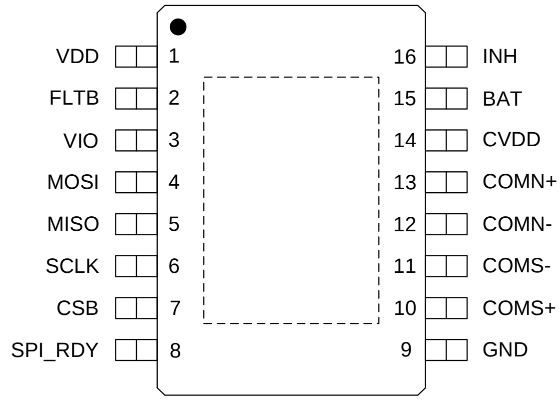
Figure 5-1. Block Diagram

6. Ordering Information

Ordering Part Number	Package Type	Top Mark
SA63000BHFP	TSSOP16E	KDBxyz

x=year code, y=week code, z=lot number code

Pinout (Top View)



Pin Description

Name	Pin	Description
VDD	1	1.8V LDO power output pin. Power supply for digital circuit.
FLTB	2	Fault indication output pin. Open drain output and active-low. Connect it to the host GPIO port and the VIO pin with a 100kΩ pull-up resistor.
VIO	3	3.3V or 5V power input pin. Power supply for the SPI communication module.
MOSI	4	SPI communication data input pin. Connect it to the SPI controller MOSI port and the VIO pin with a 10kΩ pull-up resistor.
MISO	5	SPI communication data output pin. Connect it to the SPI controller MISO port and the VIO pin with a 10kΩ pull-up resistor.
SCLK	6	SPI communication clock input pin. Connect it to the SPI controller SCLK port and the GND pin with a 10kΩ pull-down resistor.
CSB	7	SPI communication chip-select input pin. Active-low and pull it down to the ground to enable peripheral SPI communication. Connect it to the SPI controller CSB port and the VIO pin with a 10kΩ pull-up resistor.
SPI_RDY	8	SPI communication state indication pin. Active-high and indicates whether SPI module is ready to receive or transmit data. Connect it to the SPI controller GPIO port and the VIO with a 100kΩ pull-up resistor.
GND	9	Ground pin.
COMS+	10	Daisy-chain UART communication south positive pin. Connect it to the stack device's COMN+ pin via an isolator.
COMS-	11	Daisy-chain UART communication south negative pin. Connect it to the stack device's COMN- pin via an isolator.
COMN-	12	Daisy-chain UART communication north negative pin. Connect it to the stack device's COMS- pin via an isolator.
COMN+	13	Daisy-chain UART communication north positive pin. Connect it to the stack device's COMS+ pin via an isolator.
CVDD	14	5.5V LDO power output pin. Power supply for daisy-chain UART communication circuit.
BAT	15	Device power input pin. Power supply for the transceiver device. An automotive 12V battery system or 5V SBC module is suitable.
INH	16	Alert indication output pin to support reverse wake-up function. Active-high and alerts the SBC module when a fault is detected during sleep mode. Connect it to the ground with a 100kΩ pull-down resistor.

7. Specifications

7.1 Absolute Maximum Ratings(1)

Parameter	Min	Max	Unit
BAT, INH	-0.3	+40	V
VIO, CVDD, SCLK, MISO, MOSI, CSB, FLTB, SPI_RDY	-0.3	+6	
VDD	-0.3	+2	
COMN+, COMN-, COMS+, COMS- (relative to GND)	-10	+10	
COMN+ to COMN-, COMS+ to COMS-	-6	+6	
Junction Temperature	-40	+150	°C
Lead Temperature (Soldering, 10s)		+260	
Storage Temperature	-65	+150	

7.2 ESD Susceptibility

Parameter	Min	Max	Unit
HBM (Human Body Mode)	-2	+2	kV
CDM (Charged Device Mode) for pin1,8,9,16	-750	+750	V
CDM (Charged Device Mode) for other pins	-500	+500	V

7.3 Recommended Operating Conditions(2)

Parameter	Min	Max	Unit
BAT	+4.75	+24	V
VIO, SCLK, MISO, MOSI, CSB, FLTB, SPI_RDY	+3.1	+5.2	
Ambient Temperature Range	-40	+125	°C

7.4 Thermal Information(3)

Parameter	Typ	Unit
θ_{JA} (Junction-to-ambient thermal resistance)	28.4	°C/W
$\theta_{JC(top)}$ (Junction-to-case(top) thermal resistance)	20	
$\theta_{JC(bottom)}$ (Junction-to-case(bottom) thermal resistance)	2.6	
θ_{JB} (Junction-to-board thermal resistance)	15.3	
Ψ_{JT} (Junction-to-top characterization parameter)	0.3	

8. Electrical Characteristics[4]

V_{BAT} =12V, V_{VIO}=3.3V, –40ºC ≤T_A≤125ºC. T_A=25ºC for typical, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage						
Operation Voltage	V_{BAT}	When the reverse wake-up feature is used, the BAT pin is powered by a “12V battery” system	5.5		24	V
		When the reverse wake-up feature is not used, BAT and CVDD are powered together by regulated 5V voltage	4.75		5.5	V
Thermal Sleep						
Thermal Sleep Threshold	T_{TSLP_R}[5]	Rising edge		150		°C
	T_{TSLP_HYS}[5]	Falling hysteresis		10		°C
Supply Current						
Current in Sleep Mode	I_{SLP_IDLE}	V_{BAT}=12V, V_{VIO}=0V, V_{INH}=0V, no fault, COMS RX enabled, measured through BAT pin		5	10	μA
Baseline Current in Active Mode	I_{ACT_IDLE}	V_{BAT}=12V, V_{VIO}=3.3V, no communication, measured through BAT pin		3	4	mA
Additional Communication Current to Baseline Current in Active Mode	I_{ACT_COMM}	Supports any number of bytes for continuous communication at COMN or COMS ports (with two1kΩ terminal resistors in parallel at daisy-chain UART)		10		mA
Power Supply (CVDD)						
CVDD Output Voltage	V_{CVDD}	No load, C_{CVDD}=1μF, in active mode	5.3	5.5	5.7	V
CVDD Limit Current	I_{CVDD_LIMIT}	V_{CVDD} falls to 4V	44	60	75	mA
CVDD Short Current	I_{CVDD_SHORT}	V_{CVDD} falls to 0V		14	24	mA
CVDD Dropout Voltage	V_{DROP_CVDD}	I_{CVDD}=10mA		0.13	0.25	V
Power Supply (VDD)						
VDD Output Voltage	V_{VDD}	No load, C_{VDD}=1μF, in active mode	1.75	1.8	1.86	V
VDD Limit Current	I_{VDD_LIMIT}	V_{VDD} falls to 1.65V	5	16	27	mA
Power Supply (VIO)						
VIO UV Rising Threshold	$V_{VIO\_UV\_R}$	Measured threshold voltage by increasing VIO voltage until the device can be awakened	2.68	2.8	2.93	V
VIO UV Hysteresis	$V_{VIO\_UV\_HYS}$			200		mV
INH Driver						
Voltage Drop from BAT to INH	V_{DROP_INH}	I_{INH}=0.5mA, when INH is pulled high		0.6	1	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital I/Os (MISO, SPI_RDY, FLTB, CSB, SCLK, MOSI)						
Output Logic High Voltage	V_{OH}	MOSFET pull up, I_{OUT} = 0.5mA, V_{VIO} = 3.3V or 5V	V_{VIO}-0.1V			
Output Logic Low Voltage	V_{OL}	MOSFET pull down, I_{IN} = 0.5mA, V_{VIO} = 3.3V or 5V			0.15	V
Input Logic High Voltage	V_{IH}	V_{VIO} = 3.3V or 5V	0.75×V_{VIO}			
Input Logic Low Voltage	V_{IL}	V_{VIO} = 3.3V or 5V			0.25×V_{VIO}	
FLTB Pull-down Impedance	R_{FLTB_PD}				1000	Ω
Daisy-chain UART Communication Bus						
Common Mode Voltage (COMN+/ COMN-/ COMS+/ COMS- Pins)	V_{DCCM_ACT}	Measured voltage from COMN/S ports to the ground in active mode	2.65		2.85	V
	V_{DCCM_SLP}	Measured voltage from COMS port to the ground in sleep mode	0.9	1	1.2	V
COMN/S Ports Receiving Voltage Threshold	$V_{COM\_THRESH\_R}$	Differential(|V_{COMN+}-V_{COMN-}| or |V_{COMS+}-V_{COMS-}|) rising edge threshold for communication and tone detection	0.35		1.35	V
	$V_{COM\_THRESH\_F}$	Differential(|V_{COMN+}-V_{COMN-}| or |V_{COMS+}-V_{COMS-}|) falling edge threshold for communication and tone detection	0.25		1.05	V
COMN/S Ports Transmitting Impedance	R_{COM}	Pull-up or pull-down impedance on COMN+/COMN-/COMS+/COMS- pin when communication and tone transmitting		12	25	Ω
Operational Modes Switching Timing						
Startup Time from Sleep Mode to Active Mode	$t_{SLP2ACT}$	From WAKE ping received to fully operation. C_{CVDD}= 1μF, C_{VDD} = 1μF			2.2	ms
Reset Time in Active Mode	t_{RST}	From WAKE ping received to digital reset completed in active mode			350	μs
Time from Active Mode to Sleep Mode	$t_{ACT2SLP}$	From SLEEP ping received to entering sleep mode			30	μs
INH Driver Timing						
Delay Time of INH is Activated	t_{INH_DLY}	From first couplet of FLT tone received to INH pin pulling high	719	720	721	μs
Ping Signal Timing						
WAKE Ping Low Time on MOSI Pin	t_{HLD_WAKE}	MOSI pin low-pulse width to awaken device, V_{BAT} = 12V, V_{VIO} = 3.3 or 5V	2.5		3	ms
SLEEP Ping Low Time on MOSI Pin	t_{HLD_SLP}	MOSI pin low-pulse width to make device enter sleep mode, V_{BAT} = 12V, V_{VIO} = 3.3 or 5V	12.5			ms
Daisy-chain UART Communication Bus Timing						

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Data Pulse Width Transmitting on COMN/S Ports	t_{WIDTH_DATA}	Differential half bit time of transmitting communication data		250		ns
Tone Pulse Period Time	t_{PERIOD_TONE}			12		μs
Tone Pulse Width	t_{WIDTH_TONE}			1		μs
HB(Heartbeat) Tone Time Out Threshold	t_{HB_TO}		718	820	930	ms
HB Tone Fast Time Threshold	t_{HB_FAST}		190	200	230	ms
HB Tone Pulse Number Threshold for Detection	$N_{HB\_TONE\_DET}$			20		
FLT Tone Pulse Number Threshold for Detection	$N_{FLT\_TONE\_DET}$			60		
WAKE Tone Pulse Number	N_{WAKE_TONE}			90		
STA(Sleep to Active) Tone Pulse Number	N_{STA_TONE}			30		
SD(Shutdown) Tone Pulse Number	N_{SD_TONE}			270		
SPI Timing (CSB, SCLK, MOSI, MISO) (Refer to Figure 10-6 and Figure 10-7)						
SPI Clock Frequency	f_{SCLK}		2		6	MHz
SPI COMM CLEAR Signal	$N_{SPI(CLR)}$			8		bit
SPI Clock Rising Edge Time	t_{SCLK_R}	25% to 75%			10	ns
SPI Clock Falling Edge Time	t_{SCLK_F}	75% to 25%			10	ns
SPI Clock High Time	t_H		83			ns
SPI Clock Low Time	t_L		83			ns
MISO Rising Edge Time	t_{MISO_R}	V_{VIO}=3.3V or 5V, no capacitor load		15		ns
MISO Falling Edge Time	t_{MISO_F}	V_{VIO}=3.3V or 5V, no capacitor load		15		ns
MOSI Rising/Falling Edge Time	$t_{MOSI\_R/F}$				10	ns
CSB Falling Edge (25%) to SCLK Rising Edge (75%)	t_1		500			ns
SCLK Falling Edge (25%) to CSB Rising Edge (75%)	t_2		500			ns
CSB Falling Edge (25%) to Stable MISO(L:20%, H:80%)	t_3	Timing is defined at device pins, exclude propagation delay of PCB traces (from device perspective)			72	ns
SCLK Falling Edge (25%) to Stable MISO(L:20%, H:80%)	t_4	Timing is defined at device pins, exclude propagation delay of PCB traces (from device perspective)			72	ns
MOSI Setup Time, from MOSI Falling Edge (25%) or Rising Edge (75%) to SCLK Rising Edge(75%)	t_5		40			ns
MOSI Hold Time, from SCLK Rising Edge (75%) to Stable MOSI (L: 20%, H: 80%)	t_6		40			ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CSB Rising Edge (75%) to CSB Falling Edge (25%)	t_7		1			μs
SPI Byte Period Time	t_8	Byte period time (including byte and byte interval time) within one write or read operation at SPI			7.5	μs
Oscillator						
High Frequency Oscillator	f_{HFO}		30.38	32	33.5	MHz
Low Frequency Oscillator	f_{LFO}		243	256	267	kHz

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The device is not guaranteed to function outside its operating conditions.

Note 3: Package thermal resistance is measured in the natural convection at T_A = 25˚C and chip mounted on a high effective four layers PCB with thermal via in accordance with JESD 51-5 and 51-7.

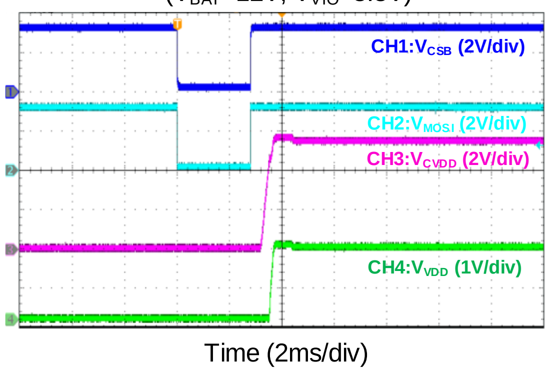
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25˚C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production test.

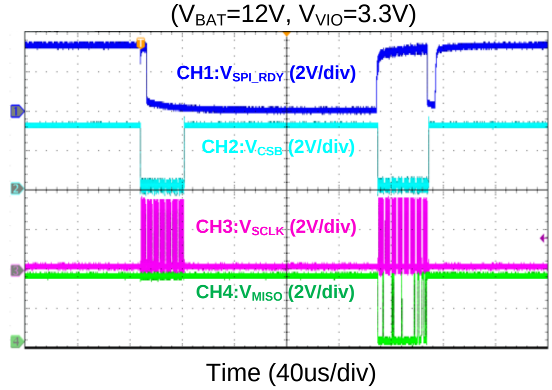
9. Typical Performance Characteristics

(V_{BAT} = 12V, V_{VIO} = 3.3V, T_A = 25°C, otherwise specified.)

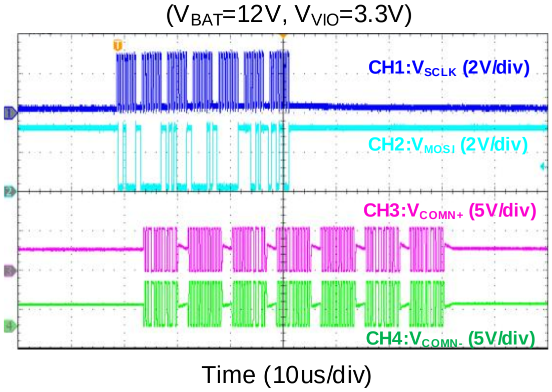
Wake up from Sleep Mode to Active Mode by Wake Ping (V_{BAT}=12V, V_{VIO}=3.3V)



SPI Communication (Read Command and Response) (V_{BAT}=12V, V_{VIO}=3.3V)



Command Propagation in COMN+/- Ports (V_{BAT}=12V, V_{VIO}=3.3V)



Reversely Wake up in Sleep Mode (V_{BAT}=12V, V_{VIO}=3.3V)

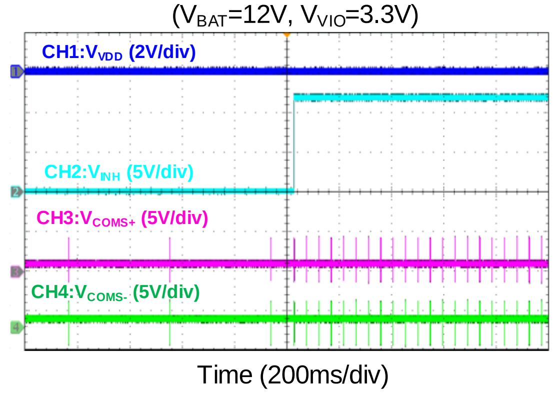


Figure 9-1. Test Results

10. Operating Description

10.1 Device Operating Mode

10.1.1 Sleep Mode

The lowest power dissipation state without power supply VIO occurs in sleep mode. In this mode, the SA63000B can detect fault states in the system (SA63000B and stack(1) devices). The HB tone and FLT tone from stack devices will be monitored. Upon detecting a fault, the SA63000B can alert the host via the INH pin, triggering a reverse wake-up.

10.1.2 Active Mode

In the fully operational state, the SA63000B functions as a bridge(2) device, facilitating communication between the host and stack devices. The bridge device uses SPI to communicate with the host and daisy-chain UART to communicate with stack devices. Additionally, the SA63000B can independently communicate with the host.

10.1.3 Mode Switch

Available functions under different operating modes are shown in Table 10-1:

Table 10-1. Mode/State Summary

	Sleep Mode	Active Mode
CVDD	/	Y
VDD	/	Y
WAKE ping detection	Y	Y
SLEEP ping detection	/	Y
SPI and daisy-chain UART communication	/	Y
FLT tone detection	Y	/
HB tone detection	Y	/

Different modes/states can be switched by the methods shown in Figure 10-1.

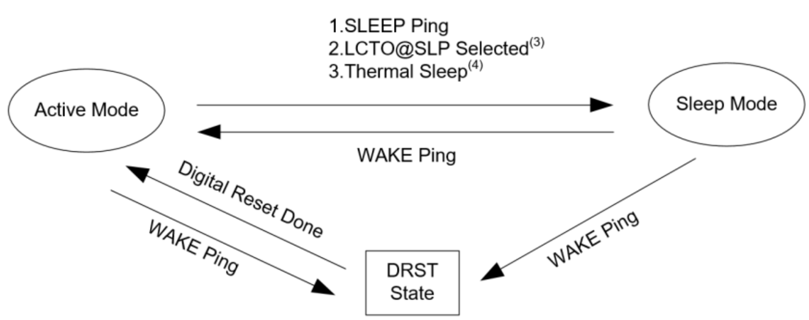


Figure 10-1. Mode/State Switch Diagram

The power mode transition sequence is shown in Figure 10-2.

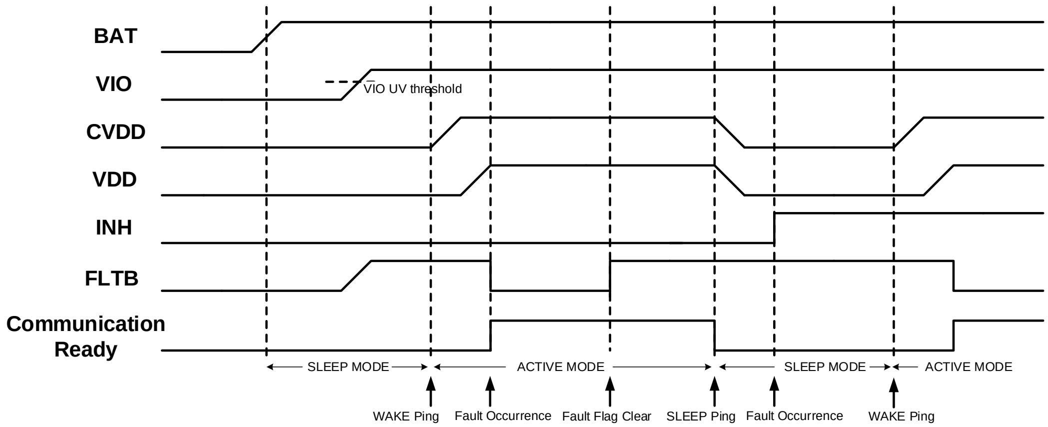


Figure 10-2. Power Mode Transition Sequence

A ping is a specific signal pattern used to change mode of the SA63000B, as shown in Figure 10-3. There are two types of pings: WAKE ping and SLEEP ping.

- If a WAKE ping is received via SPI in sleep mode, the SA63000B will enter active mode. If a WAKE ping is received in active mode, the digital core will reset.
- If a SLEEP ping is received via SPI in active mode, the SA63000B will enter sleep mode.

Pings are generated by the CSB signal and MOSI signal. The ping time width definitions are specified by t_{HLD_WAKE} and t_{HLD_SLP} in the Electrical Characteristic Table.

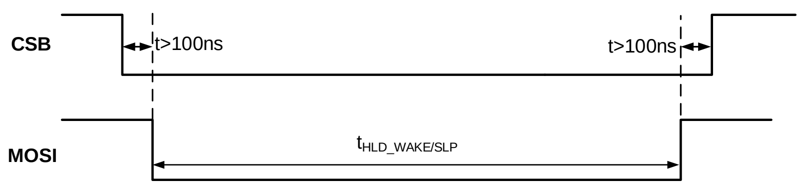


Figure 10-3. Ping Characteristic

Note:

1. Stack devices: BMS series devices(device 1 to device n).
2. Bridge device: SA63000B device.
3. LCTO@SLP: The SA63000B will enter sleep mode when a long communication timeout occurs. The timeout duration is set by the register COMM_TO[LONG<5:3>] if COMM_TO[LCTO_SEL]=1. Meanwhile the FLT2[LCTO_SLP] fault will be triggered.
4. Thermal Sleep(TSLP): The device will enter sleep mode if the junction temperature exceeds the T_{TSLP_R} defined in the Electrical Characteristic Table. Meanwhile, the FLT1[TSLP] fault will be triggered.

10.2 Communication

10.2.1 Communication Transceiver Overview

When the host communicates with stack devices, the bridge device receives command(CMD) data from the host via SPI[1] and propagates it to stack devices via the daisy-chain UART interface[2]. The bridge device then receives response(RESP) data from stack devices via daisy-chain UART interface and outputs it to the host via SPI. When the host communicates with the SA63000B itself, the SA63000B receives commands from the host via SPI, propagates the command to the daisy-chain UART interface, and replies with the response via SPI.

Note:
1. SPI: SPI communication interface(CSB/SCLK/MOSI/MISO/SPI_RDY pins).
2. Daisy-chain UART interface: COMN port(COMN+/COMN- pins) and COMS port(COMS+/COMS- pins).
- When register COMM_CONF[SPI_DIR]=0, transceiving command and response data via COMN port.
- When register COMM_CONF[SPI_DIR]=1, transceiving command and response data via COMS port.

The transmission path of command and response data can only be chosen in one direction at a time(COMN or COMS port alternative for bridge device) shown in Figure 10-4:

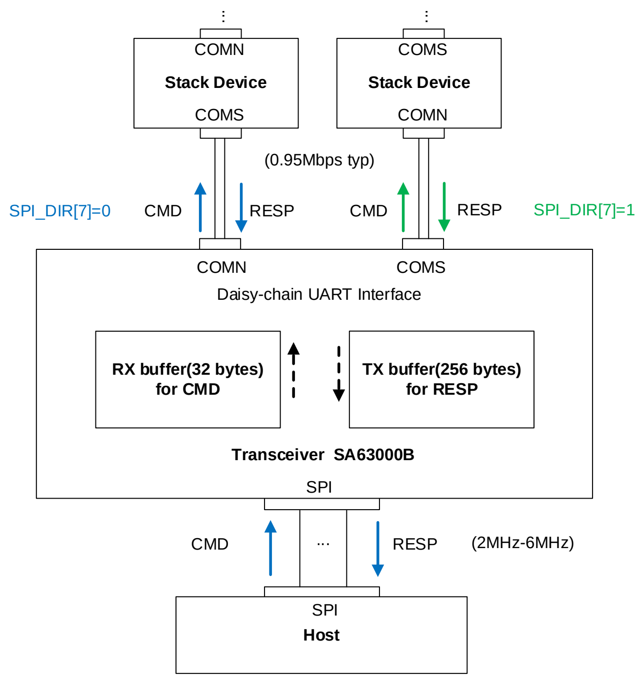


Figure 10-4. Communication Transceiver Diagram

The bridge device includes two types of buffers: a 32-byte receiving buffer(RX buffer) and a 256-byte transmitting buffer(TX buffer). These buffers are essential for the bridge device due to the differing nature of the communication interfaces. SPI operates with synchronous communication, while the daisy-chain UART interface operates with asynchronous communication, and the two interfaces communicate at different rates.

The RX buffer stores command data from SPI and outputs data to daisy-chain UART interface. The 32-byte RX buffer is sufficient for one command. The FLT1[RX_BUF_OF] fault will be reported if the RX buffer is filled (32 bytes) and the host continues transmitting command data bytes to the RX buffer. Consecutive commands must have a sufficient time interval in SPI to ensure that the previous command finishes transmitting via the daisy-chain UART interface.

The TX buffer stores response data from the daisy-chain UART interface or bridge device itself and outputs data to SPI. As the number of response data bytes from stack devices may exceed 256 bytes, the TX buffer consists of two 128-byte buffers (buffer1 and buffer2). These buffers alternate as follows:
1. When buffer1 is filled, buffer2 will store incoming data.
2. While buffer2 is being filled, buffer1 should be read simultaneously. Buffer1 must be emptied (read out) before buffer2 is full.
3. After buffer2 is filled, buffer1 resumes storing incoming data.

4. This loop (step 1 to 3) continues until all response data are received via the daisy-chain UART interface and read out via SPI.
5. Host has to read the TX buffer quickly enough so that one buffer is read out before the other is full. If incoming data needs to be stored in a buffer that hasn't been read out, the FLT1[TX_BUF_OF] fault will be reported. If the TX buffer is empty but still being read, the FLT1[TX_BUF_UF] fault will be reported.

Any command data received from the host will be propagated to stack devices. The delay time for the first byte from SPI to daisy-chain UART interface is about one-byte time for the bridge device.

Any response data received from stack devices via daisy-chain UART interface will be output to the host via SPI. The delay time for the first byte from the daisy-chain UART interface to SPI is related to the SPI_RDY signal, which will be introduced in Section 10.2.3, SPI Overview.

10.2.2 Communication Protocol

The communication protocol at the daisy-chain UART interface is consistent with SPI for bridge device, despite the synchronous and asynchronous communication mechanisms differing between the two interfaces. The communication protocol is detailed below.

The frame type for read-write operation for the bridge device is shown in Table 10-2:

Table 10-2. Frame Type Summary for Bridge Device

Frame Type			Function
Command	Write	Single Write	Write bridge device
	Read	Single Read	Read bridge device
Response			Corresponding to read command

The frame type for read-write operation for stack devices is shown in Table 10-3. The bridge device acts as a copy between host and stack devices.

Table 10-3. Frame Type Summary for Stack Device

Frame Type			Function
Command	Write	Single Write	Write one stack device
		Stack Write	Write all stack devices
	Read	Single Read	Read one stack device
		Stack Read	Read all stack devices
	Addressing		Identify stack devices' address, identify top device in the chain
Response			Corresponding to read command or addressing command

- One write operation consists of one write command frame.
- One single read operation consists of one read command frame and one read response frame.
- One stack read operation consists of one read command frame and several read response frames. One read response frame corresponds to one stack device.
- One addressing operation consists of one addressing command frame and several addressing response frames. One addressing response frame corresponds to one stack device.

Different frames consist of different byte types shown in Table 10-4:

Table 10-4. Frame Byte Type

Frame Type	Byte Type				
	INIT	DEV_ADD	REG_ADD_H&L	DATA1~n	CRC_H&L
	Initialization byte, including basic information of the frame	Device address byte, unique ID for each stack device and bridge device	Register address bytes, first register address for continuous writing or reading	Data bytes to be transmitted or received, payload	Cyclic redundancy check bytes
Single Write	√	√	√	√	√
Single Read	√	√	√	√	√
Stack Write	√	/	√	√	√
Stack Read	√	/	√	√	√
Addressing	√	/	√	√	√
Response	√	√	√	√	√

The byte sequence of a frame is shown in Figure 10-5:

INIT	DEV_ADD	REG_ADD_H	REG_ADD_L	DATA1	···	DATAn	CRC_H	CRC_L

Figure 10-5. Frame Byte Sequence

The INIT byte definition is shown in Table 10-5:

Table 10-5. INIT Byte Definition

<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="6">1:
Command frame</td><td colspan="3">001: Single Write</td><td colspan="4" rowspan="2">Number of data bytes (payload) of the command frame, excluding initial byte, device address, register address and CRC bytes.
0000 = 1 byte
0001 = 2 bytes
…
1111 = 16 bytes</td></tr>
<tr><td colspan="3">011: Stack Write</td></tr>
<tr><td colspan="3">000: Single Read</td><td colspan="4" rowspan="4">0000</td></tr>
<tr><td colspan="3">010: Stack Read</td></tr>
<tr><td colspan="3">100: Addressing</td></tr>
<tr><td colspan="3">101-111:Reserved</td></tr>
<tr><td>0:
Response frame</td><td colspan="7">Number of data bytes (payload) of the response frame.
0000000: 1 byte
0000001: 2 bytes
…
1110111: 120 bytes</td></tr>
</table>

The DEV_ADD byte definition is shown in Table 10-6:

Table 10-6. DEV_ADD Byte Definition

<table>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td colspan="7">The SA63000B device address is fixed at 0x00. Stack device addresses must be assigned different value.
0000000:device address=0x00</td></tr>
</table>

	0000001:device address=0x01 0000010:device address=0x02 ... 1111111:device address=0x7F

The REG_ADD_H&L byte definition is shown in Table 10-7:

Table 10-7. REG_ADD_H&L Byte Definition

D7	D6	D5	D4	D3	D2	D1	D0
REG_ADD_H: high 8 bits of 16-bit register address(range:0x00-0xFF) REG_ADD_L: low 8 bits of 16-bit register address(range:0x00-0xFF) For example: register address=0x4010, REG_ADD_H=0x40, REG_ADD_L=0x10. **Note:** REG_ADD_H or L can not be 0xC0, to access the data at register address 0xXXC0 or 0xC0XX, use continuous reading to read register address at least +1 ahead.							

The DATA1-n byte definition is shown in Table 10-8:

Table 10-8. DATA1-n Byte Definition

D7	D6	D5	D4	D3	D2	D1	D0
• For write command: DATA1-DATAn: Represent the data, which will be written into corresponding register. When continuously written, the register address will automatically increase by 1 for the following data bytes. Each data value range: 0x00-0xFF							
• For read command: DATA1: Represent the wanted number of continuous data bytes (payload in the response frame) from the first register address. 0x00=1 byte 0x01=2 bytes … 0x77=120 bytes(max) **Note:** DATA2-DATAn are not existent.							
• For addressing command: DATA1: Represent the device address to be written into register of the first stack device. D7 shall always be 1. **Note:** DATA2-DATAn are not existent. Only address of the first stack device need to be defined. The address of other stack devices will add 1 in turn from the bottom device to the top device. For example: DATA1=0x81 represent: stack device 1 address is 0x01 stack device 2 address is 0x02 … stack device 127 address is 0x7F(max)							
• For response: DATA1-DATAn: Represent the data being read in the corresponding register. The register address will automatically increase by 1 for the following data bytes when continuously read. Each data value range: 0x00-0xFF							

SA63000B uses the CRC-16 polynomial ($x^{16} + x^{15} + x^2 + 1$) with 0xFFFF initialization to calculate CRC result.

For example: addressing command [0xC0, 0x00, 0x00, 0x81], the CRC result is 0xFC44. So the complete command frame is [0xC0, 0x00, 0x00, 0x81, 0xFC, 0x44].
All bytes in a frame will be covered by CRC. If the CRC result of received command is wrong, this command will be discarded and not be executed. Meanwhile FLT1[FR_CRC] fault will be triggered.
CRC_H&L byte definition is shown in Table 10-9:

Table 10-9. CRC_H&L Byte Definition

D7	D6	D5	D4	D3	D2	D1	D0
CRC_H: high 8 bits of 16-bit CRC result(range:0x00-0xFF) CRC_L: low 8 bits of 16-bit CRC result(range:0x00-0xFF) For example: CRC result=0xFC44, CRC_H=0xFC, CRC_L=0x44							

Note:
The total number of bytes for all response frames in a read operation must not be 128 or multiples of 128.
For example, if there are two stack devices, the number of bytes in the response frame for each stack device cannot be 64.

10.2.3 SPI Overview

Communication between the host and the bridge device is half-duplex SPI communication. The host is always the SPI controller, while the SA63000B is always a peripheral. At the physical layer, SPI is a five-pin interface including CSB, SCLK, MOSI, MISO, and SPI_RDY pins. Figure 10-6 and Figure 10-7 illustrate the SPI communication sequence.
For the byte format, one byte consists of 8 bits with the MSB first.

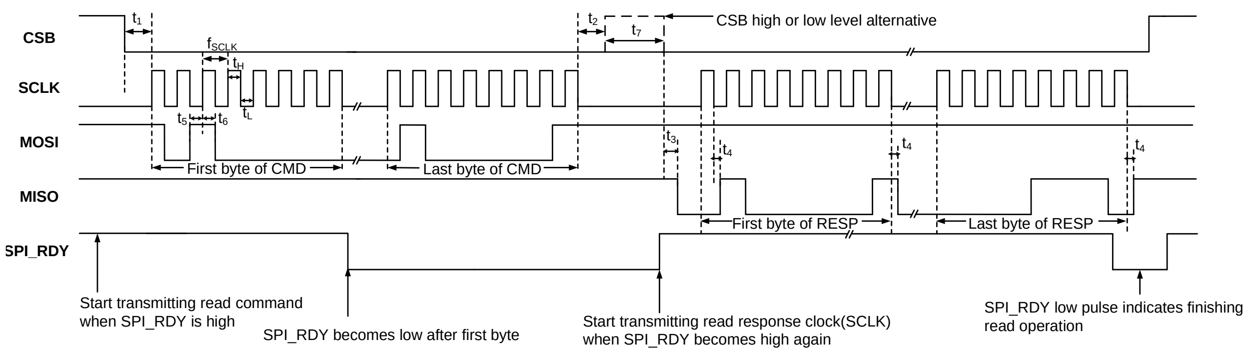


Figure 10-6. SPI Read Timing Definition

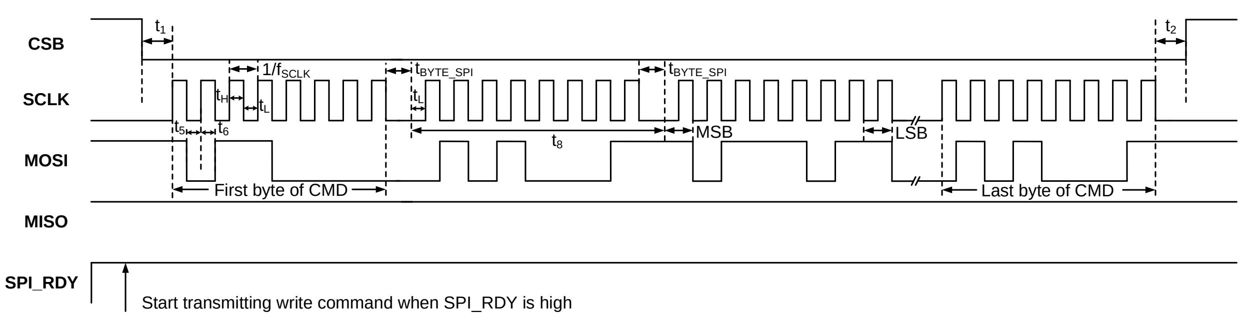


Figure 10-7. SPI Write Timing Definition

CSB Signal:

For a read-write operation, the bridge device uses the falling edge of CSB as the start indication and the rising edge as the end indication.
For a write operation, the host must toggle and keep CSB low for the entire write command frame, then toggle CSB high at the end of the frame. Pulsing CSB in the middle of the write command frame is not supported.
For a read or addressing operation, the host must toggle and keep CSB low for the entire command frame. During the interval between the command frame and the response frame, either high or low level is acceptable. For the response frame, CSB is not required to remain low throughout. The host can toggle CSB high and stop SPI reading in the middle of the frame (at byte boundary) to communicate with another peripheral on the SPI bus, if any, or simply to pause.
To avoid communication collisions, the host must wait until all expected response frames are read out before transmitting the next command frame to the bridge device.

SCLK Signal:

Synchronous clock signal. In SPI, each bit of one byte is sampled on the rising edge of SCLK signal. Therefore, data should complete flipping after the falling edge of the SCLK signal and before the rising edge of the SCLK signal. The idle state of the SCLK signal is low.

MOSI Signal:

The host outputs and the SA63000B inputs signal. The host transmits command data to the MOSI pin. The idle state of the MOSI signal is high.

MISO Signal:

The host inputs and the SA63000B outputs signal. The SA63000B transmits response data to the MISO pin. The idle state of the MISO signal is high.

SPI_RDY Signal:

SPI_RDY is an output signal of the SA63000B that indicates whether communication is ready for the host.
• When the SPI_RDY signal outputs a high level, the host can start the read-write operation.
• When the SPI_RDY signal outputs a low level, the read-write operation should be suspended.
SPI_RDY signal behavior is shown in Table 10-10:

Table 10-10. SPI_RDY Behavior

	High → Low	Low → High
Write Operation	Remaining bytes number in RX buffer >= 24 bytes	Remaining bytes number in RX buffer < 8 bytes

	High → Low	Low → High
Read/Addressing Operation	The first byte of the command frame is received in the RX buffer	Buffer1 or buffer2 is full(=128 bytes) if total bytes number of response data >= 128 bytes
	One of the TX buffer has been read out by the host, while the other TX buffer hasn't finished receiving data (either hasn't been filled up or a timeout occurs) if the total number of	All expected response data is received in the TX buffer and meets 60μs timeout(3)

	response data bytes exceeds 128 bytes(1)	
	All received response data in TX buffer is read out(2)	

Note:
1. When one of the TX buffer is read out and the other has already time out, the SPI_RDY signal will hold high until the other TX buffer is read out.
2. When all received response data in the TX buffer is read out by the host, the SPI_RDY signal will hold low for 6us and then recover to the default high level.
3. TX buffer timeout:
   Timer resets and starts counting after the TX buffer receives one byte of response data. This timer expires if no consecutive data is received within 60μs.

Apart from monitoring the SPI_RDY signal, the host must leave a certain interval time t_{FR}, when transmitting consecutive command frames. This interval time ensures that the bridge device correctly recognizes and propagates consecutive command frames.
The interval for consecutive command frame in SPI is shown in Figure 10-8:

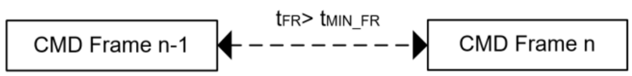


Figure 10-8. SPI CMD Frame Interval

The min interval time between two consecutive command frames:

$$t_{MIN\_FR} = M*[(6.5\mu s+t_{BYTE\_UART}) - (8/f_{SPI\_SCLK}+t_{BYTE\_SPI})] + 15\mu s.$$

- M=total bytes number of previous command frame.
- t_{BYTE_SPI}: the interval time of consecutive bytes received via SPI.
- t_{BYTE_UART}: the interval time of consecutive bytes transmitting via daisy-chain UART interface and is configured by register COMM_CONF[BYTE_INTERVAL<5:0>] bits.

SPI COMM CLEAR:

The SPI COMM CLEAR signal is 1-byte 0x00, as shown in Figure 10-9. The COMM CLEAR signal is used to clear the SPI buffer and reset the SPI module. The COMM CLEAR signal canIt stops the SA63000 bridge device from sendingoutputting response data to the host, and it cannot stop daisy-chainstack devicesstack devices from sendingpropagatingreplying response data back to SA63000the bridge device. The If host still couldn't communicate towith the device, host can ultimately use WAKE ping to reboot the device. DeviceSA63000B only responses toidentifiesrecognizes the COMM CLEAR signal only in active mode.
Use SPI COMM CLEAR signal when:
- SPI_RDY remains low for an extended period beyond the expected time.
- Data read back to the host has a CRC error.
- The host cannot complete the read-write operation normally.

COMM CLEAR signal is ineffective for addressing error. If the host still cannot communicate with the SA63000B normally, it can ultimately use the WAKE ping to reboot the device.

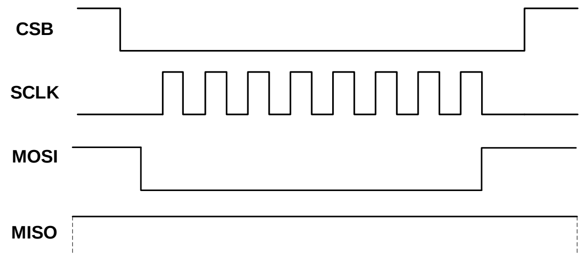


Figure 10-9. SPI COMM CLEAR Signal

Communication Timeout:

A long or short communication timeout fault (FLT1[SCTO] / FLT1[LCTO]) will be triggered if no valid communication occurs beyond a certain time between the host and the SA63000B in SPI. Valid communication refers to a correctly formatted read-write operation in SPI.

- Long communication timeout is set by the register COMM_TO[LONG<5:3>] bits.
- Short communication timeout is set by the register COMM_TO[SHORT<2:0>] bits.

The SA63000B enters sleep mode if a long communication timeout occurs, regardless of COMM_TO[LCTO_SEL] being 1 or 0 for a single read-write operation to a stack device. For other read-write operations to stack devices, the SA63000B enters sleep mode if a long communication timeout occurs when COMM_TO[LCTO_SEL] is 1. The SA63000B enters sleep mode if a long communication timeout occurs when COMM_TO[LCTO_SEL] is 1 for a single read-write operation to the bridge device.

10.2.4 Daisy-chain UART Interface Overview

CMD and RESP Byte Format:

The bit sequence of a byte at daisy-chain UART interface is shown in Figure 10-10:

- The PRE/SYNC0/SYNC1/POS bit is a fixed logic, as shown in Figure 10-10.
- The SOF bit in the INIT byte is always logic “1”, regardless of whether it is a command or response frame. The SOF bits in other bytes of a command frame are logic “0”.
- The D0-D7 bits are the payload, with the LSB (D0) transmitted first.
- The SPARE bit is reserved.

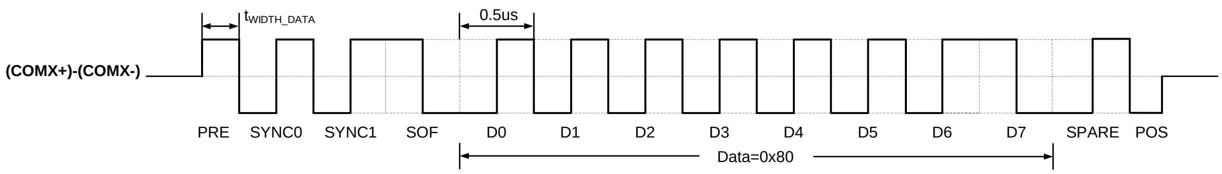


Figure 10-10. Daisy-chain UART Byte Format

COMX refers to either COMN or COMS. The voltage levels of the COMX+ and COMX- pin are complementary. If COMX+ is at a high voltage level, COMX- will be at a low voltage level. The high voltage level is approximately equal to the CVDD voltage, and the low voltage level is approximately equal to the GND voltage.

The bit logic (excluding PRE half bit and POS half bit) definition is shown in Figure 10-11.

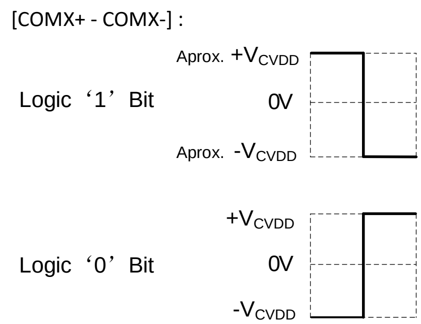


Figure 10-11. Daisy-chain UART Bit Format

The byte interval time within a command frame (nothing with response frame receiving) at the daisy-chain UART can be programmed using the COMM_CONF[BYTE_INTERVAL<5:0>] bits in the bridge device. The new settings will take effect starting with the next command frame after configuring these register bits. The byte interval definition is shown in Figure 10-12.

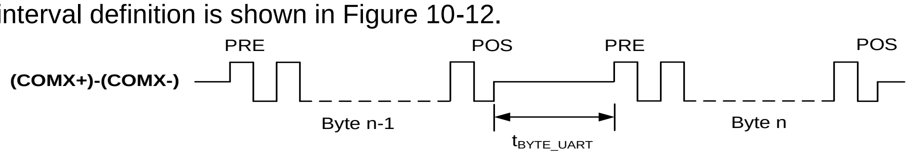


Figure 10-12. Daisy-chain UART Byte Interval

Tone Format:

Tone is a type of differential signal pattern transmitted/received via the daisy-chain UART, as shown in Figure 10-13 and Table 10-11.
The bridge device can generate WAKE tone, STA tone, and SD tone to stack devices. The transmitting port can be selected using the COMM_CONF[SPI_DIR] bit.
The bridge device detects FLT tone and HB tone only at the COMS port in sleep mode, regardless of whether COMM_CONF[SPI_DIR] is set to 0 or 1.

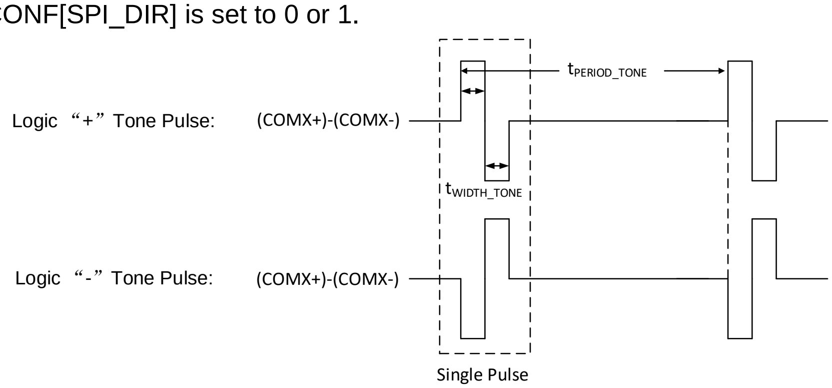


Figure 10-13. Daisy-chain UART Tone Format

Table 10-11. Tone Type Summary

	WAKE Tone	STA Tone	SD Tone	FLT Tone	HB Tone
Pulse Logic	+	+	-	-	-
Pulse Number	90	30	270	90	30
Effective Pulse Number for Detection	/	/	/	60	20

The FLT2[FLT_TONE_DET] fault will be triggered if the bridge device detects FLT tone coming from stack devices during sleep mode.
The FLT2[HB_TO] fault will be triggered if HB tone couplets interval time is greater than t_{HB_TO}. The FLT2[HB_FAST] fault will be triggered if HB tone couplets interval time is less than t_{HB_FAST}.

10.2.5 Ring Architecture

If a ring architecture is used, increased availability can be achieved when any daisy-chain communication cable is open. Communication can continue in the other direction after the bridge's direction is switched using the COMM_CONF[SPI_DIR] bit and the stack devices are re-addressed.
Furthermore, the reverse wake-up function during sleep mode relies on the ring architecture. This is because the FLT tone and HB tone are detected only at the COMS port, while the default communication port for the bridge device is the COMN port. See Figure 10-14.
After changing the COMM_CONF[SPI_DIR] bit, the direction switch will take effect with the next command frame.

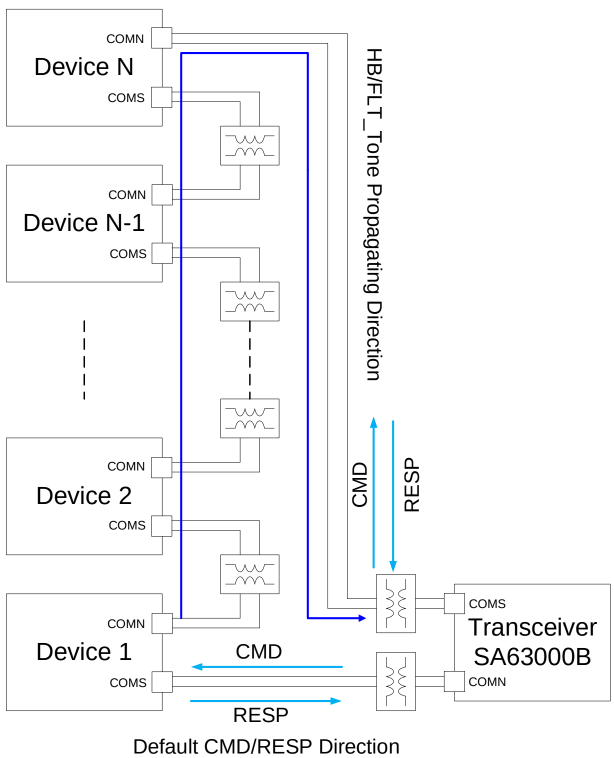


Figure 10-14. Ring Architecture Diagram

10.3 Fault

10.3.1 Fault Detection

Faults are detected in active mode, as shown in Table 10-12:

Table 10-12. Fault Detection Type in Active Mode

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

FLT1	TSLP	SCTO	LCTO	RX_BUF_OF	TX_BUF_OF	TX_BUF_UF	FCOMM	FR_CRC
FLT2	---		LCTO_SLP	---				

• FLT1[TSLP] / FLT2[LCTO_SLP] faults are introduced in Section 10.1.3.
• FLT1[SCTO] / FLT1[LCTO] faults are introduced in Section 10.2.3.
• FLT1[RX_BUF_OF] / FLT1[TX_BUF_OF] / FLT1[TX_BUF_UF] faults are introduced in Section 10.2.1.
• FLT1[FR_CRC] fault is introduced in Section 10.2.2.
• The FLT1[FCOMM] fault indicates that embedded fault information from stack devices has been detected. Embedded fault information means that at least two SOF bits are '1' in the DEV_ADD, REG_ADD_H, or REG_ADD_L bytes at the daisy-chain UART.

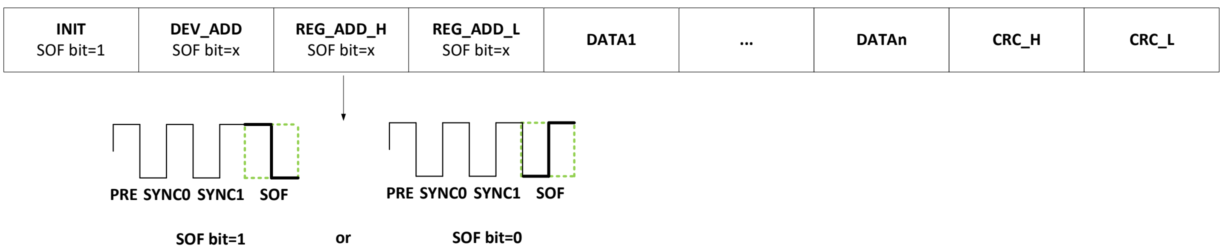


Figure 10-15. Embed Fault Info in RESP

The situation where at least two SOF bits are '1' is shown in Table 10-13.

Table 10-13. SOF Bits Indication Summary

SOF bit in DEV_ADD	SOF bit in REG_ADD_H	SOF bit in REG_ADD_L
1	1	0
1	0	1
0	1	1
1	1	1

Faults detected in sleep mode are shown in Table 10-14:

Table 10-14. Fault Detection Type in Sleep Mode

Name	Bit7	Bit6-Bit3	Bit2	Bit1	Bit0
FLT1	TSLP	---			
FLT2	---		HB_FAST	HB_TO	FLT_TONE_DET

• FLT1[TSLP] faults are introduced in Section 10.1.3.
• FLT2[HB_FAST] / FLT2[HB_TO] / FLT2[FLT_TONE_DET] faults are introduced in Section 10.2.4.

10.3.2 Fault Indication

Once a fault is detected, the fault flag bit will be set to 1 and will remain latched. The fault flag bit is reset by writing '0' to the bit after the fault is cleared.

The FLTB pin is active low to alert the host that a fault flag bit has been set to '1', and the fault occurrence may be in active or sleep mode. The FLTB pin indicates a fault only in active mode and remains at a high level in sleep mode.

The INH pin is active high to alert the SBC module that a fault has occurred during sleep mode. The INH pin will remain at a high level until the fault flag bit is reset in active mode.

When a specific fault mask bit is set to ‘1’, the fault flag bit will not be set to ‘1’ upon the occurrence of the masked fault. This also prevents the SA63000B from alerting the host via the FLTB pin in active mode or alerting the SBC module via the INH pin in sleep mode.

11. Register Map

Name	Add	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
COMM_CONF	0x0000	SPI_DIR	RSVD	BYTE_INTERVAL<5:0>						00
COMM_TO	0x0001	LCTO_SEL	RSVD	LONG<5:3>			SHORT<2:0>			BB
FLT_MASK1	0x0002	TSLP_MSK	SCTO_MSK	LCTO_MSK	RX_BUF_OF_MSK	TX_BUF_OF_MSK	TX_BUF_UF_MSK	FCOMM_MSK	FR_CRC_MSK	00
FLT_MASK2	0x0003	RSVD<7:6>		LCTO_SLP_MSK	RSVD<4:3>		HB_FAST_MSK	HB_TO_MSK	FLT_TONE_DET_MSK	00
CONTROL	0x2000	RSVD<7:3>					WAKE_TONE_GEN	STA_TONE_GEN	SD_TONE_GEN	00
FLT1	0x5002	TSLP	SCTO	LCTO	RX_BUF_OF	TX_BUF_OF	TX_BUF_UF	FCOMM	FR_CRC	00
FLT2	0x5003	RSVD<7:6>		LCTO_SLP	RSVD<4:3>		HB_FAST	HB_TO	FLT_TONE_DET	00

COMM_CONF (Register 0x0000)

Bit	W/R	Default	Name	Description
7	W/R	0	SPI_DIR	This bit can be used to select the propagated direction of command from SPI to COMN port or COMS port. 0: From SPI to COMN port 1: From SPI to COMS port
6	R	0	RSVD	
5	W/R	0	BYTE_INTERVAL<5:0>	These bits can be used to set the byte interval time within one command frame at daisy-chain UART interface. 000000: 1.875μs 000001: 2.125μs(1.875μs+1*0.25μs) 000010: 2.375μs(1.875μs+2*0.25μs) …… 111110: 17.375μs(1.875μs+62*0.25μs) 111111: 17.625μs(1.875μs+63*0.25μs)
4	W/R	0		
3	W/R	0		
2	W/R	0		
1	W/R	0		
0	W/R	0		

COMM_TO (Register 0x0001)

Bit	W/R	Default	Name	Description
7	W/R	1	LCTO_SEL	This bit can be used to select the target mode when the long communication watchdog timer times out. 0: Keep in active mode

Bit	W/R	Default	Name	Description
				1: Enter sleep mode
6	R	0	RSVD	
5	W/R	1	LONG<5:3>	These bits can be used to program the long communication watchdog timer threshold. 000: 0.1s 001: 2s 010: 10s 011: 1min 100: 3min 101: 10min 110: 30min 111: 1hour
4	W/R	1		
3	W/R	1		
2	W/R	0	SHORT<2:0>	These bits can be used to program the short communication watchdog timer threshold. The short communication timeout (SHORT) must be smaller than the long communication timeout (LONG). 000: 0.1s 001: 2s 010: 10s 011: 1min 100: 3min 101: 10min 110: 30min 111: 1hour
1	W/R	1		
0	W/R	1		

FLT_MASKx(Register 0x0002-0x0003)

Bit	W/R	Default	Name	Description
X	W/R	0	XXX_MSK	This bit can be used to mask the corresponding fault flag bit FLTx[XXX] (register 0x5002-0x5003) from being set to 1 when the corresponding fault occurs. 0: Not mask 1: Mask

CONTROL(Register 0x2000)

Bit	W/R	Default	Name	Description
7	R	0	RSVD<7:3>	
6	R	0		
5	R	0		
4	R	0		
3	R	0		
2	W/R	0	WAKE_TONE_GEN	This bit is used to execute the WAKE tone generation according to the COMM_CONF[SPI_DIR] bit. Self-clear bit. 0: Ready 1: Execute
1	W/R	0	STA_TONE_GEN	This bit is used to execute the STA tone generation according to the COMM_CONF[SPI_DIR] bit. Self-clear bit. 0: Ready 1: Execute

Bit	W/R	Default	Name	Description
0	W/R	0	SD_TONE_GEN	This bit is used to execute the SD tone generation according to the COMM_CONF[SPI_DIR] bit. Self-clear bit. 0: Ready 1: Execute

FLT1(Register 0x5002)

Bit	W/R	Default	Name	Description
7	W/R	0	TSLP	This bit indicates that the device junction temperature exceeds the thermal sleep threshold T_{TSLP_R}, and then the device enters sleep mode. When FLT_MASK1[TSLP_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
6	W/R	0	SCTO	This bit indicates that short communication watchdog timer timeout. When FLT_MASK1[SCTO_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
5	W/R	0	LCTO	This bit indicates that long communication watchdog timer timeout. When FLT_MASK1[LCTO_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
4	W/R	0	RX_BUF_OF	This bit indicates that RX buffer overflow(>32 bytes). When FLT_MASK1[RX_BUF_OF_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
3	W/R	0	TX_BUF_OF	This bit indicates that one of the TX buffer (buffer1 or buffer2) starts storage new bytes data but the original stored data has not been read out yet. When FLT_MASK1[TX_BUF_OF_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
2	W/R	0	TX_BUF_UF	This bit indicates that no bytes left in TX buffer but still being read. When FLT_MASK1[TX_BUF_UF_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.

Bit	W/R	Default	Name	Description
1	W/R	0	FCOMM	This bit indicates that embedded fault information in response frame at daisy-chain UART is detected. When FLT_MASK1[FCOMM_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
0	W/R	0	FR_CRC	This bit indicates that CRC error in command frame is detected in SPI. When FLT_MASK1[FR_CRC_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.

FLT2(Register 0x5003)

Bit	W/R	Default	Name	Description
7	W/R	0	RSVD<7:6>	
6	W/R	0		
5	W/R	0	LCTO_SLP	This bit indicates that the device has entered sleep mode due to a long communication watchdog timer timeout. When FLT_MASK2[LCTO_SLP_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
4	R	0	RSVD<4:3>	
3	R	0		
2	W/R	0	HB_FAST	This bit indicates that detected HB tone couplets interval time < t_{HB_FAST}. When FLT_MASK2[HB_FAST_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
1	W/R	0	HB_TO	This bit indicates that detected HB tone couplets interval time > t_{HB_TO}. When FLT_MASK2[HB_TO_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.
0	W/R	0	FLT_TONE_DET	This bit indicates that FLT tone is detected in sleep mode at COMS port. When FLT_MASK2[FLT_TONE_DET_MSK]=1, the corresponding fault flag bit will be masked from being set to 1. 0: No fault or clear fault 1: Fault This bit can only be written to 0 to clear, it can't be written to 1.

12. Design Procedure

Note:
The following application information is just a guide to design schematic and select components. Silergy does not guarantee its accuracy and completeness. Customers should design and validate peripheral circuit of the SA63000B carefully based on system and application requirements.

12.1 Power Supply Recommendation

Table 12-1. Power Supply Parameters Selection Guide

Symbol	Parameter	Description
R_{BAT}	10Ω	This resistor and capacitor can form an RC filter for the BAT pin. A larger RC value may eliminate noise over a wider frequency range. Recommended values should be used for optimal surge performance. The BAT pin operating voltage range is 4.75V-24V. V_{BAT} shall be guaranteed considering the maximum operating current when R_{BAT} is selected. Max(R_{BAT}) =(Input Voltage -4.75V) / I_{PEAK}. Where: I_{PEAK} is the highest operational current, which should account for inrush start-up current. This current (approximately 20mA) depends on PCB components and layout, so it is recommended that the user characterizes this value in their design. The C_{BAT} rating is based on peak voltage spike observed on the pack.
C_{BAT}	100nF/50V	
C_{CVDD}	1μF/16V	Bypass capacitor.
C_{VDD}	1μF/16V	Bypass capacitor.
C_{VIO}	100nF/16V	Bypass capacitor.

12.2 Daisy-chain Isolation Recommendation

There are two typical daisy-chain isolation solutions for PCB: internal isolation for short-distance applications and external isolation for long-distance applications.

Table 12-2. Daisy-chain Isolation Parameters Selection Guide

Symbol	Parameter	Description
R_{TERM}	1kΩ	Termination resistor should be added to reduce differential noise, but the smaller resistance, the bigger current consumption during communication, then 1kΩ termination resistor is reasonable.
R_{SERIES}	51Ω	Add bypass filter to reduce common mode noise, but the bigger series resistor, the smaller amplitude of differential signal, and the bigger capacitor, the worse distortion of differential signal, then 51Ω series resistor and 220pF capacitor are reasonable.
C_{BYPASS}	220pF/50V	

For internal isolation within one PCB, 2.2nF capacitors with a voltage rating of 2x the module voltage can serve as the isolator. TVS diodes should be added to meet higher system ESD requirement and for hot-plug protection.

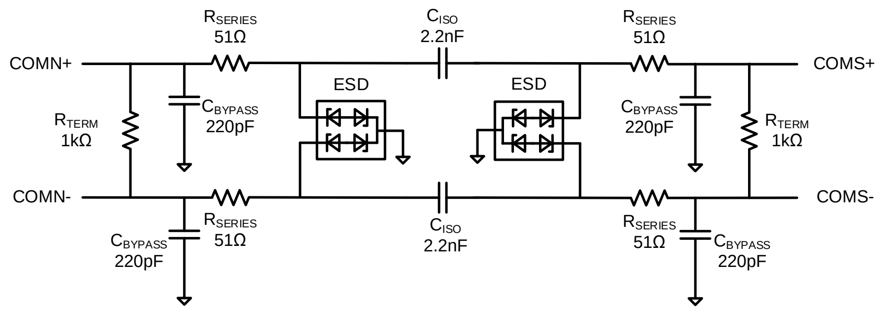


Figure12-1. Capacitor Isolation

For external isolation among different PCBs, such as the low-voltage and high-voltage boundary for galvanic isolation, a transformer with a tap can be used as the isolator. To ensure robust communication, it is highly recommended that the effective differential signal width at the receiver port be greater than 160ns. The transformer selection guidelines are shown in Table 12-3.

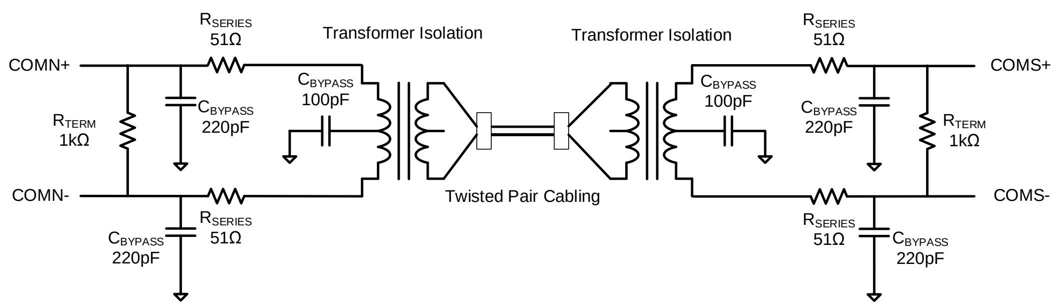


Figure12-2. Transformer Isolation

Table 12-3.Transformer Key Parameter Selection Guide

Parameter	Recommended	Comment
OCL/μH	150 - 450	Generally, it is best to keep pulse edges as fast as possible. A smaller effective pulse width seen by the receiver will reduce the noise margin. If the OCL(Open Circuit Inductance) is too low, the pulse amplitude will decay over the pulse period. Some droop is acceptable as long as it is a relatively small percentage of the total pulse amplitude. LL affects the t_r and t_f.
LL/μH	<2.5	
Turn Ratio	1:1(5%)	
DCR/Ω	<2	

The transformer is a non-standard material and it is an experience value in above table. Customers should select and test carefully based on system and application requirements.

12.3 SPI Communication Recommendation

Table 12-4. SPI Parameters Selection Guide

Symbol	Parameter	Description
R_{MISO}	10kΩ	Pull-up resistor. Considering output logic low voltage < 0.15V, so $R_{DOWN\_MISO} \times V_{VIO} / (R_{MISO}+R_{DOWN\_MISO})$ <0.15V. Where R_{DOWN_MISO} is approximately 100Ω，(Max)V_{VIO} is approximately 5V. The MISO pin has been connected to the VIO pin internally through a pull-up resistor of approximately 60k, so external R_{MISO} serves as a reinforcing effect and is unnecessary.

R_{SPI_RDY}	100kΩ	Pull-up resistor. SPI_RDY pin is an open-drain output pin and needs connect to VIO through R_{SPI_RDY} to keep high-level state default. Considering output logic low voltage < 0.15V, so $R_{DOWN\_SPI\_RDY} \times V_{VIO} / (R_{SPI\_RDY}+R_{DOWN\_SPI\_RDY}) < 0.15V$, Where $R_{DOWN\_SPI\_RDY}$ is approximately 200Ω，(Max)V_{VIO} is approximately 5V.
R_{SCLK}	10kΩ	Pull-down resistor. SCLK pin has been connected to the ground internally through a weak pull-down resistor to keep low level state default, so external R_{SCLK} serves as a reinforcing effect and is unnecessary.
R_{MOSI}	10kΩ	Pull-up resistor. MOSI pin has been connected to VIO internally through a weak pull-up resistor to keep high level state default, so external R_{MOSI} serves as a reinforcing effect and is unnecessary.
R_{CSB}	10kΩ	Pull-up resistor. CSB pin has been connected to VIO internally through a weak pull-up resistor to keep high level state default, so external R_{CSB} serves as a reinforcing effect and is unnecessary.

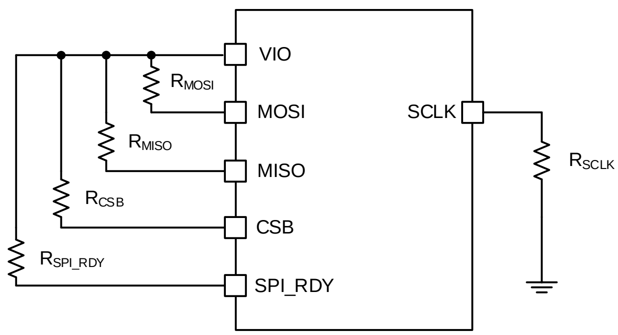


Figure12-3. SPI Communication Ports Connection

12.4 INH/FLTB Indication Recommendation

Table 12-5. INH/FLTB Pin Parameters Selection Guide

Symbol	Parameter	Description
R_{INH}	100kΩ	Pull-down resistor. INH pin should keep a low level state default through R_{INH}.
R_{FLTB}	100kΩ	Pull-up resistor. FLTB pin is an open-drain output pin and should keep a high level state default through R_{FLTB}.

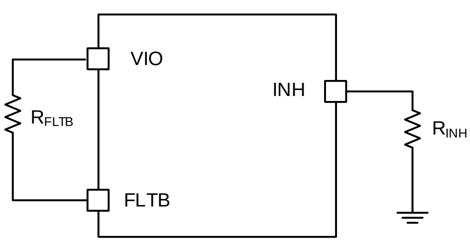


Figure12-4. Indication Pin Connection

12.5 System Connection Recommendation

The SA63000B is a communication transceiver that acts as a bridge device to connect the host and stack devices via SPI communication and daisy-chain UART communication, respectively. The host power supply is the SBC module, which can be enabled by the INH and other signals. The SA63000B power supply is an automotive 12V battery or a 5V SBC module. Stack devices are powered by automotive battery packs. Capacitor Isolation and transformer isolation are typically used for PCB internal isolation and external isolation application, respectively. A ring architecture is recommended for bidirectional communication and the reverse wake-up function. The system connection diagram is shown in Figure 12-5.

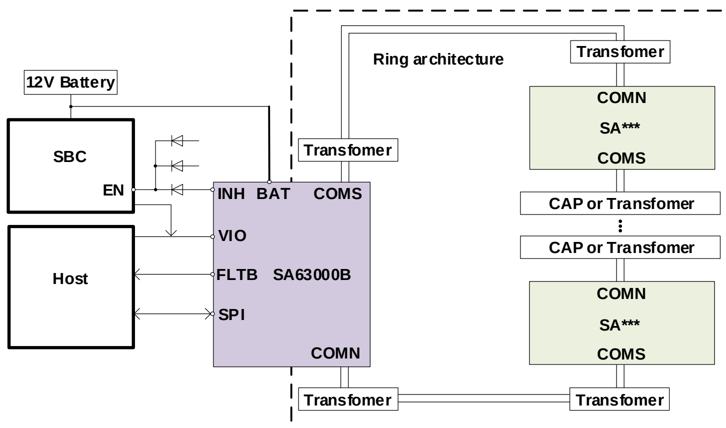


Figure 12-5. Simplified System Diagram

12.6 Application Schematic

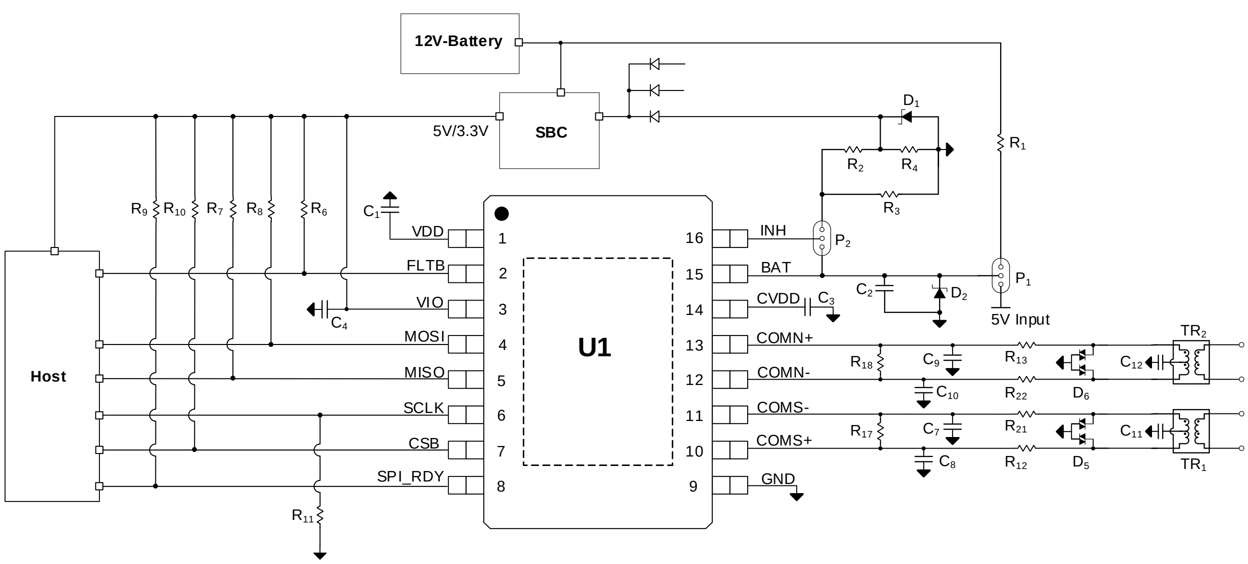


Figure 12-6. Schematic Diagram

12.7 BOM List

Table 12-6. BOM List

Designator	Description	Part Number	Manufacturer
U1	SPI Communication Transceiver	SA63000BHFP	Silergy
C1, C3	16V/1μF, 0603, 10%	GRM188R71C105KE15D	Murata
C2	50V/100nF, 0603, 10%	GCM188R71H104KA57D	Murata
C4	16V/100nF, 0603, 10%	GCM188R71C104KA37J	Murata
C7, C8, C9, C10	50V/220pF, 0603, 5%	GRM1885C1H221JA01D	Murata
C11, C12	50V/100pF, 0603, 5%	GCM1885C1H101JA16J	Murata
R1	10Ω, 0603, 1%		
R3, R6, R9	100kΩ, 0603, 1%		
R7, R8, R10, R11	10kΩ, 0603, 1%		
R12, R13, R21, R22	51Ω, 0603, 5%		
R17, R18	1kΩ, 0603, 1%		
D2	TVS Diode	SMBJ24A	
D5, D6	PESD5V0L2BT		
TR1, TR2	BMS Transformer	C20121T016	Sumida
P1(1), P2(2)	Header, 3-Pin		
R2, R4, D1	NA		

Note:

1. P1 is used to select either a 12V input or a 5V input for the BAT pin.

2. The INH pin is pulled down to the ground by connecting the INH pin and R3 with P2.

12.8 Layout Design

For optimal performance of the SA63000B, the following guidelines must be followed:

- Grounding and bypass
  The bypass capacitors must be tied to the device pins and the corresponding ground.
- Daisy-chain communication
  For robust daisy-chain communication, keep differential traces as short and straight as possible.
  Run the traces in parallel with ground shielding and maintain matching trace impedance.
  Create a keep-out area for the daisy-chain communication components.

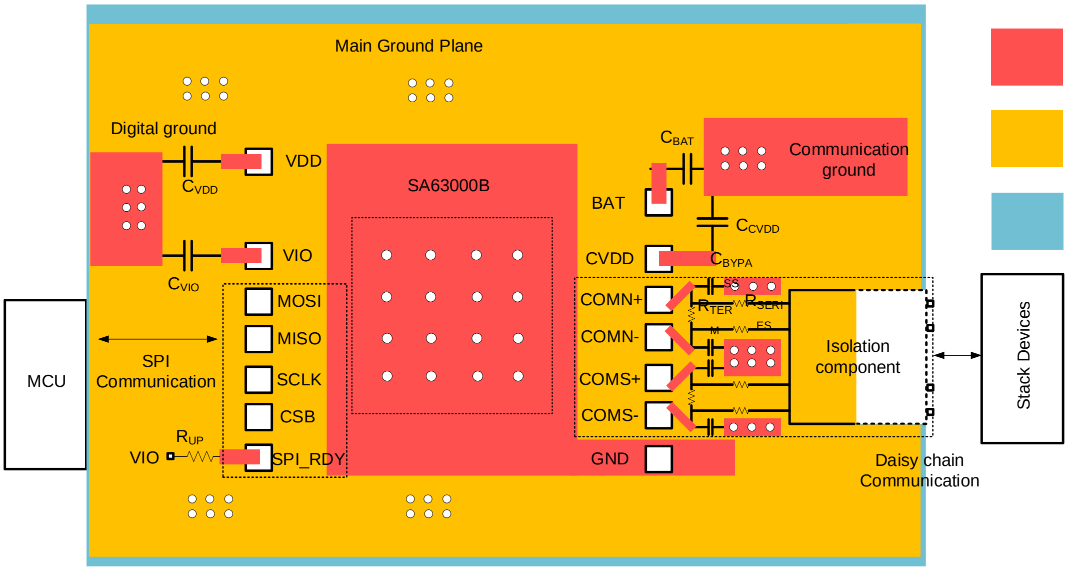
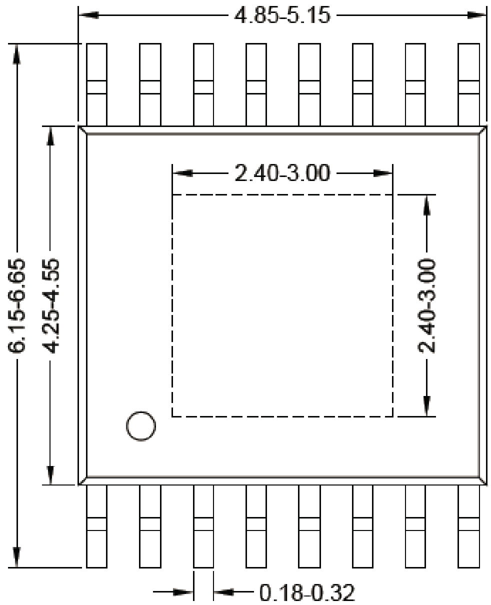
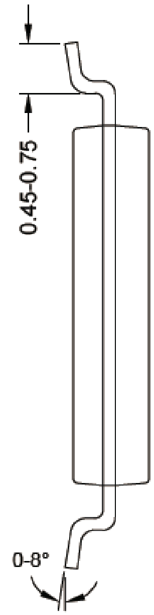


Figure 12-7. PCB Layout Consideration

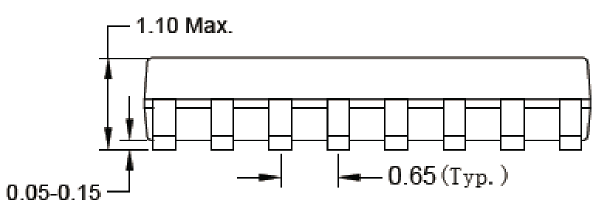
TSSOP16E Package Outline Drawing



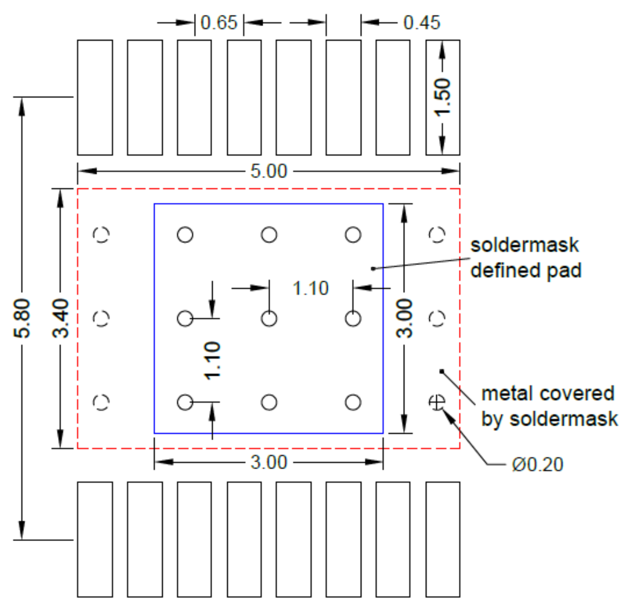
Top View



Side View A



Side View B

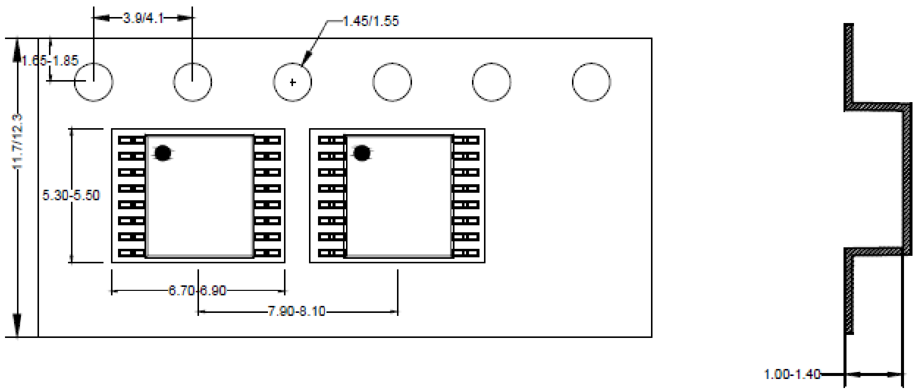


Recommended PCB Layout
(Reference only)

Notes: *All dimension in millimeter and exclude mold flash & metal burr.*

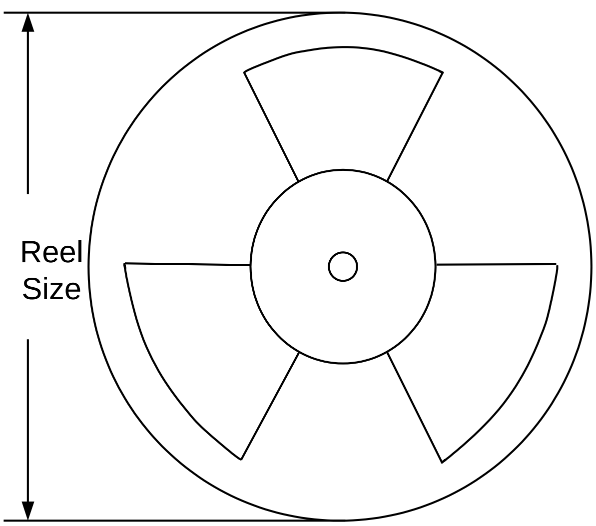
Taping & Reel Specification

1. TSSOP16E taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP16E	12	8	13"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
2024/9/30	0.0	Initial Release
2025/4/1	1.0	P3 Release

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