SY22645A

High Efficiency 60V, 2.0A, 500KHz Constant Current Step-down Regulator

General Description

SY22645A is a high efficiency, 12V-60V wide input voltage range DC/DC regulator targeting at LED applications. The device integrates the low $R_{DS(ON)}$ MOSFET and internal compensation. Along with the small SO8E package, the device achieves an extremely small solution size for LED driver design. SY22645A also supports PWM dimming and Analog dimming function.

Features

- Low $R_{DS(ON)}$ for internal switches :160mΩ
- Input range: 12V-60V
- 500kHz switching frequency
- PWM/Analog dimming available
- 2.0A LED current output
- Compact package: SO8E
- RoHS Compliant and Halogen Free
- ±2% 100mV reference

Ordering Information

SY22645□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY22645AFCC	SO8E	----

Applications

- PAR Lamp
- Tube Lamp
- Bulb

Typical Applications

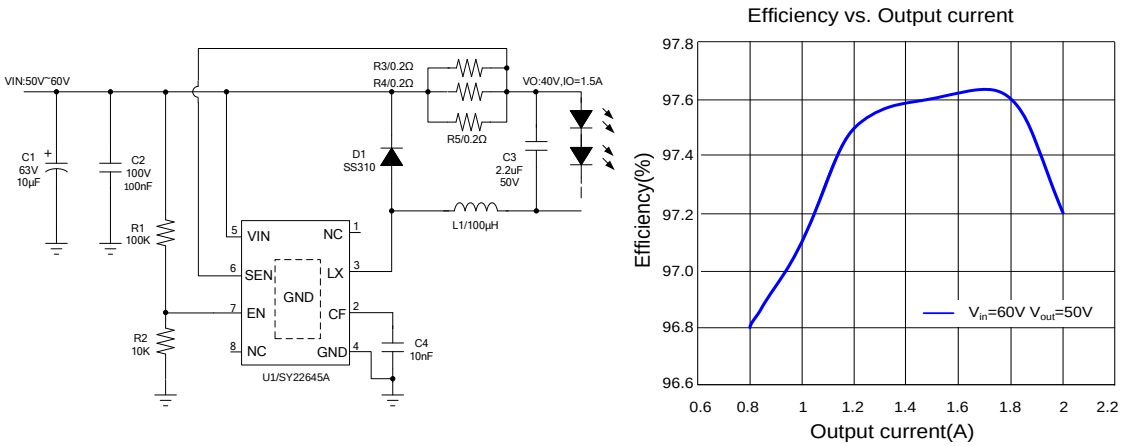
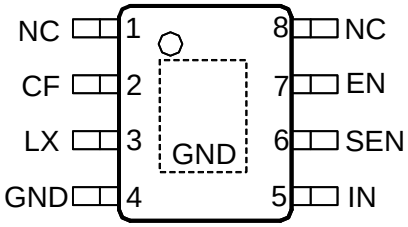


Figure 1. Schematic diagram

Pinout (top view)

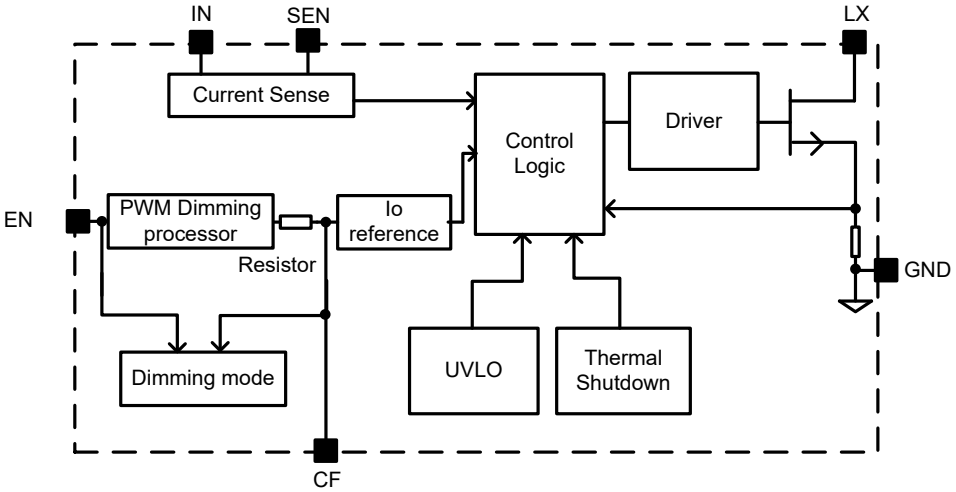


SO8E

Top Mark: BUC*xyz* (device code: BUC, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	SO8E	Pin Description
NC	1	No connection
CF	2	Dimming mode selection: VCF≥1.6V, PWM dimming mode. VCF≤1.4V, analog dimming mode.
LX	3	Inductor node. Connect an inductor from power input to LX pin.
GND	4	Ground pin
IN	5	Input pin. Decouple this pin to GND pin with 1μF ceramic cap. Also used as the positive current sense pin.
SEN	6	Negative Current Sense Pin.
EN	7	Analog dimming mode selection: VEN≥8.5V, add 0~1.0V signal to CF PIN, 0~1.0V analog dimming mode.(EN connect to VIN is doable) VEN≤6.5V, add PWM signal to EN, analog dimming with PWM signal input. At analog dimming mode, recommend to connect a 10nF capacitor between CF PIN and GND.
NC	8	No connection

Block Diagram



Absolute Maximum Ratings

LX, IN, EN, CF------ ---------- -0.3V to 63V
SEN ---------- -0.3V to V_{IN} ± 0.6V
Power Dissipation, PD @ TA = 25°C SO8E, ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

IN---------- 12V to 60V
SEN ---------- V_{IN} ± 0.4V
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} =24V, V_{OUT}=12V, I_{OUT}=100mA, TA = 25°C unless otherwise specified)

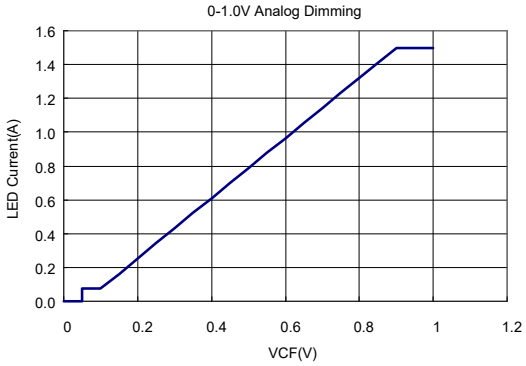
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		12		60	V
Shutdown Current	I_{SHDN}	EN=0		7.5		μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$		120	160	200	mΩ
Switching Frequency	F_{SW}		400	500	600	kHz
Internal Current Sense Reference	V_{IN-SEN}		98	100	102	mV
Min current sense reference	V_{IN-SEN_MIN}		4.0	5.0	6.0	mV
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.25	V
VIN turn-on threshold	V_{IN_ON}		9.0	10.0	11.0	V
VIN turn-off threshold	V_{IN_OFF}		8.5	9.5	10.5	V
Dimming section:						
Analog dimming range on CF	V_{CF}	At Minimum I_{LED}		100		mV
		At Maximum I_{LED}		900		mV
Thermal Shutdown Temperature	T_{SD}			155		°C
Thermal Hysteresis	Hyst			20		°C

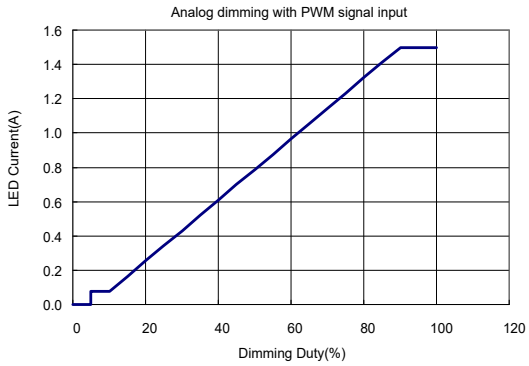
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

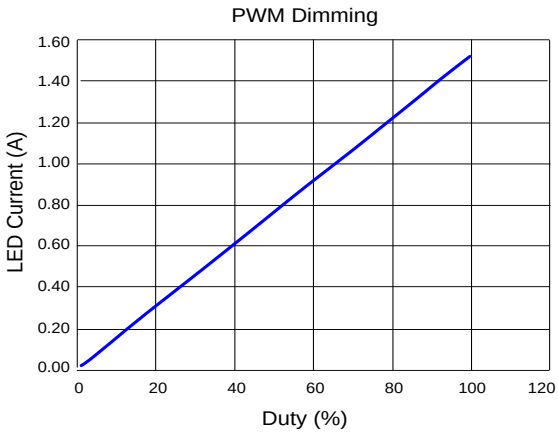
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

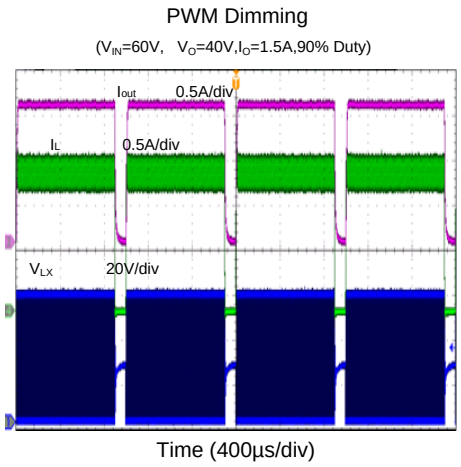
Note 3. The device is not guaranteed to function outside its operating conditions

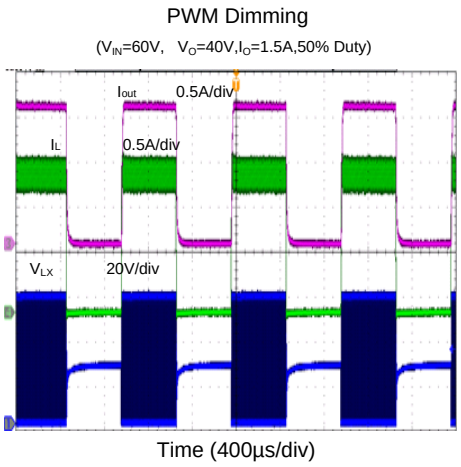
Typical Performance Characteristics





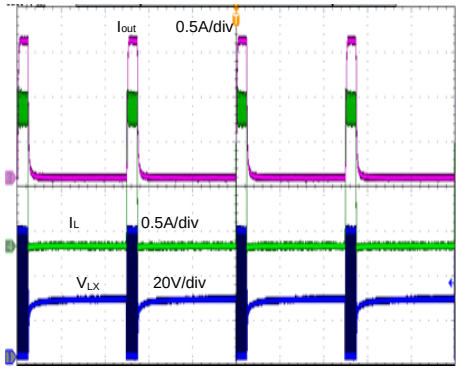






PWM Dimming

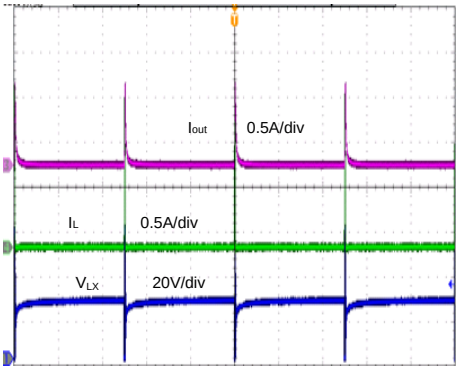
(V_{IN}=60V, V_O=40V,I_O=1.5A,10% Duty)



Time (400μs/div)

PWM Dimming

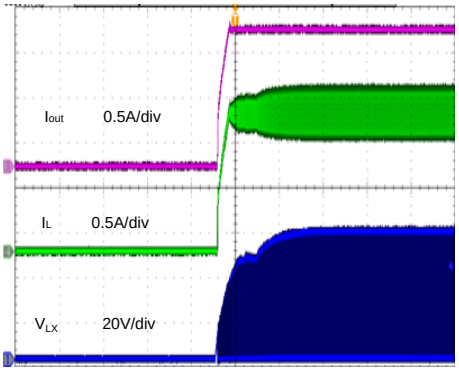
(V_{IN}=60V, V_O=40V,I_O=1.5A,1% Duty)



Time (400μs/div)

Startup

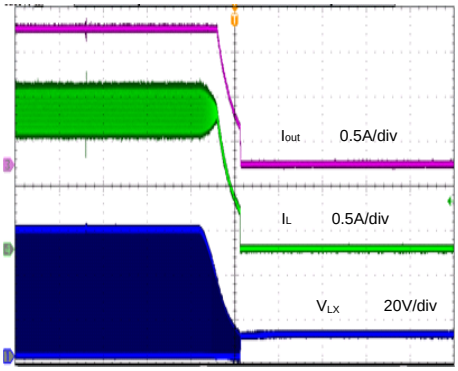
(V_{IN}=60V,V_O=50V,I_O=1.5A)



Time (20ms/div)

Shutdown

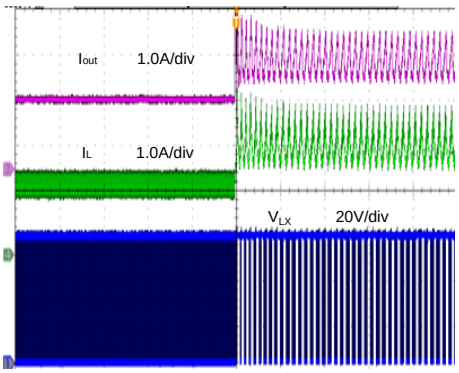
(V_{IN}=60V,V_O=50V,I_O=1.5A)



Time (20ms/div)

Short LED

(V_{IN}=60V,V_O=50V,I_O=1.5A)



Time (200μs/div)

Operation

SY22645A is a grounding switch buck regulator IC that integrates the PWM control, power MOSFET on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power MOSFET and proprietary PWM control, this regulator IC can achieve the high efficiency and Along with the small SO8E package, the device achieves an extremely small solution size for LED driver design. SY22645A also supports PWM/Analog dimming function.

Applications Information

Because of the high integration in the SY22645A IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and current sense resistor R_{SEN} need to be selected for the targeted applications specifications.

Current sense resistor R_{SEN}:

Choose R_{SEN} to program the proper output Current:

$$I_{LED}(A) = \frac{0.1(V)}{R_{SEN}(\Omega)}$$

Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

A typical X7R or better grade ceramic capacitor with suitable capacitance should be chosen to handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output current ripple noise requirements. For the best performance, it is recommended to use X7R or better grade ceramic capacitor greater than 1μF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the LED current.

The SY22645A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

Dimming Operation:

Dimming mode:

1: 0~1.0V analog dimming. Set $V_{EN} \geqslant 8.5V$, and add 0~1.0V dimming signal to CF PIN.

2: Analog dimming with PWM signal input. Recommend to connect a capacitor to CF PIN, and add PWM signal to EN ($V_{EN\_HIGH} \leqslant 6.5V$)

3: PWM dimming. Set VCF$\geqslant$1.6V, and add PWM signal to EN PIN.

PWM	CF	Dimming mode
--	$\geqslant$1.6V	PWM dimming
PWM$\geqslant$8.5V	$\leqslant$1.4V	0~1.0V analog dimming
PWM$\leqslant$6.5V	$\leqslant$1.4V	Analog dimming with PWM signal input

At PWM dimming mode, the minimum T_{PWM_ON} time is suggest setting bigger than 20μs.

Soft Start:

Add a ceramic capacitor C_{CF} on CF to achieve soft start, the soft start time can be adjusted by C_{CF}.

SCP:

If V_{VIN}-V_{SEN}>=0.2V, PWM is disabled, When V_{VIN}-V_{SEN} =0.15V, IC will recover work.

EN OFF:

IC shut down after EN OFF with 15ms.

Layout Design:

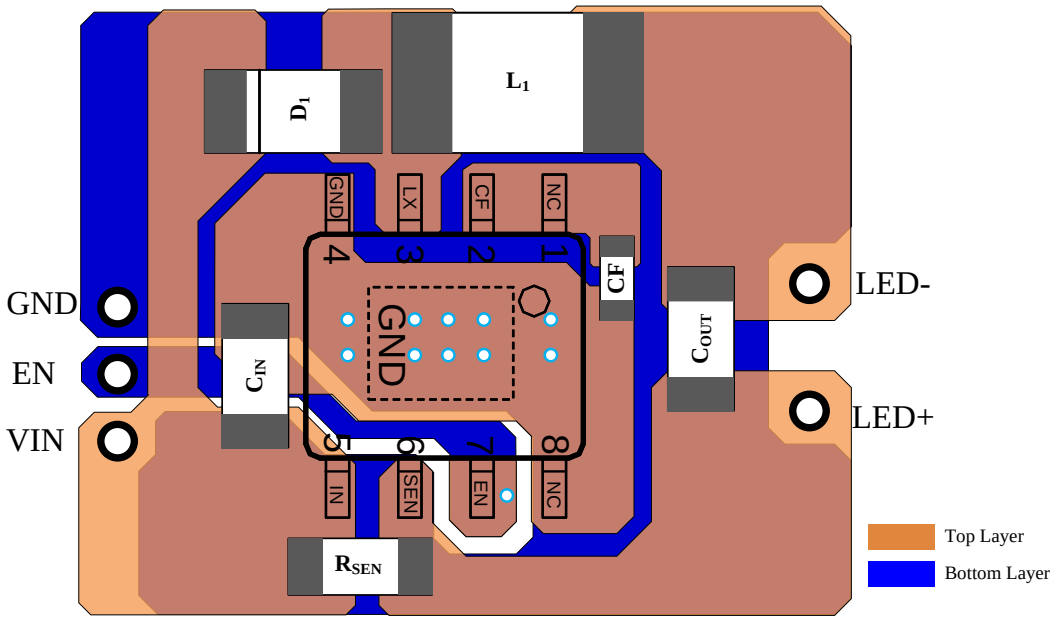
The layout design of SY22645A regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, C_{OUT}, CF and R_{SEN}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

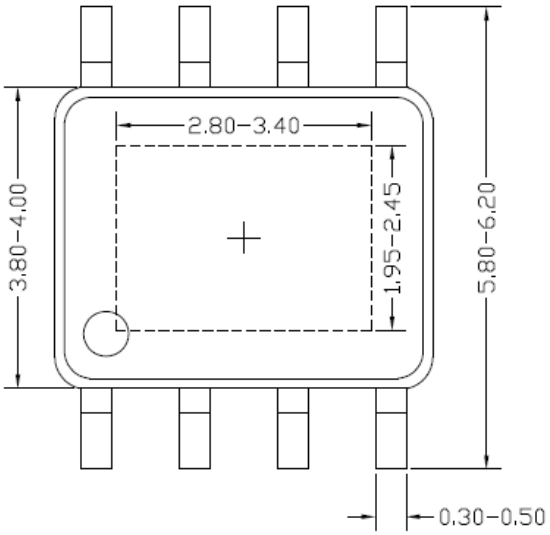
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

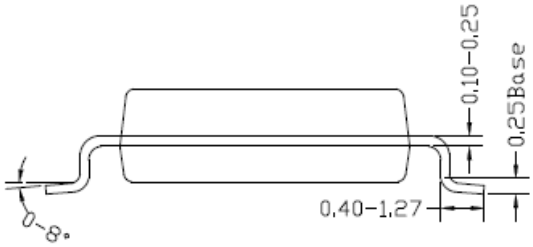
PCB Layout Suggestion



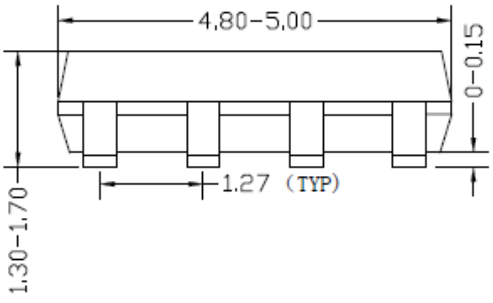
SO8E Package Outline & PCB layout



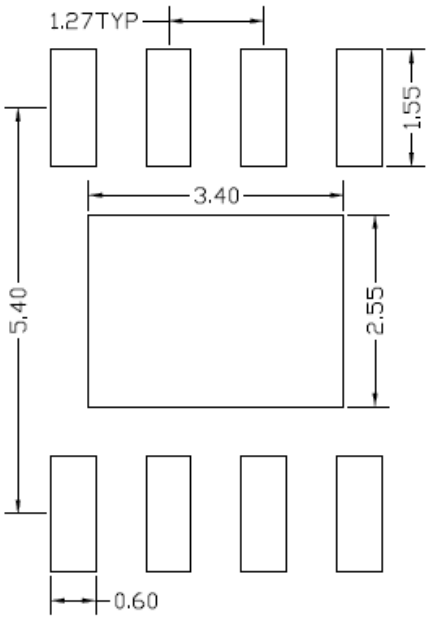
Top view



Side view



Front view



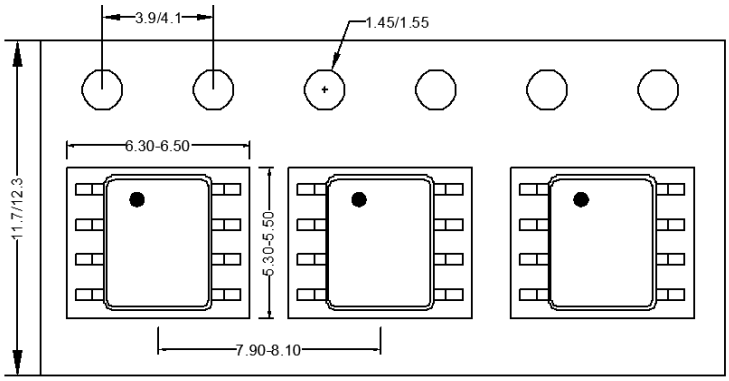
Recommended PCB Layout (Reference Only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

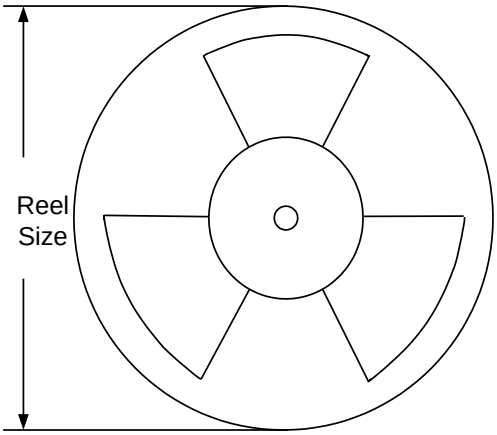
1. Taping orientation

SO8E



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
October 31,2019	Revision 0.9	Initial Risk Production Release
October 31,2020	Revision 1.0	Initial Production Release

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