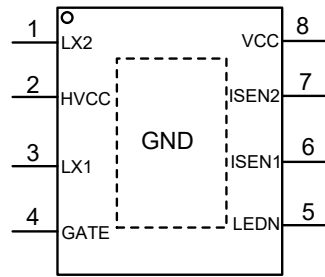


Pinout (top view)



(SO8E)

Part Number	Package type	Top Mark [Ⓞ]
SY22638A2FCP	SO8E	EDQxyz
SY22638B4FCP	SO8E	EDRxyz

Note ①: x=year code, y=week code, z=lot number code

Pin Name	Pin number	Pin Description
LX2	1	Drain of Bleeding MOS pin.
HVCC	2	HV power supply pin.
LX1	3	Drain of Main MOS pin.
GATE	4	Gate of integrated current ripple remover MOSFET.
LEDN	5	Connect to the Cathode of LED load.
ISEN1	6	Main MOS Current Sense Pin. The output current is decided by $I_{OUT} = \frac{V_{REF}}{R_{ISEN1} + R_{ISEN2}}$
ISEN2	7	BLD MOS Current Sense Pin. Latching current is adjusted by R _{ISEN2} . Recommended value: R _{ISEN2} > 0.75 ohm.
VCC	8	Power supply pin.
GND	9	Ground.

Block Diagram

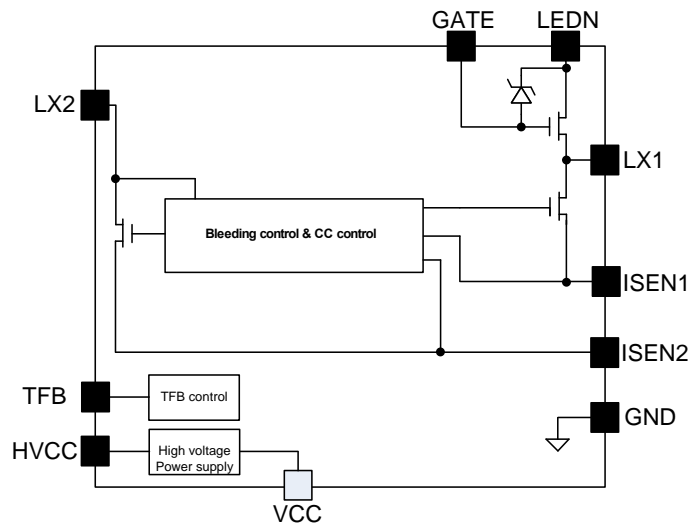


Figure.3 Block Diagram

Absolute Maximum Ratings (Note 1)

LX2, HVCC	-----	-0.3V~700V
LX1, GATE, LEDN	-----	-0.3V~500V
ISEN1, ISEN2	-----	-0.3V~3.6V
VCC	-----	-0.3~ 25V
LEDN to LX1	-----	-0.3~ 20V
GATE to LX1	-----	-0.3~ 3.6V
Power Dissipation, @ T _A = 25°C SO8E	-----	3.3W
Package Thermal Resistance (Note 2)		
SO8E, θ_{JA}	-----	30°C/W
SO8E, θ_{JC}	-----	10°C/W
Junction Temperature Range	-----	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C

Recommended Operating Conditions (Note 3)

Junction Temperature Range	-----	-40°C to 150°C
Ambient Temperature Range	-----	-40°C to 120°C

Electrical Characteristics

(V_{IN} = 15V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V _{VIN_ON}			12		V
VIN Turn-off Threshold	V _{VIN_OFF}			8.8		V
Quiescent Current	I _Q			350		μA
Error Amplifier Section						
Internal Reference Voltage	V _{REF}			0.3		V
MOS Section						
BV of LX1 MOS	V _{BV_LX1}		500			V
BV of LX2 MOS	V _{BV_LX2}		700			V
Inter Ripple Remover Section						
Zener Voltage between LEDN and GATE of SY22638A2	V _{Zener}			11.5		V
Zener Voltage between LEDN and GATE of SY22638B4	V _{Zener}			18		V
Thermal Section						
Thermal Foldback Temperature	T _{FB}			155		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

Operation

SY22638A2/B4 is a HV TRIAC Linear Controller. It recognizes ac mode, leading edge mode, trailing edge mode automatically in first sixteen ac cycles.

It's integrated a current ripple remover to eliminate low frequency current ripple

For improving the efficiency, the current of LX1 is compensated by VBUS. In the peak voltage of VBUS, the current of LX1 is the smallest, and then the loss is decreased.

In leading edge mode, SY22638A2/B4 controls the fire current automatically which is the Silergy exclusive patent.

For trailing edge dimmer, SY22638A2/B4 has a good performance by Reliable reset control.

TFB is available to be set for different application.

PF is higher than 0.7 suitable for European market.

Applications Information

AC Mode

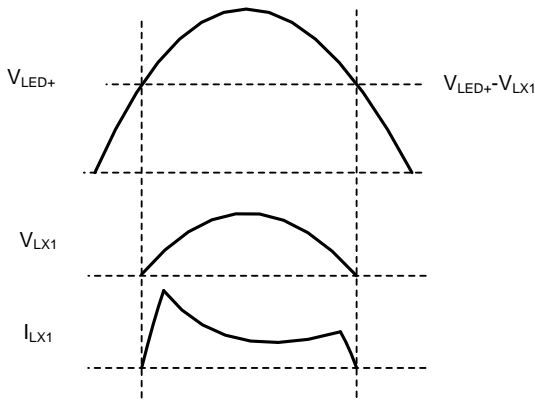


Fig.4 state in ac mode

In ac mode, the wave is showed above. The current of LX1 is compensated by VBUS for good efficiency performance.

In any kinds of mode, the output current is regulated by ISEN1 and ISEN2.

$$I_{OUT} = \frac{V_{REF}}{R_{ISEN1} + R_{ISEN2}}$$

Trailing edge mode

In trailing edge mode, SY22638A2/B4 tries to reset the dimmer when the current of LX1 MOS is off. As showed below.

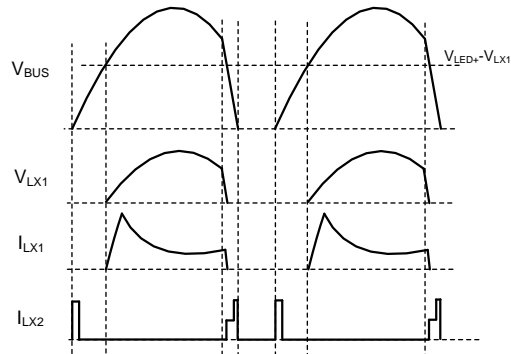


Fig.5 state in trailing edge mode

Trailing edge mode

In trailing edge mode, the fire current is decided by the resistor of ISEN2.

With smaller R_{ISEN2} , the latching current of LX2 is larger. For improving the efficiency, recommend to choose larger value of R_{ISEN2} , and satisfy appropriate compatibility.

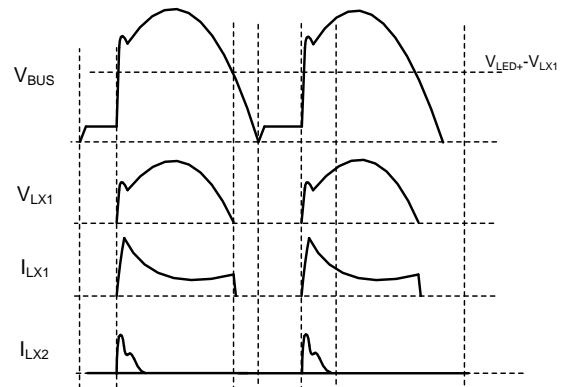


Fig.6 state in leading edge mode

The current of LX1 and LX2 flow through R_{ISEN2} simultaneously. So the actual fire current contains both two currents which help to decrease the fire loss. Recommend value: $R_{ISEN1} > 0.7 \text{ ohm}$.

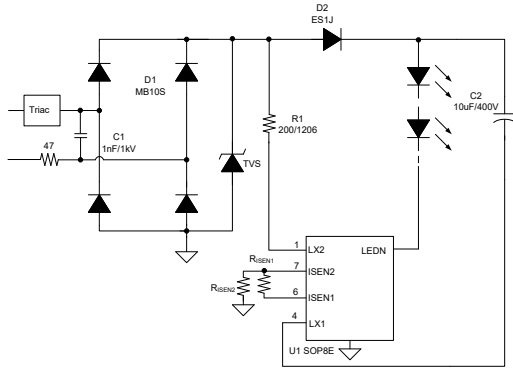


Fig.6 fire current sample resistor

CV logic

For further improve efficiency, SY22638A2/B4 integrate automatic CV regulation logic. So the loss caused by holding current is reduced.

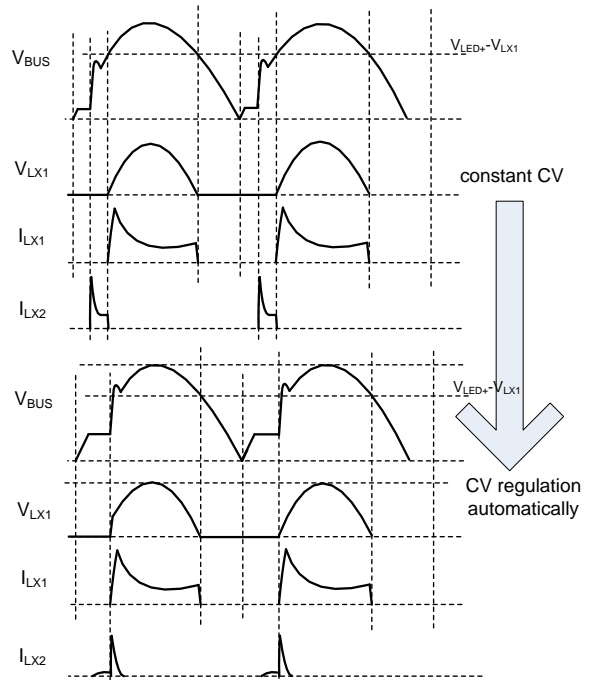


Fig.7 CV logic

Design Example

A design example of typical application is shown below step by step.

Example A

#1. Identify design specification

Target parameter			
I_{OUT}	22mA	T_{TFB}	150°

#1. Set R_{ISEN1} and R_{ISEN2}

Set $R_{ISEN2}=0.75\text{ ohm}$

$$R_{ISEN1} = \frac{V_{REF}}{I_{OUT}} - R_{ISEN2} = \frac{0.3}{0.022} - 0.75 \approx 13\text{ ohm}$$

#2 set TFB pin

$R_{TFB}=NC.$

#3 final result

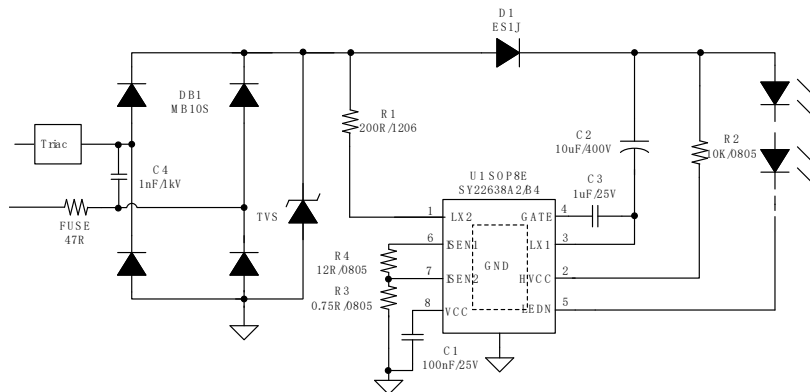
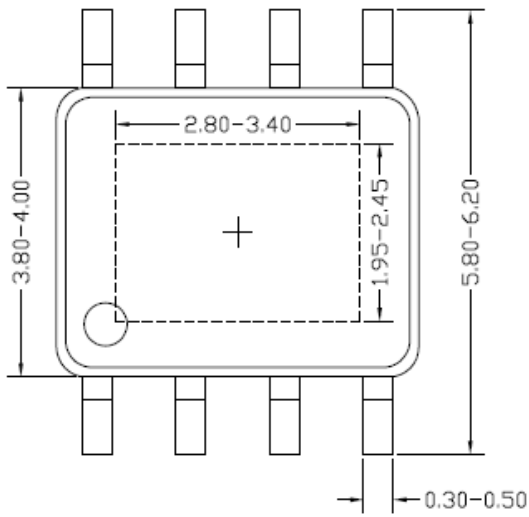
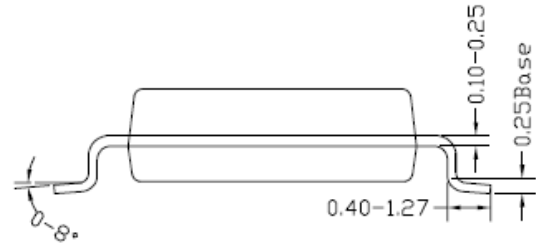


Fig.9 Final Design Result

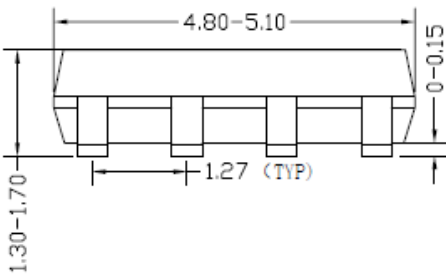
SO8E Package Outline & PCB layout



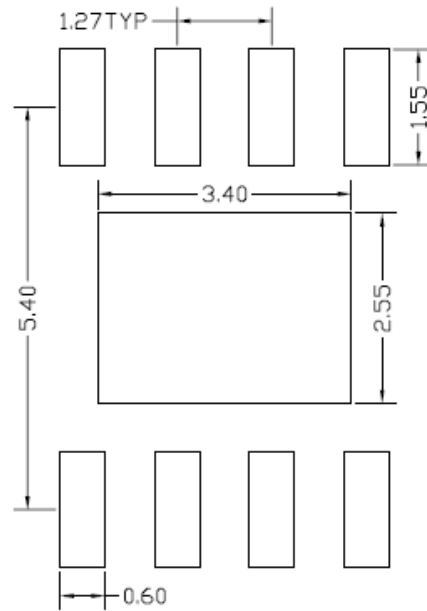
Top view



Side view



Front view



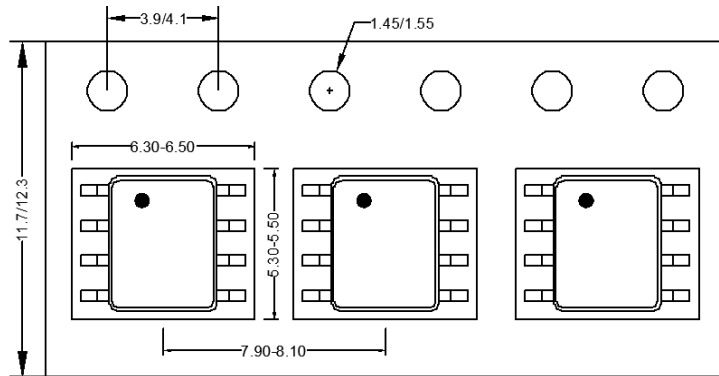
**Recommended PCB layout
(Reference Only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

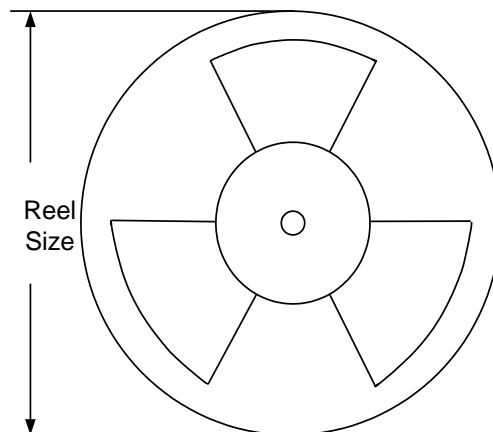
1. Taping orientation

SO8E



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
March 30, 2023	Revision 0.9	Initial Risk Production Release
March 30, 2024	Revision 1.0	Initial Production Release

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