SY5018C

Single Stage Flyback and PFC Controller with CV Control

General Description

The SY5018C is a single stage Flyback and PFC controller targeting at Constant Voltage (CV) applications. The primary side control is applied to reduce the feedback circuit cost. It drives the Flyback converter in the Quasi-Resonant mode for the high efficiency and achieves the high-power factor by a constant on-time control scheme. The adaptive PWM/PFM control is adopted for the highest average efficiency. It integrates the THD compensation to achieve the higher PF and lower THD.

Ordering Information

SY5018□(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5018CFAP	SO8	----

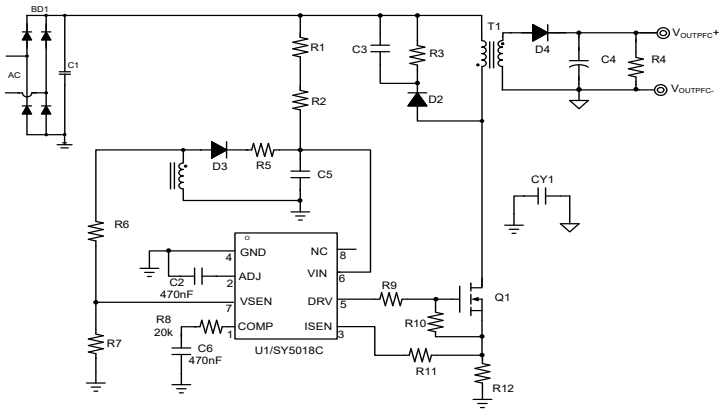
Features

- Primary Side CV Control Eliminates the Opto-coupler.
- Valley Turn-on of the Primary MOSFET to Achieve Low Switching Losses
- Integrate THD Compensation, PF>0.9, THD<20% during 40% Load to 100% Load
- Fast Load Regulation
- Internal High Current MOSFET Driver: 0.1A Sourcing and 0.5A Sinking
- Maximum Switching Frequency Limitation 100kHz
- Compact Package: SO8

Applications

- AC/DC Adapters
- Battery Chargers
- LED Lighting

Typical Applications



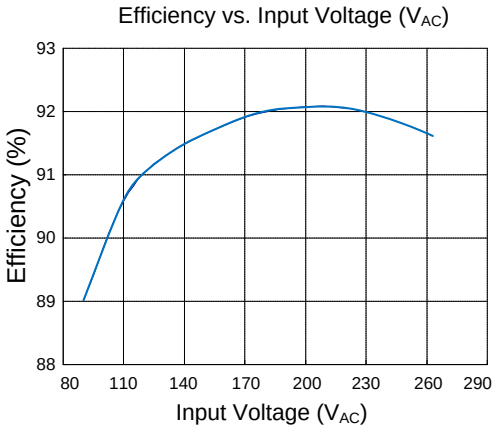
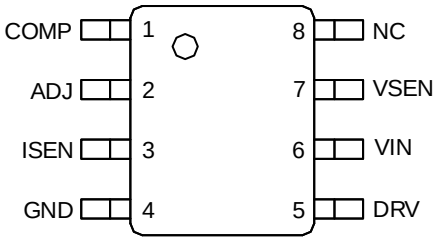


Figure 1. Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: FCR *xyz* (device code: FCR, ***x=year code, y=week code, z= lot number code***)

Pin	Name	Description
1	COMP	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
2	ADJ	Triangular wave compensation lope amplitude can be adjusted by parallel 330nF~560nF ceramic capacitor to GND.
3	ISEN	Current limit pin.
4	GND	Ground pin.
5	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET with a resistor.
6	VIN	Power supply pin.
7	VSEN	Output voltage and inductor current zero detection Pin. This pin receives the auxiliary winding voltage by a resistor divider.

Block Diagram

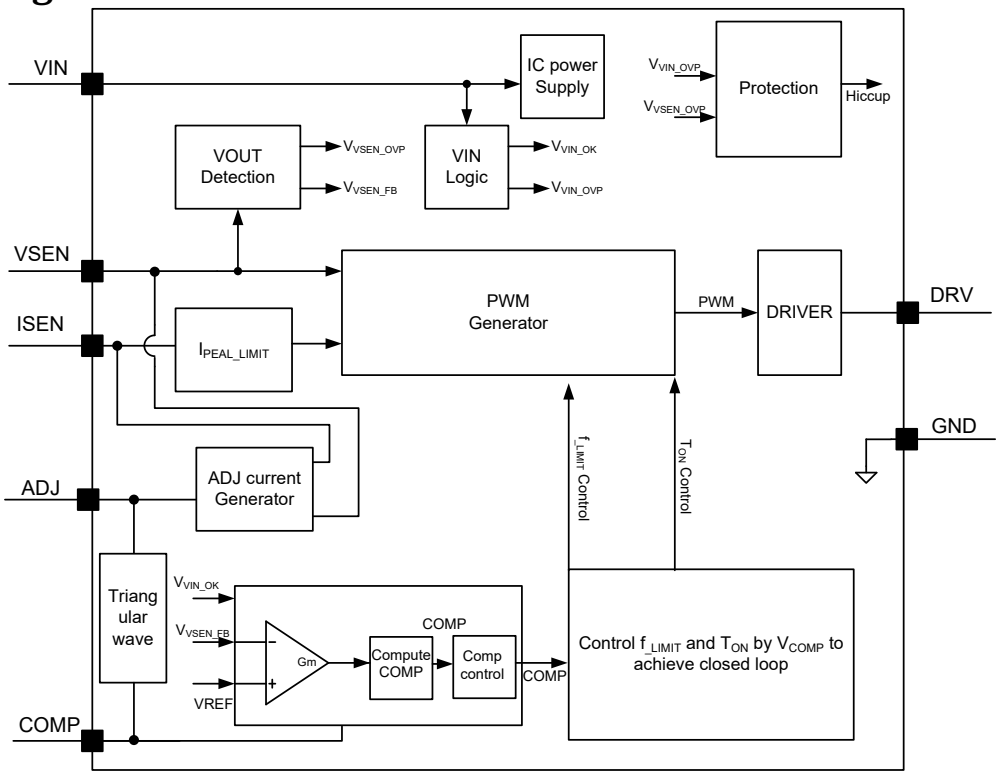


Fig.2 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN, DRV ---------- -0.3V to 27V
Supply Current I_{VIN} ---------- 20mA
VSEN ---------- -0.3V to 3.6V
ISEN, COMP, ADJ ---------- 3.6V
Power Dissipation, @ TA = 25°C SO8 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} ---------- 88°C/W
SO8, θ_{JC} ---------- 45°C/W
Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV ---------- 9V~22V
Absolute Maximum Range---------- -40°C to 150°C

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input Voltage Range	V_{VIN}		9		22	V
VIN Turn-on Threshold	V_{VIN_ON}		18.5	21.5	23.5	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.5	7.5	8.5	V
VIN OVP Voltage	V_{VIN_OVP}		22	24.5	27	V
Start-up Current	I_{ST}	$V_{VIN}<V_{VIN\_OFF}$	0.75	1.85	3	μA
Shunt Current in OVP Mode	I_{VIN_OVP}	$V_{VIN}>V_{VIN\_OVP}$		15		mA
Error Amplifier Section						
Current Limit Voltage	V_{ISEN_LIMIT}	1.0V>VSEN>0.2V	0.9	1.0	1.1	V
Protect Current Limit Voltage	V_{ISEN_OCP}		1.2	1.5	1.8	V
V_{FB} at Fast Start-up	V_{FB_LOW}		1.04	1.12	1.2	V
Internal Reference Voltage	V_{REF}		1.225	1.250	1.275	V
Threshold Value of Max V_{FB}	V_{FB_HIGH}		1.32	1.38	1.46	V
OVP Voltage Threshold	V_{FB_OVP}			V_{FB_HIGH}+0.1		V
Blanking Time for OFF Time	T_{OFF_MIN2}	V_{ISEN_HOLD}=0.40V	1.6	2.5	3.4	μs
Gate Driver Voltage	V_{Gate}			12		V
Typical Source Current	I_{SOURCE}			75		mA
Typical Sink Current	I_{SINK}			400		mA
Max ON Time	T_{ON_MAX}	Vcomp=2.5V	6.5	10	13.5	μs
Min ON Time	T_{ON_MIN}		0.3	0.45	0.6	μs

Maximum Switching Frequency	F_{MAX}		75	100	125	kHz
ADJ ON	V_{ISEN}		220	255	290	mV
ADJ OFF	V_{ISEN}		205	240	275	mV
ADJ Max Current	I_{ADJ}		17.5	20	22.5	uA
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			155		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

Operation

The SY5018C is a constant voltage Flyback controller with the primary side control and PFC function that targets at LED lighting applications.

The device provides the primary side control to eliminate the opto-couplers or the secondary feedback circuits, which would cut down the cost of the system. The high-power factor is achieved because of the integrated THD compensation.

The start-up process is optimized inside SY5018C, and the quick start-up (less than 500ms) is achieved without any additional circuit

In order to reduce the switching losses and improve the EMI performance, a Quasi-Resonant switching mode is applied, the power MOSFET is turned on at the voltage valley. The start-up current of SY5018C is rather small (5μA typically) to reduce the standby power loss further. The maximum switching frequency is clamped to 100kHz to reduce the switching losses and improve the EMI performance. The specific design is adopted to ensure a good load dynamic performance.

The adaptive PWM/PFM control is adopted for the highest average efficiency.

The SY5018C provides the reliable protections such as Short Circuit Protection (SCP), Over Temperature Protection (OTP), output open protection, transformer shorted protection and power diode shorted protection, etc.

The SY5018C is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by the BUS voltage through a start-up resistor R_{ST}. Once V_{VIN} rises to V_{VIN_ON}, the internal blocks will start to work and the PWM output will be enabled.

The output voltage is feedback by VSEN pin, which is taken as V_{FB}. If V_{FB} is lower than the certain threshold V_{FB_LOW}, the output voltage will not be built up, V_{COMP} is pulled up to high clamped; if V_{FB} is higher than V_{FB_LOW}+0.05V, V_{COMP} is charged by the internal gain modulator.

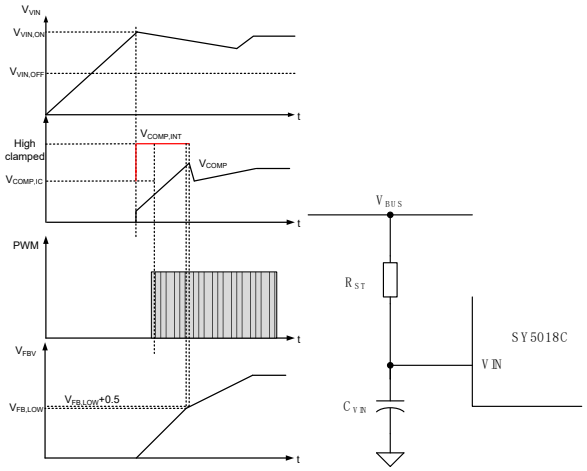


Fig3. Start up

This operation is aimed to build up the enough output voltage for auxiliary winding bias supply as quickly as possible. It is enabled only one time just when V_{VIN} is over V_{VIN_ON}.

V_{COMP} is pre-charged by the internal current source (Typ.12uA) to V_{COMP_IC} and hold at this level until fast start up process is finished.

The start-up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start-up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

(d) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

(e) When V_{FB}<0.2V, V_{ISEN} will be limited at 0.4V, when 1.1V≥V_{FB}≥0.2V, V_{ISEN} will be limited at 1.0V.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for the Flyback converter.

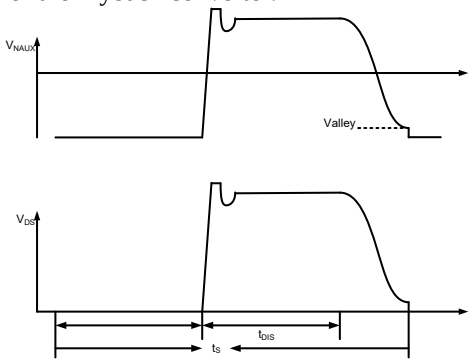


Fig.4 QR Mode Operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Output Voltage Control

In order to achieve the primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

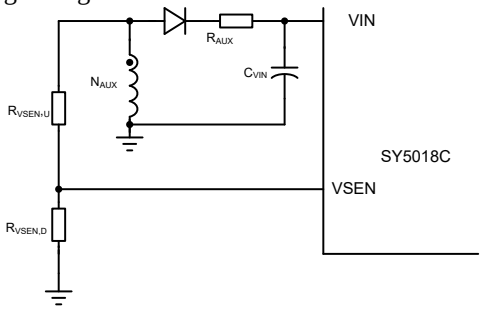


Fig.5 VSEN Pin Connection

As shown in Fig.6, during the off time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S}$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$V_{OUT} = \frac{V_{SEN\_REF}}{\frac{R_{VSEN\_D}}{R_{VSEN\_U} + R_{VSEN\_D}} \times \frac{N_{AUX}}{N_S}}$$

Where V_{VSEN_REF} is the internal voltage reference.

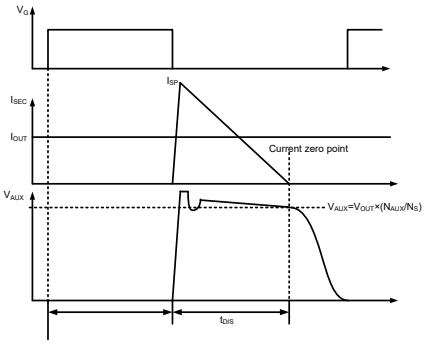


Fig.6 Auxiliary Winding Voltage Waveforms

THD Compensation

In order to eliminate CBB current, Triangular wave compensation is achieved by ADJ pin.

When Visen ≥260mV，C_{ADJ} begin to be charged，till Visen≤250mV, Vadj reset.

Triangular wave lope amplitude can be adjusted by the parallel 330nF~560nF ceramic capacitor to GND.

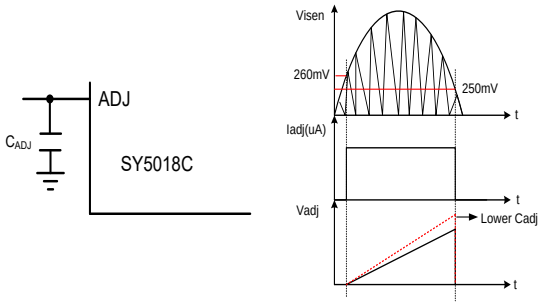
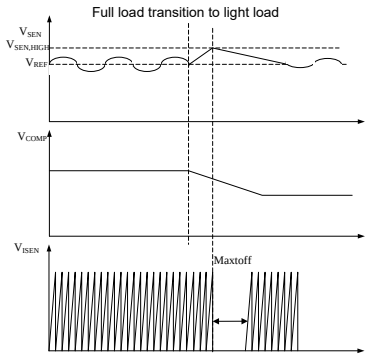


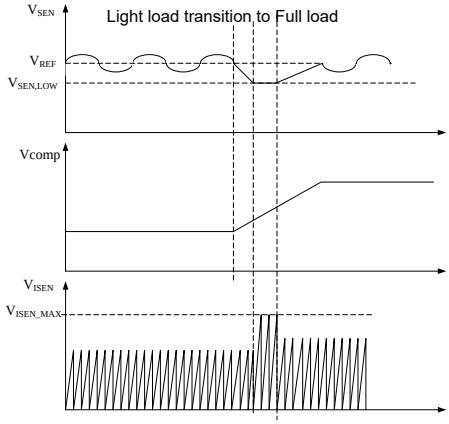
Fig.7 ADJ Compensation

Special Design For Transition

To have good transition performance, special design is integrated into the SY5018C.



When VSEN touch V_{FB_HIGH}, the IC work at Max t_{off} mode to decrease the output energy, and COMP is pulled down to decrease the energy output.



When VSEN touch V_{FB_LOW}, the IC work at Max I_{peak} to expedite the output energy, and COMP is charged to increase the energy output.

Design of R_{ISEN}

The maximum power inductor current ($I_{P\_PK\_MAX}$) occur in the minimum input voltage when full load. So R_{ISEN} could be selected by:

$$R_{ISEN} = \frac{90\% \times V_{ISEN\_LIMIT}}{I_{P\_PK\_MAX}}$$

Where $V_{ISEN,LIMIT}$ is a protection for transformer(If V_{ISEN} touch this voltage, the gate will turn off), and $I_{P\_PK\_MAX}$ is the maximum power inductor in steady.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so the valley signal cannot be detected by VSEN. Without valley detection, MOSFET cannot be turned on until the maximum off time $t_{OFF,MAX}$ is matched. If MOSFET is turned on by $t_{OFF,MAX}$ 64 times continuously, the IC will be shut down and enter into the hiccup mode.

Single fault design

If VSEN pin is shorted to GND pin or floating, the valley detection is failed, which is like SLP, the system will operate in hiccup mode.

If the transformer is shorted, V_{ISEN} will exceed V_{ISEN_EX}, which will trigger the IC hiccup operation. The protection above is also suitable for the secondary diode short.

Power Device Design

MOSFET and Diode

When the operation condition is with the maximum input voltage and full load, the voltage stress of MOSFET and the secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$

Where V_{AC_MAX} is the maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with THE minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX}$$
$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX}$$
$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$
$$I_{D\_AVG} = I_{OUT}$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are the maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t3 as shown

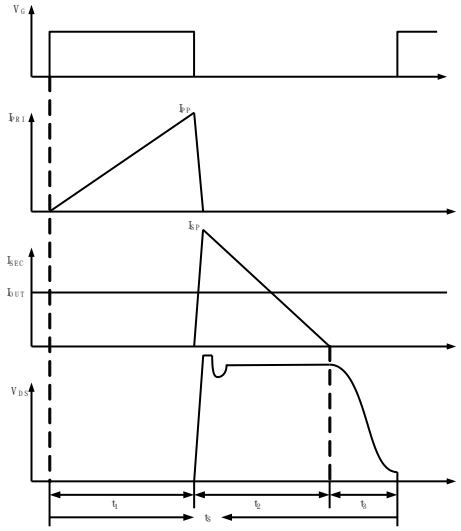


Fig.8 Switching Waveforms

The system operates in the constant on time mode to achieve the high-power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency fS-MIN happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency fS-MIN is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a)Select NPS

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

(b) Preset minimum frequency fS-MIN (Generally, fS_MIN is not suggested higher than 70kHz when the input voltage is whole range)

(c) Compute relative tS, t1 (t3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}}$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$

(d) Design inductance LM

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$

(e) Compute t3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$

Where CDrain is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current IP-PK-MAX and RMS current IP-RMS-MAX for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX}$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$

$$t_2' = t_S' - t_1' - t_3$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX}$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e}$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}}$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}}$$

Where V_{VIN} is the working voltage of VIN pin (10V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

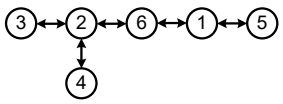
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}}$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground of signal trace
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of ‘Source pin – current sample resistor – GND pin’ should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

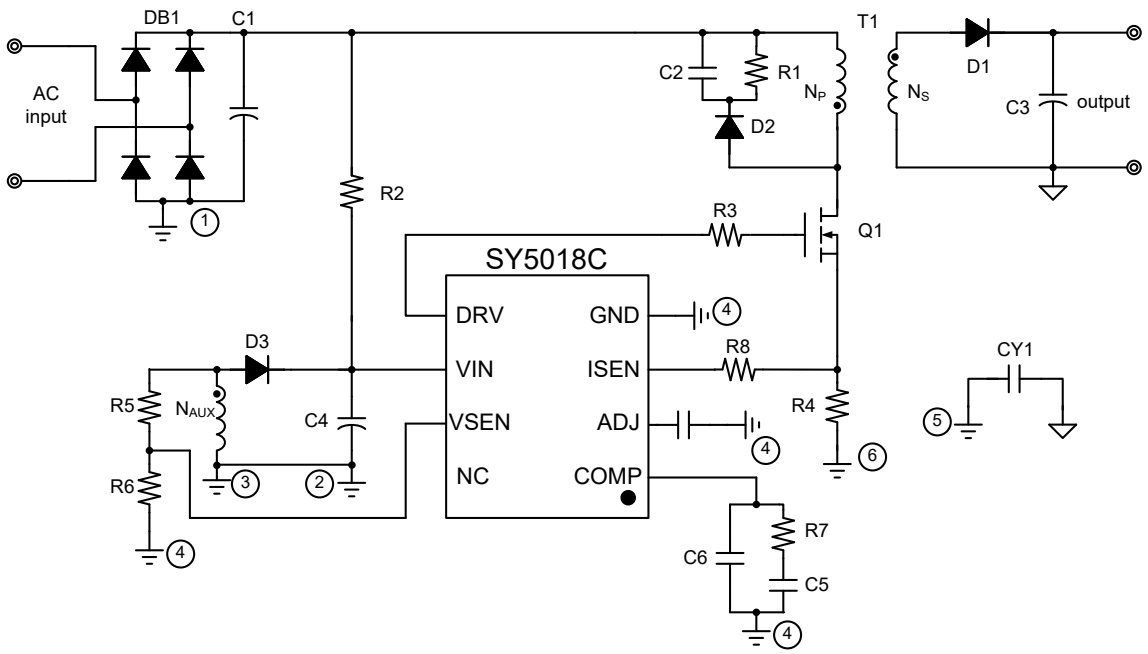
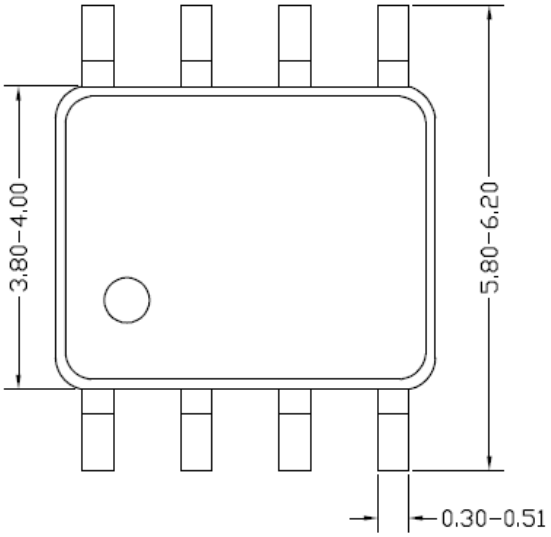
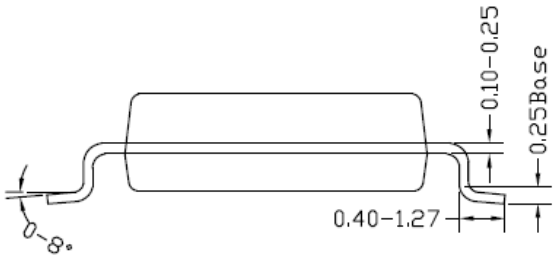


Fig.9. Recommended Connection of GND

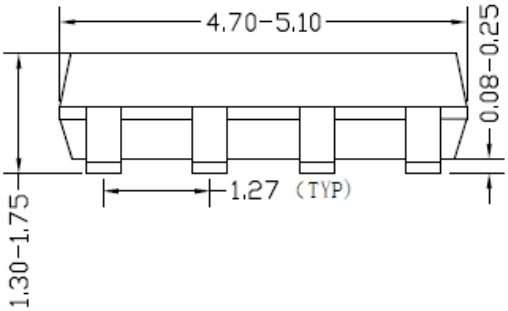
SO8 Package outline & PCB layout design



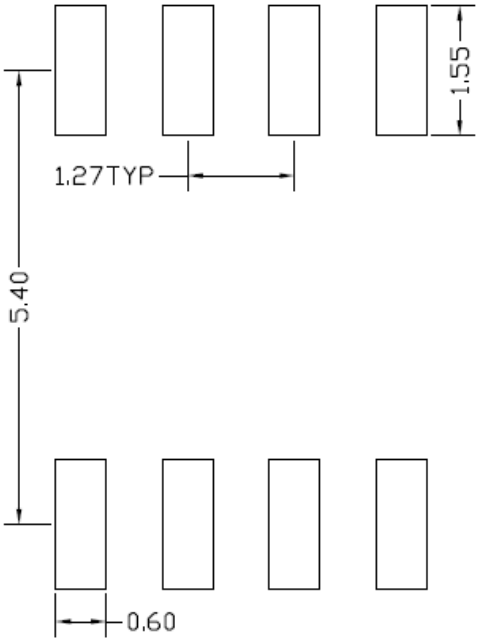
Top view



Side view



Front view

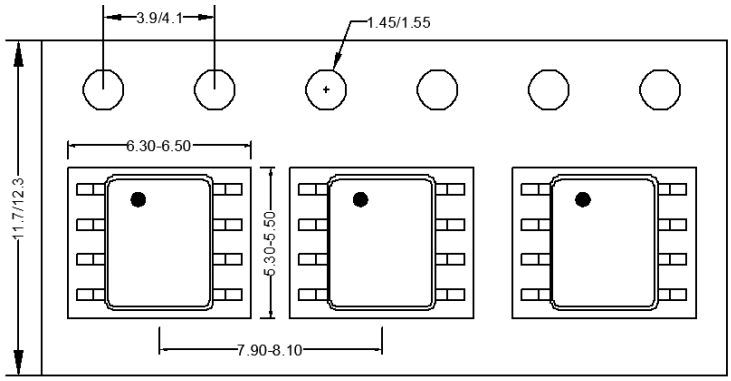


Recommended Pad Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

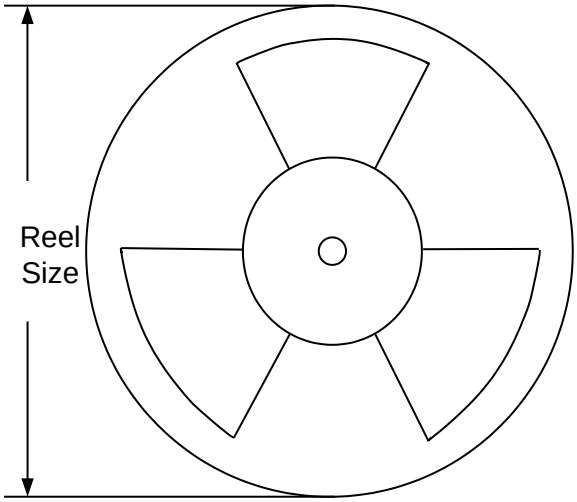
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 15, 2023	Revision 1.0	Initial Release

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