SY22650S

Single Stage Flyback and PFC Controller

General Description

SY22650S is a single stage Flyback and PFC controller targeting at LED driver applications. The output current accuracy is further improved by the secondary side feedback with opt-coupler. Furthermore, it applies CV control with primary side feedback.

It drives the Flyback converter in the Quasi-Resonant mode for high efficiency and achieves high power factor by constant on time control scheme. Adaptive PWM/PFM control is adopted for highest average efficiency.

Ordering Information

SY22650□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY22650SFAP	SO8	----

Features

- Secondary Side CC Control Improves Output Current Accuracy.
- Primary Side CV Control for Output Overvoltage Protection when Opt-coupler fails.
- Valley Turn-on of the Primary MOSFET to Achieve Low Switching Losses
- Internal High Current MOSFET Driver: 75mA Sourcing and 400mA Sinking
- Power Factor >0.90 with Single-stage Conversion
- Maximum Switching Frequency Limitation 100kHz
- Compact Package: SO8

Applications

- LED Lighting

Typical Applications

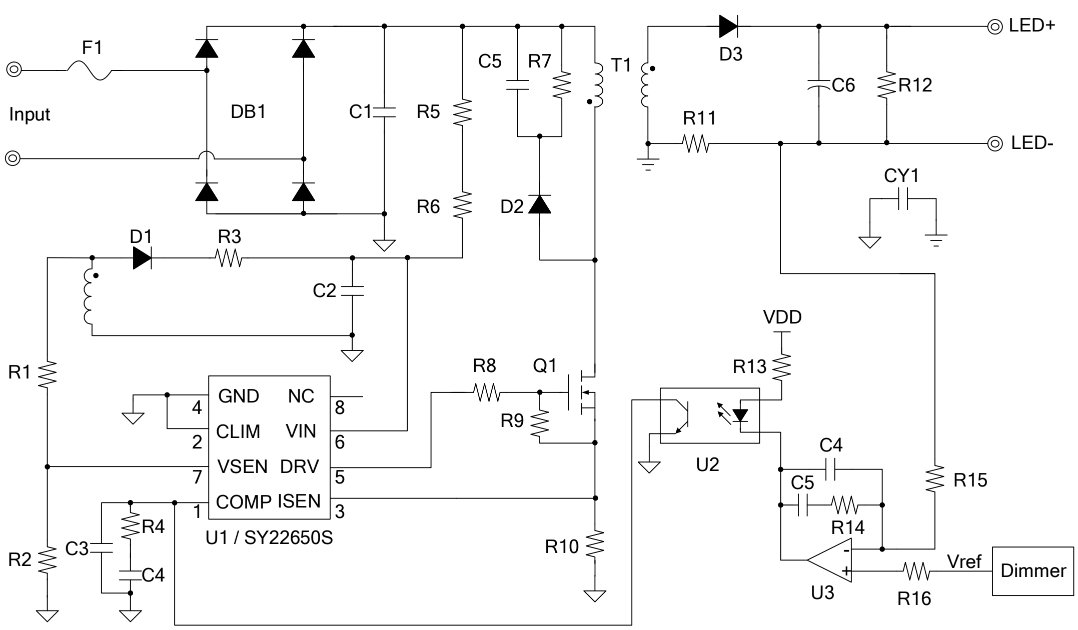
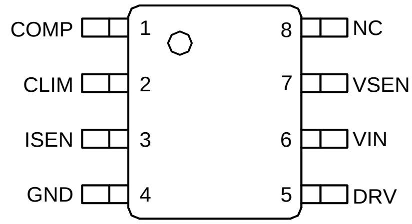


Figure 1. Schematic Diagram

Pinout (top view)



(Top View)

(SO8)

Top Mark: EBE *xyz* (device code: EBE, ***x=year code, y=week code, z= lot number code***)

Pin	Name	Description
1	COMP	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
2	CLIM	Add 220nF ceramic capacitor to GND, output current will be limited to about 1.2 times the rated current. If do not need this function, connect CLIM PIN to GND.
3	ISEN	Current limit PIN.
4	GND	Ground pin.
5	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET with a resistor.
6	VIN	Power supply pin.
7	VSEN	Output voltage and inductor current zero detection PIN. This pin receives the auxiliary winding voltage by a resistor divider.

Block Diagram

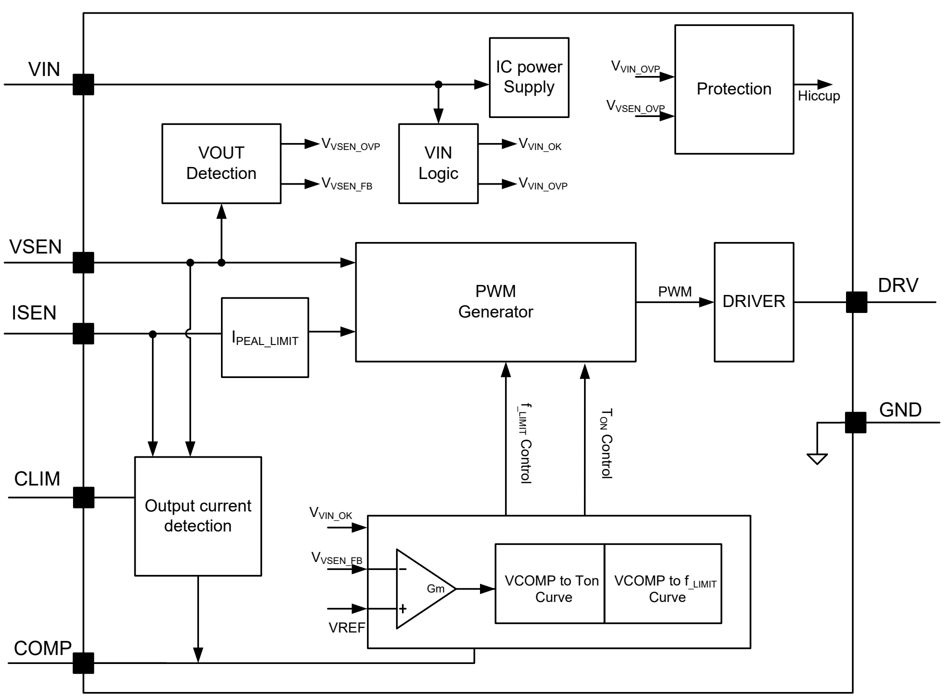


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

VIN, DRV -- -0.3V to 36V
Supply current I_{VIN} -- 20mA
VSEN --- -0.3V to V_{IN}+0.3V
ISEN, COMP, CLIM--- 3.6V
Power Dissipation, @ T_A = 25°C SO8 -- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA}--- 88°C/W
SO8, θ_{JC} -- 45°C/W
Temperature Range --- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

VIN, DRV --- 9V~22V
Absolute maximum range--- -40°C to 150°C

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input Voltage Range	V_{VIN}		9		22	V
VIN Turn-on Threshold	V_{VIN_ON}			21.5		V
VIN Turn-off Threshold	V_{VIN_OFF}			7.5		V
VIN OVP Voltage	V_{VIN_OVP}			24.0		V
Start up Current	I_{ST}	V_{VIN}<V_{VIN_OFF}		2.0		µA
Quiescent Current	I_Q			0.5		mA
Discharge Current in Protection Mode	I_{VIN_P}	V_{VIN}>V_{VIN_OVP}		5.0		mA
Error Amplifier Section						
Current Limit Voltage	V_{ISEN_LIMIT}	V_{VSEN}<0.2V		0.4		V
		V_{VSEN}>0.2V		1.0		V
Protect Current Limit Voltage	V_{ISEN_EX}			1.5		V
V_{FB} at Fast Start up	V_{FB_LOW}			0.2		V
Internal Reference Voltage	V_{REF}		1.225	1.250	1.275	V
Threshold Value of Max V_{FB}	V_{FB_HIGH}			1.40		V
OVP Voltage Threshold	V_{FB_OVP}			1.50		V
Blanking Time for OFF Time	T_{OFF_MIN1}	V_{ISEN_HOLD}=0.15V		1.7		µs
	T_{OFF_MIN2}	V_{ISEN_HOLD}=0.40V		2.6		µs
Gate Driver Voltage	V_{Gate}			12		V
Typical Source Current	I_{SOURCE}			75		mA
Typical Sink Current	I_{SINK}			400		mA
Max ON Time	T_{ON_MAX}	Vcomp=2.5V		10		µs
Min ON Time	T_{ON_MIN}			0.5		µs
Maximum Switching Frequency	F_{MAX}			100		kHz
Output Current Limit	V_{CLM}			0.33		V
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			155		℃

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

SY22650S is a single Flyback controller with PFC function that targets at LED lighting applications.

The output current accuracy is further improved by the secondary side feedback with opto-coupler. Furthermore, SY22650S provides primary side detection of output voltage.

High power factor is achieved by constant on operation mode, with which the control scheme and the circuit structure are both simple.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley;

The start up current of SY22650S is rather small (2μA typically) to reduce the standby power loss further.

The maximum switching frequency is clamped to 100kHz to reduce switching losses and improve EMI performance; Specific design is adopted to ensure good performance when transition.

Adaptive PWM/PFM control is adopted for highest average efficiency.

SY22650S provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), transformer shorted protection and power diode shorted protection, etc.

SY22650S is available with SO8 package.

Applications Information

Start Up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises to V_{VIN_ON}, the internal blocks start to work and PWM output is enabled.

The whole start up procedure is divided into two sections shown in Fig.3. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage build-up section. The start-up time t_{ST} is composed of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

t_{STO} is fast start-up stage, which will help to create output voltage quickly. After t_{STO}, IC works in constant on time mode.

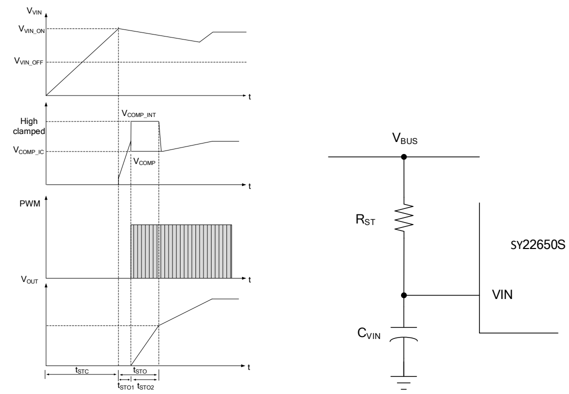


Fig.3 Start up

In t_{STO1}, V_{COMP} is pre-charged by internal current source to V_{COMP_IC} (800mV typically) and hold at this level until fast start up process is finished.

In t_{STO2}, V_{VSEN} is lower than certain threshold $V_{FB,LOW}$, which means the output voltage is not built up. During this time, peak current mode is adopted to reduce start up time shown in Fig.3.

The startup resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than 1mA.

$$\frac{V_{BUS}}{1mA} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Shut Down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

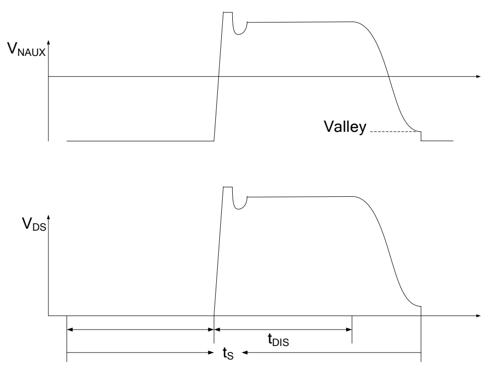


Fig4. QR mode operation

The voltage across drains and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drains and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Secondary Side Feedback Control

The turn on time of the MOSFET is a function of V_{COMP}, and the turn off time of the MOSFET is up to the valley detection of VSEN pin, so the output power can be controlled by V_{COMP}.

SY22650S is compatible with opto-coupler to support output current control or output voltage control, which is shown by Fig.5 and Fig.6.

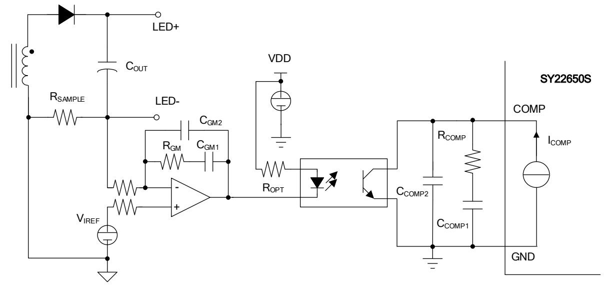


Fig.5 Output Current Control

In the constant current output control of secondary side feedback, the output current can be represented by

$$I_{OUT} = \frac{V_{IREF}}{R_{SAMPLE}} \tag{3}$$

Where V_{IREF} is the external reference, R_{SAMPLE} is the output current sense resistor.

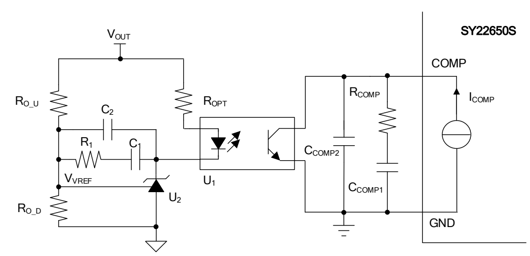


Fig.6 Output Voltage Control

In the constant voltage output control of secondary side feedback, the output voltage can be represented by

$$V_{OUT} = V_{VREF} \times \frac{R_{O\_U} + R_{O\_D}}{R_{O\_D}} \tag{4}$$

Where V_{VREF} is the external reference, R_{O_U} and R_{O_D} compose the resistor divider.

Here are several COMP controls circuits below.

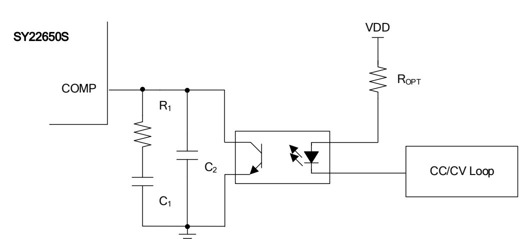


Fig.7 COMP Control Circuit 1

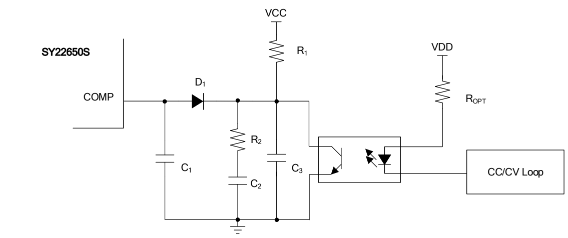


Fig.8 COMP Control Circuit 2

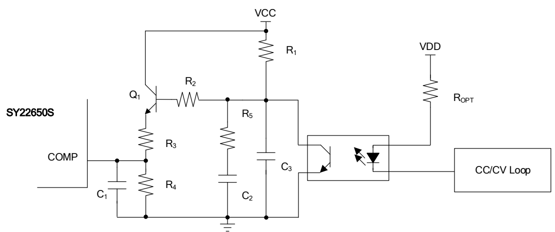


Fig.9 COMP Control Circuit 3

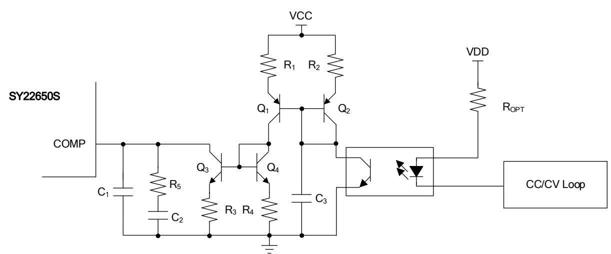


Fig.10 COMP Control Circuit 4

In order to match the order of magnitude of the output current of the opto-coupler, Circuits 2~4 are recommended.

Design of R_{ISEN} and Output Current Limit

The maximum power inductor current ($I_{P\_PK\_MAX}$) occur in minimum input voltage when full load. Generally R_{ISEN} could be selected by

$$R_{ISEN} = \frac{90\% \times V_{ISEN,LIMIT}}{I_{P\_PK\_MAX}} \quad (5)$$

Where V_{ISEN_LIMIT} is a protection for transformer (If V_{ISEN} touch this voltage, power MOSFET will turn off), and $I_{P\_PK\_MAX}$ is the maximum power inductor current in steady.

The output current could be monitored by SY22650S with primary side detection.

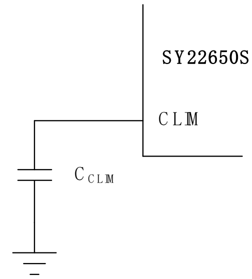


Fig.11 CLIM Pin Connection

If the output current limit function is adopted, a capacitor (220nF~1uF is recommended) should be added between the CLIM pin and GND. At this time, the output current can be limited to about 1.2 times the rated current. If this function is not required, connect the CLIM pin to GND.

Over Voltage Protection (OVP) & Open LED Protection (OLP)

SY22650S provides primary side detection of output voltage.

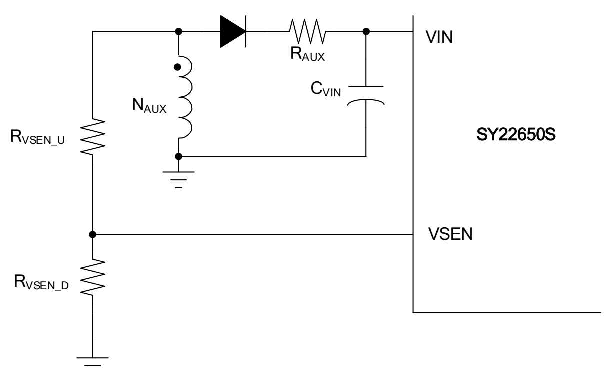


Fig.12 VSEN Pin Connection

When SY22650S is used for constant current output control of secondary side feedback, the OVP function is mainly guaranteed by SY22650S.

The output voltage is reflected by the auxiliary winding voltage of the Flyback transformer, and VSEN pin provides over voltage protection function. When the large transient happens, resulting in V_{VSEN} exceeds V_{FB_HIGH}, the over voltage protection is triggered. SY22650S will stop switching and discharge the V_{VIN} voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$V_{OUT\_OVP} = \frac{V_{FB\_HIGH}}{\frac{R_{VSEN\_D}}{R_{VSEN\_U} + R_{VSEN\_D}} \times \frac{N_{AUX}}{N_S}} \quad (6)$$

Where V_{OUT_OVP} is the output over voltage specification; V_{FB_HIGH} is the internal voltage reference; R_{VSEN_U} and R_{VSEN_D} compose the resistor divider. N_S and N_{AUX} are the turns of secondary winding and auxiliary winding separately.

When SY22650S is used for constant voltage output control of secondary side feedback, the OVP function is mainly guaranteed by external CV loop.

Short Circuit Protection (SCP)

When the output is shorted to ground, the following conditions may occur.

(1) The output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN pin. Without valley detection, MOSFET cannot be turned ON until maximum off time t_{OFF_MAX} is matched. If MOSFET is turned ON by t_{OFF_MAX} 64 times continuously, IC will be shut down and enter into hiccup mode.

(2) The output current is still determined by the external CC loop, but the output voltage is clamped to zero, which indirectly leads to insufficient power supply of SY22650S. SY22650S keep restarting.

Single Fault Design

If VSEN pin is shorted to GND pin or floating, valley detection is failed, which is similar to SCP, the system will operate in hiccup mode.

If the transformer is shorted, V_{ISEN} will exceeds V_{ISEN_EX}, which will trigger IC hiccup operation. The protection above is also suitable for secondary diode short.

If the opto-coupler fails, the OVP or output current limit function is triggered to protect the system from over power.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (7)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (8)$$

Where V_{AC_MAX} is maximum input AC RMS voltage; N_{PS} is the turn's ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (9)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (10)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (11)$$

$$I_{D\_AVG} = I_{OUT} \quad (12)$$

Where $I_{P\_PK\_MAX}$ and $I_{P\_RMS\_MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (13)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.13.

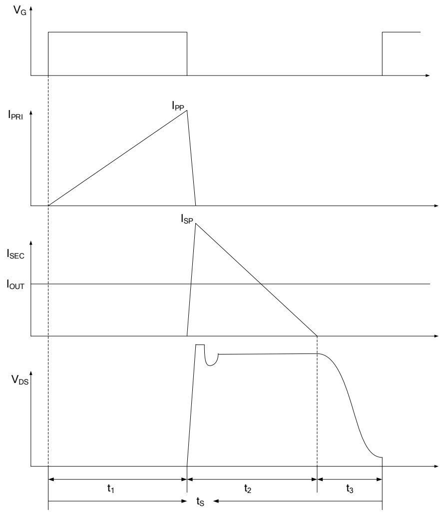


Fig.13 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency f_{S_MIN} happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (14)$$

(b) Preset minimum frequency f_{S_MIN} (Generally, f_{S_MIN} is not suggested higher than 70kHz when the input voltage is whole range)

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}} \quad (15)$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (16)$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \quad (17)$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} \quad (18)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\_PK\_MAX}$ and RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

(19)

Where η is the efficiency; P_{OUT} is rated full load power.

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3.

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}} \quad (20)$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \quad (21)$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} \quad (22)$$

(g) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (23)$$

$$t_2' = t_S' - t_1' - t_3 \quad (24)$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} \quad (25)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area, A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times \frac{V_{ISEN\_LIMIT}}{R_{ISEN}}}{\Delta B \times A_e} \quad (26)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (27)$$

(e) compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (28)$$

Where V_{VIN} is the working voltage of VIN pin (10V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from $4A/mm^2$ to $10A/mm^2$.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

$$C_{OUT} = \frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2 - 1}}{4\pi f_{AC} R_{LED}} \quad (29)$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first.

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (30)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; V_{D_F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (31)$$

The C_{RCD} is related with the voltage ripple of the snubber ΔV_{C_RCD}:

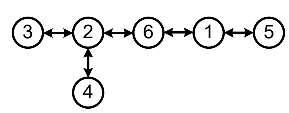
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (32)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor

Ground ②: ground of bias supply capacitor and GND pin
Ground ③: ground node of auxiliary winding
Ground ④: ground of signal trace except GND pin
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of 'Source pin – current sample resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

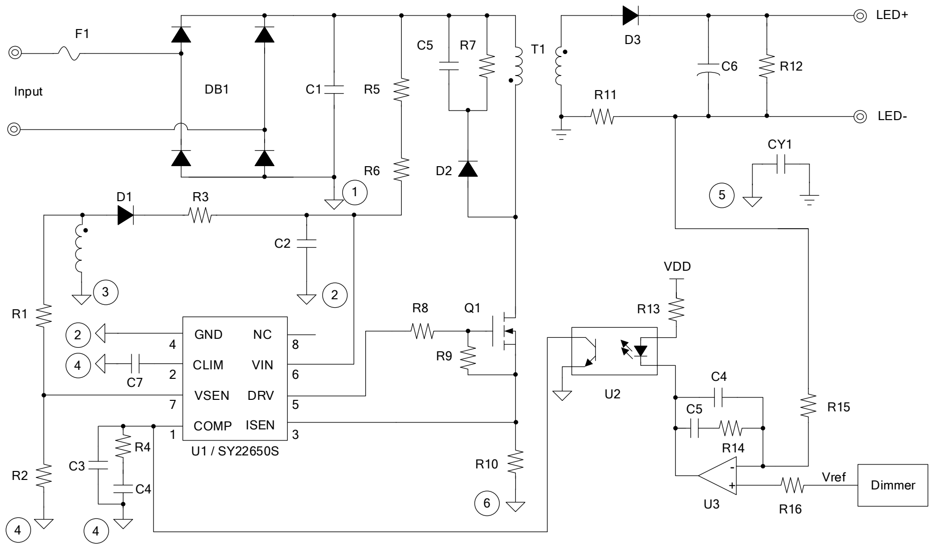


Fig.14 Recommended Connection of GND

Design Example

A design example of typical constant current output application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	120V~277V	V_{OUT}	40V
I_{OUT}	1A	η	88%
V_{OUT_OVP}	48V		

#2. Transformer design (N_{PS}, L_M)

Refer to **Power Device Design**

Conditions			
V_{AC_MIN}	120V	V_{AC_MAX}	277V
ΔV_S	50V	$V_{MOS\_(BR)DS}$	600V
P_{OUT}	40W	$V_{D,F}$	1.05V
C_{Drain}	100pF	f_{S_MIN}	40kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$
$$= \frac{600V \times 0.9 - \sqrt{2} \times 277V - 50V}{40V + 1.05V}$$
$$\approx 2.4$$

N_{PS} is set to

$$N_{PS} = 2.0$$

(b) f_{S_MIN} is preset

$$f_{S,MIN} = 40kHz$$

(c) Compute the switching period t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S\_MIN}} = 25\mu s$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2} V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$
$$= \frac{25\mu s \times 2.0 \times (40V + 1.05V)}{\sqrt{2} \times 120V + 2.0 \times (40V + 1.05V)}$$
$$\approx 8.15\mu s$$

(d) Compute the inductance L_M

$$\begin{aligned} L_M &= \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \\ &= \frac{120V^2 \times 8.15\mu s^2 \times 0.88}{2 \times 40W \times 25.0\mu s} \\ &\approx 421\mu H \end{aligned}$$

Set

$$L_M = 400\mu H$$

(e) Compute the quasi-resonant time t_3

$$\begin{aligned} t_3 &= \pi \times \sqrt{L_M \times C_{Drain}} \\ &= \pi \times \sqrt{400\mu H \times 100pF} \\ &\approx 628ns \end{aligned}$$

(f) Compute primary maximum peak current $I_{P\_PK\_MAX}$

$$\begin{aligned} I_{P\_PK\_MAX} &= \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta} \\ &\approx 3.37A \end{aligned}$$

Adjust switching period t_S and ON time t_1 to t'_S and t'_1.

$$\begin{aligned} t'_S &= \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}} \\ &= \frac{0.88 \times 400\mu H \times 3.37A^2}{4 \times 40W} \\ &\approx 24.985\mu s \end{aligned}$$

$$\begin{aligned} t'_1 &= \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \\ &= \frac{400\mu H \times 3.37A}{\sqrt{2} \times 120V} \\ &\approx 7.94\mu s \end{aligned}$$

Compute primary maximum RMS current $I_{P\_RMS\_MAX}$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t'_1}{6t'_S}} \times I_{P\_PK\_MAX} = \sqrt{\frac{7.94\mu s}{6 \times 24.985\mu s}} \times 3.37A = 0.78A$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2 \times 3.37A = 6.74A$$

$t_2' = t_S' - t_1' - t_3 = 24.985\mu s - 7.94\mu s - 0.628\mu s \approx 16.42\mu s$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} = \sqrt{\frac{16.42\mu s}{6 \times 24.985\mu s}} \times 6.74A \approx 2.23A$$

#3. Select power MOSFET and secondary power diode

Refer to **Power Device Design**

Known conditions at this step			
V_{AC_MAX}	277V	N_{PS}	2.0
V_{OUT}	40V	V_{D_F}	1.05V
ΔV_S	50V	η	88%

(a) Compute the voltage and the current stress of MOSFET:

$$\begin{aligned} V_{MOS\_DS\_MAX} &= \sqrt{2} V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \\ &= \sqrt{2} \times 277V + 2.0 \times (40V + 1.05V) + 50V \\ &\approx 524V \end{aligned}$$

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} = 3.37A$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.78A$$

(b) Compute the voltage and the current stress of secondary power diode

$$\begin{aligned} V_{D\_R\_MAX} &= \frac{\sqrt{2} V_{AC\_MAX}}{N_{PS}} + V_{OUT} \\ &= \frac{\sqrt{2} \times 277V}{2.0} + 40V \\ &\approx 236V \end{aligned}$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2.0 \times 3.37A = 6.74A$$

$$I_{D\_AVG} = I_{OUT} = 1A$$

#4. Select the output capacitor C_{OUT}

Refer to **Output capacitor C_{OUT}**

Conditions			
I_{OUT}	1A	ΔI_{OUT}	$0.2 \times I_{OUT}$
f_{AC}	50Hz	R_{LED}	19.2Ω

The output capacitor is

$$C_{OUT}=\frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2-1}}{4\pi f_{AC}R_{LED}}$$

`

$$=\frac{\sqrt{(\frac{2\times 1A}{0.2\times 1A})^2-1}}{4\pi\times 50Hz\times 19.2\Omega}$$

$$\approx 825\mu F$$

#5. Set VIN pin

Refer to **Start Up**

Conditions			
V_{BUS_MIN}	120V×1.414	V_{BUS_MAX}	277V×1.414
I_{ST}	2.0µA (typical)	V_{IN_ON}	21.5V (typical)
t_{ST}	500ms (designed by user)		

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS}}{I_{ST}}=\frac{120V\times 1.414}{34\mu A}=4.99M\Omega\ ,$$

$$R_{ST}>\frac{V_{BUS}}{1mA}=\frac{277V\times 1.414}{1mA}=391k\Omega\ ,$$

Set R_{ST}

$$R_{ST}=330k\Omega\times 2=660k\Omega$$

(b) Design C_{VIN}

$$C_{VIN}=\frac{(\frac{V_{BUS}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}$$

$$=\frac{(\frac{120V\times 1.414}{660k\Omega}-2\mu A)\times 500ms}{21.5V}$$

$$=5.93\mu F$$

Set C_{VIN}

$$C_{VIN}=4.7\mu F$$

#6 Set opto-coupler output

Recommended parameters			
R_{opto1}	2.4kΩ	C_{opt1}	1uF
C_{opot2}	10nF		

#7 Feedback Loop Design

Recommended parameters			
C_{GM1}	470nF	C_{GM2}	10nF
R_{GM}	300kΩ		

#8 Set output current sense resistor to achieve ideal output current

Refer to **Secondary Side Feedback Control**

Known conditions at this step			
V_{IREF}	0.1V	I_{OUT}	1A

The current sense resistor is

$$R_{SAMPLE}=\frac{V_{IREF}}{I_{OUT}}=\frac{0.1V}{1A}=0.1\Omega$$

#9 set ISEN pin

Refer to **Design of R_{ISEN} and Output Current Limit**

Known conditions at this step			
V_{ISEN_LIMIT}	1.0V	$I_{P\_PK\_MAX}$	3.37A

The ISEN resistor is

$$R_{ISEN}=\frac{90\%\times V_{ISEN\_LIMT}}{I_{P\_PK\_MAX}}=\frac{0.9V}{3.37A}\approx 0.267\Omega$$

Set R_{ISEN}

$$R_{ISEN}=0.82R//0.82R//0.82R$$

#10 set VSEN pin

Refer to **Over Voltage Protection (OVP)**

First compute N_P, N_S and N_{AUX}.

Conditions			
L_M	400uH	$I_{P\_PK\_MAX}$	3.37A
ΔB	0.28T	Ae	119mm^2

$$N_P=\frac{L_M\times\frac{V_{ISEN\_LIMIT}}{R_{ISEN}}}{\Delta B\times Ae}=\frac{400\times 10^{-6}\times\frac{1.0}{0.267}}{0.28\times 119\times 10^{-6}}\approx 46$$

$$N_S=N_P/N_{PS}=23$$

$$N_{AUX}=N_S\times\frac{V_{VIN}}{V_{OUT}}=23\times\frac{40V}{40V}=23$$

Next compute R_{VSEN_U} and R_{VSEN_D}.

Conditions			
V_{FB_HIGH}	1.40V	V_{OUT_OVP}	48V
V_{OUT}	40V		
Parameters designed			
N_S	23	N_{AUX}	23

R_{VSEN_D} is preset

$$R_{VSEN\_D}=10k\Omega$$

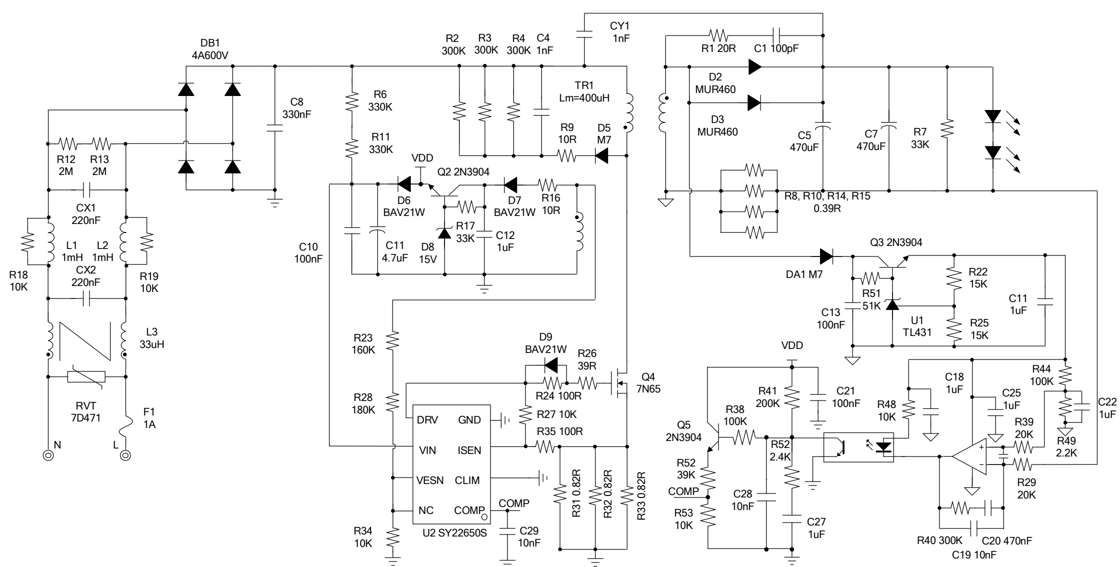
Hence R_{VSEN_U} is set to

$$\begin{aligned} R_{VSEN\_U} &= \frac{V_{OUT\_OVP}}{V_{REF}} \times \frac{N_{AUX}}{N_S} \times R_{VSEN\_D} - R_{VSEN\_D} \\ &= \frac{48V}{1.40V} \times \frac{23}{23} \times 10k\Omega - 10k\Omega \\ &= 333k\Omega \end{aligned}$$

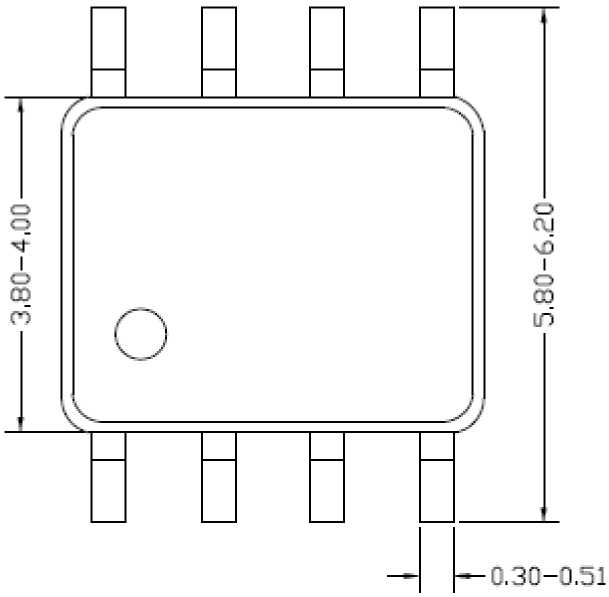
Set R_{VSEN_U}

$$R_{VSEN}=180k\Omega+160k\Omega$$

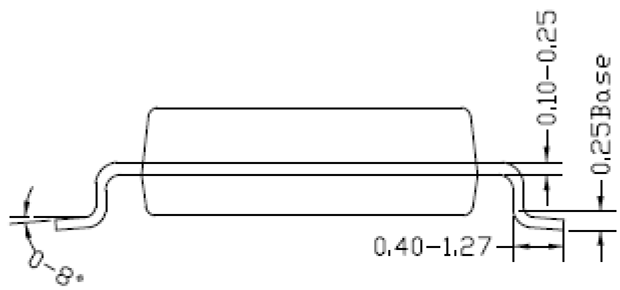
#11 final result



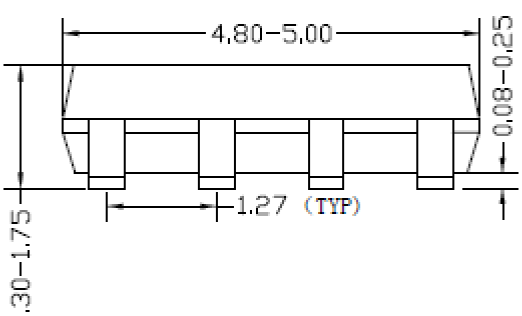
SO8 Package outline & PCB layout design



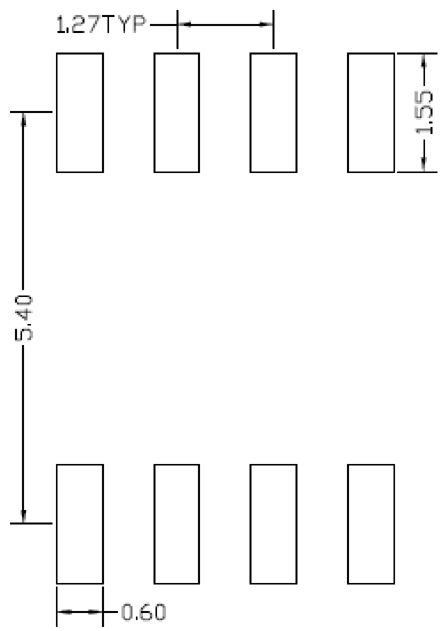
Top view



Side view



Front view

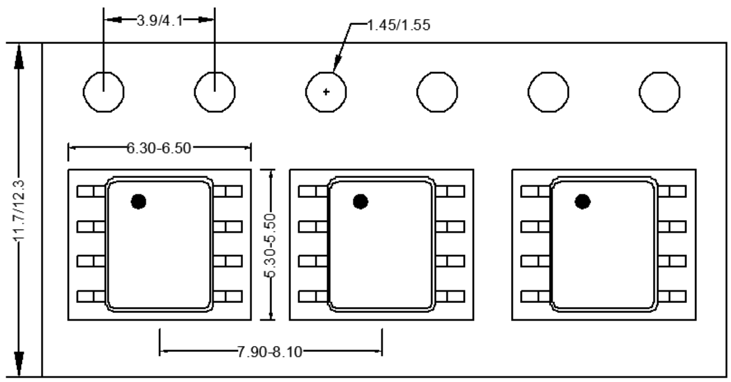


Recommended Pad Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

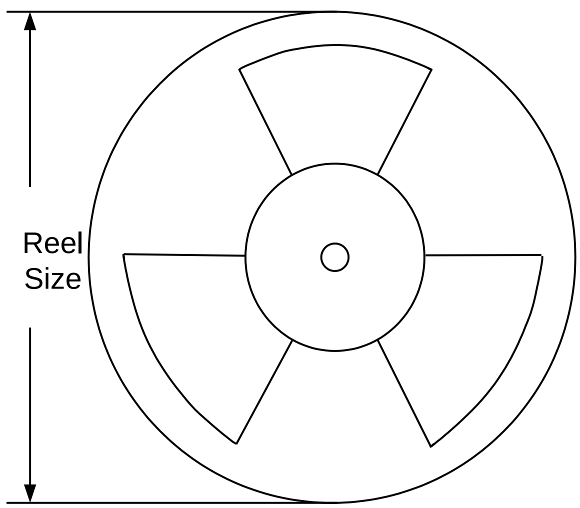
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 30，2022	Revision 0.9	Initial Risk Production Release
December 30，2023	Revision 1.0	Initial Production Release

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