SY5072A

Boost PFC Controller

General Description

The SY5072A is a constant voltage boost controller featuring a Power Factor Correction (PFC) function. Constant ON Time control is utilized to achieve high power factor (PF) and low total harmonic distortion (THD) without the need for a multiplier. It operates the boost converter in Quasi-Resonant mode to enhance efficiency and improve electromagnetic interference (EMI) performance. The design incorporates features for quick startup and reliable protection to meet safety requirements.

Features

- 9V to 22V Input Voltage Range
- Valley Turn-on to Achieve Low Switching Losses
- Frequency Reduction in light load Conditions
- Internal High-current MOSFET driver: 75mA sourcing and 400mA sinking
- Low Startup Current: 1.9μA Typical(typ.)
- MOSFET Over-Current Protection (OCP)
- Internal THD Optimization to Achieve Low THD
- Internal Transition Optimization
- Compact Package: SOT23-6

Applications

- AC/DC Adapters
- Pre-stage for Two-stage AC/DC Converter
- LED Lighting

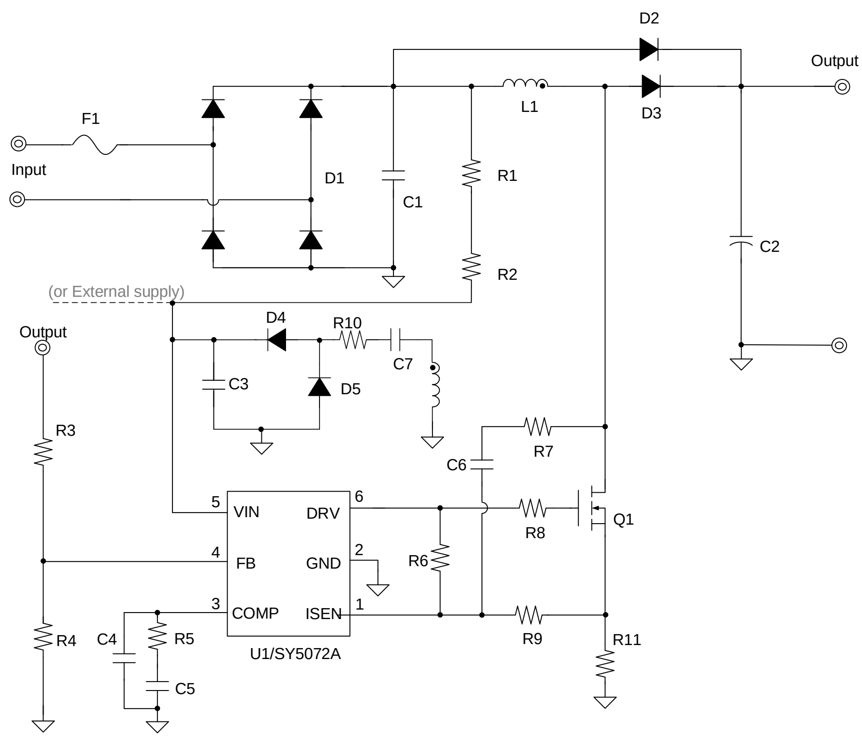


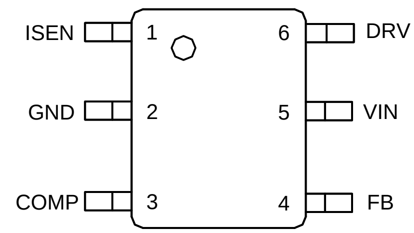
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SY5072AABT	SOT23-6 RoHS-Compliant and Halogen-Free	**HTH*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	ISEN	Current limit and valley detection pin.
2	GND	Ground pin.
3	COMP	Loop compensation pin: Connect an RC network between this pin and ground to stabilize the control loop.
4	FB	Feedback pin: This pin receives the output feedback voltage. The internal reference voltage is 1.25 V.
5	VIN	Power supply pin.
6	DRV	Gate driver pin: Connect this pin to the gate of the primary MOSFET using a resistor.

Block Diagram

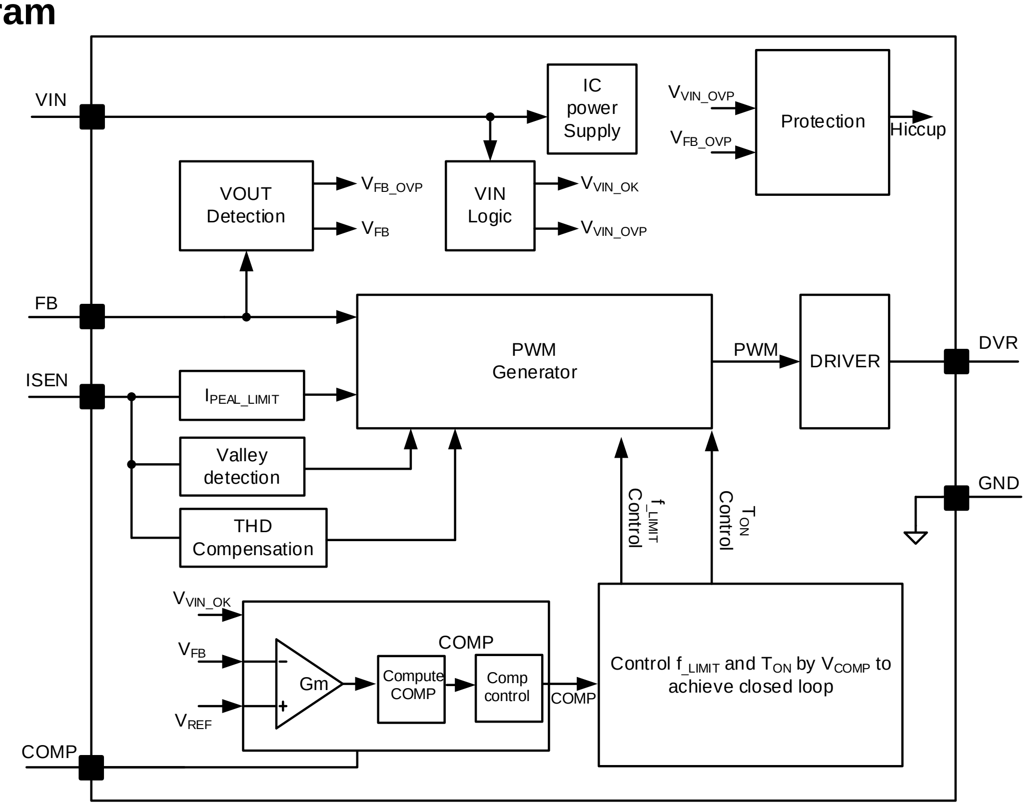


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter(**Note 1**)	Min	Typ	Max	Unit
VIN	-0.3		28	V
DRV	-0.3		25	
ISEN(Note 2)	-0.4		25	
COMP,FB			3.6	
Lead Temperature (Soldering, 10 sec.)			260	°C
Junction Temperature, Operating	-40		150	
Storage Temperature	-65		150	

Thermal Information

Parameter (**Note 2**)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		140	°C/W
θ_{JC} Junction-to-case Thermal Resistance		130	
PD Power Dissipation T_A = 25°C		0.6	W

Recommended Operating Conditions

Parameter (**Note 3**)	Min	Max	Unit
VIN, DRV	9	22	V
Junction Temperature Range	-40	125	°C

ESD Rating

Parameter	Typ	Unit
V_{ESD_HBM}(Human Body Model, HBM), all pins	±2000	V
V_{ESD_CDM}(Charged Device Model, CDM), all pins	±500	V

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply	VIN Turn-on Threshold	V_{VIN_ON}		13.3	14.6	15.8	V
	VIN Turn-off Threshold	V_{VIN_OFF}		6.5	7.5	8.5	V
	VIN OVP Voltage	V_{VIN_OVP}		22.0	24.5	27.0	V
	Startup Current	I_{ST}	$V_{VIN}<V_{VIN\_ON}$	0.75	1.9	3.0	µA
	Quiescent Current	I_Q	No switching	0.24	0.42	0.6	mA
	Discharge Current in Protection Mode	I_{VIN_P}	$V_{VIN}>V_{VIN\_OVP}$		5		mA
Error Amplifier	V_{FB} at Fast Start up	V_{FB_LOW}		1.00	1.10	1.20	V
	Internal Reference Voltage	V_{REF}		1.225	1.250	1.275	V
	Output OVP Threshold	V_{FB_OVP}		1.25	1.35	1.46	V
Current Sense	Current Limit Voltage	V_{ISEN_LIMIT}		0.88	1.00	1.12	V
	Protect Current Limit Voltage	V_{ISEN_OCP}		1.8	2		V
Gate Driver	Gate Driver Voltage	V_{Gate}		10	12	14	V
	Typical Source Current	I_{SOURCE}	Vgate=9V	63	75	87	mA
	Typical Sink Current	I_{SINK}	Vgate=3V	300	400	500	mA
	Max ON Time	t_{ON_MAX}	Vcomp=2.5V		23		µs
	Min ON Time	t_{ON_MIN}			0.45		µs
	Max OFF Time	t_{OFF_MAX1}	No the valley signal detected	27	33	41	us
		t_{OFF_MAX2}	Minimum operating frequency	435	535	650	µs
Thermal Shutdown	Thermal Shutdown Threshold	$T_{TSD\_shutdown}$			150		°C
	Thermal Shutdown Recovery	$T_{TSD\_recovery}$			120		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

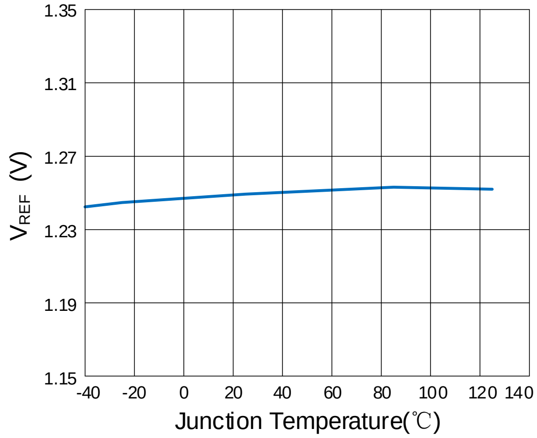
Note 2: When the ISEN voltage is less than -0.4 V, the pin is safe if the negative current through the pin is less than 200 mA and the duration is less than 500 ns.

Note 3: θ_{JA} is measured in natural convection at T_A = 25°C on a low effective single-layer thermal conductivity test board according to the JEDEC 51-3 thermal measurement standard. Test conditions: the device is mounted on a 2" x 2" FR-4 substrate PCB with 2 oz of copper, featuring a minimum recommended pad on the top layer and thermal vias to the bottom layer ground plane.

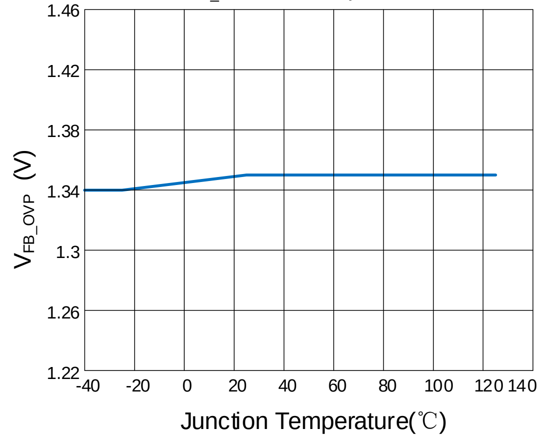
Note 4: Increase the VIN pin voltage gradually above the V_{VIN_ON} voltage, then reduce it to 12V.

Typical Performance Characteristics

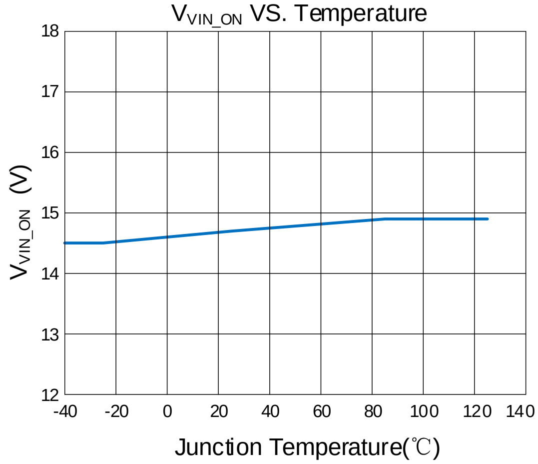
V_{REF} VS. Temperature



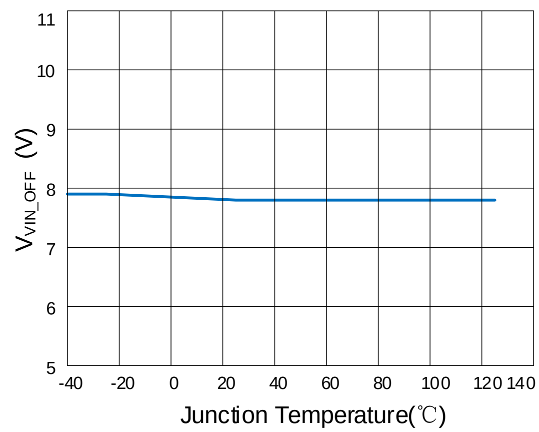
V_{FB_OVP} VS. Temperature



V_{VIN_ON} VS. Temperature

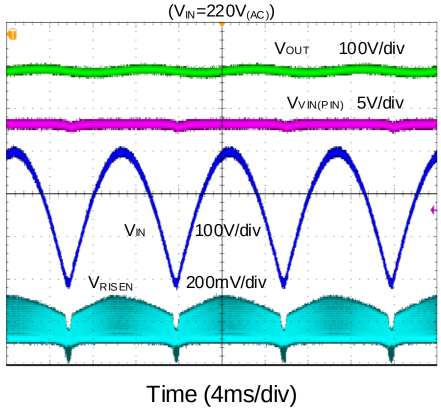


V_{VIN_OFF} VS. Temperature



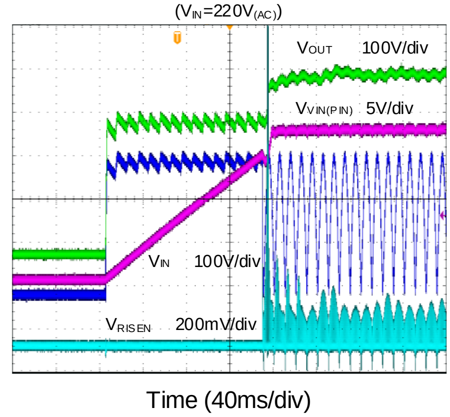
Steady States

(V_{IN}=220$V_{(AC)}$)



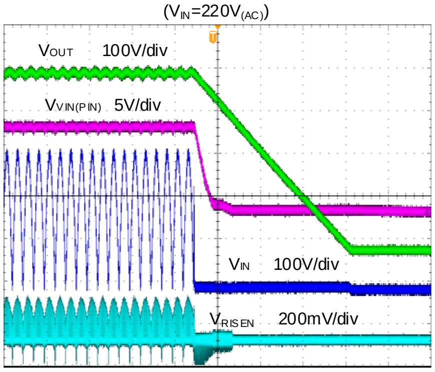
Startup

(V_{IN}=220$V_{(AC)}$)



Shutdown

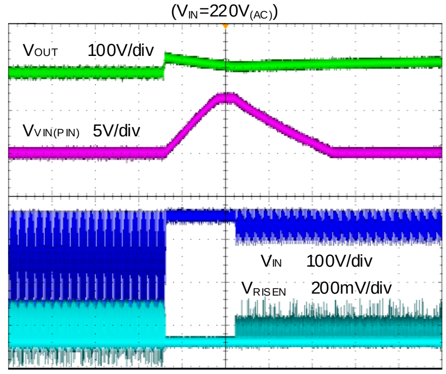
(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Output Open Protection

(V_{IN}=220$V_{(AC)}$)



Time (400ms/div)

Operation

The SY5072A is a constant voltage boost controller with Power Factor Correction (PFC) functionality, designed to drive cost-effective pre-converters that comply with line current harmonic limits. The SY5072A operates in constant on-time mode. Its voltage mode (constant on-time control) scheme enables it to achieve near-unity power factor without requiring a line voltage sensing network. To reduce switching losses and improve EMI performance, a Quasi-Resonant switching mode is implemented. It integrates adjustable Total Harmonic Distortion (THD) compensation for different applications to achieve low THD. Enhanced line and load transitions are facilitated through internal optimization. The SY5072A provides reliable protections, including Over Voltage Protection (OVP), Over Current Protection (OCP), and Over Temperature Protection (OTP).

Applications Information

Startup

After the AC supply or DC bus is powered on, the capacitor C_{VIN} (connected between the VIN and GND pins) is charged by the bus voltage through a startup resistor R_{ST}. The low startup current consumption (1.9 µA) minimizes standby power dissipation. When V_{VIN} rises above V_{VIN_ON}, the internal blocks activate, and V_{VIN} decreases due to the power consumption of the device until the external supply or the auxiliary winding of the boost inductor can support V_{VIN}. The SY5072A includes an under-voltage lockout (UVLO) feature that ensures operation until V_{VIN} falls below V_{VIN_OFF}. This hysteresis provides sufficient time for VIN to be supplied from the external source or the auxiliary winding. The startup sequence consists of two sections, as shown in Figure 5: t_{STC}, the C_{VIN} charging section, and t_{STO}, the output voltage buildup section. The total startup time, t_{ST}, comprises t_{STC} and t_{STO}. Typically, t_{STO} is much shorter than t_{STC}.

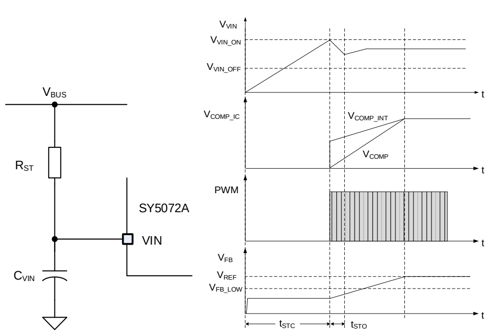


Figure 2. Startup

If V_{FB} is lower than a certain threshold, V_{FB_LOW}, it indicates that the output voltage has not yet built up. In this case, V_{COMP} is pulled up by a large resistor (R_g) to a high clamped level, V_{COMP_INT}, and is held at this level until V_{FB} approaches V_{REF}. This operation is designed to build up sufficient output voltage as quickly as possible. The simple logical diagram is shown in Figure 3.

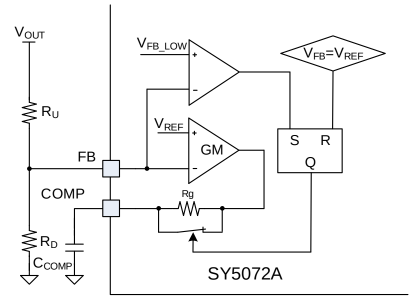


Figure 3. Startup Logical Diagram

The startup resistor R_{ST} and capacitor C_{VIN} are selected using the following steps:

1. Ensure that the current through R_{ST} is greater than the minimum startup current I_{ST} and less than 1 mA.

$$\frac{V_{BUS}}{1mA} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the bus line voltage.

2. Select C_{VIN} to achieve an optimal startup time (t_{ST}) and ensure that the output voltage reaches the nominal value within the target time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

3. If necessary, repeat the steps above to obtain the final values for C_{VIN} and t_{ST}.

Shutdown

After the AC supply or DC bus is powered off, the energy stored in the bus capacitor will be discharged. If the auxiliary winding cannot supply sufficient energy to the VIN pin, V_{VIN} will drop. When V_{VIN} falls below V_{VIN_OFF}, the device will shut down, and V_{COMP} will be discharged to zero.

Quasi-Resonant(QR) Operation

QR mode operation provides low turn-on switching losses in MOSFETs.

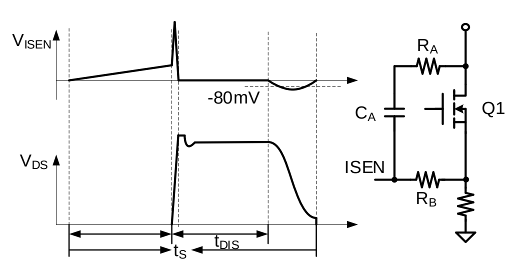


Figure 4. QR Mode Operation

Thus, C_A=10pF and R_A=1K is recommended. The voltage of the MOSFET (V_{DS}) is reflected to the device by the RC network (R_A and C_A) connected between the drain of the MOSFET and the ISEN pin. A resistor (R_B) is connected between the ISEN pin and the ISEN resistor to detect negative voltage. Capacitor C_A is needed for voltage valley detection. The larger the capacitance, the greater the capacitance losses. Therefore, C_A = 10 pF and R_A = 1 kΩ are recommended.

Error Amplifier Regulation

The SY5072A regulates the boost output voltage using a transconductance internal error amplifier (EA). The inverting terminal of the EA is connected to the feedback (FB) pin, while the non-inverting terminal is linked to an internal 1.25V voltage reference. The output of the EA is connected to the compensation (COMP) pin (see Figure 5). The resistance R_g is a parasitic resistance that aids in loop control, with a typical value of approximately 8 kΩ. Due to the operation of the transconductance error amplifier, the FB pin can also be utilized to detect both output overvoltage and undervoltage conditions.

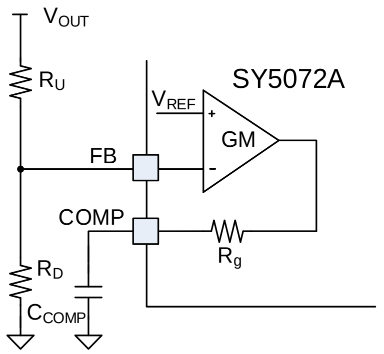


Figure 5. Output Voltage Feedback Circuit

A resistor divider (R_U and R_D) scales down the Boost output voltage (V_{OUT}) and connects to the FB pin. If the output voltage is less than the regulation, the control voltage (V_{COMP}) increases the on-time of the driver, which enhances the power transferred from the input to the output. If V_{OUT} is higher than the regulation, V_{COMP} decreases the on-time to limit the power transfer. The output voltage is calculated using the following equation:

$$V_{OUT} = V_{REF} \times \left(\frac{R_U + R_D}{R_D} \right)$$

Over-Voltage Protection (OVP)

Due to the extremely low bandwidth of the PFC's voltage loop, there is a risk of overshoots on the output side during startup, load steps, and line steps. To ensure reliable operation, overvoltage protection (OVP) is necessary to prevent the output voltage from exceeding the ratings of the PFC stage components.

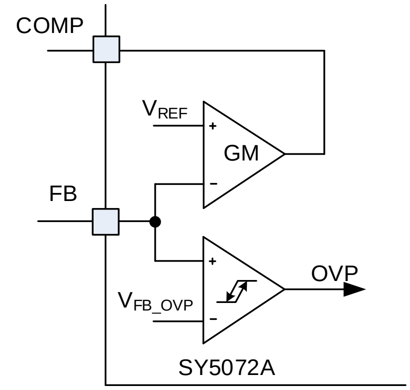


Figure 6. Output Protection Circuit

The value of C_{OUT} is sized to ensure that OVP is not inadvertently triggered by the 100 Hz or 120 Hz ripple of V_{OUT}. In steady state, the minimum value of C_{OUT} is calculated using the following equation, assuming that the ESR of the output capacitor is insignificant.

$$V_{OUT\_OVP} = V_{FB\_OVP} \times \left(\frac{R_U + R_D}{R_D} \right)$$

The value of C_{OUT} is sized to ensure that OVP is not inadvertently triggered by the 100 Hz or 120 Hz ripple of V_{OUT}.

In the steady states, the minimum value of C_{OUT} is calculated using by the following equation and assume that the ESR of output capacitor is insignificant.

$$C_{bulk} \geq \frac{P_{OUT}}{2 \times \pi \times V_{ripple(peak-peak)} \times f_{line} \times V_{OUT}}$$

Where $V_{ripple(peak-peak)}$ is the peak-to-peak output voltage ripple, typically selected in the range of 3.0% of the output voltage. f_{line} is the AC line frequency (50 Hz or 60 Hz).

Frequency reduction

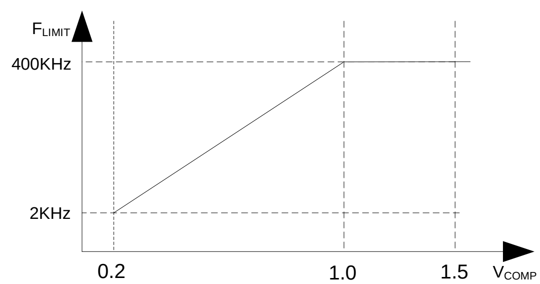


Figure 7. Frequency Reduction

Frequency reduction is dependent on V_{COMP}: When V_{COMP} is greater than 1.0 V, the frequency is limited to 400 kHz. When V_{COMP} is less than 1.0 V, the frequency will gradually decrease from 400 kHz to 2 kHz.

Special Design for Transition

To achieve good transition performance, a special design is integrated into the SY5072A.

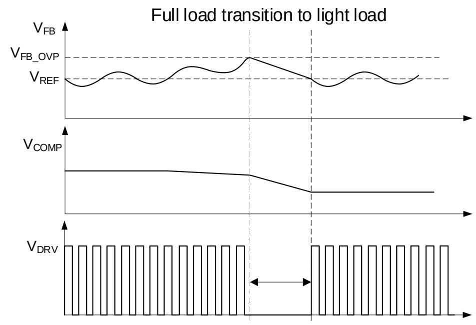


Figure 8. Load Transition (Full Load to Light Load)

When FB touches V_{FB_OVP}, the device will stop DRV to reduce output energy, and then V_{COMP} will decrease through the feedback loop to achieve a new balance.

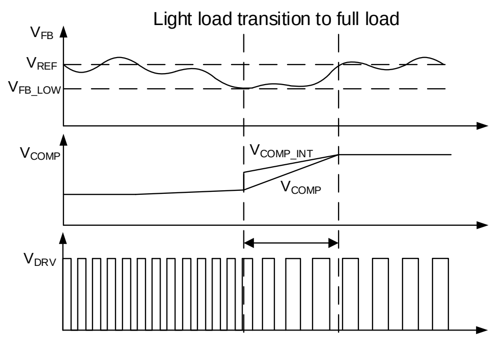


Figure 9. Load Transition (Light Load to Full Load)

When FB touches V_{FB_LOW}, a large resistor will be connected to COMP (refer to startup logic). Consequently, V_{COMP_INT} will be higher than V_{COMP}, causing the ON time of the DRV to increase suddenly to expedite output energy until FB reaches V_{REF} and V_{COMP} equals V_{COMP_INT} again. V_{COMP} will then reach a new balance. Line transitions are similar to load transitions. If the input voltage changes from low to high, it can be considered a transition from full load to light load; if the input voltage changes from high to low, it can be considered a transition from light load to full load.

Over Current Protection (OCP)

The dedicated ISEN pin of the SY5072A limits the MOSFET peak current on a cycle-by-cycle basis if the voltage of the ISEN pin exceeds V_{ISNE_LIMIT}. The maximum power inductor current (I_{PK_MAX}) occurs at minimum input voltage under full load conditions. Therefore, R_{ISEN} can be selected using the following equation:

$$R_{ISEN} = \frac{90\% \times V_{ISEN\_LIMIT}}{I_{PK\_MAX}}$$

Where V_{ISEN_LIMIT} serves as a protection mechanism for the inductor (if V_{ISEN} reaches this voltage, the gate will turn off), and I_{PK_MAX} represents the maximum power of the inductor in a steady state. When V_{ISEN} continues to increase to V_{ISEN_OCP}, the device will discharge V_{VIN} using an internal current source I_{VIN_P}. Once V_{VIN} falls below V_{VIN_OFF}, the device will shut down and will be recharged by the BUS voltage through the startup resistor.

Internal THD Compensation

Due to the presence of the inductance and the capacitance C_{ds} of the MOSFET, when the inductive current is zero, they begin to resonate in an LC circuit. Before the MOSFET turns on, there is a component of negative current in the inductive current.

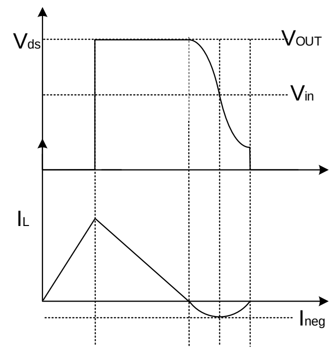


Figure 10. Current of Inductance

The term I_{neg} is a function of Vin, V_{OUT}, L, and C_{ds}. During resonance, we can assume no losses and apply energy conservation to calculate it:

$$i_{neg} = (V_{out} - V_{in}) \times \sqrt{C_{ds}/L}$$

The waveform of the inductance current over a power frequency period is shown in Figure 11.

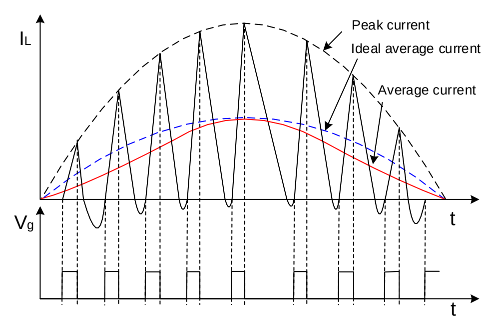


Figure 11. Average Current Waveform of Inductance

The ideal average current controlled by COT is a sine wave that follows the input voltage. However, the actual average current has been distorted, which negatively impacts THD performance. THD compensation helps mitigate the effect of negative current, resulting in improved THD. The analog implementation example shown in Figure 12 resembles a standard COT, with the addition of a voltage comparator featuring a fixed threshold of 200 mV. The Ton generator does not activate until the ISEN exceeds the fixed threshold of 200 mV. Once this occurs, the comparator output is set high to enable the Ton generator, allowing it to begin operation. The compensation current ΔI can be calculated using the following equation:

$$\Delta I = \frac{200mV}{R_S}$$

If $\Delta I = I_{neg}$, the effect of the negative current will be offset, optimizing the total harmonic distortion (THD).

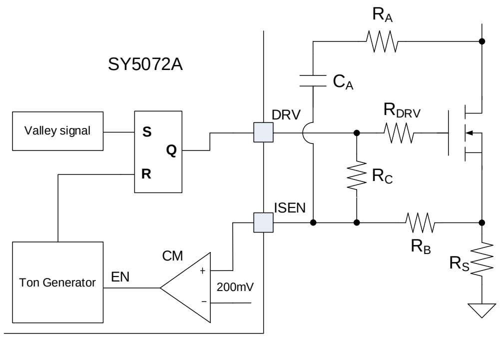


Figure 12. THD Compensation Logic

Different applications will have varying LC parameters, resulting in different I_{neg} values. The SY5072A supports external parameter modifications to change the compensation current and achieve optimal THD. The external parameters are the resistors R_B and R_C, as shown in Figure 12. Assuming $R_C >> R_B$, the compensation ΔI can be calculated using the following equation:

$$\Delta I = (200mV - V_{DRV}/R_C \times R_B)/R_S$$

Different applications need different ΔI . R_C is the discharge resistor of MOSFET and 10K is the recommend. Then changing R_B can achieve ideal THD preferment.

Power Device Design

MOSFET and Diode

When the operating condition is maximum voltage input and full load output, the MOSFET and boost diode experience the maximum voltage stress. Considering the output voltage, the overvoltage magnitude, and the derating margin for safety, a 600V device is commonly selected. When the operating condition is minimum voltage input and full load output, the semiconductor devices experience the maximum current stress.
Peak current of the inductor:

Peak current of inductor:

$$I_{L(peak)} = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times V_{IN\_MIN}}$$

Peak current of the MOSFET

$$I_{MOSFET(peak)} = I_{DIODE(peak)} = I_{L(peak)}$$

RMS Current of Inductor:

$$I_{L(rms)} = \frac{2 \times P_{OUT}}{\sqrt{3} \times \eta \times V_{IN\_MIN}}$$

RMS Current of MOSFET:

$$I_{MOSFET(rms)} = \frac{2}{\sqrt{3}} \times \frac{P_{out}}{\eta \times V_{IN\_MIN}} \times \sqrt{1 - (\frac{\sqrt{2} \times 8 \times V_{IN\_MIN}}{3 \times \pi \times V_{OUT}})}$$

RMS Current of Diode:

$$I_{DIODE(rms)} = \frac{4}{3} \times \frac{P_{OUT}}{\eta \times \sqrt{V_{IN\_MIN} \times V_{OUT}}} \times \sqrt{\frac{2 \times \sqrt{2}}{\pi}}$$

Average Diode Current:

$$I_{DIODE(ave)} = I_{OUT} = \frac{P_{OUT}}{V_{OUT}}$$

Where P_{OUT} is the output power, V_{OUT} is the output voltage, V_{IN_MIN} is the minimum input AC voltage, and η is the estimated efficiency.

Boost inductor

Once the minimum frequency, f_{sw_MIN}, is set, the inductance can be determined. According to the operating principle, the boost inductor is calculated using the following equation:

$$L_{MAX} = \frac{V_{IN}^2 \times (V_{OUT} - \sqrt{2} \times V_{IN})}{2 \times f_{sw\_MIN} \times P_{IN} \times V_{OUT}}$$

Where f_{sw_MIN} is the preset minimum switching frequency and VIN is the input voltage. Once the inductance is established, we can calculate the winding turns for a specific core. The design rules are as follows:
1. Select the magnetic core and identify the effective area Ae.
2. Preset the maximum magnetic flux ΔB, typically within 0.2-0.3 T.
3. Compute the number of turns for the primary winding N:

$$N = \frac{L \times I_{L(peak)}}{Ae \times \Delta B}$$

Select an appropriate wire diameter and grind the core to achieve the required inductance with the calculated number of turns.

Typical Application Schematic

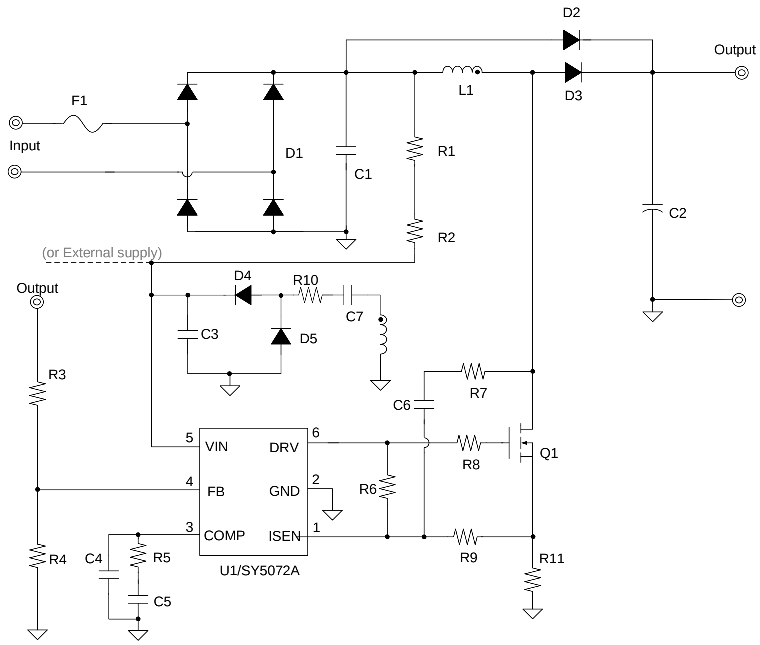


Figure 13. Ground Layout

PCB Layout Guideline

Follow these PCB layout guidelines for optimal performance and effective thermal dissipation:

● To achieve better EMI performance and reduce line frequency ripples, connect the output of the bridge rectifier to the bus line capacitor first, then to the switching circuit.

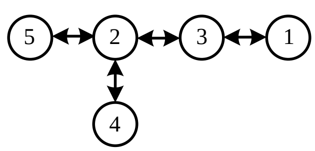
● Keep the circuit loop of all switching circuits small, including both the power loop and the auxiliary power loop.

● Connect the bias supply trace to the bias supply capacitor first, rather than to the GND pin. Position the bias supply capacitor next to the device.

● Minimize the loop of the 'Source pin – current sample resistor – GND pin.'

● It is recommended to place the resistor divider connected to the FB pin beside the device.

● Connect the primary ground as follows:



Ground ①: ground of BUS line capacitor

Ground ②: ground of bias supply capacitor and GND pin

Ground ③: ground node of current sample resistor.

Ground ④: ground of signal trace

Ground ⑤: ground node of auxiliary winding

Recommended PCB Layout

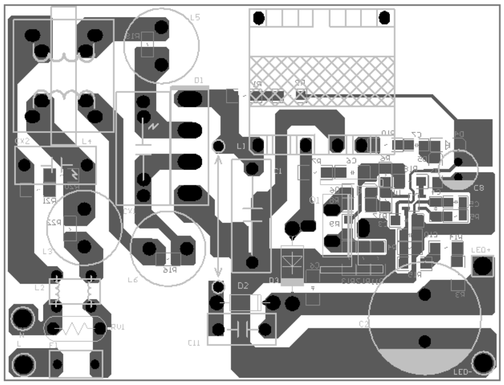
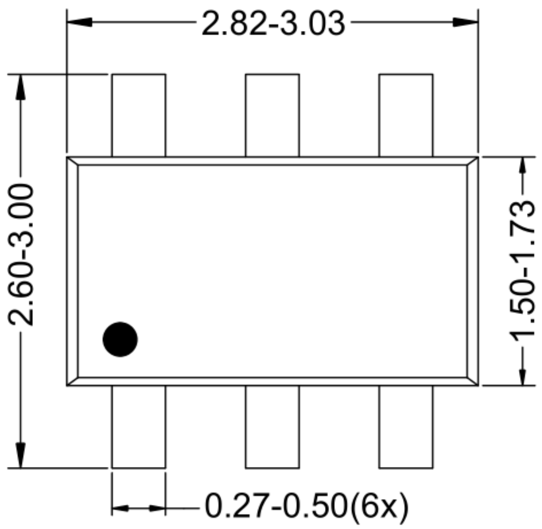


Figure 14. EVB Layout

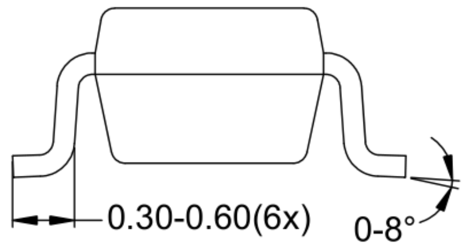
BOM List

Ref Des	Description	Manufacturer	Part Number	Comment
C1	330n/630V/±10%	PANASONIC	ECQE6334KF	Capacitor, Film
C2	33uF/450V/±20%	Nichicon	UCS2W330MHD	Capacitor, Aluminum
C3	100nF/25V/0805/X7R	YAGEO	CC0805KRX7R8BB104	Capacitor, Ceramic
C4	220nF/25V/0805/X7R	YAGEO	CC0805KRX7R8BB224	Capacitor, Ceramic
C6	10pF/1KV/1206	YAGEO	CC1206JKNPOCBN100	Capacitor, Ceramic
C7	22nF/50V/0805/X7R	YAGEO	CC0805KRX7R9BB223	Capacitor, Ceramic
L1	1.2mH/132:6/PQ2020	——	——	Inductor
D1	4A/600V	GOODWORK	KBL406	Bridge Rectifier
D2	1A/1KV/SOD-123	GOODWORK	1N4007W	Diode, Universal
D3	4A/600V/DO-201AD	Onsemi	MUR460G	Diode, fast
D4, D5	250V/250mA/SOD-123	GOODWORK	BAV21WS	Diode, Universal
Q1	10A/650V/0.81Ω/ITO-220AB-3	GOODWORK	10N65F	MOSFET, N-CH
R1, R2	300K/1206/±5%/250mW	YAGEO	RC1206JR-07300KL	Resistor
R3, R14, R15	1Meg/1206/±1%/250mW	YAGEO	RC1206FR-071ML	Resistor
R4	9.1K/0805/±1%/125mW	YAGEO	RC0805FR-079K1L	Resistor
R6	10K/0805/±5%/125mW	YAGEO	RC0805JR-0710KL	Resistor
R7	1K/1206/±5%/250mW	YAGEO	RC1206JR-074KL	Resistor
R8	100R/0805/±5%/125mW	YAGEO	RC0805JR-07100RL	Resistor
R9	130R/0805/±5%/125mW	YAGEO	RC0805JR-07130RL	Resistor
R10	10R/0805/±5%/125mW	YAGEO	RC0805JR-0710RL	Resistor
R11, R12, R13	1.2R/1206/±1%/250mW	YAGEO	RC1206FR-071R2L	Resistor
U1	SY5072A/SOT23-6	SILERGY	SY5072AABT	IC

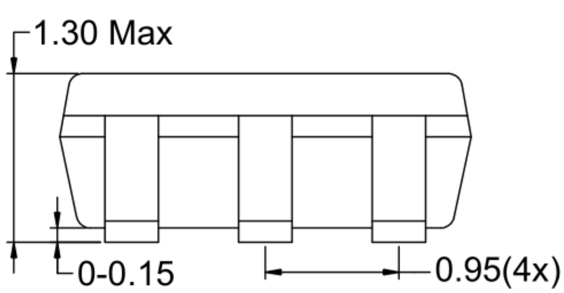
SOT23-6 Package Outline & PCB layout



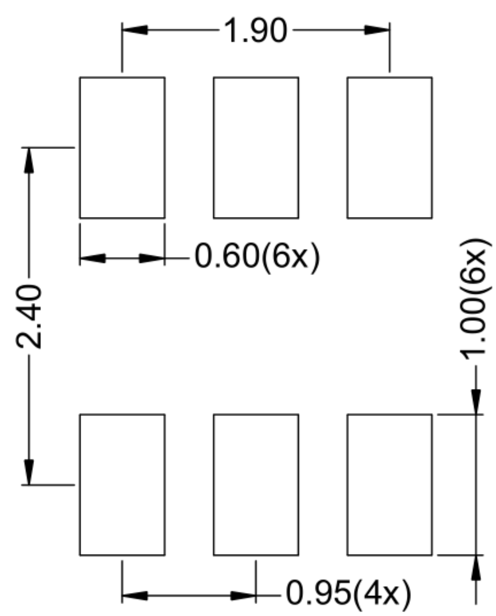
Top View



Side View



Side View



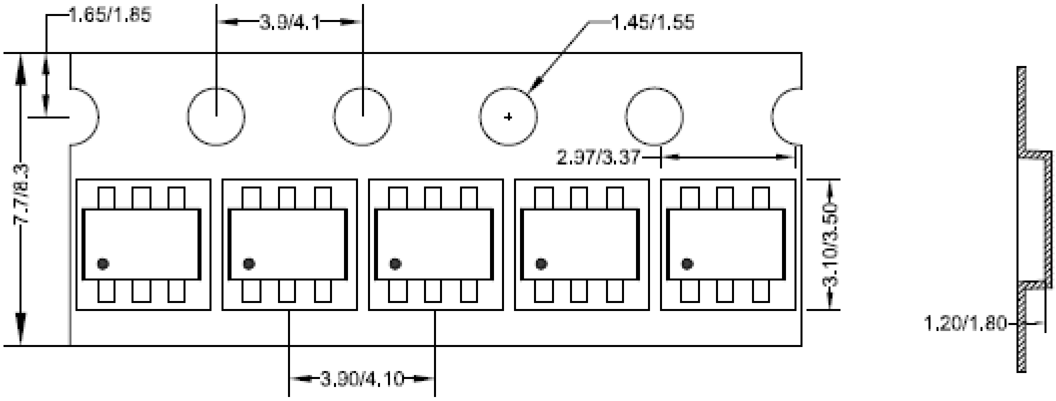
Recommended PCB Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

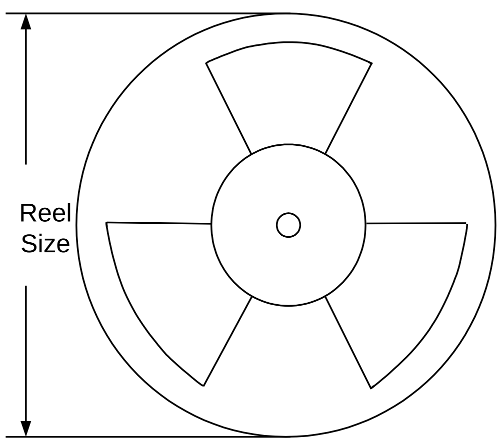
1. Taping orientation

SOT23-6



Feeding direction→

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SOT23-6	8	4	7"	280	160	3000

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
October 31 ,2024	Revision 1.0	Initial Release

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