SY59526

Charge Pump PFC LLC High Side Controller, High PF, Low THD

General Description

The SY59526 is the high side LLC controller integrated with a 650V MOSFET, it is used in charge pump PFC application. The high PF is achieved by inherent PFC function and the low LED current ripple is achieved by LLC topology. The single stage structure and primary side regulation save BOM cost a lot. Meanwhile, the LLC topology improves efficiency and EMI.

The SY59526 should work with SY59525, which is the low side LLC controller integrated with a 650V MOSFET.

Features

- Integrated 650V MOSFET
- Charge Pump PFC LLC Topology with Low BOM Cost
- PF>0.95, THD<20%
- Primary Side I_{LED} Regulation and Less than 2% I_{LED} Ripple
- Short LED Protection (SLP), Open LED Protection (OLP), E-cap over Voltage Protection (HV OVP)
- Zero Voltage Overshoot on Resonant Capacitor at Startup
- Compact Package: SO8

Applications

- LED Lighting

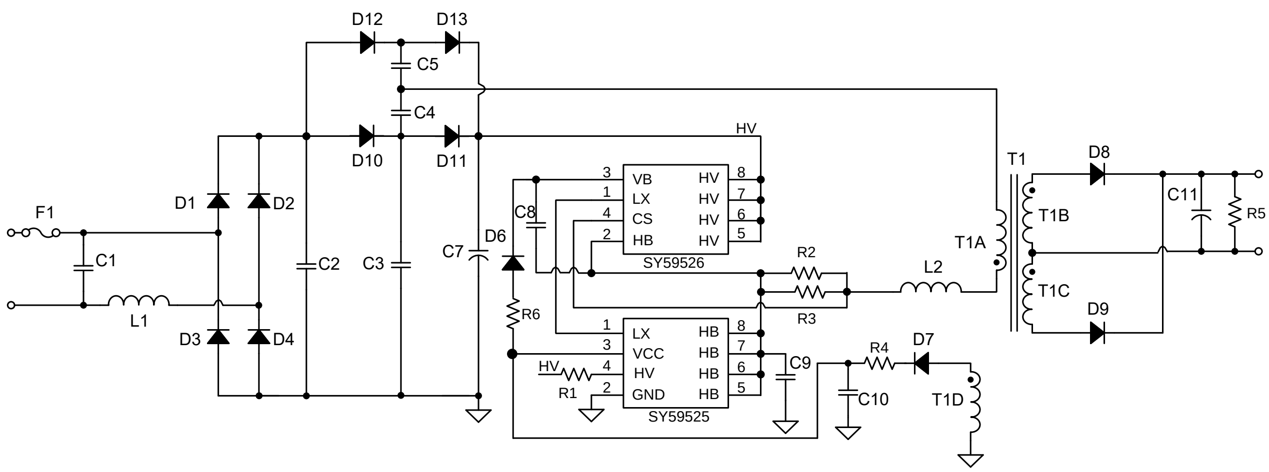


Figure 1a. Typical Application Circuit

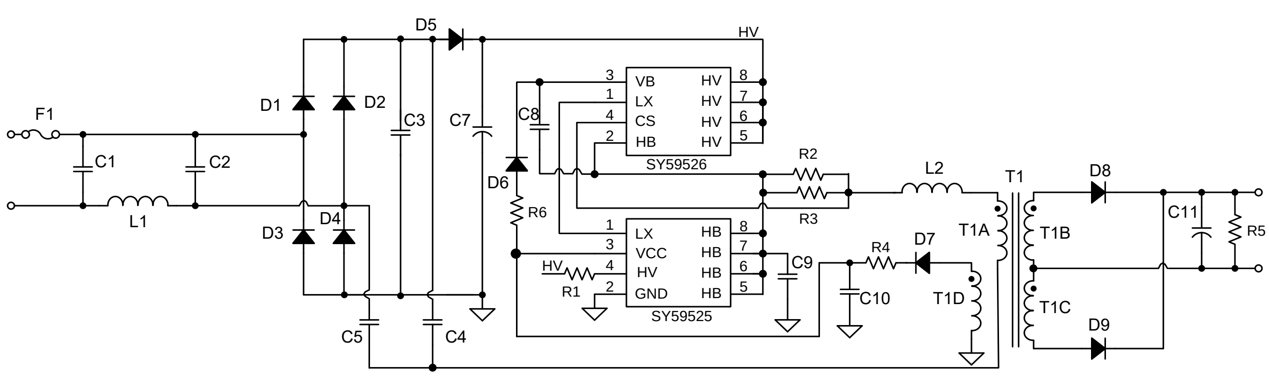


Figure.1b Typical Application

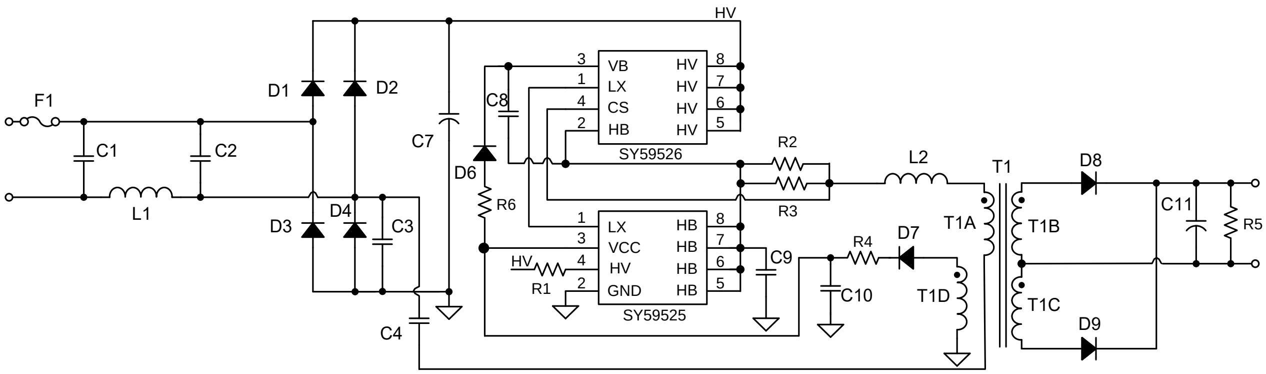


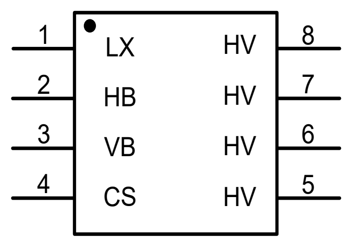
Figure.1c Typical Application

Ordering Information

Ordering Part Number	Package type	Top Mark
SY59526FAP	SO8 RoHS Compliant and Halogen Free	**FLD *xyz***

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	LX	Low side driver control pin, this pin sends the control signal to SY59525.
2	HB	High-side floating supply reference ground. Source of high side internal 650V MOSFET.
3	VB	High-side floating supply.
4	CS	Primary current sense pin, this pin receives the primary resonant current by sample resistors and realizes OCP function.
5-8	HV	Drain of internal 650V MOSFET.

Block Diagram

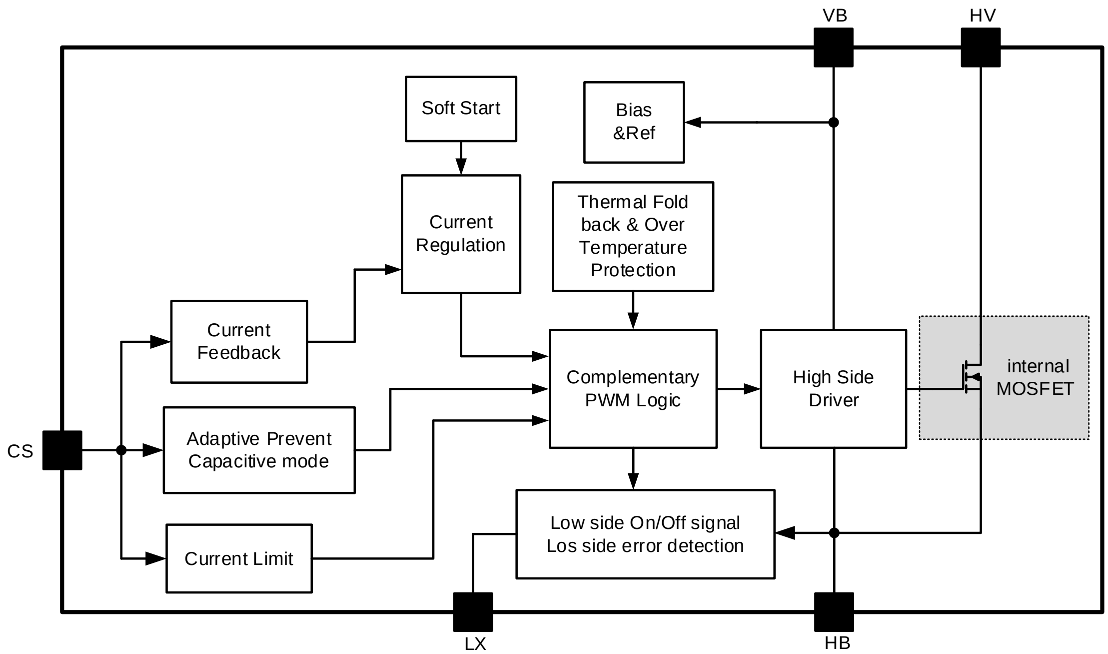


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter(**Note 1**)	Min	Max	Unit
HV	-0.3	650	V
LX	-0.3	36	
VB	-0.3	36	
CS	-0.6	0.6	
Maximum Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (**Note 2**)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		88	°C/W
θ_{JC} Junction-to-case Thermal Resistance		45	
PD Power Dissipation T_A = 25°C		1.1	W

Recommended Operating Conditions

Parameter	Min	Max	Unit
HV	180	450	V
LX	0	35	
VB	11	35	
CS	-0.5	0.5	
Junction Temperature	-40	150	°C
Ambient Temperature	-40	150	

Electrical Characteristics

(V_{IN} = 15V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
Power Supply	VB Turn-on Threshold	V_{VB_ON}		20.5	23	25.5	V
	VB Turn-off Threshold	V_{VB_OFF}		8.7	9.7	10.7	V
	Quiescent current	I_Q	before VB_ON	170	230	290	µA
CS Pin	Current Reference Voltage	V_{REF}		147.5	152	156.5	mV
MOSFET	MOSFET Rdson	R_{dson}		0.75	1	1.25	Ω
	Breakdown Voltage	V_{BV}	V_{GS}=0, I_{DS}=250µA	650			V
Frequency Limit	Maximum Switching Frequency	F_{MAX}		210	230	260	kHz
	Minimum Switching Frequency	F_{MIN}		25	29	33	kHz
	Minimum On Time	T_{MIN_ON}		450	575	700	ns
Thermal	Thermal Fold Back Temperature	T_{FB}		139	149	159	℃
	Thermal Shut Down Temperature	T_{SD}			160		℃

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Operation

SY59526 is the high side LLC controller integrated with a 650V MOSFET, it is used in charge pump PFC application, which is targeting at LED lighting applications. High PF is achieved by inherent PFC function and low LED current ripple is achieved by LLC topology. Single stage structure and primary side regulation save BOM cost a lot.

SY59526 contains reliable turn on and turn off logic, which can avoid LLC half bridge shoot through and support high switching frequency more than 200kHz. SY59526 also adopts special design to achieve zero voltage overshoot on resonant capacitor at startup. It also uses slope detection function to make sure the valley turn on of MOSFET to achieve higher efficiency.

LLC topology improves efficiency and EMI, furthermore, one external NP0 capacitor can be put between midpoint between LLC half bridge and GND point (or BUS point) to further improve system performance.

SY59526 provides reliable protections including over current protection (OCP), over temperature protection (OTP), thermal fold back (TFB) and so on.

SY59526 is available with SO8 package, and should work with SY59525, which is the low side LLC controller integrated with a 650V MOSFET.

Applications Information

Start up

After AC supply or DC BUS is powered on, capacitor C_{VCC} across VCC and GND pin is charged by internal current source. This current source comes from HV pin, which is connected to V_{BUS} through one external resistor R_{HV_EXT}.

The whole start up process can be divided into 4 sections shown in Fig.3, HO and LO are internal gate of SY59526 and SY59525, respectively. t_{STC1} is the C_{VCC} charging up section. t_{STD} is midpoint HB voltage and HV voltage detecting section, during this time, C_{VCC} will charge back and forth between V_{VCC_ON} and V_{VCC_OFF}, until HB voltage is below 6V and HV voltage is lower than HV OVP. SY59525 provides a constant internal current to pull down HB voltage through LX pin, so when MOSFET of SY59525 is turned on, there won't be large resonant current flowing through resonant capacitor. After the above two conditions are met, SY59525 will exit t_{STD} stage and enter into t_{STC2} stage. t_{STC2} is the C_{VCC} together with C_{VB} charging up section, once V_{VB} reaches V_{VB_ON}, internal MOSFET of SY59525 is turned off, switching control starts to work and HV pin stops to provide charge current. t_{STO} is the output voltage building up section, V_{VCC} and V_{VB} will be pulled down by internal consumption current until the auxiliary winding of LLC transformer can supply enough energy to maintain V_{VCC} above V_{VCC_OFF}.

Design of HV pin resistor R_{HV_EXT}, C_{VCC} and C_{VB} is not strict, below are some suggestions:

a) Use R_{HV_EXT} smaller than 200kohms, resistance of R_{HV_EXT} will influence E-cap over voltage protection (HV OVP).

b) Use C_{VCC} larger than 1uF, use C_{VB} larger than 1uF, there no need to use very large C_{VCC} or C_{VB} capacitor, suggest using 2uF C_{VCC} and 1uF C_{VB}.

c) If C_{VCC} and C_{VB} are not big enough to build up output voltage at one time, increase C_{VCC} and C_{VB}, or check whether the output E-cap is too large.

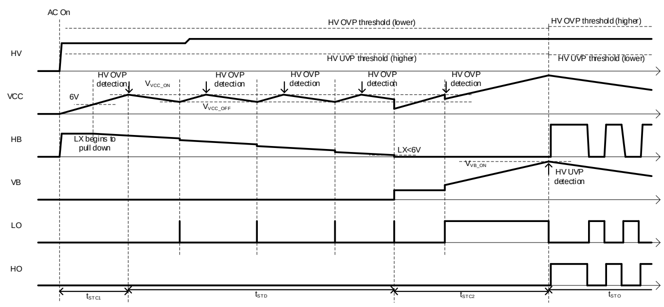


Fig.3 Start up Process of SY59526 and SY59525

After V_{VB_ON} and high side MOSFET is turned on, soft start up function works, it prevents resonant current from being too high at start up. Switching frequency is fixed at maximum switching frequency f_{SW_MAX} during the first few resonant periods.

Primary side LED current regulation (PSR)

The PSR principle is as follows: LED current is estimated by sensing primary side resonant current, sampling resistor is put between HB and inductor or transformer, HB is the source of internal MOSFET of SY59526 and the drain of internal MOSFET of SY59525, so both current flowing into HB and current flowing out of HB can be detected.

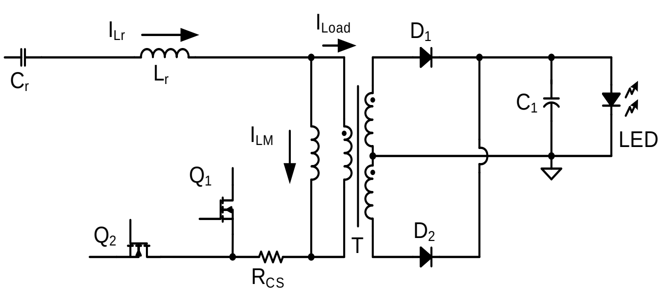


Fig.4 PSR principle of SY59526

The output current program is shown as below:

$$I_{LED} \approx \frac{V_{REF} \times N_{PS}}{R_{CS}}$$

So I_{LED} can be programmed by CS pin resistor.

Shut down

After AC supply or DC BUS is powered off, LLC still works for a while to consume the energy stored in input E-cap. During this time, auxiliary winding can still provide stable VCC voltage so SY59525 and SY59526 can continue with the internal working logic. Once HV pin voltage reaches E-cap under voltage protection (HV UVP), SY59525 will keep internal MOSFET off and SY59526 will turn off its internal MOSFET soon. Once high side and low side MOSFET are turned off, C_{VCC} and C_{VB} will discharge, discharge current of C_{VCC} is quiescent current of SY59525 and discharge current of C_{VB} is constant 6mA. Usually, V_{VB} reaches V_{VB_OFF} earlier than V_{VCC} reaches V_{VCC_OFF}. When V_{VB} reaches V_{VB_OFF}, 6mA discharge current will be removed. When V_{VCC} reaches V_{VCC_OFF}, SY59525 will restart and HV pin starts to provide charge current.

Over current protection (OCP), Over temperature protection (OTP), Thermal fold back (TFB)

OCP: CS voltage reflects resonant current, when $|V_{RCS}|$ reaches 500mV, SY59526 will force change the LX state and force switch the high side and low side MOSFET. Under normal parameter design, it's not easy to trigger OCP. OCP is also not common in other protections, such as OTP, OLP, and SLP. Under special conditions, such as resonant inductor fault or transformer fault, OCP can protect the system from overheating. OCP won't restart the system, it only increases the switching frequency, because the MOSFET is switched earlier.

TFB: When temperature is too high, V_{REF} will begin to drop, the specific curve is shown in Fig.5. When SY59526 reaches 149℃, V_{REF} begins to drop, as the temperature rises, V_{REF} goes down at a constant slope. When SY59526 reaches 155℃, V_{REF} drops to 50% of the rated value and if the temperature keeps rising, V_{REF} keeps constant and stops to drop.

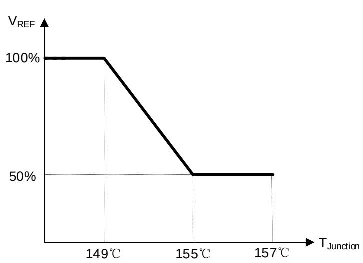


Fig.5 Thermal Fold Back Curve of SY59526

OTP: When SY59526 reaches 157℃, SY59526 will enter fault state, it will turn off high side MOSFET and pull up LX, so low side MOSFET is turned off, too. At the same time, SY59526 begins to discharge by 6mA until V_{VB} reaches V_{VB_OFF}. Later when V_{VCC} reaches V_{VCC_OFF}, SY59525 begins to restart. After restart, SY59526 will recognize OTP signal after V_{VB_ON}, so even if temperature is always too high, MOSFET won't switching and system's heat is very low, there is no risk of overheating.

Magnetic Element Design

According to the design table, calculate the resonant inductor, resonant capacitor and boost capacitor. Left part of design table is one standard design with good performance, this topology has good normalized property, which means the resonant parameters is related to output current I_O, resonant frequency f_r and maximum output voltage V_{O_MAX}.

Inductor

System works in LC resonant condition, the peak value and RMS value of resonant current can be calculated:

$$I_{r\_peak} = 2 \times I_O / N_{ps}$$

$$I_{RMS} = \frac{I_{r\_peak}}{\sqrt{3}}$$

Usually select B_{max_ind} between 0.2 and 0.3, so turn number of inductor can be calculated:

$$n_{ind} = \frac{I_{r\_peak} \times L_r}{A_{e\_ind} \times B_{max\_ind}}$$

It's recommended to use litz wire for lower temperature rise. Current density j_{ind} is selected at 8A/mm², so the number of 0.1mm enameled wire n_{litz} can be calculated:

$$n_{litz} = \frac{4 \times I_{RMS}}{\pi \times j_{ind} \times 0.1^2}$$

Transformer

RMS value of primary winding current is the same as inductor, so the wire diameters of primary and secondary winding are easy to get. Usually select B_{max_trans} as 0.3, and the turn number of primary winding can be calculated:

$$n_{p\_trans} = \frac{V_{O\_MAX} \times n_{ps}}{4 \times f_r \times B_{max\_trans} \times A_{e\_trans}}$$

$$n_{s\_trans} = \frac{n_{s\_trans}}{n_{ps}}$$

The auxiliary winding should satisfy the following conditions:

$$V_{O\_OLP} + V_D = \frac{N_S}{N_{AUX}} \times \left(V_{VCC\_OVP} + V_D\right)$$

$$\left(V_{O\_MIN} + V_D\right) \times \frac{N_{AUX}}{N_S} - V_D > 13V$$

No air gap is required for transformer cores, large inductance of primary winding is needed, it's suggested that the ratio of inductance of primary winding and resonant inductor be larger than 3. If the ratio is small, it needs to change the bobbin and core size of inductor or transformer.

Magnetic integrated design

It's recommended to use magnetic integrated design for better efficiency and power density. In this design, leakage inductance of transformer primary winding is used as resonant inductor, so the key of magnetic integrated design is the control of leakage inductance. Fig.6 shows the structure of magnetic integrated transformer, primary and secondary windings are placed at left side and right side, respectively, between them is a big gap for larger leakage inductance. Leakage inductance mainly depends on the turn number of primary winding, bobbin size and the big gap in the middle. Red line represents the leakage inductance of primary winding, which is equivalent to the role of resonant inductor, and the green line represents the transformer excitation loop.

In magnetic integrated design, usually it's no need to consider the inductance ratio between primary winding and resonant inductor, because the bobbin size of transformer becomes larger than discrete design, the excitation inductance is much larger.

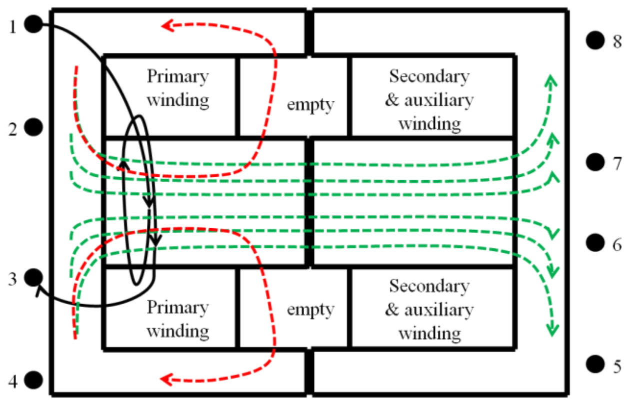


Fig.6 Structure of Magnetic Integrated Transformer

Layout

(a) Because of the charge pump structure, it's not necessary to put the input E-cap close to bridge rectifier. Make sure the loop composed of input E-cap, HV of SY59526, HB of SY59526, HB of SY59525 and GND of SY59525 to be as small as possible.

(b) The circuit loop of CS sampling should be kept small.

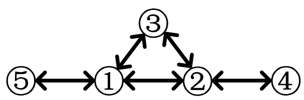
(c) The C_{VB} charge loop should be kept small, C_{VB} should be put near SY59526.

(d) The C_{VCC} and N_{AUX} charging loop should be kept small, C_{VCC} should be put near SY59525.

(e) Not recommend to put high voltage track under low voltage components, such as HV and LX.

(f) Recommend to use a high voltage MLCC in parallel with input E-cap, recommend to connect the core of inductor to low frequency input line after filter.

(g) The connection of ground is recommended as:



Ground ①: ground of input E-cap

Ground ②: ground of SY59525 and C_{VCC}

Ground ③: ground of external high voltage NP0 MLCC

Ground ④: ground of auxiliary winding

Ground ⑤: ground of bridge rectifier and C_{boo}

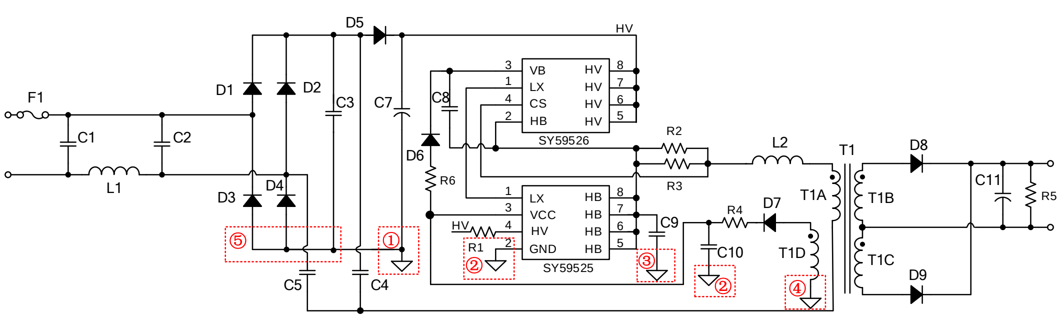


Fig.7 Ground Connection Recommended

Design Example

Table 1 and table 2 show the key parameters of standard design in design table and parameters defined by the customer, respectively. The relationship between them is also provided.

Table 1 Key Parameters of Standard Design

System Conditions		
Maximum Output Voltage	$V_{O\_MAX\_S}$	42V
Output Current	I_{O_S}	1A
Output Diode Drop	V_{DF_S}	1.3V
Main Resonant Frequency	f_{r_S}	52.5kHz
Key Parameters		
Turns Ratio	N_{PS_S}	1.75
Sampling Resistor	R_{CS_S}	0.26Ω
Resonant Inductor	L_{r_S}	700uH
Main Resonant Capacitor	C_{r_S}	27nF
Minor Resonant Capacitor	C_{r2_S}	3.3nF
Boost Capacitor	C_{boost_S}	15nF
Input E-cap	C_{in_S}	15uF

Table 2 Parameters Defined by Customer

System Conditions		
Maximum Output Voltage	$V_{O\_MAX\_C}$	40V
Output Current	I_{O_C}	0.8A
Output Diode Drop	V_{DF_C}	1.3V
Main Resonant Frequency	f_{r_C}	70kHz
Key Parameters		
Turns Ratio	N_{PS_C}	1.83
Sampling Resistor	R_{CS_C}	0.34Ω
Resonant Inductor	L_{r_C}	689uH
Main Resonant Capacitor	C_{r_C}	15.4nF
Minor Resonant Capacitor	C_{r2_C}	1.9nF
Boost Capacitor	C_{boost_C}	8.6nF
Input E-cap	C_{in_C}	11uF

$$N_{PS\_C} = N_{PS\_S} \times \frac{V_{O\_MAX\_S} + V_{DF\_S}}{V_{O\_MAX\_C} + V_{DF\_C}}$$

$$R_{CS\_C} = 0.15 \times \frac{N_{PS\_C}}{I_{O\_C}}$$

$$L_{r\_C} = L_{r\_S} \times \frac{V_{O\_MAX\_S} \times I_{O\_S} \times f_{r\_S}}{V_{O\_MAX\_C} \times I_{O\_C} \times f_{r\_C}}$$

$$C_{r\_C} = C_{r\_S} \times \frac{V_{O\_MAX\_C} \times I_{O\_C} \times f_{r\_S}}{V_{O\_MAX\_S} \times I_{O\_S} \times f_{r\_C}}$$

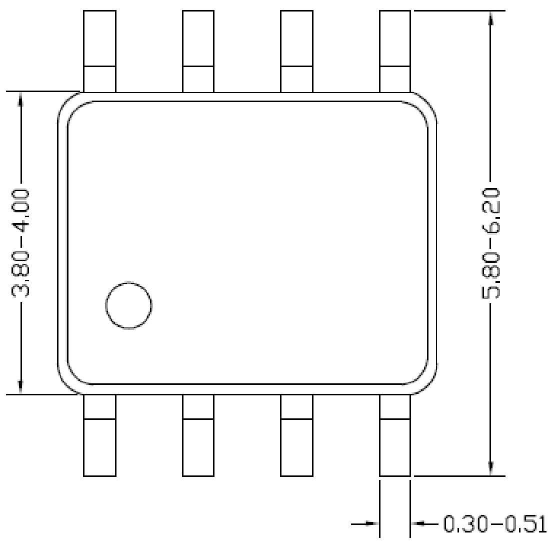
$$C_{r2\_C} = C_{r2\_S} \times \frac{V_{O\_MAX\_C} \times I_{O\_C} \times f_{r\_S}}{V_{O\_MAX\_S} \times I_{O\_S} \times f_{r\_C}}$$

$$C_{boost\_C} = C_{boost\_S} \times \frac{V_{O\_MAX\_C} \times I_{O\_C} \times f_{r\_S}}{V_{O\_MAX\_S} \times I_{O\_S} \times f_{r\_C}}$$

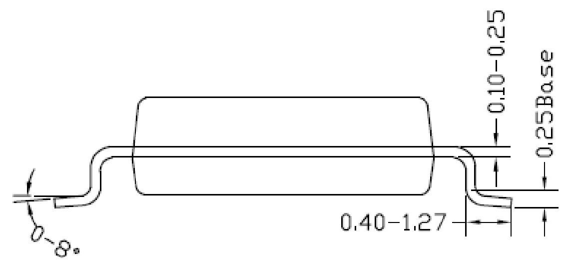
$$C_{in\_C} = C_{in\_S} \times \frac{V_{O\_MAX\_C} \times I_{O\_C}}{V_{O\_MAX\_S} \times I_{O\_S}}$$

$V_{O\_MAX\_C}$, I_{O_C}, V_{DF_C} and f_{r_C} are defined by customer, and other key parameters will be calculated according to the above normalization formula.

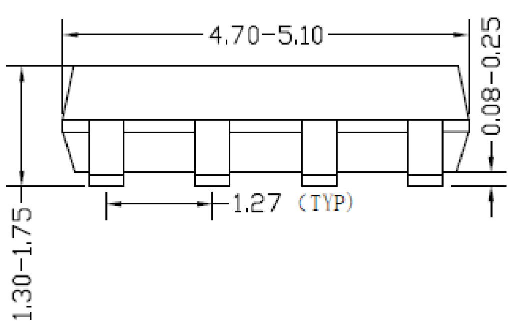
SO8 Package outline & PCB layout design



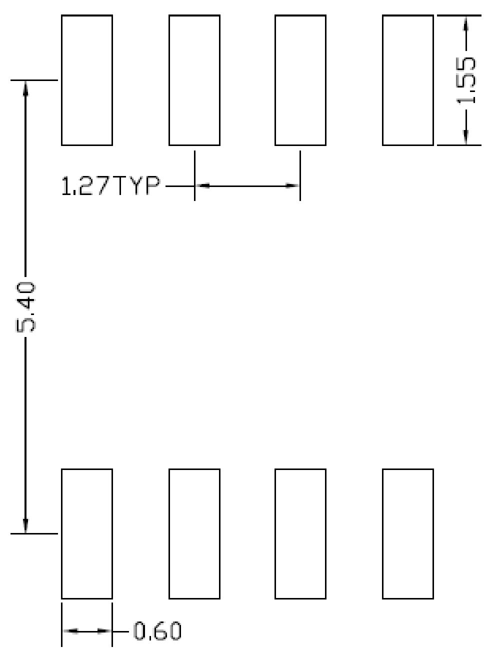
Top view



Side view



Front view

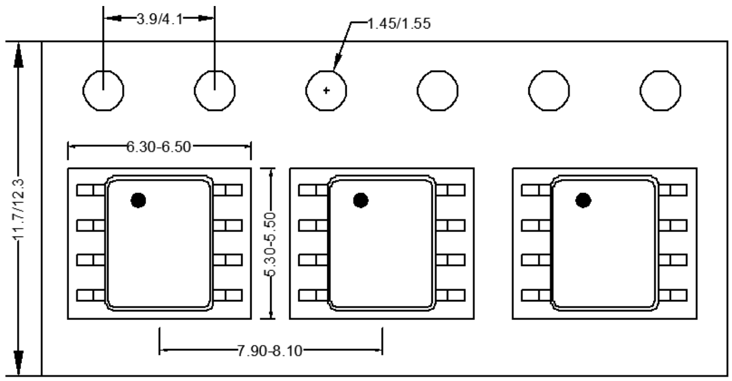


Recommended Pad Layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

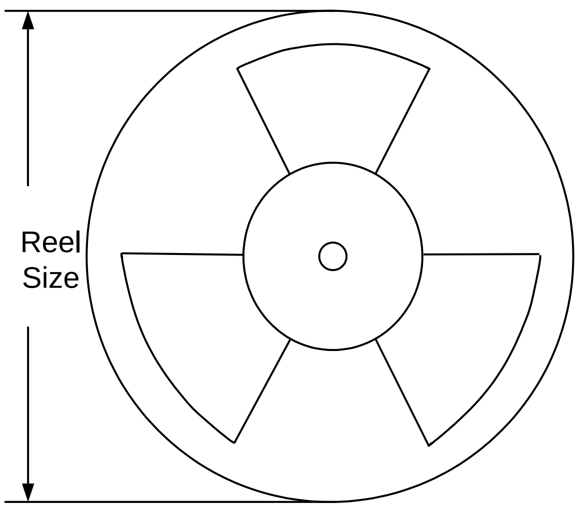
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 11, 2024	Revision 1.0	Initial Release

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