

General Description

The SY24640 is a current sensing comparator with over-current protection and used for the over-current protection applications.

It measures the voltage developed across a shunt resistor and compares this voltage with an externally configured threshold. Independent of the supply voltage, the common voltage range of SY24640 is between 0V to 36V and the differential input range from 0mV to 250mV. An open drain alert output can be configured to operate in either transparent mode or latched mode. The device response time setting is selectable, which allows over-current alerts to be issued within 10 μ s.

The SY24640 operates from a single 2.7V to 5.5V supply, drawing a typical supply current of 135 μ A. The device is provided in DFN2x2-10 and MSOP10 packages, and is specified over the extended operating temperature range of -40 $^{\circ}$ C to +125 $^{\circ}$ C.

Features

- Wide Common Mode Range: 0V ~ 36V
- Accuracy:
 - Offset Voltage: $\pm 500\mu$ V (Max)
 - Offset Voltage Drift: 0.5 μ V/ $^{\circ}$ C (Max)
- Programmable Threshold:
 - Adjust Using Single Resistor
 - Programmable from 0 mV to 250 mV
- Active Quiescent Current: 135 μ A (Typ)
- Selectable Disable Mode
 - Disabled Quiescent Current: 1.2 μ A (Max)
 - Disabled Input Bias Current: 500nA (Max)
- Three Selectable Response Times: 10 μ s, 50 μ s, 100 μ s
- Three Selectable Hysteresis: 2 mV, 4 mV, 8 mV
- Open Drain Output with Latch Mode Available
- Packages: DFN2x2-10 and MSOP10

Applications

- Over-current Protection
- Computers
- Servers
- Telecom Equipment
- Power Supplies
- Battery Chargers

Typical Application

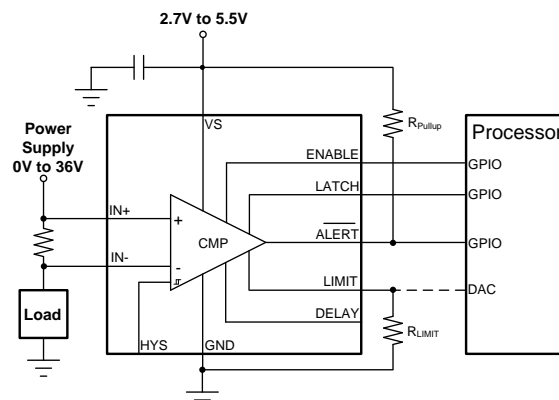


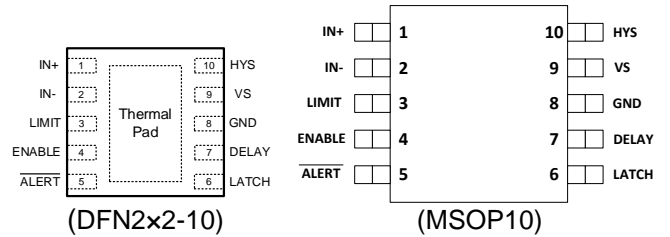
Figure 1. Typical Application

Ordering Information

Ordering Part Number	Package type	Top Mark
SY24640TDD	DFN2x2-10	W2xyz
SY24640FBP	MSOP10	EAAxyz

x=year code, y=week code, z=lot number code

Pinout (Top View)



Pin Description

Pin Number	Pin Name	Function Description
1	IN+	Connect to supply side of shunt resistor.
2	IN-	Connect to load side of shunt resistor.
3	LIMIT	Alert threshold limit input.
4	ENABLE	Enable or disable selection input.
5	$\overline{\text{ALERT}}$	Over-limit alert, active-low, open-drain output.
6	LATCH	Transparent or latch mode selection input.
7	DELAY	Response time selection input.
8	GND	Ground.
9	VS	Power supply, 2.7 V to 5.5 V.
10	HYS	Hysteresis setting input.
Thermal pad	DFN2x2-10 Only	This pad can be connected to ground or left floating.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VS	-0.3	6	V
Differential $V_{IN+} - V_{IN-}$	-40	40	
Common mode, V_{IN+}, V_{IN-}	-0.3	40	
Alert output V_{ALERT}	-0.3	6	
Input voltage at Any Pin	-0.3	VS+0.3	
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance(DFN2x2-10)	80	°C/W
θ_{JC} Junction-to-case Thermal Resistance(DFN2x2-10)	38	
P_D Power Dissipation $T_A = 25^\circ\text{C}$ (DFN2x2-10)	1.2	W
θ_{JA} Junction-to-ambient Thermal Resistance(MSOP10)	75	°C/W
θ_{JC} Junction-to-case Thermal Resistance(MSOP10)	37	
P_D Power Dissipation $T_A = 25^\circ\text{C}$ (MSOP10)	1.3	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Differential $V_{IN+} - V_{IN-}$	0	250	mV
VCC	2.7	5.5	V
Common mode, V_{IN+}, V_{IN-}	0	36	
Junction Temperature Range	-40	125	°C

Electrical Characteristics

At $T_A=25^{\circ}\text{C}$, $V_{IN}=V_{IN+}-V_{IN-}=0\text{mV}$, $V_S=3.3\text{V}$, $V_{IN+}=12\text{V}$, $V_{LIMIT}=10\text{mV}$, and $\text{DELAY}=100\mu\text{s}$, unless otherwise noted.

Parameter(Notes 4)	Symbol	Test condition	Min	Typ	Max	Units
Input						
Common Mode Input Voltage	V_{CM}		0		36	V
Differential Input Voltage	V_{IN}	$V_{IN}=V_{IN+}-V_{IN-}$	0		250	mV
Common Mode Rejection	CMR	$V_{IN}=0\text{V}\sim 36\text{V}$, $T_A=-40^{\circ}\text{C}\sim +125^{\circ}\text{C}$	110	120		dB
Offset Voltage, RTI	V_{OS}	$V_S=3.3\text{V}$, $\text{DELAY}=100\mu\text{s}$		-75	-500	μV
		$V_S=3.3\text{V}$, $\text{DELAY}=50\mu\text{s}$		-125	-500	
		$V_S=3.3\text{V}$, $\text{DELAY}=10\mu\text{s}$		-350	-650	
Offset Voltage Drift, RTI	dV_{OS}/dT	$T_A=-40^{\circ}\text{C}\sim +125^{\circ}\text{C}$		0.1	0.5	$\mu\text{V}/^{\circ}\text{C}$
Power Supply Rejection Ratio	PSR	$V_S=2.7\text{V}\sim 5.5\text{V}$, $V_{IN+}=12\text{V}$, $T_A=-40^{\circ}\text{C}\sim +125^{\circ}\text{C}$		5	60	$\mu\text{V}/\text{V}$
Input Bias Current (Note 5)	I_B			3.5	8	μA
		Disable mode		0.05	0.5	
Input Offset Current (Note 6)	I_{OS}			± 0.1		μA
Limit Threshold Output Current	I_{LIMIT}		19.85	20	20.15	μA
		$T_A=-40^{\circ}\text{C}\sim +125^{\circ}\text{C}$	19.8		20.2	
Digital Input / Output						
Alert Propagation Delay	t_p	Delay=open, overdrive=1mV (Note 7)		10		μs
		Delay=GND, overdrive=1mV		50		
		Delay=VS, overdrive=1mV		100		
Hysteresis	HYS	HYS=open		2		mV
		HYS=GND		4		
		HYS=VS		8		
High Level Input Voltage	V_{IH}	Latch, enable	1.4		6	V
		Delay, hysteresis	$V_S-0.5$		6	
Low Level Input Voltage	V_{IL}	Latch, enable	0		0.4	V
		Delay, hysteresis	0		0.5	
Alert Low Level Output Voltage	V_{OL}	$I_{OL}=3\text{mA}$		50	100	mV
ALERT Terminal Leakage Input Current		$V_{OH}=3.3\text{V}$		0.1	1	μA
Digital Leakage Input Current		Pin ENABLE, LATCH, DELAY and HYS, $0<V_{IN}<V_S$		1	2	μA
Power Supply						
Quiescent Current	I_Q	$V_{IN}=0\text{mV}$, $T_A=-40^{\circ}\text{C}\sim +125^{\circ}\text{C}$		135	155	μA
		$V_{IN}=0\text{mV}$, disable mode, HYS=2mV		0.6	1.2	
Timing Requirements						
Start-up Time				1		ms
Enable Time	t_{en}			150		μs
Disable Time	t_{dis}			20		μs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at $T_A=25^{\circ}\text{C}$ and chip mounted on low-effective four-layer thermal conductivity test board

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25°C ; limits at -40°C to $+125^{\circ}\text{C}$ are guaranteed by design, test or statistical correlation.

Note 5: Input bias current is decided by the average of the input currents of the pin IN+ and IN-.

Note 6: Input offset current is decided by the error between the input currents of the pin IN+ and IN-.

Note 7: Overdrive = $V_{IN} - V_{LIMIT}$.

Application Information

Operation

The SY24640 is a comparator combines both the current-sense amplifier and threshold comparison into a single product designed specifically for over-current protection applications. The device features a 0V to 36V common-mode which is independent of its supply voltage in applications that use low-side or high-side configurations. The comparison threshold can be set by a single external resistor, which can simplify the circuit design. Therefore, it can allow easy adjustments to the threshold when needed. The value of the threshold setting resistor is selected based on an internal 20 μ A current source.

The device is designed to meet the broader application needs, and it puts forward higher requirements for some parameters, including common modulus voltage, noise threshold and signal range. This device can provide a wide signal threshold range of up to 250 mV, which is available to reduce the power dissipated on current sensing resistor and allows for the use of larger current sensing resistors in lower current applications.

Other features provided by the SY24640 include the disable mode which can reduce the current of the device to less than 10 μ A, the output mode selector for enable the latched or transparent alert output, the optional hysteresis value and alarm response delay.

The wide signal range of the device can be further enhanced by adjustable hysteresis values, thereby better adapting to the entire input range. The selectable alert response delays of the SY24640 helps optimize the device operation to achieve a better system noise level and working characteristics. Setting longer delays can increase the suppression of system noise, thus reducing the possibility of false alerts caused by noise spikes.

Current Limit Threshold Setting

The SY24640 will determine if there is an over-current event by comparing the measured voltage developed across the shunt resistor with the corresponding voltage configured in the LIMIT pin. Using a single external resistor, or connecting an external voltage source to the LIMIT pin can set the threshold voltage of the LIMIT pin.

Resistor Controlled Current Limit

One approach for setting the limit threshold voltage is to connect a resistor from the LIMIT pin to ground. An internal 20 μ A current source is connected to the LIMIT pin, and the corresponding threshold voltage of the LIMIT pin can be created by the value of this resistor R_{LIMIT} . This voltage is equivalent to the product of the maximum current expected to flow through the shunt resistor and the shunt resistor.

Voltage Source Controlled Current Limit

An alternate method for setting the over-current threshold is to connect the LIMIT pin to a programmable DAC (digital-to-analog converter) or other external voltage source. The benefit of this method is the ability to adjust the threshold, with the system operating conditions change.

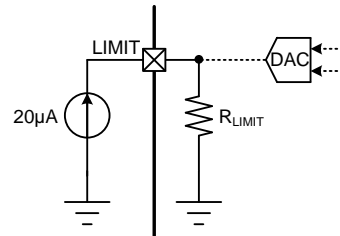


Figure 2. Voltage Source Controlled Current Limit

Delay Setting

The response time of this device can be adjusted according to the setting of the DELAY pin. It provides three response time settings, from 10 μ s to 100 μ s. The main purpose of the three different delay time is to provide a possibility of a weighing between the faster alarm response and the more accurate over-current threshold level detection.

This device has a 10 μ s comparison window. This comparison window is the basic time unit of three delay settings in the device. For 10 μ s delay settings, the device directly uses the average value of the input voltage during the 10 μ s comparison window to compare with the threshold voltage on the LIMIT pin. If the average input voltage exceeds the threshold at the end of the 10 μ s comparison window, the output alarm will trigger and the \overline{ALERT} pin will be pulled down. Conversely, if the average input will not exceed the threshold, the output alarm state does not change, and \overline{ALERT} pin will keep high levels indicating that the over-current event is not detected.

The implementation of the 50 μ s delay settings requires a counter as auxiliary. If the average input signal exceeds the threshold during the 10 μ s comparison window, the counter will be added; if the average input signal does not exceed the threshold, the counter will be reduced by one. When the counter reaches five, the output alarm will trigger and the \overline{ALERT} pin being pulled low. After the \overline{ALERT} pin is pulled down, once any 10 μ s comparison window fails to detect the over-current condition, the internal counter will be reset and the \overline{ALERT} pin will be pulled high.

The working method of 100 μ s delayed is the same as the 50 μ s method, but it is required that the counter will reach ten when the input signal exceeds the threshold, so that the alert output can be issued and the \overline{ALERT} pin be pulled low.

Successive over-current testing can help significantly reduce the possibility of false alerts caused by systemic noise, and the false alerts may be extremely unfavorable to the system operation. At the same time, by enabling the 10μs comparison window, the device can be still

flexibly used in high-speed over-current detection applications that require fast response and rapid change characteristics.

In Figure 3, the 10μs delay settings and 50μs delay settings based on the same input signal are displayed.

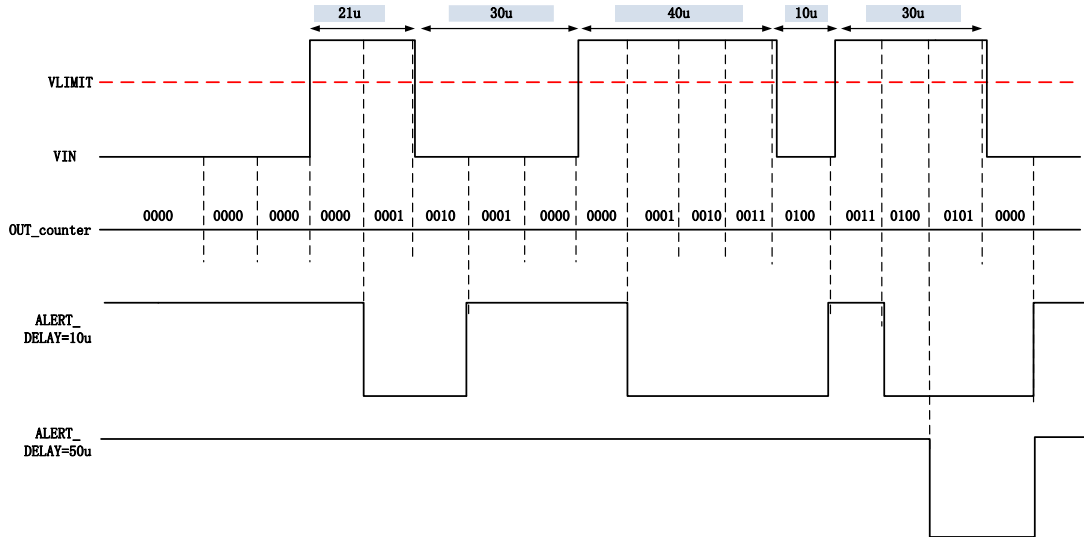


Figure 3. DELAY Terminal Settings

As mentioned above, the three different delay settings are configured according to the signal connected to the DELAY pin, as Figure 4 shown. The DELAY pin must be directly grounded, directly connected to the power, or completely float. The additional external resistance should not be connected here. If the application needs to connect the DELAY pin with the power supply or ground through the resistance, the resistance must be limited within 1kΩ to avoid conflicting with the internal level detection circuit.

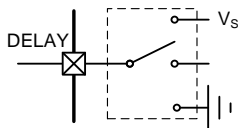


Figure 4. Delay Response

DELAY Pin	ALERT Delay Time (us)
Open or floating	10
GND	50
V _S	100

Hysteresis Setting

The hysteresis of the device can be adjusted according to the settings of the HYS pin. The minimum setting scale (2mV) on the device is achieved by keeping the HYS pin floating. Set a 4mV hysteresis by setting the HYS pin to ground; connecting this pin to the power supply voltage sets the hysteresis to 8mV, as shown in Figure 5. The HYS pin must be directly grounded, directly connected to the power, or completely float. The additional external resistance should not be connected

here. If the application needs to connect HYS pin to the power supply or ground through the resistance, the resistance must be limited within 1kΩ to avoid conflicting with the internal level detection circuit.

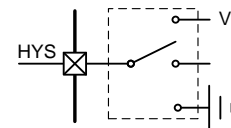


Figure 5. HYS Response

The dynamic input range of the SY24640 is very wide, so the adjustable hysteresis to ensure that it can be configured more appropriately according to specific working conditions and application requirements. Figure 6 shows the conversion level point of the ALERT pin.

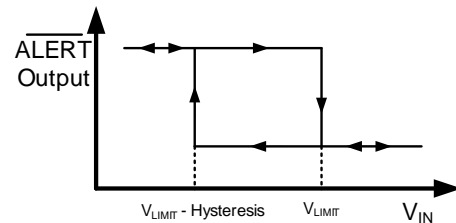


Figure 6. Typical Comparator Hysteresis

HYS Pin	Hysteresis Threshold (mV)
Open or floating	2
GND	4
V _S	8

Alert Output

The $\overline{\text{ALERT}}$ pin is an active-low, open-drain output that is designed to be pulled low when the measured voltage exceeds the configured threshold. This open-drain output pin should be connected to supply voltage through a 10k Ω pull-up resistor. The $\overline{\text{ALERT}}$ pin can be pulled up to a voltage beyond the supply voltage V_S , but the value must not exceed 5.5 V.

Alert Mode

Using the LATCH pin, the output can be configured to operate in either Transparent or Latch Mode, which is selected based on the LATCH pin setting. This will change the behavior of the alert output when the over-current condition is removed, as described in the following paragraphs.

Transparent Output Mode

The device will be set to Transparent Mode when the LATCH pin is pulled low. In this mode, the alert output changes state following the input signal with respect to the programmed alert threshold. For example, when the differential input signal rises above the alert threshold, the $\overline{\text{ALERT}}$ output pin will be pulled low. As soon as the differential input signal drops below the alert threshold, the output will return to the default high output state.

When connect the $\overline{\text{ALERT}}$ pin to a hardware interrupt input on a microcontroller, the output state change of the $\overline{\text{ALERT}}$ pin in Transparent Mode can be directly detected and over-current conditions can be handled.

Latch Output Mode

The Latch Mode is designed to accommodate applications which do not have the functionality available to continuously monitor the state of the output $\overline{\text{ALERT}}$ pin.

The device can be configured to operate in Latch Mode by connecting the LATCH pin to a high level. In this mode when an over-current condition is removed, the $\overline{\text{ALERT}}$ pin will not return to the default high state.

Only by pulling the LATCH pin low for at least 20 μs can clear the alert. When the input signal drops below the threshold, pulling the LATCH pin low then the $\overline{\text{ALERT}}$ pin can return to the default high level. If the input signal is still above the threshold limit when the LATCH pin is pulled low, the $\overline{\text{ALERT}}$ pin will remain low.

After processing the over-current condition, the external controller can return the device to Latch Mode by setting the LATCH pin to logic high.

The difference between latch mode and transparent mode is how the alert output will respond when an over-current event ends. In transparent mode, when the differential input signal drops below the limit threshold level for 10 μs , the output state will return to the default

high setting to indicate that the over-current event had ended.

The SY24640 is placed into the corresponding output mode by driving the voltage level at the LATCH pin, as shown in table.

Output Mode	Latch Terminal Setting
Transparent mode	LATCH = low
Latch mode	LATCH = high

The $\overline{\text{ALERT}}$ pin behavior is shown in Figure 7 for the Latch and Transparent Modes.

When V_{OUT} drops below the V_{LIMIT} Hysteresis threshold for the first time, the LATCH pin will be pulled high.

When the LATCH pin is pulled high, the device will be set to Latch mode. In this mode the alert output state will not return to high when the V_{OUT} drops below the V_{LIMIT} .

When the LATCH pin is pulled low, the $\overline{\text{ALERT}}$ pin will return to the default high level, indicating that the V_{OUT} is below the V_{LIMIT} . When the V_{OUT} drops below the V_{LIMIT} for the second time, the LATCH pin will be already pulled low. The device will be set to Transparent Mode at this point, and the $\overline{\text{ALERT}}$ pin will be pulled back high as soon as the V_{OUT} drops below the V_{LIMIT} .

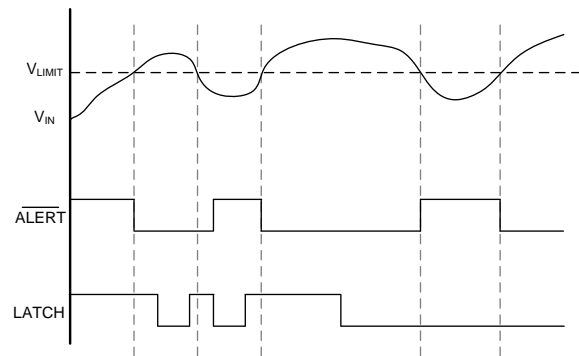


Figure 7. Transparent versus Latch Mode

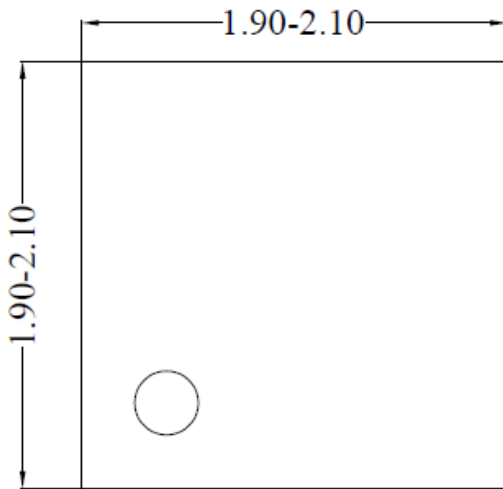
Disable Mode

The SY24640 has an ENABLE pin that allows setting the device to an enable state or a low power disabled state, and the total power consumption of all pins in the disable state is less than 10 μA . This disabled state allows this device to be used for applications that require extremely low current consumption to extend the life of batteries in the scenario that does not require continuous monitoring.

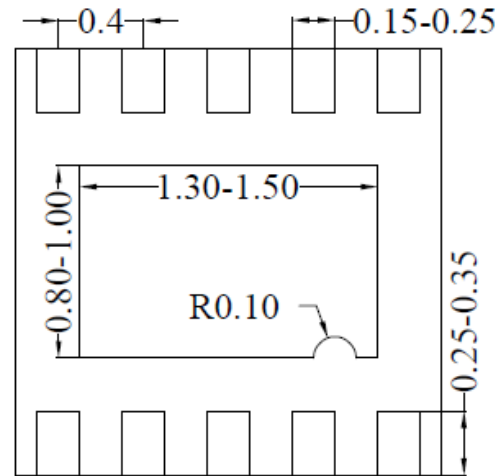
As shown in the table, when the ENABLE pin is converted from high level to low, the device will require about 20 μs to enter a low power consumption state. In order to return to the state of working, the ENABLE pin must be converted from a low level to a high. At this time, the device will require about 300 μs to exit the device with a low power consumption state and restore normal work.

Enable Mode	ENABLE Terminal Setting
Disable mode	ENABLE = low
Enable mode	ENABLE = high

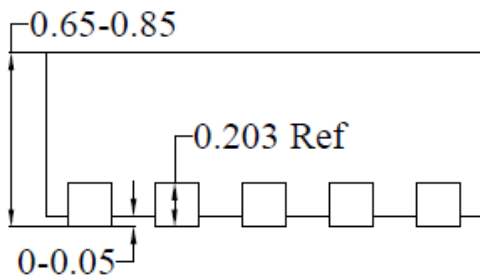
DFN2x2-10 Package Outline Drawing



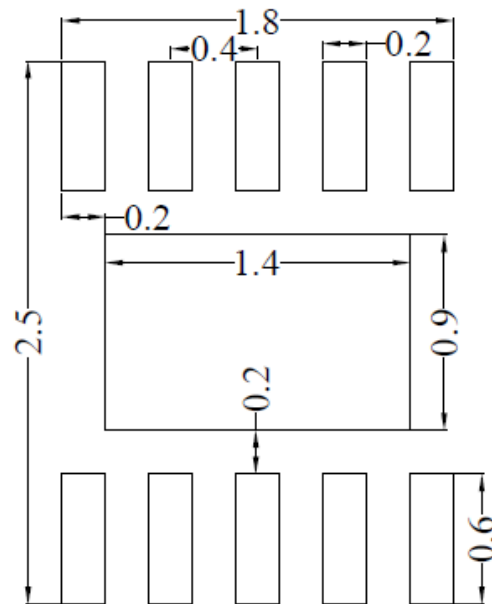
Top View



Bottom view



Bottom View

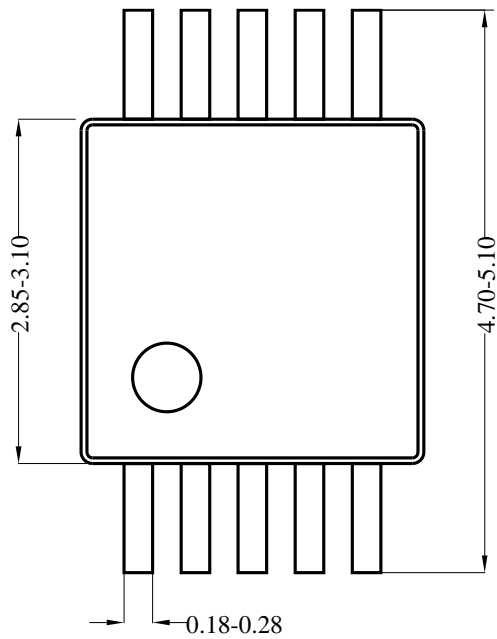


Recommended PCB layout

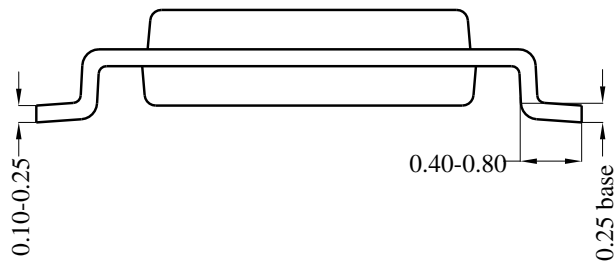
(Only for reference)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.

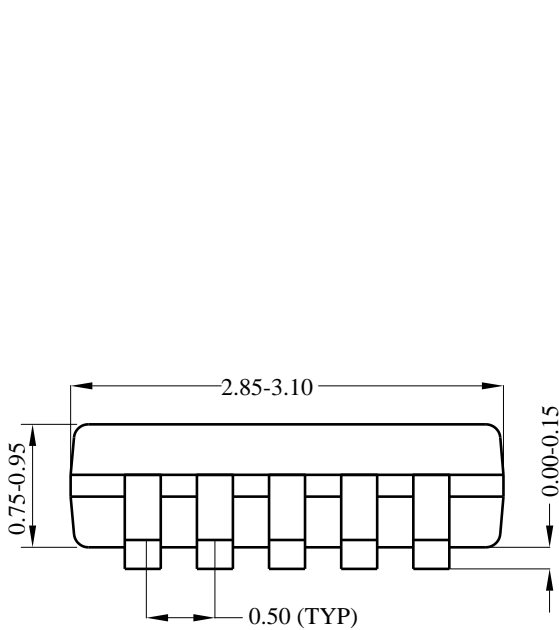
MSOP10 Package Outline & PCB Layout



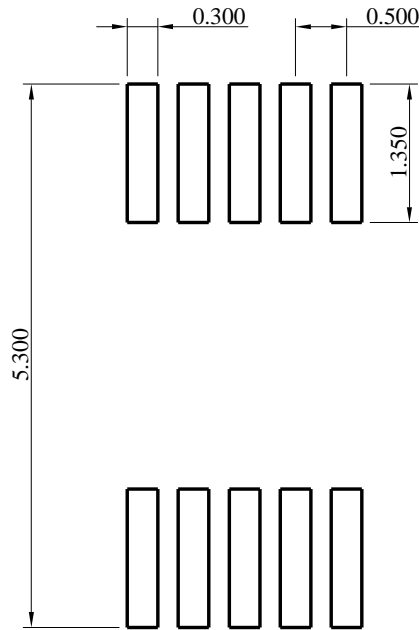
Top view



Side view



Front view



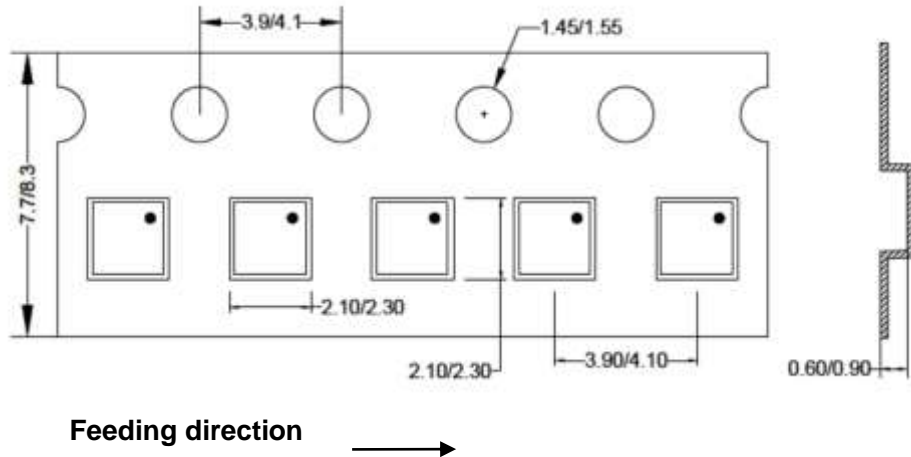
Recommended Pad Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

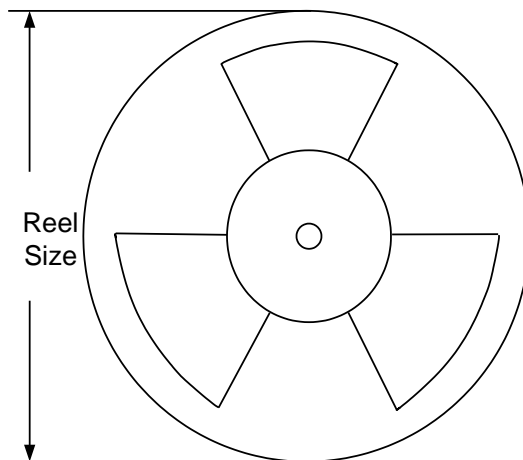
Taping & Reel Specification

1. Taping orientation

DFN2x2-10



2. Carrier Tape & Reel specification for packages



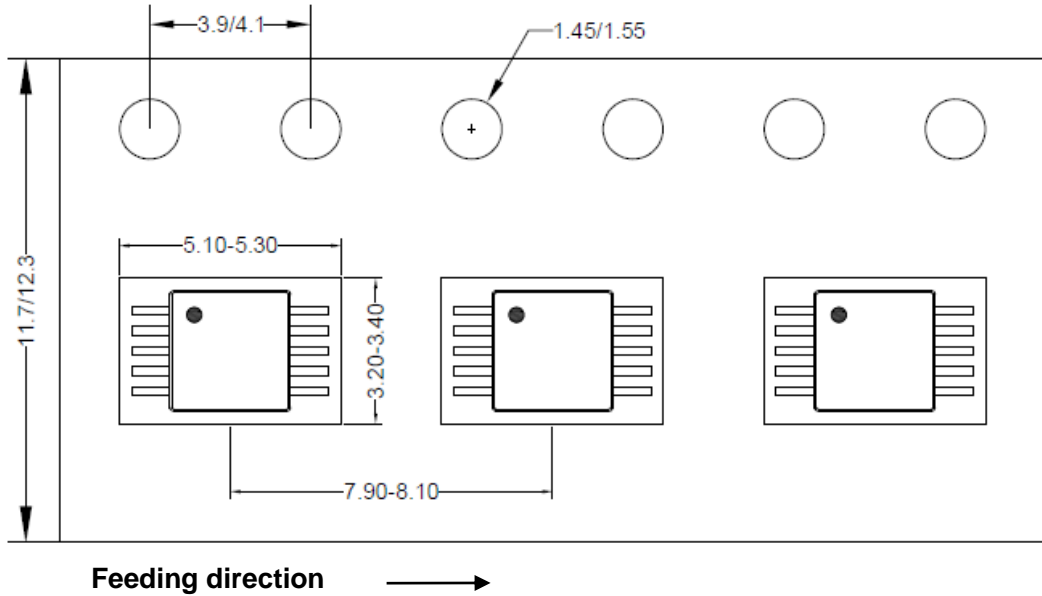
Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2-10	8	4	7"	400	160	3000

3. Others: NA

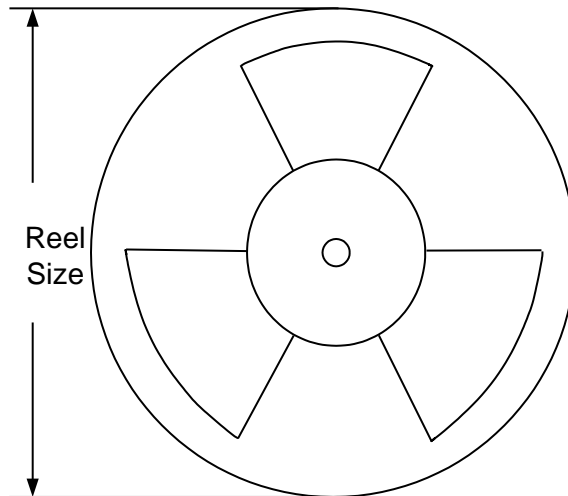
Taping & Reel Specification

1. Taping Orientation

MSOP10



2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

3. Others: NA



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Oct.9, 2021	Revision 0.9	Initial Release.
Apr.8, 2022	Revision 0.9A	Update the taping orientation in Taping & Reel Specification.
July 17, 2023	Revision 0.9B	Add new package MSOP10.
July 17, 2024	Revision 1.0	Production Release.

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