SQ52210

Triple-Channel, High-Side Measurement, Current and Power Monitor with I²C- and SMBUS-Compatible Interface

General Description

The SQ52210 is a three-channel high-side monitor designed for accurate measurement of current and power, featuring an interface compatible with both I²C and SMBus protocols. It supports simultaneous monitoring of voltage across the shunt resistor and bus supply voltage, with programmable conversion times and signal averaging options. A user-programmable calibration register, along with an integrated scaling factor, allows direct output of current in amperes and power in watts. The device also includes programmable alert functions for each channel, providing both critical and warning thresholds to signal out-of-range conditions.

The SQ52210 measures current on bus voltages ranging from 0V to 32.76V, regardless of the device's supply voltage. It supports a maximum common-mode voltage of up to 70V. Powered by a single supply between 2.7V to 5.5V, the device typically consumes 300µA of supply current. It is rated for operation across a temperature range of –40°C to +125°C and supports four programmable I²C-compatible addresses for flexible device configuration.

Features

- Power-Supply Operation: 2.7V to 5.5V
- Senses Bus Voltages From 0V to 32.76V
- 70V Common-Mode Voltage Tolerance
- Measures and Reports Current, Voltage, and Power
- High Measurement Precision:
  - Offset Voltage: ±40µV (max)
  - Gain Error: 0.25% (max)
- Configurable Averaging Modes
- Programmable Outputs for Warning and Critical Events
- Four Configurable I²C-Compatible Addresses
- MSL Rating: MSL3

Applications

- Power Management
- Computers
- Telecommunication Equipment
- Battery Chargers
- Power Supplies
- Test and Measurement Equipment

Typical Application

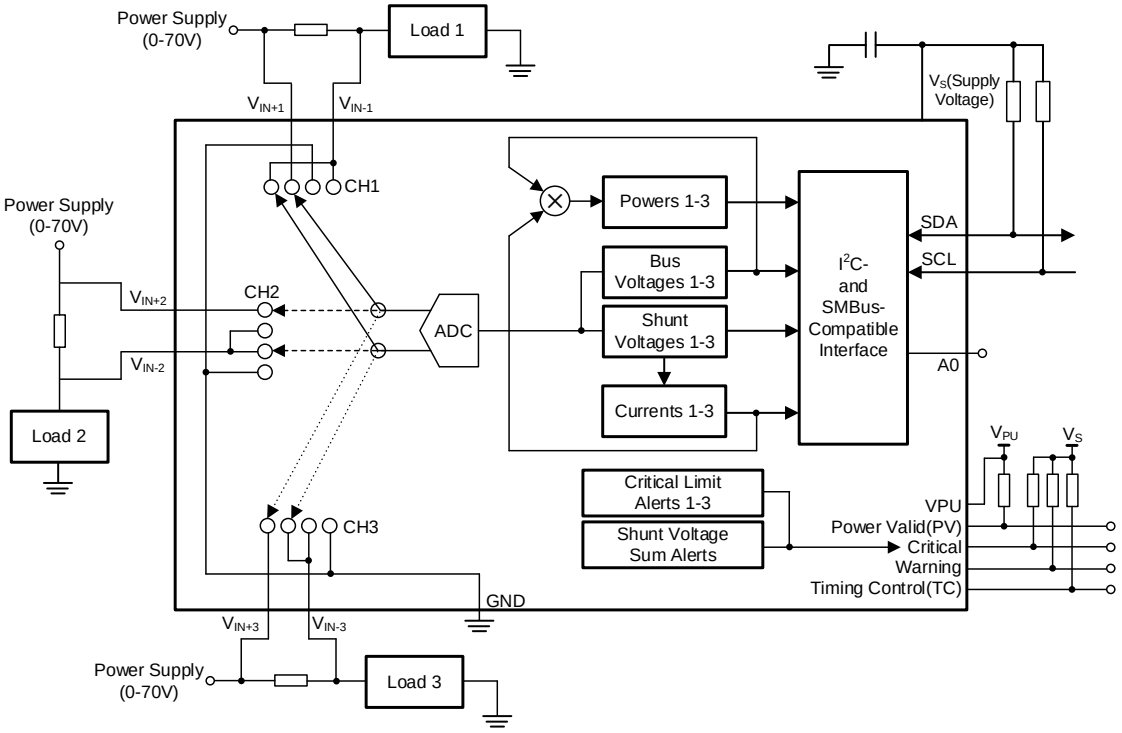


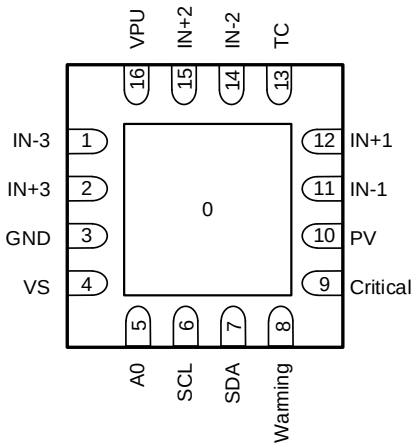
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ52210QIQ	QFN4×4-16	**HLB**xyz①

Note①： ***x=year code, y=week code, z= lot number code.***

Pinout (Top View)



(QFN4×4-16)

Pin Description

Pin No.	Pin Name	I/O	Pin Description
5	A0	Digital input	Address selection pin. Connect to GND, SCL, SDA, or VS. Refer to Table 11-1 for address configuration.
9	Critical	Digital output	Signals a critical condition triggered by conversion; open-drain.
0, 3	GND	Analog	Device ground reference.
11	IN–1	Analog input	Connects to the load side of the shunt resistor for Channel 1. Bus voltage is measured relative to ground.
12	IN+1	Analog input	Connects to the supply side of the shunt resistor for Channel 1.
14	IN–2	Analog input	Connect to load side of the Channel 2 shunt resistor. Bus voltage is the measurement from this pin to ground.
15	IN+2	Analog input	Connects to the supply side of the shunt resistor for Channel 2.
1	IN–3	Analog input	Connects to the load side of the shunt resistor for Channel 3. The bus voltage is measured relative to ground.
2	IN+3	Analog input	Connects to the supply side of the shunt resistor for Channel 3.
10	PV	Digital output	Power valid indication output; open-drain.
6	SCL	Digital input	Clock input line for the serial interface; open-drain.
7	SDA	Digital I/O	Serial bus data line; open-drain input/output.
13	TC	Digital output	Timing control alert; open-drain.
16	VPU	Analog input	Pull-up supply input used to bias the power valid output circuitry.
4	VS	Analog	Primary power supply. Supports 2.7V to 5.5V operation.
8	Warning	Digital output	Averaged measurement warning alert; open-drain.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VS	-0.3	6	V
SDA, SCL, A0, PV, TC, Critical, Warning	-0.3	6	
Differential Analog Input (V_{IN+} – V_{IN-})	-40	40	
Common Mode	-0.3	72	
Input Current (Any Pin)	-5	+5	mA
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	34	°C/W
θ_{JC} Junction-to-Case (top) Thermal Resistance	20.8	
θ_{JC} Junction-to-Case (bottom) Thermal Resistance	3.7	
θ_{JB} Junction-to-Board Thermal Resistance	13.4	
ψ_{JB} Junction-to-Board Characterization Parameter	13.2	
P_D Power Dissipation T_A = 25°C	2.94	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VS	2.7	5.5	V
Common Mode Analog Input	0	32.76	V
Operating Ambient Temperature	-40	125	°C

Electrical Characteristics

At T_A = 25°C, V_S = 3.3V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0V, V_{CM} = $V_{IN–}$ = 12V (Note 4) (unless otherwise noted).

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Shunt Voltage Input	V_{SHUNT}		-163.84		163.835	mV
Bus Voltage Input	V_{BUS}		0		32.76	V
Common-Mode Rejection	CMRR	V_{IN+} = 0 V to +32.76V	120	134		dB
Shunt Offset Voltage, RTI (Note 5)	V_{OS}			±8	±40	µV
		T_A = –40°C to +125°C		0.1	0.5	µV/°C
	PSRR	V_S Power Supply, V_S = 2.7V to 5.5V			±6	µV/V
Bus Offset Voltage, RTI (Note 5)	V_{OS}			±8	±16	mV
		T_A = –40°C to +125°C		10	80	µV/°C
	PSRR	V_S power supply, V_S = 2.7V to 5.5V		±3		mV/V
Input Bias Current	I_B	IN+, IN-, Current Measurement Mode		0.1	100	nA
Input Leakage (Note 6)	I_{B_SHDWN}	(IN+ pin) + (IN– pin), Power-Down Mode		0.1	100	nA
IN- Input Impedance	Z_{IN-}	Bus Voltage Measurement Mode		1		MΩ
DC Accuracy						
ADC Native Resolution				13		Bits
1-LSB Step Size		Shunt Voltage		40		µV
		Bus Voltage		8		mV
Shunt Voltage Gain Error				±0.02	±0.25	%
		T_A = –40°C to +125°C			40	ppm/°C
Bus Voltage Gain Error				±0.02	±0.25	%
		T_A = –40°C to +125°C			40	ppm/°C
Differential Nonlinearity	DNL			±0.2		LSB
ADC Conversion Time	t_{CT}	Conversion time field = 0h		140	154	µs
		Conversion time field = 1h		204	224	
		Conversion time field = 2h		332	365	
		Conversion time field = 3h		588	647	
		Conversion time field = 4h		1.1	1.21	ms
		Conversion time field = 5h		2.116	2.328	
		Conversion time field = 6h		4.156	4.572	
		Conversion time field = 7h		8.244	9.068	
SMBus						
SMBus Timeout (Note 7)				28	35	ms
Digital Input / Output						
Input Capacitance	C_I			3		pF
Leakage Input Current		0V ≤ V_{SCL} ≤ V_S, 0V ≤ V_{SDA} ≤ V_S, 0V ≤ $V_{Warning}$ ≤ V_S, 0V ≤ $V_{Critical}$ ≤ V_S, 0V ≤ V_{PV} ≤ V_S, 0V ≤ V_{TC} ≤ V_S		0.1	1	µA
Address Pin (A0) Bias Current		0V ≤ V_{A0} ≤ V_S		25		µA
High-level Input Voltage	V_{IH}		1.4		5.5	V
Low-level Input Voltage	V_{IL}		GND		0.4	V
Low-level Output Voltage	V_{OL}		0		0.4	V
Hysteresis Voltage	V_{hys}			200		mV
Power Supply						
Quiescent Current				300	350	µA
		Power-Down Mode		3.7	6	
Power-On Reset Threshold				2		V
I²C Bus (Fast Mode)						
I²C Clock Frequency	$f_{(SCL)}$		1		400	kHz
Bus Free Time between STOP and START Conditions	$t_{(BUF)}$		600			ns

Hold time after a repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$		100			ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$		100			ns
STOP Condition Setup Time	$t_{(SUSTO)}$		100			ns
Data Hold Time	$t_{(HDDAT)}$		100		900	ns
Data Setup Time	$t_{(SUDAT)}$		100			ns
SCL Clock Low Period	$t_{(LOW)}$		1300			ns
SCL Clock High Period	$t_{(HIGH)}$		600			ns
Data Fall Time	t_F				300	ns
Clock Fall Time	t_F				300	ns
Clock Rise Time	t_R				300	ns
I²C Bus (High-Speed Mode)						
I²C Clock Frequency	$f_{(SCL)}$		1		3000	kHz
Bus Free Time between STOP and START Conditions	$t_{(BUF)}$		160			ns
Hold time after a repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$		100			ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$		100			ns
STOP Condition Setup Time	$t_{(SUSTO)}$		100			ns
Data Hold Time	$t_{(HDDAT)}$		100		125	ns
Data Setup Time	$t_{(SUDAT)}$		20			ns
SCL Clock Low Period	$t_{(LOW)}$		200			ns
SCL Clock High Period	$t_{(HIGH)}$		60			ns
Data Fall Time	t_F				80	ns
Clock Fall Time	t_F				40	ns
Clock Rise Time	t_R				40	ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured on a low-efficiency single-layer PCB with natural convection.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: RTI = Referred-to-input.

Note 6: Input leakage is positive (current flows into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

Note 7: SMBus timeouts in the SQ52210 reset the interface whenever SCL is low for more than 28ms.

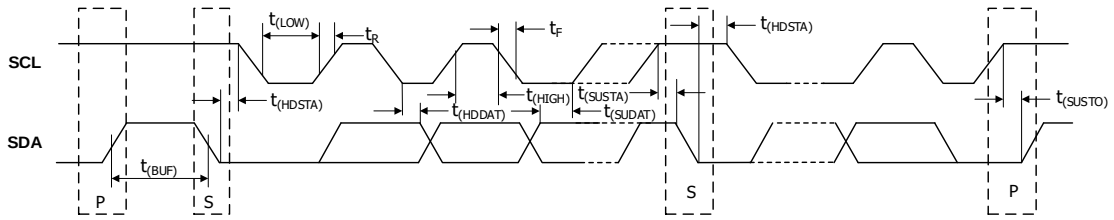


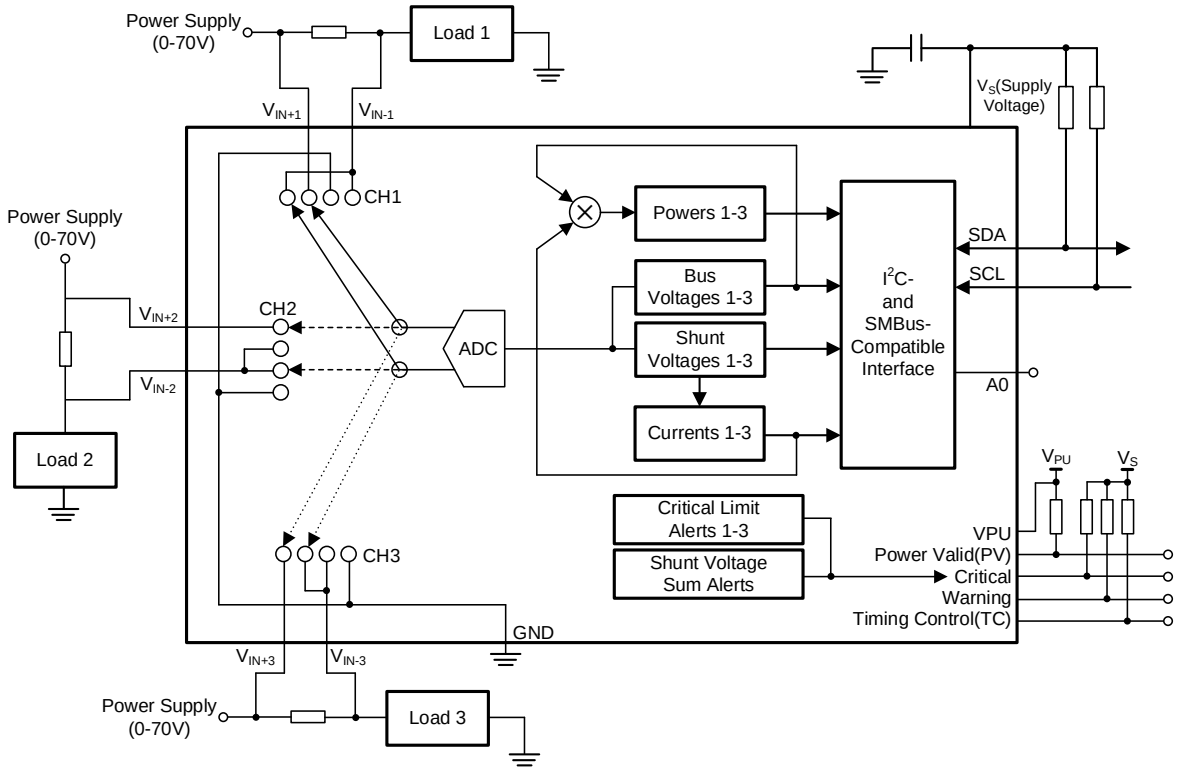
Figure 2. I²C Timing Diagram

Detailed Description

Overview

The SQ52210 is a multichannel digital current-sense amplifier that supports I²C and SMBus-compatible communication. It reports current, voltage, and power for each channel, and includes programmable out-of-range limits to trigger alerts when specified parameters exceed their normal operating range. The integrated analog-to-digital converter (ADC) offers configurable averaging modes and can be set for either continuous or triggered operation.

Functional Block Diagram



Feature Description

The SQ52210 is designed to perform two measurements on up to three power supply rails. The shunt voltage, generated by the load current passing through a shunt resistor, is measured between the IN+ and IN- pins. Additionally, the device internally measures the power-supply bus voltage at the IN- pin for each channel. The shunt voltage is measured differentially with respect to the IN- pin, while the bus voltage is measured with respect to ground.

To power the SQ52210, a separate power supply with a voltage range of 2.7V to 5.5V is typically used. The monitored supply buses can have voltages ranging from 0V to 32.76V.

There are no specific sequencing requirements between the common-mode input ranges and the device power-supply voltage since they are independent. This means that the bus voltages can be present even when the supply voltage is off, and vice versa.

The SQ52210 performs two measurements for each channel: one for shunt voltage and one for bus voltage. These measurements can be performed independently or sequentially based on the mode setting specified in bits 2-0 in the Configuration register. In the normal operating mode (MODE bits set to 111), the device continuously converts a shunt-voltage reading followed by a bus-voltage reading. This conversion process starts with one enabled channel, moves on to the next enabled channel, and continues until all enabled channels have been measured. The measurement cycle proceeds sequentially through all active channels, bypassing any that are disabled, regardless of the mode setting. The MODE setting is uniformly applied across all channels.

The SQ52210 offers two operating modes: continuous and single-shot. The mode determines the internal ADC operation after the conversions are completed. In continuous mode, the device cycles through all enabled channels until a new configuration setting is programmed.

The Configuration register MODE control bits also allow for the selection of modes that convert only the shunt or bus voltage. This feature enables the device to meet specific application requirements.

In single-shot (triggered) mode, selecting any of the single-shot conversion options in the Configuration register (MODE bits set to 001, 010, or 011) initiates a single-shot conversion. This operation generates a single set of measurements for all enabled channels. To initiate another single-shot conversion, the Configuration register must be rewritten regardless of whether the mode setting is changed. When a single-shot conversion is triggered, the device performs one complete measurement cycle for all enabled channels before transitioning into a power-down state. The SQ52210's internal registers remain accessible at all times, including during power-down, and retain the results from the most recent completed conversion. To aid in synchronizing single-shot operations, especially when extended conversion times are used, the conversion-ready flag bit (CVRF) in the Mask/Enable register is provided. This flag is asserted once all conversions have been finalized and is cleared under the following conditions:

1. When the Configuration register is written to, except when setting the MODE bits to enter power-down mode.
2. Upon reading the Mask/Enable register.

In addition to continuous and single-shot modes, the SQ52210 includes a configurable power-down mode designed to lower quiescent current and turn off current into the SQ52210 inputs. This mode minimizes supply drain when the device is not in use. The device requires 140µs to return to full operation after exiting power-down mode. While in power-down mode, all internal registers remain accessible for both read and write operations. The device remains in power-down mode until one of the active MODE settings is written to the Configuration register.

Alert Monitoring

Critical Alert

The critical-alert function evaluates each shunt-voltage channel independently, triggering alerts based on individual conversion results. By comparing the shunt-voltage conversion of each channel to the value programmed in the corresponding limit register, the critical-alert limit feature determines if the measured value exceeds the set limit. If the programmed limit is exceeded, it indicates that the current passing through the shunt resistor is too high.

Upon power-up, the default critical-alert limit value for each channel is set to the positive full-scale value, effectively disabling the alert. To start monitoring for out-of-range conditions, program the corresponding limit registers at any time. When any channel measurement exceeds the limit specified in its corresponding critical-alert limit register, the Critical alert pin goes low. To identify the channel that triggered the critical alert flag indicator bit (CF1-3) to assert (= 1), you can read the Mask/Enable register.

Additionally, the SQ52210 allows the Critical alert pin to be controlled by the summation control function. This function calculates the sum of the shunt-voltage conversions for the selected channels (determined by SCC1-3 in the Mask/Enable register) and compares it to the programmed limit.

The SCC bits are used to either disable the summation control function or allow it to include two or three channels in the Shunt-Voltage Sum register. The programmed limit value in the Shunt-Voltage Sum Limit register is compared to the value in the Shunt-Voltage Sum register to determine if the total summed limit has been exceeded. If the shunt-voltage sum limit value is surpassed, the Critical alert pin will go low.

The Critical alert pin can be controlled by the user-defined event. If the SLOWALERT bit in the Alert Configuration register is set to 0, the events set by bits 4 to 15 in the Alert Configuration register will trigger the Critical alert function.

The source of the alert when the critical alert pin goes low can be determined by either the summation alert flag indicator bit (SF) or the individual critical alert limit bits (CF1-3) in the Mask/Enable register and alert function flag (AFF1-3) in the Alert Configuration register.

For the summation limit to have a meaningful value, it is important to use the same shunt-resistor value for all included channels. If different shunt-resistor values are used for each channel, this function should not be used to directly add the individual conversion values together in the Shunt-Voltage Sum register to report the total current.

Warning Alert

The warning alert feature of the device monitors the average value of each shunt-voltage channel. The averaged value of each channel is determined based on the number of averages set using the averaging mode bits (AVG1-3) in the

Configuration register. Whenever there is a conversion on the corresponding channel, the averaged value is updated in the shunt-voltage output register. To determine if the averaged value exceeds the programmed limit in the corresponding channel Warning Alert Limit register, indicating a high average current, the device performs a comparison.

Upon power-up, each channel's warning-limit threshold is initialized to the positive full-scale value, effectively disabling the alert function by default. To enable monitoring for out-of-range conditions, the respective Warning Alert Limit registers must

be configured. When a channel's measurement exceeds its programmed threshold, the Warning alert output is asserted low.

The Warning alert pin can be controlled by the user-defined event. If the SLOWALERT bit in the Alert Configuration register is set to 1, the events set by the 15-4 bit in the Alert Configuration register can trigger the Warning alert function.

When the Warning alert output is driven low, the source channel can be identified by checking the warning flag indicator bits (WF1-WF3) in the Mask/Enable register. Additional confirmation can be obtained using the alert function flag bits (AFF1-3) in the Alert Configuration register.

Power-Valid Alert

The power-valid alert function ensures that all power rails meet minimum voltage requirements. It supports power sequencing management and validates measurement integrity according to system configuration. Upon power-up, the device automatically enables power-valid mode, monitoring each channel to ensure voltages exceed a 10V threshold. This default threshold is pre-programmed into the Power-Valid Upper-Limit register but can be reprogrammed once the SQ52210 is operating with a valid supply voltage of at least 2.7V.

When all three bus-voltage measurements meet or exceed the threshold programmed in the Power-Valid Upper-Limit register, the power-valid (PV) alert pin is set to high-impedance. Initially, the PV alert pin remains in a low state and only transitions to a high state when the power-valid conditions are met. This high state indicates that all bus-voltage rails are operating above the power-valid upper-limit value. Figure 3 illustrates the sequence of this operation.

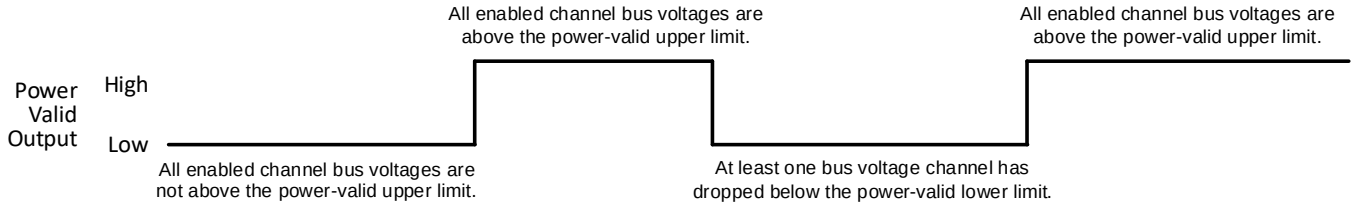


Figure 3. Power-Valid State Diagram

Once the power-valid conditions are met and the PV pin is pulled high, the SQ52210 continuously monitors if any bus-voltage measurements fall below 9V. By default, this threshold value is programmed into the Power-Valid Lower-Limit register. However, this value can be reprogrammed when the SQ52210 powers up with a supply voltage of at least 2.7V. If any of the bus-voltage measurements on the three channels drop below the value stored in the Power-Valid Lower-Limit register, the PV pin goes low, indicating that the power-valid condition is no longer satisfied. At this stage, the SQ52210 continues monitoring the power rails to verify compliance with the threshold defined in the Power-Valid Upper-Limit register.

The power-valid alert function requires all three channels to reach the threshold value programmed in the Power-Valid Upper-Limit register. If fewer than three channels are used, IN- pin of any unused channel must be externally tied to one of the active channels to enable proper operation of the power-valid alert. If the unused channel is not connected to a valid rail, the power-valid alert function cannot detect whether all three channels have reached the power-valid level. In such cases, it is recommended to leave the unused channel's IN+ pin floating.

Furthermore, the power-valid function necessitates monitoring the bus-voltage measurements. To detect any changes in the power-valid state, enable the bus-voltage measurements by selecting one of the corresponding MODE-bit settings in the Configuration register. The single-shot bus-voltage mode periodically cycles through the bus-voltage measurements to ensure that the power-valid conditions are met.

After completing all three bus-voltage measurements, the device evaluates the results against the power-valid threshold settings to determine the system's power-valid state. Each bus-voltage reading is stored in its respective channel output register until the next set of bus-voltage measurements are taken, thereby updating the output registers. Upon each update, the new values are again compared to the programmed power-valid thresholds. Without periodically taking bus-voltage measurements, the SQ52210 cannot confirm whether power-valid conditions persist.

Timing-Control Alert

The timing-control alert function in the SQ52210 is designed to verify proper power supply sequencing. Upon power-up, the device defaults to continuous conversion mode for both shunt and bus voltages. Internally, the SQ52210 monitors the bus voltage of Channel 1, comparing it against a 1.2V threshold each time Channel 1's bus voltage measurement is taken. Once Channel 1 reaches or exceeds 1.2V, the device proceeds to evaluate the bus voltage of Channel 2, checking for a 1.2V level or higher.

If, after completing four full cycles of all three channels, the SQ52210 does not detect a value of 1.2V or greater on the bus voltage measurement of Channel 2 following the detection of a 1.2V level on Channel 1, the timing control (TC) alert pin is pulled low. This indicates that the SQ52210 has not identified a valid power rail on Channel 2. As shown in Figure 4, the sequence described allows for approximately 28.6ms from the moment a 1.2V level is detected on Channel 1 for a valid voltage to be detected on Channel 2. The state diagram for the TC alert pin is illustrated in Figure 5.

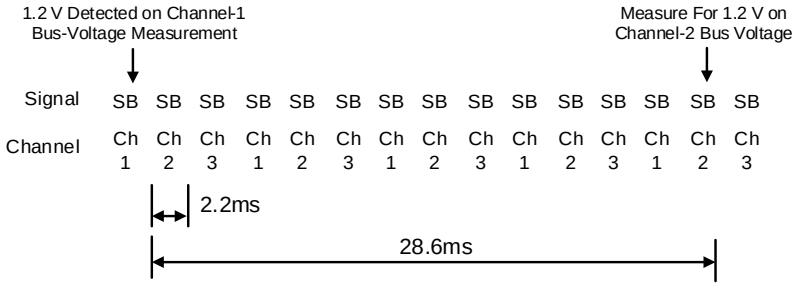


Figure 4. Timing Control Timing Diagram

NOTE: The signal refers to the corresponding shunt (S) and bus (B) voltage measurement for each channel.

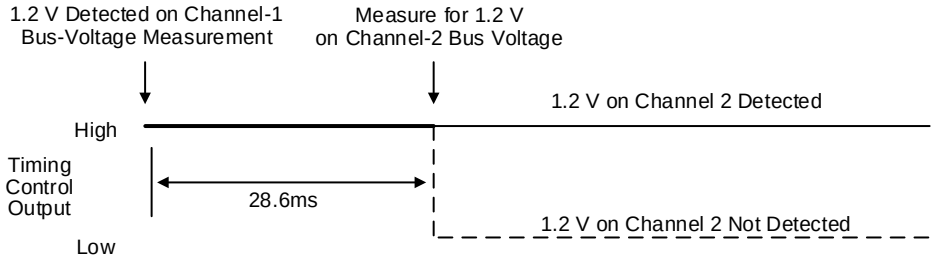


Figure 5. Timing Control State Diagram

The monitoring of the timing control alert function is limited to two scenarios: during power-up or when a software reset is initiated by setting the reset bit (RST, bit 15) in the Configuration register. The timing of the alert function is dependent on the default settings of the device during power-up. If any changes are made to the Configuration register before the timing control alert function completes its full sequence, the timing control alert will be disabled until the power is cycled or a software reset is performed.

Default Settings

The default power-up states of the registers can be found in the Register Map section. It is important to note that these registers are volatile, meaning that if they are programmed with a value different from the default values listed in Table 3, the registers must be reprogrammed each time the device is powered on.

Software Reset

The SQ52210 includes a software reset feature that allows the reinitialization of the device and register settings to their default power-up values without requiring a power cycle. To perform a software reset, utilize bit 15 (RST) of the Configuration register. By setting RST, all registers and settings, except for the power-valid output state, will be reset to their default power state.

In the event of a software reset, the SQ52210 will hold the output of the PV pin until the power-valid detection sequence is completed. Following the software reset, the Power-Valid Upper Limit and Power-Valid Lower Limit registers will revert to their default states. Consequently, any previously reprogrammed limit registers will be reset, causing the original power-valid thresholds to be used for validating power-valid conditions. This design ensures that the circuitry connected to the power-valid output remains uninterrupted during a software reset event.

Device Functional Modes

Averaging Function

The SQ52210 integrates three channels used to monitor up to three independent supply rails. However, when utilizing multichannel monitoring, there is a possibility of poor placement of shunt resistors. Ideally, shunt resistors should be positioned as close as possible to their corresponding channel input pins. However, due to system layout constraints and

the presence of multiple power-supply rails, it may be necessary to place one or more shunt resistors further away. This can result in larger measurement errors due to additional trace inductance and other parasitic impedances between the shunt resistor and input pins. Additionally, longer traces increase the potential for noise coupling if routed near noise-generating sections of the board.

To address this issue, the SQ52210 incorporates an averaging function that mitigates the impact of individual measurements on the averaged value of each measured signal. This reduces the influence of noise on the averaged value, effectively serving as an input-signal filter.

The operation of the averaging function is illustrated in Figure 6. The process begins with measuring the shunt input signal on Channel 1. The measured value is then subtracted from the previous value stored in the corresponding data output register. The resulting difference is divided by the value set by the averaging mode setting (AVG2-0, Configuration register bits 11-9), and the result is stored in an internal accumulation register. This computed result is then added to the previously loaded value in the data output register, and the updated value is loaded back into the corresponding data output register. This process is repeated for each subsequent signal measurement. By selecting a higher value for the averaging mode setting, the impact of new conversions on the average value is reduced, as depicted in Figure 6. Therefore, the averaging feature acts as a filter, diminishing input noise from the averaged measurement value.

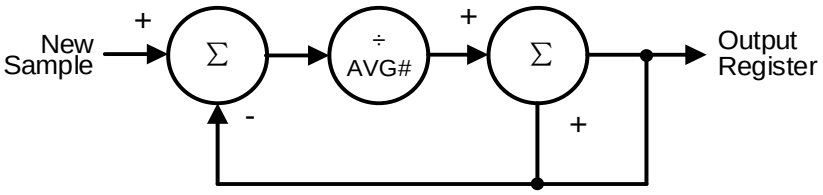


Figure 6. Averaging Function Block Diagram

Channel Configuration

The SQ52210 is capable of monitoring shunt and voltage measurements for up to three distinct power-supply rails, measuring a total of six different signals. To adjust the number of channels and signals being measured, configure the channel enable (CH1en to CH3en) and mode (MODE3-1) bits in the Configuration register. This flexibility allows for optimal customization based on the specific requirements of the system being used.

When all three channels must be monitored during power-up but only one channel requires monitoring after the system has stabilized, the SQ52210 allows you to disable the other two channels following the power-up phase. This configuration allows the SQ52210 to focus solely on monitoring the power-supply rail of interest. By disabling unused channels, the system response time can be improved, enabling a faster return to sampling the desired channel. The SQ52210 linearly monitors the enabled channels. For instance, if all three channels are enabled for both shunt- and bus-voltage measurements, an additional five conversions are completed after a signal is measured before the device returns to that specific signal to begin another conversion. To reduce this requirement to only two conversions before the device commences a new conversion on a particular channel, change the operating mode to solely monitor the shunt voltage.

Timing considerations also play a role in reducing the number of measured signals. The time required to complete a sequence of all-channel shunt- and bus-voltage conversions is equal to the sum of the shunt-voltage conversion time and the bus-voltage conversion time (programmed by the CT bits in the Configuration register) multiplied by the number of channels. Although the conversion times for shunt- and bus-voltage measurements can be programmed independently, the selected conversion times apply to all enabled channels.

Enabling a single channel with only one measured signal allows for exclusive monitoring of that specific signal. This setting ensures the fastest response over time to changes in the input signal, as there is no delay between the end of one conversion and the start of the next conversion on that channel. The conversion time remains unaffected by the enabling or disabling of other channels. However, selecting both shunt- and bus-voltage settings and enabling additional channels will prolong the time between the completion of one signal conversion and the initiation of the next conversion for that signal.

Averaging and Conversion-Time Considerations

The SQ52210 offers programmable conversion times for both shunt- and bus-voltage measurements, with a range of 140µs to 8.244ms. These conversion-time settings, combined with the programmable-averaging mode, allow the SQ52210 to optimize timing requirements for a given application. For instance, if a system requires data to be read every 2ms while monitoring all three channels, the SQ52210 can be configured with shunt- and bus-voltage conversion times set to 332µs.

Alternatively, the SQ52210 can be configured with different conversion-time settings for shunt- and bus-voltage measurements. This approach is common in applications where the bus voltage remains relatively stable. It allows for a

reduced focus on the bus voltage measurement compared to the shunt-voltage measurement. For example, the shunt-voltage conversion time can be set to 4.156ms, while the bus-voltage conversion time can be set to 588μs, resulting in a 5ms update time.

There are trade-offs associated with the conversion time and averaging mode settings. The averaging feature enhances measurement accuracy by effectively filtering the signal and reducing noise. However, this noise reduction results in a longer response time to changes in the input signal. This delayed response can be partially mitigated by using the critical alert feature, which evaluates each individual conversion to determine whether a noise-affected signal exceeds the acceptable threshold.

The chosen conversion times also affect measurement accuracy. To achieve the highest level of accuracy, it is recommended to use the longest allowable conversion times and the highest number of averages based on the system's timing requirements.

Programming

The SQ52210 supports both I²C and SMBus interfaces, as the two protocols are functionally compatible.

Throughout this datasheet, the I²C interface is primarily used as an example. The SMBus protocol is only specified when discussing any differences between the two systems. The SQ52210 connects to the serial interface through two I/O lines: the serial clock (SCL) and the data line (SDA). Both SCL and SDA are open-drain connections.

In I²C communication, the device that initiates a data transfer is known as the controller, while the devices controlled by the host are called targets. The controller device controls the bus by generating the SCL, managing bus access, and generating start and stop conditions.

To address a specific device, the controller initiates a start condition by pulling SDA from a high to a low logic level while SCL is high. On the rising edge of SCL, all targets on the bus shift in the target address byte, with the last bit indicating whether it is a read or write operation. During the ninth clock pulse, the addressed target responds to the controller by generating an acknowledge bit and pulling SDA low.

Data transfer is initiated by sending eight bits of data, followed by an acknowledge bit. During data transfer, the SDA line must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

Once all the data have been transferred, the controller generates a stop condition by pulling SDA from low to high while SCL is high. To prevent bus lock-up, the SQ52210 includes a 28ms interface timeout.

Serial Bus Address

To communicate with the SQ52210, the controller must send a target address byte, which consists of seven address bits and a direction bit indicating a read or write operation.

The SQ52210 is equipped with a single address pin, A0. Table 1 shows the configuration options corresponding to each of the four possible addresses. The state of the A0 pin is evaluated during each bus communication and must be configured before any activity occurs on the interface.

Table 1. Address Pins and Secondary Device Addresses

A0	TARGET ADDRESS
GND	1000000
VS	1000001
SDA	1000010
SCL	1000011

Serial Interface

The SQ52210 functions exclusively as a target device on both the I²C bus and SMBus. The bus connections are established using the open-drain I/O lines, SDA and SCL. These pins use integrated spike-suppression filters and Schmitt triggers to minimize the impact of noise. Although there is spike suppression integrated into the digital I/O lines, it is essential to employ proper layout techniques to minimize coupling into the communication lines. Noise can be introduced through capacitive coupling between the communication lines themselves or from other switching noise sources within the system. Routing traces in parallel with the ground between layers on a printed circuit board (PCB) typically mitigates the effects of coupling between the communication lines. Additionally, shielding the communication lines reduces the risk of unintended noise coupling into the digital I/O lines, which could be mistakenly interpreted as start or stop commands.

The SQ52210 supports a transmission protocol with both Fast mode (1kHz to 400kHz) and High-speed mode (1 kHz to 3 MHz). All data bytes are transmitted with the most significant bit (MSB) sent first.

Writing To and Reading From the SQ52210

To retrieve a specific SQ52210 register data, the user must write the corresponding value to the register pointer. Table 2 lists all registers along with their respective addresses. Figure 7 illustrates the register pointer value, which is the first byte transmitted after the target address byte with the R/W bit set low. Every write operation to the SQ52210 requires a register pointer value.

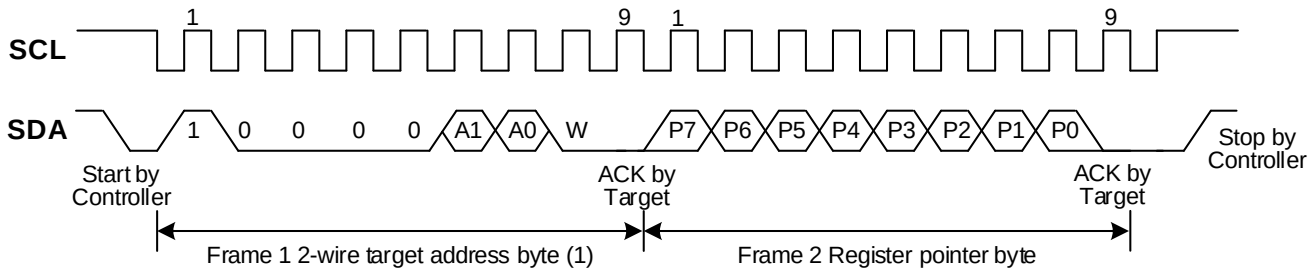


Figure 7. Typical Register Pointer Set

Note 1: The value of the target address byte is determined by the settings of the A0 pins. Refer to Table 1.

The process of writing to registers begins with the controller transmitting the first byte, which is the target address with the R/W bit set low. The SQ52210 then acknowledges the receipt of a valid address. Following this, the controller transmits the next byte, which is the register address where data will be written. This register address value updates the register pointer to the desired register. The subsequent two bytes are written to the register pointed to by the register pointer. The SQ52210 acknowledges the receipt of each data byte. The controller concludes the data transfer by generating a start or stop condition.

When reading from the SQ52210, the last value stored in the register pointer through a write operation determines which register will be read. To change the register pointer for a read operation, a new value needs to be written to the register pointer. This is achieved by sending a target address byte with the R/W bit low, followed by the register pointer byte. No additional data is necessary. Subsequently, the controller generates a start condition and transmits the target address byte with the R/W bit high to initiate the read command. The target then transmits the most significant byte of the register indicated by the register pointer. This byte is followed by an acknowledgment from the controller, after which the target transmits the least significant byte. The controller acknowledges the receipt of the data byte. The data transfer is terminated by the controller generating a not-acknowledge after receiving any data byte or by generating a start or stop condition. If repeated reads from the same register are required, there is no need to continually send the register pointer bytes as the SQ52210 retains the register pointer value until it is changed by the next write operation.

Figure 8 and Figure 9 illustrate the timing diagrams for write and read operations, respectively. It should be noted that register bytes are sent with the most significant byte first, followed by the least significant byte.

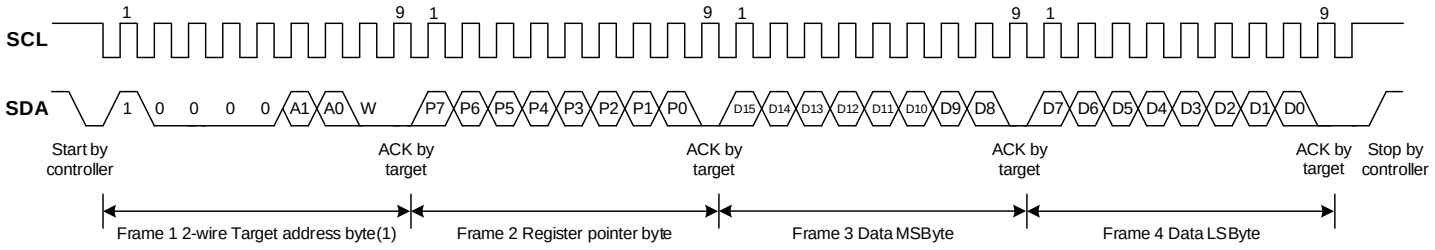


Figure 8. Timing Diagram for Write Word Format

Note 1: The value of the Target Address byte is determined by the settings of the A0 pins. Refer to Table 1.

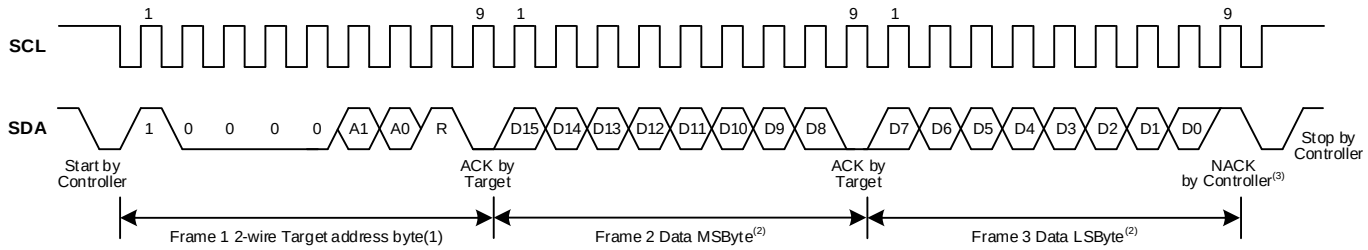


Figure 9. Timing Diagram for Read Word Format

Note 1. The value of the Target Address byte is determined by the settings of the A0 pins. Refer to Table 1.
Note 2. The data is being read from the last register pointer location. If reading a different register is desired, the register pointer must be updated first. See Figure 7
Note 3. ACK by the Controller can also be sent.

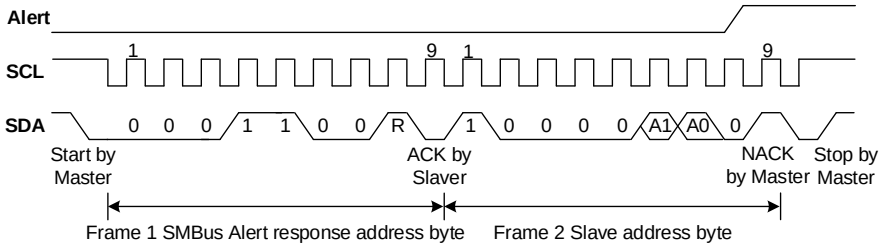


Figure 10. Timing Diagram for SMBus Alert

High-Speed I²C Mode

When the bus is idle, pull-up resistors hold the SDA and SCL lines high. The controller initiates communication by generating a start condition, followed by a valid serial byte containing the high-speed (HS) controller code 00001XXX. This transmission occurs in either Fast (400kHz) or Standard (100kHz) (F/S) mode with a maximum speed of 400kHz. Although the SQ52210 does not acknowledge the HS controller code, it recognizes the code and adjusts its internal filters to support 3MHz operation.

Subsequently, the controller generates a repeated start condition, which has the same timing as the initial start condition. After this repeated start condition, the protocol remains the same as in F/S mode, with the exception that transmission speeds of up to 3 MHz are permitted. Instead of using a stop condition, the controller utilizes repeated start conditions to maintain the bus in Hs mode. To conclude the Hs mode and revert to F/S mode, a stop condition is sent, causing all internal filters of the SQ52210 to switch back to supporting F/S mode.

SMBus Alert Response

The SQ52210 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple targets. When an Alert occurs, the controller can broadcast the Alert Response target address (0001 100) with the Read/Write bit set high. Following this Alert Response, any target that generates an alert is identified by acknowledging the Alert Response and sending the address on the bus.

The Alert Response can activate multiple target devices simultaneously, similar to the I2C General Call. If more than one target attempts to respond, bus arbitration rules are applied. The target device that doesn't win the arbitration will not generate an acknowledge. It will continue to hold the Alert line low until it is prioritized through the arbitration process.

The timing diagram for the SMBus Alert response operation is shown as Figure 10.

General Call Reset

A general call reset for multiple targets is triggered by addressing the general call address (0000 000) with the last R/W bit set to 0, followed by the data byte 0000 0110 (06h).

Upon receiving this 2-byte sequence, all targets configured to respond to the general call address are reset. All SQ52210s on the bus will perform a soft reset and return to their default power-up conditions.

Register Memory Map

The SQ52210 uses a set of registers to store configuration settings, minimum and maximum limits, measurement results, and status information. Table 2 provides a summary of these registers, while the Functional Block Diagram section illustrates how they are organized.

Table 2. SQ52210 Register Memory Map

Address	Register Name	Reset Value	Size (bits)
0h	Configuration	7127h	16
1h	Channel-1 Shunt Voltage	0000h	16
2h	Channel-1 Bus Voltage	0000h	16
3h	Channel-2 Shunt Voltage	0000h	16
4h	Channel-2 Bus Voltage	0000h	16
5h	Channel-3 Shunt Voltage	0000h	16
6h	Channel-3 Bus Voltage	0000h	16
7h	Channel-1 Critical Alert Limit	7FF8h	16
8h	Channel-1 Warning Alert Limit	7FF8h	16
9h	Channel-2 Critical Alert Limit	7FF8h	16
Ah	Channel-2 Warning Alert Limit	7FF8h	16
Bh	Channel-3 Critical Alert Limit	7FF8h	16
Ch	Channel-3 Warning Alert Limit	7FF8h	16
Dh	Shunt-Voltage Sum	0000h	16
Eh	Shunt-Voltage Sum Limit	7FFEh	16
Fh	Mask/Enable	0002h	16
10h	Power-Valid Upper Limit	2710h	16
11h	Power-Valid Lower Limit	2328h	16
12h	Alert_Config	0000h	16
14h	Calibration	0000h	16
15h	Channel-1 Current	0000h	16
16h	Channel-2 Current	0000h	16
17h	Channel-3 Current	0000h	16
18h	Channel-1 Power	0000h	16
19h	Channel-2 Power	0000h	16
1Ah	Channel-3 Power	0000h	16
1Bh	Channel-1 Alert limit	0000h	16
1Ch	Channel-2 Alert limit	0000h	16
1Dh	Channel-3 Alert limit	0000h	16
FEh	Manufacturer ID	194Fh	16
FFh	Die ID	5443h	16

Configuration Register (address = 00h) [reset = 7127h]

The Configuration register controls the operating modes for the shunt- and bus-voltage measurements on all three input channels. It also sets the conversion time and averaging mode for both measurement types. Additionally, this register enables or disables each channel independently and selects the operating mode that determines which power rails are measured.

The Configuration register can be read at any time without affecting device settings or ongoing conversions. However, writing to this register pauses any active conversion until the write operation is complete. A new conversion then begins using the updated Configuration register contents. This mechanism ensures that the conditions for the next completed conversion are always well-defined and predictable.

Table 3. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit: Setting this bit to '1' generates a system reset equivalent to a power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	CH1en	R/W	7h	Channel enable mode: These bits allow independent enabling or disabling of each channel. 0 = Channel disable 1 = Channel enable (default)
13	CH2en			
12	CH3en			
11-9	AVG2-0	R/W	0h	Averaging mode: These bits configure the number of samples to be collected and averaged. 000 = 1 (default) 001 = 4 010 = 16 011 = 64 100 = 128 101 = 256 110 = 512 111 = 1024
8-6	VBUSCT2-0	R/W	4h	Bus-voltage conversion time: These bits configure the conversion time for bus-voltage measurements. 000 = 140μs 001 = 204μs 010 = 332μs 011 = 588μs 100 = 1.1ms (default) 101 = 2.116ms 110 = 4.156ms 111 = 8.244ms
5-3	VSHCT2-0	R/W	4h	Shunt-voltage conversion time: These bits configure the conversion time for shunt-voltage measurements. The bit settings for VSHCT2-0 are identical to those of VBUSCT2-0 (bits 8-6) described in the previous row.
2-0	MODE3-1	R/W	7h	Operating mode: These bits determine the device's operating mode - continuous, single-shot (triggered), or power-down. The default setting is continuous shunt and bus voltage monitoring. 000 = Power-down 001 = Shunt voltage, single-shot (triggered) 010 = Bus voltage, single-shot (triggered) 011 = Shunt and bus, single-shot (triggered) 100 = Power-down 101 = Shunt voltage, continuous 110 = Bus voltage, continuous 111 = Shunt and bus, continuous (default)

Channel-1 Shunt-Voltage Register (address = 01h) [reset = 00h]

This register holds the average shunt voltage measurement for Channel 1. It is responsible for storing the current reading of the shunt voltage (VSHUNT) specifically for Channel 1. When dealing with negative numbers, they are expressed in twos complement format. To obtain the twos complement of a negative number, the absolute value of the binary number is complemented, and then 1 is added. The sign of the number is extended by setting the most significant bit (MSB) to 1, indicating that it is a negative number.

Full-scale range = 163.84mV (hexadecimal = 7FF8); LSB (SD0): 40μV.

Example: Calculating Two's Complement for VSHUNT = –40mV:

1. Take the absolute value: 40mV
2. Convert this number to a whole decimal number (40mV /40μV) = 1000
3. Convert to binary = 0001 1111 0100 0000
4. Take the binary complement = 1110 0000 1011 1111
5. Add 1 to obtain the twos complement = 1110 0000 1100 0000
6. Final 16-bit result (with MSB = 1 to indicate negative): 1110 0000 1100 0000 = E0C0h

Table 4. Channel-1 Shunt-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	SD11-0	R	0h	Channel-1 shunt-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-1 Bus-Voltage Register (address = 02h) [reset = 00h]

This register holds the bus voltage measurement (VBUS) for Channel 1.

Full-scale range = 32.76V (hexadecimal = 7FF8); LSB (BD0) = 8mV.

Table 5. Channel-1 Bus-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	BD11-0	R	0h	Channel-1 bus-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-2 Shunt-Voltage Register (address = 03h) [reset = 00h]

This register holds the averaged shunt voltage measurement for Channel 2.

Full-scale range = 163.84mV (hexadecimal = 7FF8); LSB (SD0): 40μV.

Table 6. Channel-2 Shunt-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	SD11-0	R	0h	Channel-2 shunt-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-2 Bus-Voltage Register (address = 04h) [reset = 00h]

This register holds the bus voltage reading (VBUS) for Channel 2.

Full-scale range = 32.76V (hexadecimal = 7FF8); LSB (BD0) = 8mV.

Table 7. Channel-2 Bus-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	BD11-0	R	0h	Channel-2 bus-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-3 Shunt-Voltage Register (address = 05h) [reset = 00h]

This register holds the averaged shunt voltage measurement for Channel 3.

Full-scale range = 163.84mV (hexadecimal = 7FF8); LSB (SD0): 40μV.

Table 8. Channel-3 Shunt-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	SD11-0	R	0h	Channel-3 shunt-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-3 Bus-Voltage Register (address = 06h) [reset = 00h]

This register holds the bus voltage reading (VBUS) for Channel 3.

Full-scale range = 32.76V (hexadecimal = 7FF8); LSB (BD0) = 8mV.

Table 9. Channel-3 Bus-Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	BD11-0	R	0h	Channel-3 bus-voltage data bits
2-0	Reserved	R	0h	Reserved

Channel-1 Critical-Alert Limit Register (address = 07h) [reset = 7FF8h]

This register holds the value used for comparison with each shunt voltage conversion on Channel 1 to detect fast overcurrent events.

Table 10. Channel-1 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	C1L11-0	R/W	FFFh	Channel-1 critical-alert-limit data bits
2-0	Reserved	R	0h	Reserved

Channel-1 Warning-Alert Limit Register (address = 08h) [reset = 7FF8h]

This register holds the value used for comparison with each averaged shunt voltage value of Channel 1 to detect a longer duration overcurrent event.

Table 11. Channel-1 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	W1L11-0	R/W	FFFh	Channel-1 warning-alert-limit data bits
2-0	Reserved	R	0h	Reserved

Channel-2 Critical-Alert Limit Register (address = 09h) [reset = 7FF8h]

This register holds the value used for comparison with each shunt voltage conversion on Channel 2 to detect fast overcurrent events.

Table 12. Channel-2 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	C2L11-0	R/W	FFFh	Channel-2 critical-alert-limit data bits
2-0	Reserved	R	0h	Reserved

Channel-2 Warning-Alert Limit Register (address = 0Ah) [reset = 7FF8h]

This register holds the value used for comparison with the averaged shunt voltage value of Channel 2 to detect a longer duration overcurrent event.

Table 13. Channel-2 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	W2L11-0	R/W	FFFh	Channel-2 warning-alert-limit data bits
2-0	Reserved	R	0h	Reserved

Channel-3 Critical-Alert Limit Register (address = 0Bh) [reset = 7FF8h]

This register holds the value used for comparison with each shunt voltage conversion on Channel 3 to detect fast overcurrent events.

Table 14. Channel-3 Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	C3L11-0	R/W	FFFh	Channel-3 critical-alert-limit data bits
2-0	Reserved	R	0h	Reserved

Channel-3 Warning-Alert Limit Register (address = 0Ch) [reset = 7FF8h]

This register holds the value used for comparison with the averaged shunt voltage value of Channel 3 to detect a longer duration overcurrent event.

Table 15. Critical-Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	W3L11-0	R/W	FFFh	Channel-3 warning-alert-limit data bits
2-0	Reserved	R	0h	Reserved

Shunt-Voltage Sum Register (address = 0Dh) [reset = 00h]

This register contains the sum of the single-conversion shunt voltages from the selected channels, as determined by the summation control bits 12, 13, and 14 in the Mask/Enable register. It is updated with the most recent sum after each complete cycle of all selected channels. The LSB value of the Shunt-Voltage Sum register is 40µV.

Table 16. Shunt-Voltage Sum Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-1	SV13-0	R	0h	Shunt-voltage sum data bits
0	Reserved	R	0h	Reserved

Shunt-Voltage Sum-Limit Register (address = 0Eh) [reset = 7FFEh]

This register contains the value compared to the Shunt-Voltage Sum register value after each completed cycle of all selected channels to detect system overcurrent events. The LSB value of the Shunt-Voltage Sum register is 40µV.

Table 17. Shunt-Voltage Sum Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-1	SVL13-0	R/W	3FFFh	Shunt-voltage sum data bits
0	Reserved	R	0h	Reserved

Mask/Enable Register (address = 0Fh) [reset = 0002h]

This register determines the selection of enabled functions that control the Critical alert and Warning alert pins, as well as the response of each warning alert to its corresponding channel. To clear any existing flag results, the Mask/Enable register must be read. Writing to this register does not clear the status of the flag bit.

To ensure that there is no uncertainty regarding the setting of the warning function that led to the flag bit being set, it is recommended to read the Mask/Enable register and clear the status of the flag bit before making any changes to the warning function setting.

Table 18. Shunt-Voltage Sum Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVF	R	0h	This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that the current and power data of either channel may be invalid.
14-12	SCC1-3	R/W	0h	Summation channel control: These bits determine which shunt voltage measurement channels contribute to the Shunt-Voltage Sum register. This selection does not affect the individual channel enable/disable status or their corresponding measurements. Each bit selects whether the associated channel is used to fill the Shunt-Voltage Sum register. 0 = Disabled (default) 1 = Enabled

11	WEN	R/W	0h	Warning alert latch enable: These bits configure the latching behavior of the Warning alert pin. 0 = Transparent (default) 1 = Latch enabled
10	CEN	R/W	0h	Critical alert latch enable: These bits configure the latching behavior of the Critical alert pin. 0 = Transparent (default) 1 = Latch enabled
9-7	CF1-3	R	0h	Critical-alert flag indicator: These bits are asserted when the corresponding channel measurement exceeds the critical alert limit, causing the Critical alert pin to be asserted. Read these bits to determine which channel triggered the critical alert. The critical alert flag bits are cleared upon reading the Mask/Enable register.
6	SF	R	0h	Summation-alert flag indicator: This bit is asserted when the Shunt Voltage Sum register exceeds the Shunt Voltage Sum Limit register. When asserted, it also triggers the Critical alert pin. The Summation Alert Flag bit is cleared upon reading the Mask/Enable register.
5-3	WF1-3	R	0h	Warning-alert flag indicator: These bits are asserted when the corresponding channel's averaged measurement exceeds the warning alert limit, causing the Warning alert pin to be asserted. Read these bits to identify which channel triggered the warning alert. The Warning Alert Flag bits are cleared upon reading the Mask/Enable register.
2	PVF	R	0h	Power-valid-alert flag indicator: This bit allows software-based monitoring of the Power Valid (PV) alert pin status. It reflects the current state of the PV pin are remains asserted until the alert condition is resolved and the PV pin is asserted.
1	TCF	R	1h	Timing-control-alert flag indicator: This bit allows software to detect if the Timing Control (TC) alert pin has been asserted. It reflects the current state of the TC pin and remains asserted until power is recycled or a software reset is performed. The default state of the Timing Control Alert Flag is high.
0	CVRF	R	0h	Conversion-ready flag: Although the SQ52210 can be read at any time and retains the most recent conversion data, the conversion-ready bit facilitates coordination of single-shot conversions. This bit is set once all conversions are complete and is cleared under the following conditions: 1. Writing to the Configuration register (except when selecting power-down or disable modes). 2. Reading the Mask/Enable register.

Power-Valid Upper-Limit Register (address = 10h) [reset = 2710h]

The value stored in this register is utilized to determine whether the power-valid conditions are satisfied. The power-valid condition is deemed fulfilled when all bus-voltage channels surpass the limit set in this register. Once the power-valid condition is met, the PV alert pin is activated with a high signal to indicate that the SQ52210 has verified that all bus voltage channels are exceeding the upper-limit value for power-validity. To enable the monitoring of the power-valid conditions, the bus measurements must be enabled by setting one of the corresponding MODE bits in the Configuration register.

The power-valid upper-limit LSB value is 8mV. Power-on reset value is 2710h = 10.000V.

Table 19. Power-Valid Upper-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R/W	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	PVU11-0	R/W	4E2h	Power-valid upper-limit data bits
2-0	Reserved	R	0h	Reserved

Power-Valid Lower-Limit Register (address = 11h) [reset = 2328h]

The value stored in this register is utilized to determine whether any of the bus-voltage channels fall below the lower-limit for power validity when the power-valid conditions are satisfied. This limit is used to compare the readings of all bus channels to ensure that they remain above the lower limit, thereby preserving the power-valid condition. When any bus-voltage channel drops below the power-valid lower-limit, the PV alert pin is pulled low, indicating that the SQ52210 has detected a bus voltage reading below the lower-limit for power-validity. To enable the monitoring of the power-valid condition, the bus measurements must be enabled by setting the mode (MODE3-1) bits in the Configuration register.

The power-valid lower-limit LSB value is 8mV. Power-on reset value is 2328h = 9V.

Table 20. Power-Valid Lower-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R/W	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-3	PVL11-0	R/W	465h	Power-valid lower-limit data bits
2-0	Reserved	R	0h	Reserved

Alert Configuration Register (address = 12h) [reset = 0000h]

The Alert Configuration Register selects the function enabled to control the Critical or Warning pin and defines the behavior of that pin. If multiple functions are enabled, the Alert Function with the highest significant bit position (D15-D4) takes priority and responds to the Alert Limit Register.

Table 21. Alert Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	SUL_Select	R/W	0h	Shunt under limit alert channel control: These bits determine which channels are enabled to monitor shunt under-limit events. The selection does not impact the individual channel enable or disable status, or the corresponding channel measurements. The corresponding bit is used to select if the channel is compared against the threshold value. 0 = Disabled (default) 1 = Enabled
12-10	BOL_Select	R/W	0h	Bus over limit alert channel control: These bits determine which channels are enabled to monitor bus over-limit events. The selection does not impact the individual channel enable or disable status, or the corresponding channel measurements. The corresponding bit is used to select if the channel is compared against the threshold value. 0 = Disabled (default) 1 = Enabled
9-7	BUL_Select	R/W	0h	Bus under voltage limit channel control: These bits determine which channels are enabled to monitor bus under-limit events. The selection of these bits does not impact the individual channel enable or disable status, or the corresponding channel measurements. The corresponding bit is used to select if the channel is compared against the threshold value. 0 = Disabled (default) 1 = Enabled
6-4	POL_Select	R/W	0h	Power over limit alert channel control: These bits determine which channels are enabled to monitor power over limit event. The selection of these bits does not impact the individual channel enable or disable status, or the corresponding channel measurements. The corresponding bit is used to select if the channel is compared against the threshold value. 0 = Disabled (default) 1 = Enabled
3-1	AFF1-3	R	0h	While only one Alert Function can be monitored at the Critical/Warning pin at a time, other events can be enabled to assert the Critical/Warning pin. Reading the Alert Function Flag following a Critical/Warning allows the user to determine if the Alert Function was the source of the Critical/Warning. When the CEN/WEN bit is set to Latch mode, the Alert Function Flag bit clears only when the Alert Configuration Register is read. When the CEN/WEN bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in a Critical/Warning condition.
0	SLOWALERT	R/W	0h	When enabled, the Warning pin is asserted on the completed averaged value. Otherwise, the Critical pin is asserted on the individual averaged value. This gives the flexibility to delay the ALERT until after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value

Calibration Register (address = 14h) [reset = 0000h]

This register provides the device with the value of the shunt resistor used to generate the measured differential voltage and sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable for use in overall system calibration.

Table 22. Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved
14-0	CAL14-0	R/W	0h	Calibration data bits

Channel-1 Current (address = 15h) [reset = 0000h]

The Channel-1 Current register is shown in Table 23.

Table 23. Channel-1 Current Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-0	C1CD14-0	R	0h	Channel-1 current data bits

Channel-2 Current (address = 16h) [reset = 0000h]

The Channel-2 Current register is shown in Table 24.

Table 24. Channel-2 Current Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0h	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-0	C2CD14-0	R	0h	Channel-2 current data bits

Channel-3 Current (address = 17h) [reset = 0000h]

The Channel-3 Current register is shown in Table 25.

Table 25. Channel-3 Current Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SIGN	R	0	Sign bit: 0 = positive number 1 = negative number in twos complement format
14-0	C3CD14-0	R	0h	Channel-3 current data bits

Channel-1 Power (address = 18h) [reset = 0000h]

The Channel-1 Power register is shown in Table 26.

Table 26. Channel-1 Power Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	C1PD15-0	R	0h	Channel-1 power data bits

Channel-2 Power (address = 19h) [reset = 0000h]

The Channel-2 Power register is shown in Table 27.

Table 27. Channel-2 Power Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	C2PD15-0	R	0h	Channel-2 power data bits

Channel-3 Power (address = 1Ah) [reset = 0000h]

The Channel-3 Power register is shown in Table 28.

Table 28. Channel-3 Power Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	C3PD15-0	R	0h	Channel-3 power data bits

Channel-1 Alert limit (address = 1Bh) [reset = 0000h]

The Alert Limit-1 Register holds the value of Channel-1 used to compare to the register selected in the Alert_config Register to determine if a limit has been exceeded.

Table 29. Channel-1 Alert limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	C1AL12-0	R/W	0h	Channel-1 alert limit bits
2-0	Reserved	R	0h	Reserved

Channel-2 Alert limit (address = 1Ch) [reset = 0000h]

The Alert Limit-2 Register holds the value of Channel-2 used to compare to the register selected in the Alert_config Register to determine if a limit has been exceeded.

Table 30. Channel-2 Alert limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	C2AL12-0	R/W	0h	Channel-2 alert limit bits
2-0	Reserved	R	0h	Reserved

Channel-3 Alert limit (address = 1Dh) [reset = 0000h]

The Alert Limit-3 Register holds the value of Channel-3 used to compare to the register selected in the Alert_config Register to determine if a limit has been exceeded.

Table 31. Channel-3 Alert limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	C3AL12-0	R/W	0h	Channel-3 alert limit bits
2-0	Reserved	R	0h	Reserved

Manufacturer ID Register (address = FEh) [reset = 194Fh]

This register holds a factory-programmable identification value that identifies this device as being manufactured by Silergy. This register distinguishes this device from other devices that are on the same I^2C bus. The contents of this register are 194Fh.

Table 32. Manufacturer ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D15-0	R	194Fh	Manufacturer ID bits

Die ID Register (address = FFh) [reset = 5443h]

This register holds a factory-programmable identification value that identifies this device as an SQ52210. This register distinguishes this device from other devices that are on the same I^2C bus. The Die ID for the SQ52210 is 5443h.

Table 33. Die ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	D15-0	R	5443h	Die ID bits

Application and Implementation

Device Measurement Range and Resolution

The full-scale differential input across the IN+ and IN– pins is ±163.84mV. The range for the bus voltage measurement is from 0V to 32.76V.

Table 34 describes the full-scale voltage ranges for shunt and bus measurements, along with their associated step size.

Table 34. ADC Full Scale Values

PARAMETER	FULL SCALE VALUE	RESOLUTION
Shunt voltage	±163.84mV	40μV/LSB
Bus voltage	0V to 32.76V	8mV/LSB

The device shunt voltage and bus voltage measurements can be read from the Shunt and Bus registers, respectively. These registers provide a 13-bit digital output. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore, the data value in the Shunt register can be positive or negative. The voltage data values are always positive. The output data can be directly converted into voltage by multiplying the digital value by its respective resolution size.

The device provides the flexibility to report calculated current in Amperes and power in Watts.

Current and Power Calculations

To report current and power values accurately, several registers must be configured in the following sequence. The following example applies to Channel 1.

Step 1: Select the resolution of the Current Register (15h): Current_LSB.

The highest resolution for the Current Register (15h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current IMAX as shown in Equation (1). While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (15h) and Power Register (18h) to amperes and watts, respectively.

$$\text{Current\_LSB} = \frac{\text{Maximum Expected Current}}{2^{15}} \quad (1)$$

Where: Current_LSB is the resolution of the Current Register (15h).

In addition, the value of the shunt resistor is selected based on the shunt voltage measurement range and IMAX.

Step 2: Configure the Calibration Register (14h)

The Calibration Register allows the user to scale the Current Register (15h) and Power Register (18h) to values suitable for the application. When properly configured, the Calibration Register (14h) enables direct readout of the measured current by multiplying the Current Register value by the Current_LSB. The value of the Calibration Register (14h) denoted as CAL[R], should be configured according to Equation (2) below:

$$\text{CAL[R]} = \frac{256 \times \text{Shunt\_LSB}}{\text{Current\_LSB} \times R_{SHUNT}} \quad (2)$$

Where: CAL[R] is the value of the Calibration Register (14h); Shunt_LSB is the resolution of the Shunt Voltage Register (01h), Shunt_LSB is 40μV/LSB; Current_LSB is the resolution of the Current Register (15h); and RSHUNT is the shunt resistor value.

After programming the Calibration Register, the Current Register (15h) and Power Register (18h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (15h) and Power Register (18h) remain at zero.

Step 3: Readout of the power

The resolution of the Power Register is fixed as 20 times the resolution of the Current Register. The power value is expressed using equation (3):

$$\text{Power} = \text{Power[R]} \times \text{Power\_LSB} \quad (3)$$

Configuration Example

The following figure illustrates a nominal 10A load generating a differential voltage of 20mV across a 2mΩ shunt resistor. The SQ52210 measures the bus voltage at the IN- pin, to measure the voltage level delivered to the load. For this example, the IN– pin measures 11.98V due to the voltage drop across the shunt resistor.

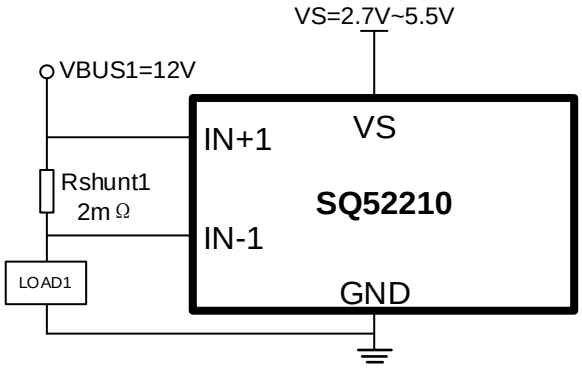
In this example, with a maximum expected current of 15A, the Current_LSB is calculated to be 0.458mA/bit using Equation (1). Selecting a Current_LSB value of 0.5mA/bit or 1mA/bit simplifies conversion from the Current Register (15h) and Power Register (18h) to amperes and watts. For this example, a value of 1mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process on the user side. Using Equation (2) with a Current_LSB value of 1mA/bit and a 2mΩ shunt resistor results in a Calibration Register value of 5120 (1400h).

The Current Register (15h) is calculated through the Shunt Voltage Register (01h) and Calibration Register (14h). For this example, the Shunt Voltage Register holds a value of 0FA0h (representing 20mV), and the Current Register (15h) contains a value of 2710h, which equals 10000 in decimal. Multiplying this value by 1mA/bit results in the original 10A level stated in the example.

The LSB for the Bus Voltage Register (02h) is fixed at 8mV/bit. Therefore, the 11.98V present at the IN- pin corresponds to a register value of 2ED0h, which is 11984 in decimal. Note that the MSB of the Bus Voltage Register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

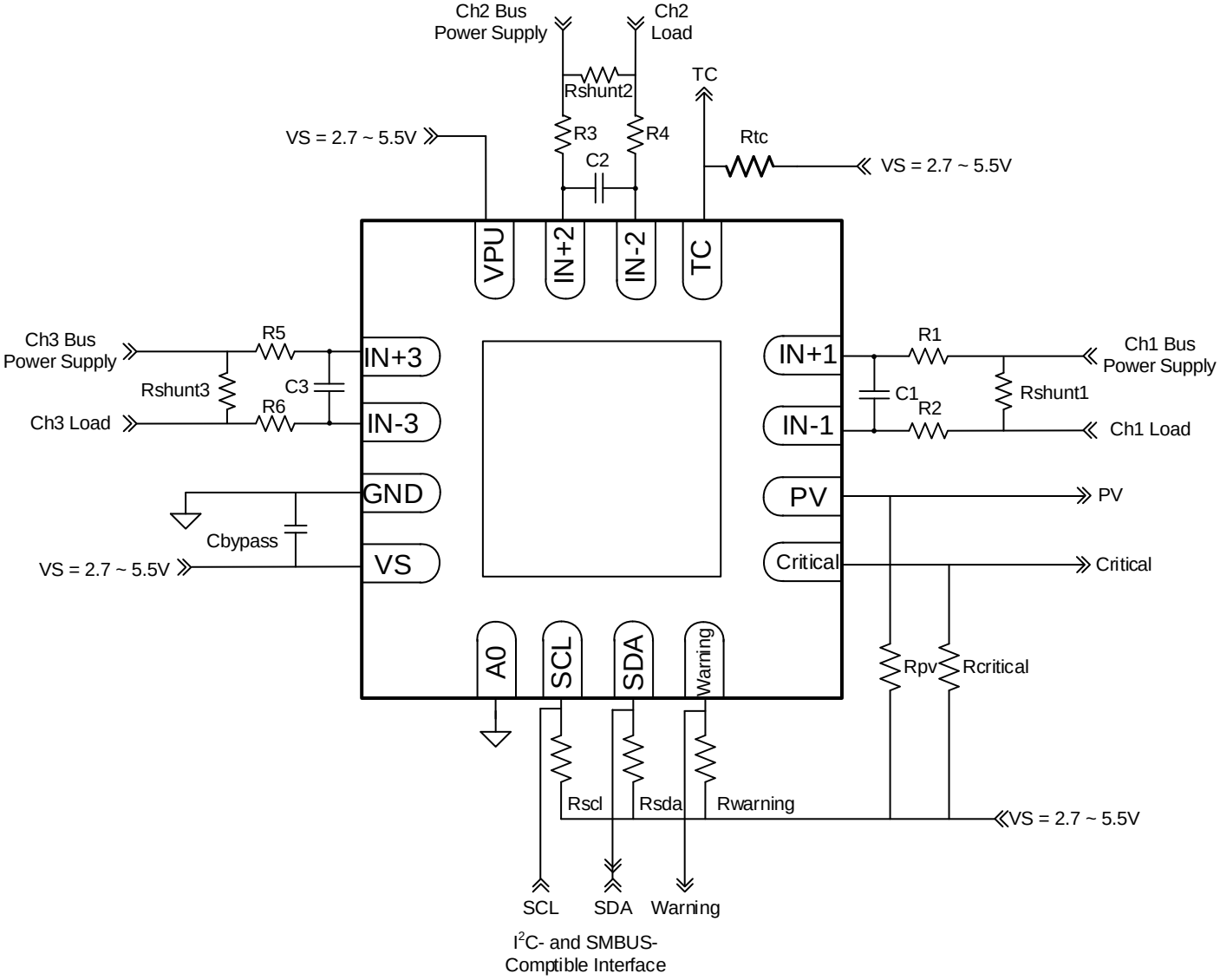
The result for the Power Register (18h) is 1768h, or a decimal equivalent of 5992. Multiplying this result by the power LSB (20 times Current_LSB]) results in a power calculation of (5992× 20mW/bit), or 119.8W. The power LSB has a fixed ratio to the Current_LSB of 48. For this example, 1mA/bit Current_LSB results in a power LSB of 20mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98V multiplied by the load current of 10A to give a result of 119.8W.

The following table presents the results of configuring, measuring and calculating current and power values for the SQ52210 under the conditions: Load = 10A, VCM=12V, RSHUNT=2mΩ, and VBUS=12V.



REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Configuration Register	00h	7127h			
Shunt Register	01h	0FA0h	4000	40μV	20mV
Bus Voltage Register	02h	2ED0h	11984	8mV	11.98V
Calibration Register	09h	1400h	5120		
Current Register	15h	2710h	10000	1mA	10A
Power Register	18h	1768h	5992	20mW	119.8W

Application Schematic



BOM List

Designator	Description
C_{bypass}	0.1μF/50V/X7R, 0603
R_{shunt1}, R_{shunt2}, R_{shunt3}	10mΩ/1W, 2512, 1%
R_{scl}, R_{sda}, $R_{warning}$, $R_{critical}$, R_{pv}, R_{tc}	2kΩ/0.1W, 0603
C1, C2, C3	100nF/50V, 0805
R1, R2, R3, R4, R5, R6	100Ω/0.1W, 0603

Layout Design

Follow these PCB layout guidelines for optimal performance:

- It is recommended to place a high-quality capacitor across analog input pairs with differential connections to ensure signal integrity.
- Place the bypass capacitor (a 0.1μF MLCC is recommended) as close as possible to the VS and GND pins.

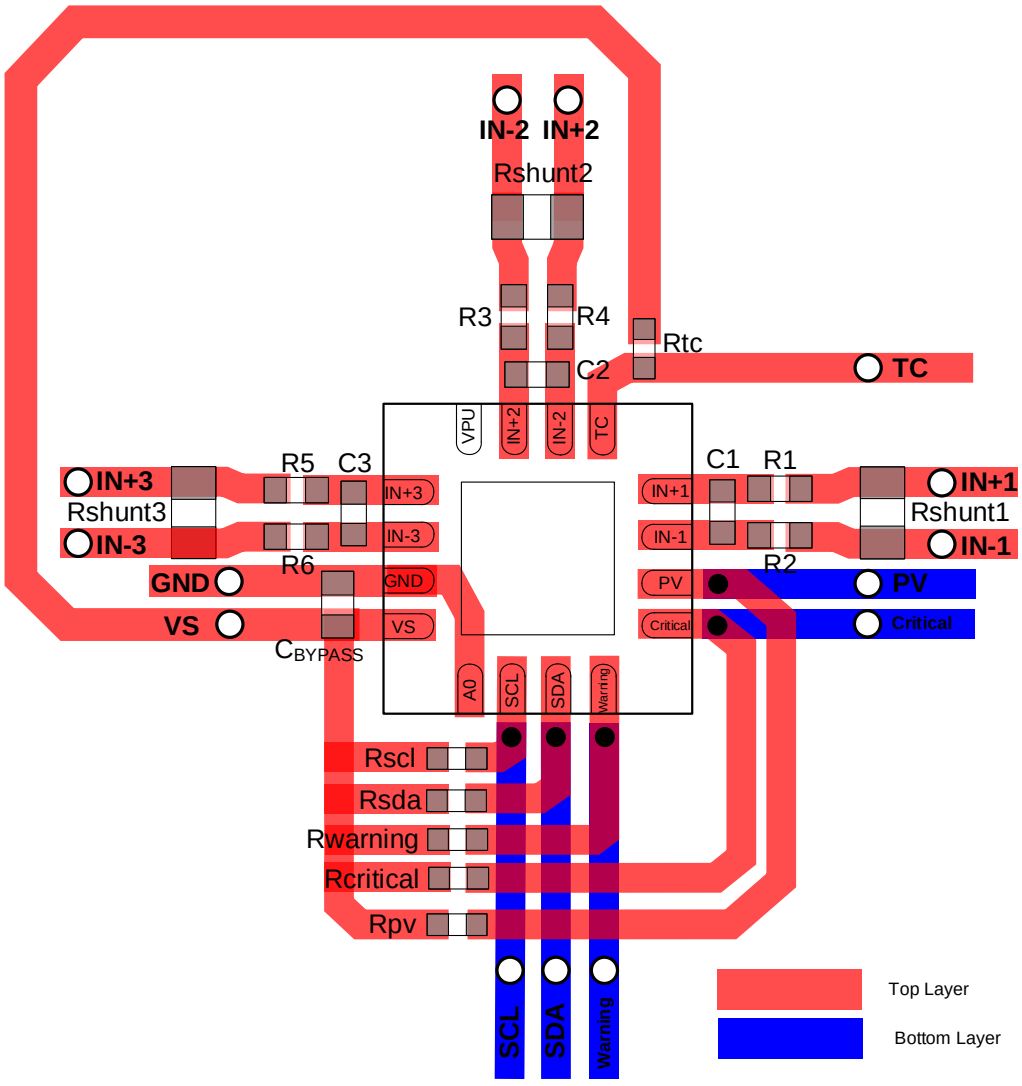
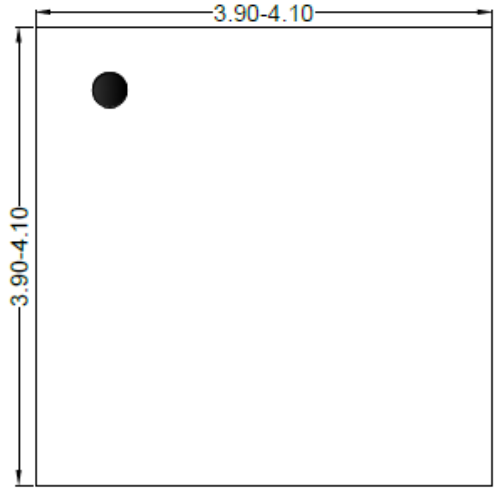
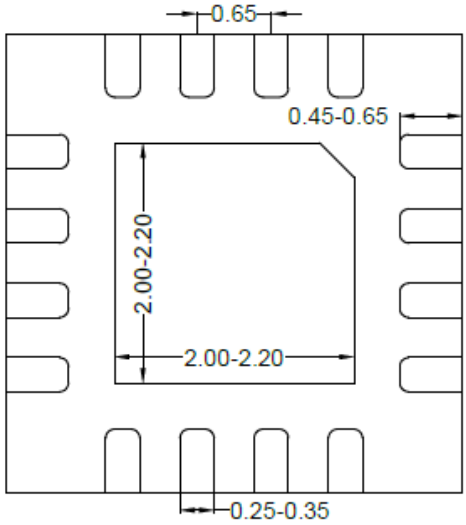


Figure 11. Suggested PCB Layout

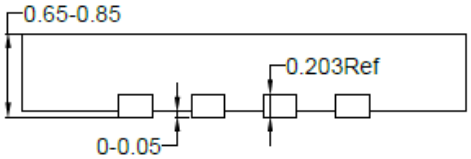
QFN4x4-16 Package Outline Drawing



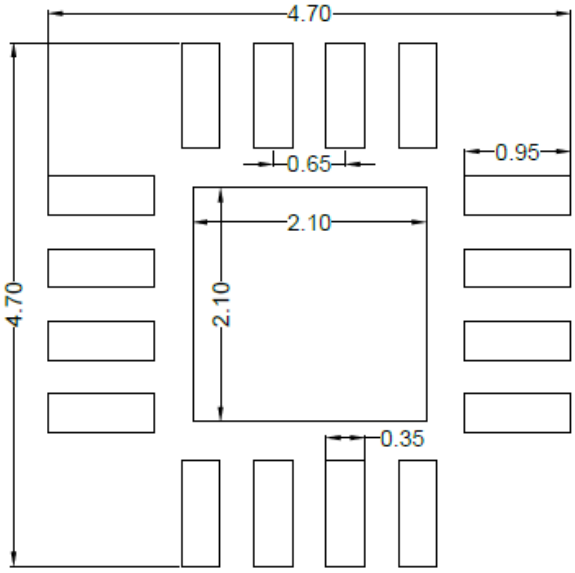
Top View



Bottom View



Side View

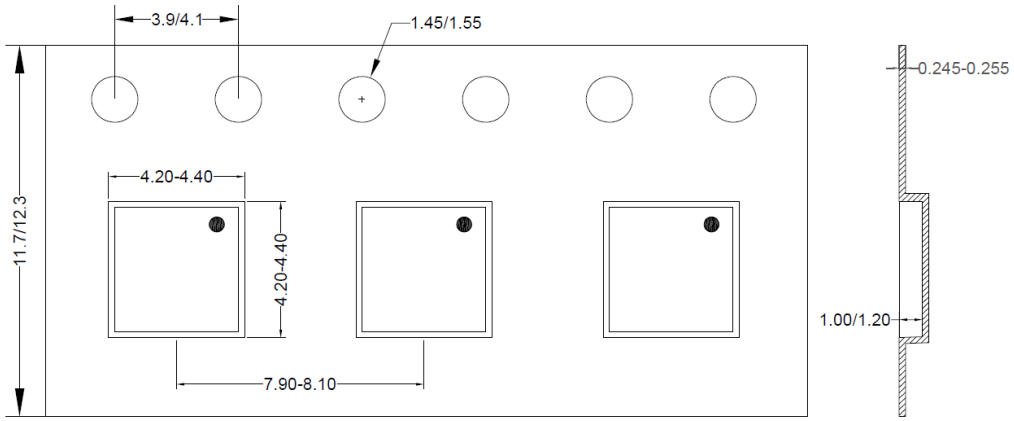


Recommended PCB Layout (Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

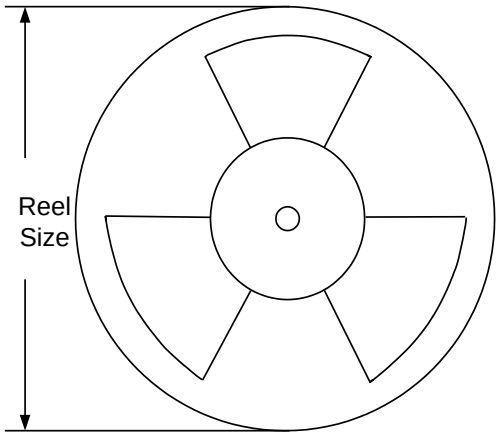
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Feeding direction ⟶

Reel Dimensions



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug. 30, 2025	Revision 1.0	Initial Release.

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