SQ52206

120V 16bit High-Precision Power/Energy/Charge Monitor with I^2C Interface

General Description

The SQ52206 is a high-precision digital power monitor engineered for current-sensing applications, featuring a 16-bit delta-sigma ADC. It is capable of measuring a full-scale differential input, including ±163.84 mV, ±81.92mV, or ±40.96 mV, across a resistive shunt sense element. The device supports a common-mode voltage that spans from -0.3V to +120V.

The SQ52206 features a highly accurate integrated temperature sensor that enables precise measurement of die temperature. This temperature sensor is also useful for monitoring the ambient temperature of the system.

Additionally, the device is equipped with an integrated oscillator that enables it to report various measurements including current, bus voltage, temperature, power, energy, and charge accumulation. It performs all the necessary calculations in the background.

The device's low input bias current allows for the use of larger current-sense resistors, enabling accurate current measurements even in the microampere range. With low offset and gain drift, the device is suitable for precise systems that do not require multi-temperature calibration during manufacturing. In addition, it's extremely low offset voltage and noise make it ideal for sensing applications ranging from amperes to kiloamperes, while maintaining a wide dynamic range without significant power dissipation losses on the sensing shunt element.

The device offers selectable ADC conversion times from 66µs to 8.23ms as well as sample averaging from 1x to 1024x to further minimize noise in the measured data.

Features

- High-Resolution, 16-bit Delta-Sigma ADC
- Wide Common-Mode Range: –0.3V to +120V
- Shunt Full-Scale Differential Range Options: ±163.84mV, ±81.92mV, ±40.96 mV
- Bus Voltage Sense Input Range: 0V to 120V
- Selectable ADC Conversion Time and Sample Averaging
- Programmable Resistor Temperature Compensation
- Low Input Bias Current: 0.1nA (Typical)
- Operates on a 2.7V to 5.5V Power Supply
    - Operational Current: 1050µA (Typical)
    - Shutdown Current: 4.5µA (Typical)
- 2.94 MHz High-Speed I^2C Interface with 16 Pin-Selectable Addresses
- MSL Rating: MSL3
- Package: MSOP10

Applications

- Servers
- Telecom Equipment
- Computing
- Power Management
- Battery Chargers
- Power Supplies
- Test Equipment

Typical Application

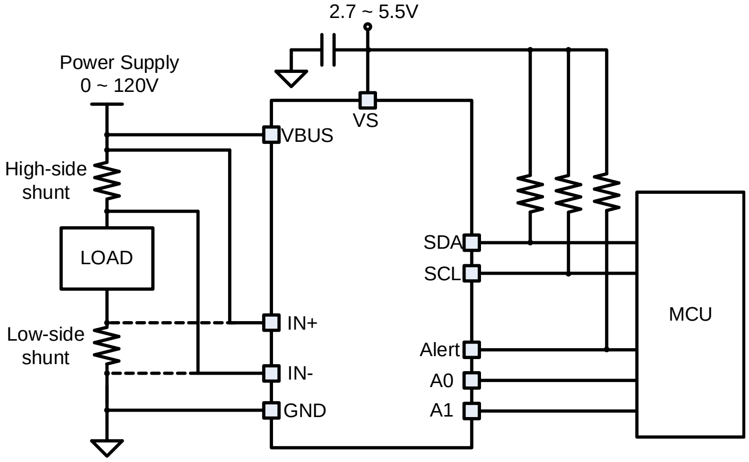


Figure 1. Typical Application Circuit

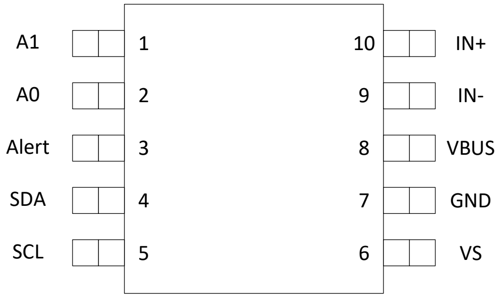
Ordering Information

Ordering Number	Package Type	Top Mark
SQ52206FBP	MSOP10	GLN*xyz*

Device code: **GLN**

x=year code, y=week code, z= lot number code.

Pinout (Top View)



(MSOP10)

Pin Description

Pin No.	Pin Name	Pin Description
1	A1	Address pin. Connect to GND, VS, SDA, or SCL.
2	A0	Address pin. Connect to GND, VS, SDA, or SCL.
3	Alert	Multi-functional alert, open-drain output.
4	SDA	Serial bus data line, open-drain input/output.
5	SCL	Serial bus clock line, open-drain input.
6	VS	Power supply, 2.7V to 5.5V.
7	GND	Ground.
8	VBUS	Bus input voltage.
9	IN–	Negative differential input voltage. Connect to load side of shunt resistor.
10	IN+	Positive differential input voltage. Connect to supply side of shunt resistor.

Block Diagram

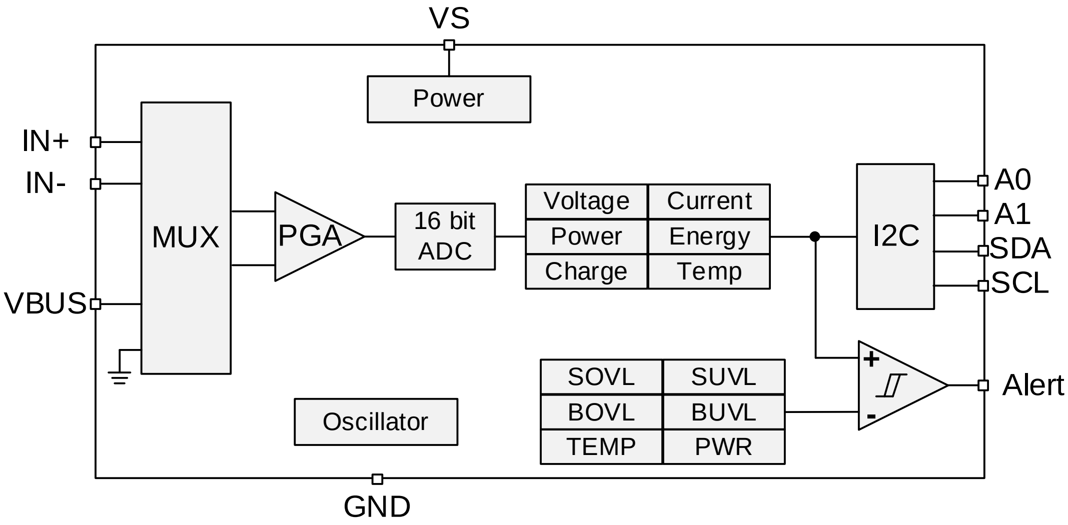


Figure 2. Functional Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VS	-0.3	6	V
Differential Analog Input (VIN+ – VIN-)	-40	40	
Common Mode	-0.3	120	
VBUS	-0.3	120	
VSDA/VSCL/VA0/VA1	-0.3	6	
Input Current into Any Pin	-5	+5	mA
Open-Drain Digital Output Current	-10	+10	mA
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	216.75	°C/W
θ_{JC} Junction-to-Case (top) Thermal Resistance	34	
P_D Power Dissipation T_A = 25°C	0.58	mW

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VS	2.7	5.5	V
Common Mode Analog Input	0	120	V
Operating Ambient Temperature Range	-40	125	°C

Electrical Characteristics

At T_A = 25 °C, VS = 3.3V, VSENSE = VIN+ – VIN– = 0V, VCM = VIN– = 48V (unless otherwise noted). (Note 4)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Common-Mode Input Range	V_{CM}	T_A = –40°C to +125°C	-0.3		120	V
Bus Voltage Input Range	V_{BUS}		0		120	V
Common-Mode Rejection	CMRR	-0.3 V < V_{CM} < 120V, T_A = –40°C to +125°C	144	160		dB
Shunt Voltage Input Range	V_{DIFF}	T_A = –40°C to +125°C, ADCRANGE = 00	-163.84		163.84	mV
		T_A = –40°C to +125°C, ADCRANGE = 01	-81.92		81.92	mV
		T_A = –40°C to +125°C, ADCRANGE = 10/11	-40.96		40.96	mV
Shunt Offset Voltage	V_{OS}	V_{CM} = 48V, T_{CT} > 1.1ms		±1	±5	µV
Shunt Offset Voltage Drift	dV_{OS}/dT	T_A = –40°C to +125°C		±2	±20	nV /°C
Shunt Offset Voltage vs Power Supply	PSRR	V_S = 2.7V to 5.5V, T_A = –40°C to +125°C		±1	±3	µV/V
V_{BUS} Offset Voltage	V_{OS_BUS}	V_{BUS} = 20mV		±2	±5	mV
V_{BUS} Offset Voltage Drift	dV_{OS}/dT	T_A = –40°C to +125°C		±4	±20	µV/°C
V_{BUS} Offset Voltage vs Power Supply	PSRR	V_S = 2.7V to 5.5V		±2	±5	mV/V
Input Bias Current	I_B	Either input, IN+ or IN–, V_{CM} = 120V		0.1	2.5	nA
VBUS Pin Input Impedance	Z_{VBUS}	Active mode		1		MΩ
Input differential impedance	R_{DIFF}	Active mode, V_{IN+} - V_{IN-} < 164mV		150		kΩ
VBUS Pin Leakage Current	I_{VBUS}	Shutdown mode, V_{BUS} = 120V		10		nA
DC Accuracy						
Shunt Voltage Gain Error	G_{SERR}	ADCRANGE = 00, Shunt FSR = ±163.84 mV		±0.16	±0.27	%
		ADCRANGE = 01, Shunt FSR = ±81.92 mV		±0.03	±0.14	%
		ADCRANGE = 10/11, Shunt FSR = ±40.96 mV		±0.04	±0.17	%
Shunt Voltage Gain Error Drift	G_{S_DRFT}			±10	±40	ppm/°C
V_{BUS} Voltage Gain Error	G_{BERR}			±0.03	±0.14	%
V_{BUS} Voltage Gain Error Drift	G_{B_DRFT}			±10	±40	ppm/°C
Power Total Measurement Error (TME)	P_{TME}	T_A = –40°C to +125°C, at full scale			±0.8	%
Energy and Charge TME	E_{TME}	At full scale power			±3.6	%
ADC Resolution				16		Bits
1 LSB Step Size	T_{CT}	Shunt voltage, ADCRANGE = 00		5		µV
		Shunt voltage, ADCRANGE = 01		2.5		µV
		Shunt voltage, ADCRANGE = 10/11		1.25		µV
		Bus voltage		3.75		mV
		Temperature		7.8125		m°C
ADC Conversion Time	t_{CT}	Conversion time field = 0h		66		µs
		Conversion time field = 1h		118		
		Conversion time field = 2h		310		
		Conversion time field = 3h		566		
		Conversion time field = 4h		1070		
		Conversion time field = 5h		2090		
		Conversion time field = 6h		4140		
		Conversion time field = 7h		8230		
Integral Non-Linearity	INL			±2		m%
Differential Non-Linearity	DNL			0.2		LSB

Clock Source						
Internal Oscillator Frequency	f_{OSC}			1		MHz
Internal Oscillator Frequency Tolerance	f_{OSC_TOL}	$T_A = 25°C$			±0.5	%
		$T_A = –40°C$ to $+125°C$			±2	%
Temperature Sensor						
Measurement Range			-40		+125	°C
Temperature Accuracy		$T_A = 25°C$		±0.2	±1	°C
		$T_A = –40°C$ to $+125°C$		±0.6	±2	°C
Power Supply						
Operating Supply Range			2.7		5.5	V
Quiescent Current	I_Q	$V_{SENSE} = 0V$	800	1050	1300	μA
		$V_{SENSE} = 0V$, $T_A = –40°C$ to $+125°C$			1.46	mA
Quiescent Current, Shutdown	I_{QSD}	Shutdown mode		4.5	15	μA
Device Start-Up Time	T_{POR}	Power-up (NPOR)		500		μs
		From shutdown mode		480		μs
Digital Input / Output						
Logic Input Level, High	V_{IH}	SDA, SCL	1.4		6	V
Logic Input Level, Low	V_{IL}		-0.5		0.4	V
Logic Output Level, Low	V_{OL}	$V_{OL} = 3mA$	0		0.4	V
Digital Leakage Input Current	I_{IO_LEAK}	$0 V \le V_{SCL} \le V_S$, $0 V \le V_{SDA} \le V_S$		0.1	1	μA
Address Pin Input Current	I_{addr}	$V_{A0} = V_S$, $V_{A1} = V_S$		15		μA

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Tested with natural convection and chip mounted on a low effective single-layer PCB in accordance with JESD5-3.

Note 3: The device is not guaranteed to function outside its recommended operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25℃$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Timing Requirements (I^2C)

Parameter	Conditions	Min	Typ	Max	Units
I^2C BUS (Fast Mode)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time following a repeated START condition. After this time, the first clock pulse is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
I^2C BUS (High-Speed Mode)					
$F_{(SCL)}$	I^2C clock frequency	1		2940	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time following a repeated START condition. After this time, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

Timing Diagram

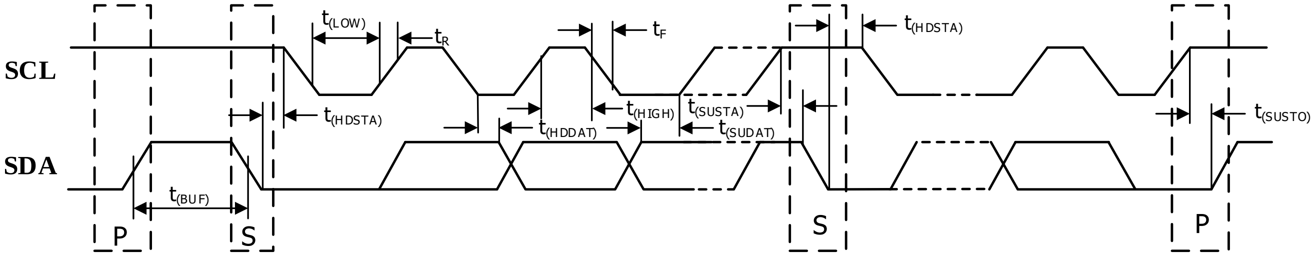
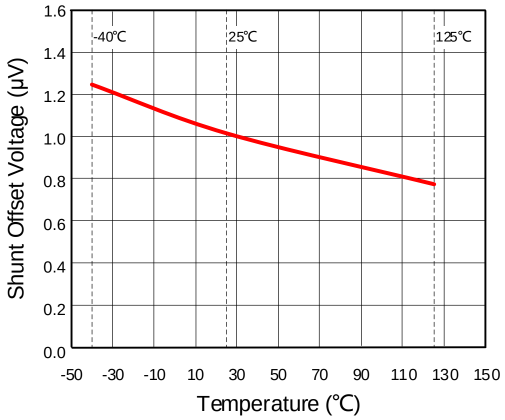
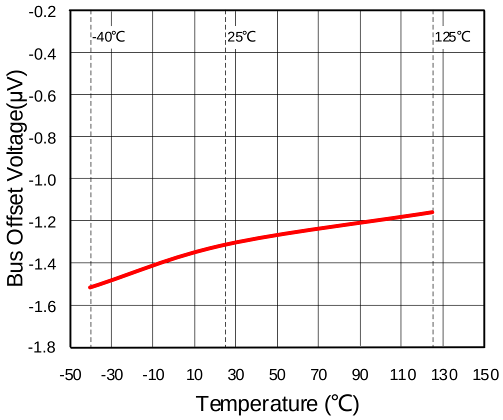


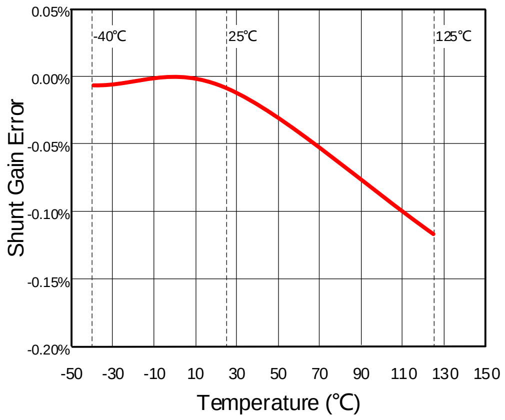
Figure 3. I^2C Timing Diagram

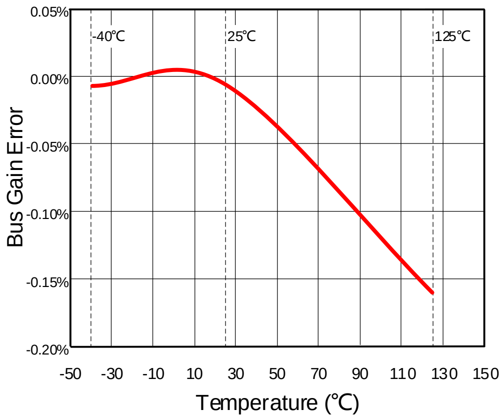
Typical Performance Characteristics

At T_A = 25 °C, VS = 3.3V, V_{SENSE} = V_{IN+} – $V_{IN–}$ = 0V, V_{CM} = $V_{IN–}$ = 48V，ADCRANGE = 01 (unless otherwise noted).


Shunt Offset Voltage vs. Temperature


Bus Offset Voltage vs. Temperature
(VBUS=20mV)


Shunt Voltage Gain Error vs. Temperature


Bus Voltage Gain Error vs. Temperature

Detailed Description

Overview

The SQ52206 is a digital current-sense amplifier equipped with an I^2C digital interface, designed to accurately measure shunt voltage, bus voltage, and internal temperature. These measurements enable precise calculations of current, power, energy, and charge, supporting accurate decision-making in controlled systems. The programmable registers offer flexibility in configuring measurement precision and selecting between continuous or triggered operation modes. For detailed register information refer to the Register Map section.

Block Diagram

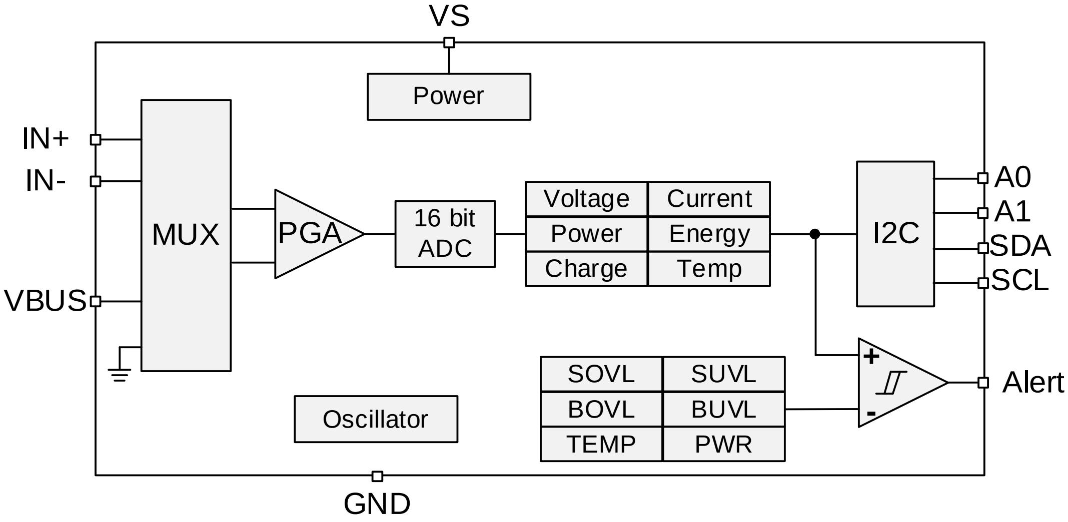


Figure 4. Functional Block Diagram

Feature Description

High Voltage Measurement Capability

The SQ52206 operates within a supply range of 2.7V to 5.5V and can measure voltage and current on rails as high as 120V. To measure current, the device detects the voltage drop across an external shunt resistor connected to the IN+ and IN- pins. The input stage of the SQ52206 is designed to accommodate input common-mode voltages higher than the device's supply voltage, V_S. This allows for a supported common-mode voltage range of -0.3V to +120V at the input pins, making the device suitable for both high-side and low-side current measurements. Notably, there are no specific power-supply sequencing requirements, as the common-mode input range and device supply voltage are independent of each other. Consequently, the bus voltage can be present even when the supply voltage is off, and vice versa, without risking any damage to the device.

In addition to current measurement, the SQ52206 also measures the bus supply voltage via the VBUS pin and incorporates an integrated temperature sensor for temperature measurement. The differential shunt voltage is measured between the IN+ and IN- pins, while the bus voltage is measured relative to the device's ground. The monitored bus voltages can span from 0V to 120V, while the monitored temperatures can range from -40ºC to +125ºC.

Internal Measurement and Calculation Engine

After measuring the shunt voltage, the SQ52206 device calculates the current and charge, while the power and energy calculations are based on the latest bus voltage measurement. If the value in the SHUNT_CAL register is zero, the reported power, energy, and charge values will be zero as well.

In *Figure **5***, current, voltage, and temperature values are immediately available when the number of averages is set to one. When averaging is enabled, each ADC measurement becomes an intermediate result stored in the corresponding averaging registers. After each ADC sample, the newly calculated current, voltage, and temperature values are added to their respective averaging registers until the desired number of averages is reached. Once all samples have been measured, the average current and voltage are determined, the power is calculated, and the results are loaded into the appropriate output registers for reading.

Energy and charge values occur with each conversion cycle; thus, the SQ52206's averaging function does not apply to these calculations. Power, charge, and energy calculations occur in the background and do not contribute to the overall conversion time.

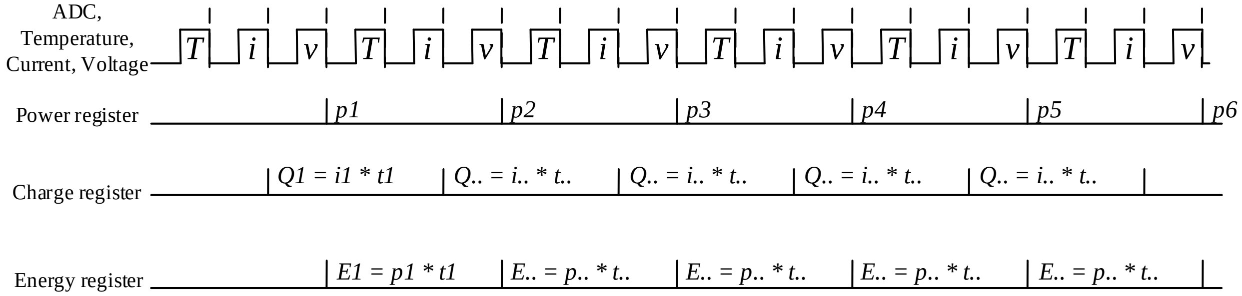


Figure 5. Power, Energy, and Charge Calculation Scheme

Low Bias Current

The SQ52206 offers the advantage of having an extremely low input bias current, which provides several benefits. This low input bias current greatly minimizes power consumption by the device in both active and shutdown states. This low bias current allows the use of input filters to eliminate high-frequency noise before the conversion of the signal into digital data. In conventional digital current-sense amplifiers, incorporating input filters often compromises accuracy. However, because of the low bias current of the SQ52206, the reduction in accuracy caused by input filters is mitigated. Additionally, the low bias current enables the use of a larger shunt resistor to accurately measure smaller currents. By utilizing a higher-value shunt resistor, the device is capable of precisely monitoring currents within the sub-mA range.

It is important to note that the bias current in the SQ52206 is the lowest when the sensed current is at zero. As the current begins to increase, there is a corresponding increase in the differential voltage drop across the shunt resistor, thereby causing an increase in the bias current.

High-Precision Delta-Sigma ADC

The SQ52206 integrates a high-performance, low-drift, low-offset delta-sigma ADC optimized for bidirectional current measurement on the shunt voltage measurement channel. The selection of measured inputs is achieved through a high-voltage input multiplexer that routes them to the ADC inputs. The architecture of the ADC ensures lower drift measurements across temperature and consistent offset measurements across variations in common-mode voltage, temperature, and power supply. The low-offset design provides near 0V offset voltage, maximizing the dynamic range in current-sensing applications.

The ADC conversion time for each input can be independently configured using the VSHCT, VBUSCT, and VTCT bits in the ADC_CONFIG register, ranging from 66μs to 8.23ms. Additionally, the SQ52206 incorporates a sample averaging function, which can be selected using the AVG bits in the ADC_CONFIG register, with a range of 1x to 1024x.

The SQ52206 can measure the bus voltage, shunt voltage, and die temperature, or a combination thereof, depending on the selected MODE bits setting in the ADC_CONFIG register. This flexibility allows for the configuration of the monitoring function to match specific application requirements. Without averaging, the converted values are immediately updated in their respective registers after an ADC conversion and can be read through the digital interface. The conversion time for each input is independently adjustable, ranging from 66μs to 8.23ms, based on the values programmed in the ADC_CONFIG register. Enabled measurement inputs are converted sequentially, so the total conversion time depends on the conversion time of each input and the number of enabled inputs. When averaging is enabled, intermediate values accumulate until the specified average count is reached, after which the final values update in the registers. These values remain in the data output registers until they are replaced by the next completed conversion results. It is important to note that reading the data output registers does not impact a conversion in progress.

The ADC offers two conversion modes: continuous and triggered, which can be set using the MODE bits in the ADC_CONFIG register. In continuous-conversion mode, the ADC continuously converts the input measurements and updates the output registers in a continuous loop. In triggered-conversion mode, the ADC performs the conversion as described above, and then enters shutdown mode until another single-shot trigger is generated by writing to the MODE bits. Writing to the MODE bits interrupts and restarts triggered or continuous conversions that are in progress. While the device can be read at any time, and the data from the last conversion remains accessible, the Conversion Ready flag (CNVRF bit in the DIAG_ALRT register) is provided to assist in coordinating triggered conversions. This flag is set after all conversions and averaging have been completed.

The Conversion Ready flag (CNVRF) clears under the following conditions:

- Writing to the ADC_CONFIG register (except for selecting shutdown mode)
- Reading the DIAG_ALRT Register

While operating in either conversion mode, the SQ52206 device utilizes a dedicated digital engine to calculate the current, power, charge, and energy values in the background, as explained in the Internal Measurement and Calculation Engine section. In triggered mode, the accumulation registers (ENERGY and CHARGE) are not updated, as the device does not keep track of elapsed time. Therefore, for applications requiring precise measurements regarding the accumulation of time for energy and charge, it is necessary to configure the device to use continuous conversion mode. In this mode, the accumulated results are continuously updated, providing an accurate charge and energy consumption in a system. All calculations are performed in the background and do not affect the conversion time.

For applications that require synchronization with other components in the system, the SQ52206 conversion can be delayed by programming the CONVDLY bits in the CONFIG register, within the range of 0 (no delay) to 522.24ms. The resolution for programming the conversion delay is 2.048 ms, with a default setting of 0. This conversion delay feature can assist in synchronizing measurements when multiple external devices are used for voltage or current monitoring. By introducing a delay in the current measurement, it is possible to align the external voltage and current measurements to occur at approximately the same time. While the internal time base for the ADC is precise, synchronization may be lost over time due to internal and external time base mismatch.

The ADC conversion times for shunt voltage, bus voltage, and temperature can be set independently within a range of 66μs to 8.23ms. This flexibility in conversion time allows for reliable operation in various noisy environments. Additionally, the device offers programmable averaging times, ranging from a single conversion to an average of 1024 conversions. The selected amount of averaging applies uniformly to all active measurement inputs. By increasing the conversion time and the number of averages, the effective resolution of the SQ52206 ADC can be enhanced.

Shunt Resistor Drift Compensation

The SQ52206 device is equipped with an internal temperature sensor, allowing for die temperature measurement within the range of -40°C to +125°C. The accuracy of this temperature sensor is ±2°C across the entire operational temperature range. The temperature value is stored in the DIETEMP register and can be accessed through the digital interface.

In addition, the device is capable of utilizing the temperature measurement to compensate for any variance in the shunt resistor due to temperature. To enable this feature, the TEMPCOMP bit in the CONFIG register must be set. The SHUNT_TEMPCO register can be programmed to input the temperature coefficient of the shunt resistor used. The full-scale value of the SHUNT_TEMPCO register is 16384ppm/°C. It is important to note that the temperature compensation is referenced to +25 °C. The shunt resistor is assumed to have a positive temperature coefficient, and the temperature compensation follows Equation 1:

$$R_{ADJ} = R_{NOM} + \frac{R_{NOM} \text{ x } (\text{DIETEMP} - 25) \text{ x } \text{SHUNT\_TEMPCO}}{10^6} \qquad (1)$$

Where:

- RNOM is the nominal shunt resistance in Ω at 25 °C.
- DIETEMP is the temperature value in the DIETEMP register in °C.
- SHUNT_TEMPCO is the shunt temperature coefficient in ppm/°C.

Once this feature is enabled and properly configured, the data in the CURRENT register is adjusted by continuously monitoring the die temperature, resulting in a temperature-dependent function. The effectiveness of this compensation is contingent upon the degree of thermal coupling between the resistor and the SQ52206, as the compensation utilizes the die temperature of the SQ52206 itself.

Integrated Precision Oscillator

The device utilizes an internal oscillator to establish its internal time base, which is precisely calibrated to maintain a tolerance of less than 0.5% at room temperature. This highly accurate oscillator serves as the timing source for ADC conversions and is also used for calculating energy and charge. While temperature variations can affect the digital filter response, the precise clock ensures consistent filter response and notch frequency across varying temperatures.

Multi-Alert Monitoring and Fault Detection

The SQ52206 is equipped with a multipurpose ALERT output pin configured in an open-drain mode. This pin can report various diagnostics or function as an indicator to signal the completion of ADC conversions in both triggered and continuous conversion modes. The ALERT pin continually monitors the diagnostics listed in Table 1 and can signal out-of-range conditions when the measured values are crossing their respective thresholds, providing the means of reporting these monitored values.

Table 1. ALERT Diagnostics Description

SQ52206 Diagnostic	Status Bit in Diag_Alert Register (Ro)	Out-Of-Range Threshold Register (R/W)	Register Default Value
Shunt Under Voltage Limit	SHNTUL	SUVL	0x8000 h (two's complement)
Shunt Over Voltage Limit	SHNTOL	SOVL	0x7FFF h (two's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (two's complement, positive values only)
Temperature Over-Limit	TMPOL	TEMP_LIMIT	0xFFFF h (two's complement, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (two's complement)

A read of the DIAG_ALRT register is used to determine which diagnostic has triggered the ALERT pin. This register, shown in Table 15, is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert Latch Enable: When the ALERT pin is triggered, this function holds the pin value even after all diagnostic conditions are cleared. Reading the DIAG_ALRT register resets the status of the ALERT pin. This function is activated by setting the ALATCH bit.
- Conversion Ready Enable: Setting the CNVR bit enables the ALERT pin to assert when an ADC conversion is complete and output values are ready to be read through the digital interface. Conversion completion events can also be checked through the CNVRF bit, regardless of the CNVR bit setting.
- Alert Comparison on Averaged Output: This feature enables the averaged ADC output data to be compared against the out-of-range threshold value, reducing the likelihood of false alerts due to noise. By using the averaged data, noise is filtered out, but it introduces a delay in diagnostics due to the time needed for averaging. This functionality is activated by setting the SLOWALERT bit.
- Alert Polarity: This setting allows inversion of the active state of the ALERT pin. By default, the ALERT pin is active-low and operates as on open-drain output requiring a pull-up resistor. To configure the pin for active-high operation, set the APOL control bit.

The following diagnostic functions are not reported by the ALERT pin but can be accessed by reading the DIAG_ALRT register:

- Math Overflow: The MATHOF bit indicates that an arithmetic operation has caused an internal register overflow.
- Energy Overflow: The ENERGYOF bit signals that the ENERGY register has overflowed due to data accumulation.
- Charge Overflow: The CHARGEOF bit indicates that the CHARGE register has overflowed due to data accumulation.

When configured to report ADC conversion complete events, the ALERT pin functions as a multipurpose reporting output. For example, as shown in Figure 6, the ALERT pin can simultaneously report ADC conversion complete events alongside conditions such as shunt overvoltage (overcurrent) events, bus under voltage events, overtemperature events, and over-power-limit events on the SQ52206 device.

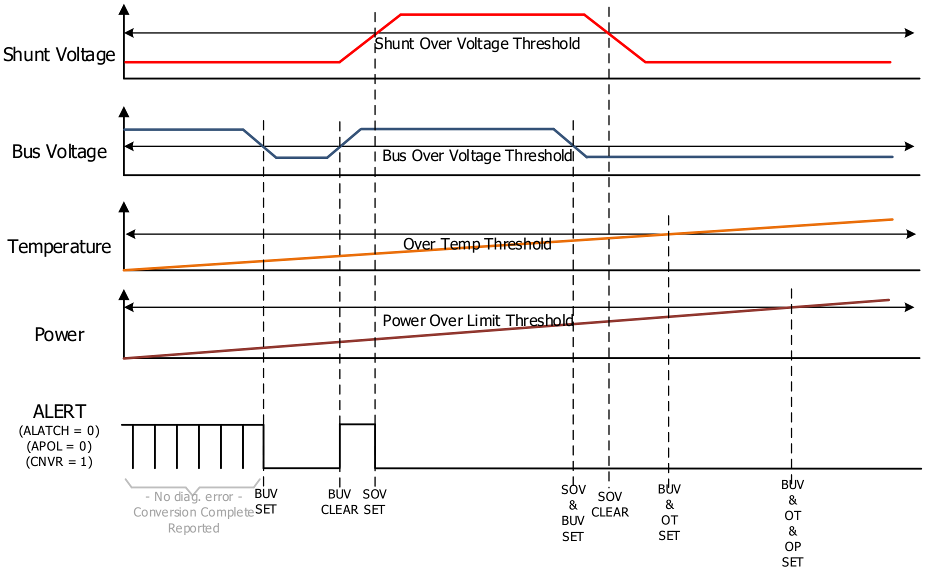


Figure 6. Multi-Alert Configuration

Device Functional Modes

Shutdown Mode

Apart from the continuous and triggered conversion modes, the SQ52206 device offers a shutdown mode (determined by the MODE bits in the ADC_CONFIG register) to minimize quiescent current to below 5μA. In this mode, the device discontinues current input, reducing power consumption when not in use. Despite being in shutdown mode, the device allows for read and write operations on its registers. The device remains in shutdown mode until it receives another command for triggered or continuous conversion.

While in shutdown mode, the device can be triggered to perform conversions. Once triggered, the ADC initiates the conversion process, and upon completion, the device reverts to the shutdown state.

It is important to note that the shutdown current is specified with an inactive communication bus. If clock and data activity on the bus is present, the current consumption will increase with the bus frequency.

Power-On Reset

When the voltage supply (VS) falls below 1.26V (typically), the power-on reset (POR) is triggered, resulting in a reset of all registers to their default values. To initiate a manual reset of the device, the RST bit in the CONFIG register can be set. The default values for each register are shown in the reset column for each register description. The register descriptions can be found in the Register Map section.

Programming

I²C Serial Interface

The SQ52206 functions exclusively as a peripheral device on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. These lines are equipped with integrated noise suppression filters and Schmitt triggers to ensure reliable operation. While the device incorporates noise suppression on its digital I/O lines, proper layout techniques are also important in reducing coupling into the communication lines. Coupling may occur due to capacitive coupling signal edges between the communication lines or other switching noise sources within the system. Routing traces in parallel with a ground plane between layers on the PCB is typically effective in mitigating coupling effects. The use of shielded communication lines also helps prevent unintended noise coupling into the digital I/O lines, which could lead to incorrect interpretation as start or stop commands.

The SQ52206 supports the transmission protocols for fast mode (1 kHz to 400 kHz) and high-speed mode (1 kHz to 2.94MHz). Data bytes are transmitted in the order of most significant byte first, following the SMBus 3.0 transfer protocol.

To communicate with the SQ52206, the controller device must first address the peripheral device by sending a device address byte. The peripheral device address byte consists of seven address bits and a direction bit to indicate whether the operation is a read or write.

The device is equipped with two address pins, A0 and A1. Table 2 provides the logic levels for each of the 16 possible addresses. The device samples the state of A0 and A1 pins during each bus communication. It is essential to set the pin states before any activity occurs on the interface when connecting the SDA pin to either A0 or A1 for device addressing. Additionally, a hold time of 100ns is required on the most significant bit (MSB) of the I^{2}C address to ensure accurate device addressing.

Table 2. Address Pins and Secondary Device Addresses

A1	A0	TARGET ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Writing to and Reading from the I^{2}C Serial Interface

To access a specific SQ52206 register, the appropriate value must be written to the register pointer. For a comprehensive list of registers and their respective addresses, please consult Table 2. As shown in *Figure **9***, after transmitting the target address byte with the R/W bit low, the first byte transferred represents the value of the register pointer. It is important to note that every write operation to the device requires a value for the register pointer to be provided.

The process of writing to a register begins with the transmission of the first byte by the controller. This byte comprises the target address, with the R/W bit set to low. The peripheral device then acknowledges the receipt of the valid address. The following byte transmitted specifies the register address, updating the register pointer to the desired location. Following this, the controller writes two bytes to the register indicated by the register pointer, with the device acknowledging the receipt of each data byte. The controller has the option to conclude the data transfer by generating a start or stop condition.

During a read operation from the device, the register pointer's last written value determines which register will be read. To modify the register pointer for a read operation, a new value must be written to it. This can be achieved by sending a target address byte with the R/W bit low, followed by the register pointer byte. No additional data is required in this write. Following this, the controller generates a start condition and sends the target address byte with the R/W bit high to initiate the read command. The peripheral then transmits the most significant byte of the register indicated by the register pointer, followed by an acknowledgment from the controller. The least significant byte is then transmitted by the peripheral, and the controller acknowledges the receipt of the data byte. The controller has the option to terminate the data transfer by generating a Not-Acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to repeatedly send the register pointer bytes as the device retains the register pointer value until it is changed by the next write operation.

Figure 7 illustrates the timing diagram for a write operation, while *Figure 8* depicts the timing diagram for a read operation.

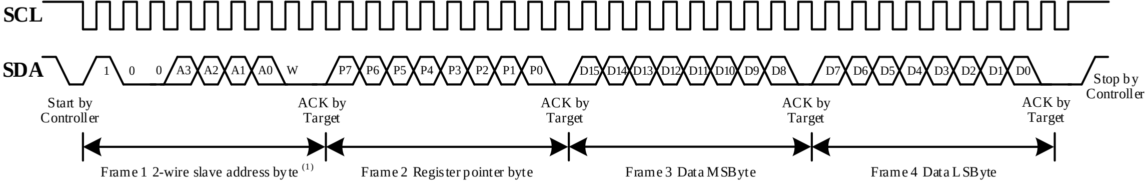


Figure 7. Timing Diagram for Write Word Format

Note: Peripheral Device Address byte value is determined by the configuration of the A0 and A1 pins. See Table 2 for details.

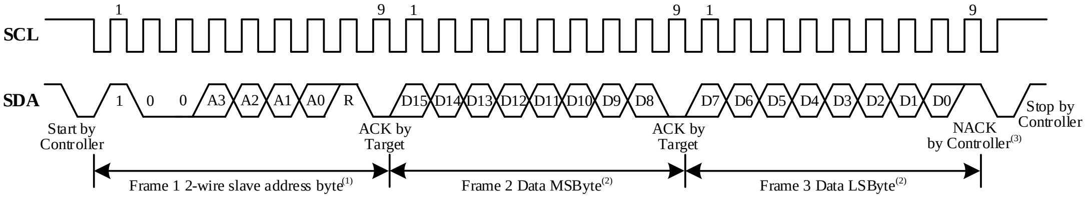


Figure 8. Timing Diagram for Read Word Format

Notes:

- The Peripheral Device Address byte value is determined by the configuration of the A0 and A1 pins. See Table 2 for details.
- Read data is retrieved from the last register pointer location. To read from a different register, the register pointer must be updated first. See Figure 9.
- An ACK can also be sent by the controller.

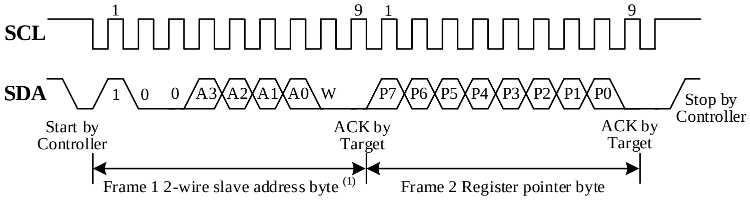


Figure 9. Typical Register Pointer Set

Note: The Peripheral Device Address byte value is determined by the configurations of the A0 and A1 pins. See Table 2 for details.

High-Speed I²C Mode

During bus idle time, both the SDA and SCL lines are pulled high by the pull-up resistors. The controller initiates a start condition, followed by the transmission of a valid serial byte that contains the high-speed (HS) main device code 00001XXX. This transmission occurs in either fast (400 kHz) or standard (100 kHz) (F/S) mode, with a maximum frequency of 400kHz. While the device does not acknowledge the HS main device code, it recognizes the code and adjusts its internal filters to enable operation at 2.94MHz.

The controller then generates a repeated start condition, identical in timing to the initial start condition. From this point, the protocol follows the standard F/S mode but allows transmission speeds of up to 2.94 MHz To maintain HS mode, repeated start conditions are used instead of a stop condition. A stop condition terminates HS mode and resets all internal filters to support F/S mode.

SMBus Alert Response

The SQ52206 is specifically designed to respond to the SMBus Alert Response address, enabling efficient fault detection in simple peripheral devices. When an Alert occurs, the controller sends out the Alert Response peripheral device address (0001 100) with the Read/Write bit set to high. Devices that issued an alert acknowledge the Alert Response and transmit their address on the bus, thereby identifying themselves.

Similar to the I²C General Call, the Alert Response can activate multiple peripheral devices simultaneously. In the event that more than one peripheral device attempts to respond, bus arbitration rules apply. The losing device will not generate an Acknowledge and will continue to hold the Alert line low until it successfully wins arbitration.

Register Map

SQ52206 Registers

Table 3 provides a list of the SQ52206 registers. Any register locations not included in Table 3 are reserved locations and should not be modified.

Table 3. Registers Map

Address	Acronym	Register Name	Size (bits)
0h	CONFIG	Configuration	16
1h	ADC_CONFIG	ADC Configuration	16
2h	SHUNT_CAL	Shunt Calibration	16
3h	SHUNT_TEMPCO	Shunt Temperature Coefficient	16
4h	VSHUNT	Shunt Voltage Measurement	16
5h	VBUS	Bus Voltage Measurement	16
6h	DIETEMP	Temperature Measurement	16
7h	CURRENT	Current Result	16
8h	POWER	Power Result	24
9h	ENERGY	Energy Result	40
Ah	CHARGE	Charge Result	40
Bh	DIAG_ALRT	Diagnostic Flags and Alert	16
Ch	SOVL	Shunt Overvoltage Threshold	16
Dh	SUVL	Shunt Undervoltage Threshold	16
Eh	BOVL	Bus Overvoltage Threshold	16
Fh	BUVL	Bus Undervoltage Threshold	16
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16
11h	PWR_LIMIT	Power Over-Limit Threshold	16
20h	PWR_PEAK	Power Peak Value	24

Configuration (CONFIG) Register (Address = 0h) [reset = 0005h]

The CONFIG register is shown in Table 4.

Table 4. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to 1 initiates a system reset, equivalent to a power-on reset, and resets all registers to their default values. 0h = Normal operation; no reset is performed. 1h = System reset; all registers are reset to default values This bit self-clears after the reset is completed.
14	RSTACC	R/W	0h	Resets the contents of the ENERGY and CHARGE accumulation registers to 0 0h = Normal operation; no reset is performed. 1h = Resets the contents of the ENERGY and CHARGE accumulation registers to 0.
13-6	CONVDLY	R/W	0h	Configures the delay before the initial ADC conversion, adjustable in steps of 2.048ms. 0h = 0s

				1h = 2.048ms FFh = 522.24ms
5	TEMPCOMP	R/W	0h	Enables temperature compensation of an external shunt 0h = Shunt temperature compensation disabled 1h = Shunt temperature compensation enabled
4-3	ADCRANGE	R/W	0h	Configures the shunt full-scale voltage range across IN+ and IN–. 0h = ±163.84 mV 1h = ± 81.92mV 2h/3h = ± 40.96mV
2-0	RESERVED	R	7h	Reserved. Always reads 5.

ADC Configuration (ADC_CONFIG) Register (Address = 1h) [reset = FB68h]

The ADC_CONFIG register is shown in Table 5.

Table 5. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	The MODE bits determine the measurement type and operation mode for bus voltage, shunt voltage, or temperature measurement. 0h = Shutdown 1h = Triggered bus voltage, single-shot 2h = Triggered shunt voltage, single-shot 3h = Triggered shunt voltage and bus voltage, single-shot 4h = Triggered temperature, single-shot 5h = Triggered temperature and bus voltage, single-shot 6h = Triggered temperature and shunt voltage, single-shot 7h = Triggered bus voltage, shunt voltage, and temperature, single-shot 8h = Shutdown 9h = Continuous bus voltage only Ah = Continuous shunt voltage only Bh = Continuous shunt and bus voltage Ch = Continuous temperature only Dh = Continuous bus voltage and temperature Eh = Continuous temperature and shunt voltage Fh = Continuous bus voltage, shunt voltage, and temperature
11-9	VBUSCT	R/W	5h	Configures the conversion time for bus voltage measurements: 0h = 66µs 1h = 118µs 2h = 310µs 3h = 566µs 4h = 1070µs 5h = 2090µs 6h = 4140µs 7h = 8230µs
8-6	VSHCT	R/W	5h	Configures the conversion time for temperature measurements: 0h = 66µs 1h = 118µs 2h = 310µs 3h = 566µs 4h = 1070µs 5h = 2090µs 6h = 4140µs 7h = 8230µs
5-3	VTCT	R/W	5h	Configures the conversion time for temperature measurements:

				0h = 66μs 1h = 118μs 2h = 310μs 3h = 566μs 4h = 1070μs 5h = 2090μs 6h = 4140μs 7h = 8230μs
2-0	AVG	R/W	0h	Specifies the number of samples used for averaging count, applied to all active inputs. When >0h, the output registers are updated after averaging is completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

Shunt Calibration (SHUNT_CAL) Register (Address = 2h) [reset = 1000h]

The SHUNT_CAL register is shown in Table 6.

Table 6. SHUNT_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved. Always reads 0.
14-0	SHUNT_CAL	R/W	1000h	This register sets the conversion constant value representing the shunt resistance, enabling the calculation of current in amperes. It also determines the resolution of the CURRENT register. Refer to the Internal Measurement and Calculation Engine section for details on value calculation.

Shunt Temperature Coefficient (SHUNT_TEMPCO) Register (Address = 3h) [reset = 0h]

The SHUNT_TEMPCO register is shown in Table 7.

Table 7. SHUNT_TEMPCO Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved. Always reads 0.
14-0	TEMPCO	R/W	1000h	Temperature coefficient of the shunt for temperature compensation correction. Calculated relative to +25 °C. The full-scale value of the register is 16383 ppm/°C. The 16-bit register provides a resolution of 1ppm/°C/LSB 0h = 0 ppm/°C 3FFFh = 16383 ppm/°C

Shunt Voltage Measurement (VSHUNT) Register (Address = 4h) [reset = 0h]

The VSHUNT register is shown in Table 8.

Table 8. VSHUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0h	The measured differential voltage across the shunt is represented as a two’s complement value. Conversion factor: 5μV/LSB: When ADCRANGE = 00 2.5μV/LSB: When ADCRANGE = 01 1.25μV/LSB: When ADCRANGE = 10/11

Bus Voltage Measurement (VBUS) Register (Address = 5h) [reset = 0h]

The VBUS register is shown in Table 9.

Table 9. VBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0h	The bus voltage output is represented as a two's complement value but is always positive. Conversion factor: 3.75 mV/LSB

Temperature Measurement (DIETEMP) Register (Address = 6h) [reset = 0h]

The DIETEMP register is shown in Table 10.

Table 10. DIETEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DIETEMP	R	0h	The internal die temperature measurement is represented as a two's complement value. Conversion factor: 7.8125 m°C/LSB

Current Result (CURRENT) Register (Address = 7h) [reset = 0h]

The CURRENT register is shown in Table 11.

Table 11. CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0h	The calculated current output, in amperes, is represented as a two's complement value. Refer to the Internal Measurement and Calculation Engine section for details on value description.

Power Result (POWER) Register (Address = 8h) [reset = 0h]

The POWER register is shown in Table 12.

Table 12. POWER Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	The power output is calculated and represented as an unsigned, always positive, value in watts. Refer to the Internal Measurement and Calculation Engine section for details on value description.

Energy Result (ENERGY) Register (Address = 9h) [reset = 0h]

The ENERGY register is shown in Table 13.

Table 13. ENERGY Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	ENERGY	R	0h	The calculated energy output value is represented as an unsigned, always positive, value in Joules. Refer to the Internal Measurement and Calculation Engine section for details on value description.

Charge Result (CHARGE) Register (Address = Ah) [reset = 0h]

The CHARGE register is shown in Table 14.

Table 14. CHARGE Register Field Descriptions

Bit	Field	Type	Reset	Description
39-0	CHARGE	R	0h	The calculated charge output value, in Coulombs, is represented as a two's complement value. Refer to the Internal Measurement and Calculation Engine section for details on value description.

Diagnostic Flags and Alert (DIAG_ALRT) Register (Address = Bh) [reset = 0001h]

The DIAG_ALRT register is shown in Table 15.

Table 15. DIAG_ALRT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ALATCH	R/W	0h	This setting determines the behavior of the Alert pin and Alert Flag bit after a fault occurs. 0h (Transparent Mode) = The Alert pin and flag reset to the idle state once the fault is cleared. 1h (Latch Mode) = The Alert pin and flag remain active after a fault until the DIAG_ALRT register is read.
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to reflect the status of the Conversion Ready Flag (bit 1), signaling that a conversion cycle has been completed. 0h = Disable the Conversion Ready Flag on the ALERT pin 1h = Enable the Conversion Ready Flag on the ALERT pin
13	SLOWALERT	R/W	0h	Configures whether the ALERT function is based on averaged or non-averaged values, providing flexibility to delay the ALERT until after the averaged value. 0h = Compare the ALERT function to the non-averaged (ADC) value 1h = Compare the ALERT function to the averaged value
12	APOL	R/W	0h	This Alert Polarity bit configures the polarity of the Alert pin. 0h = Normal mode (active-low, open-drain) 1h = Inverted mode (active-high, open-drain)
11	ENERGYOF	R	0h	This bit reflects the health of the ENERGY register. 0h = Normal operation; no overflow 1h = Overflow detected in the 40-bit ENERGY register Clears automatically when the ENERGY register is read.
10	CHARGEOF	R	0h	This bit reflects the health of the CHARGE register. If the 40-bit CHARGE register has overflowed this bit is set to 1. 0h = Normal operation; no overflow 1h = Overflow detected in the 40-bit CHARGE register

				Clears automatically when the CHARGE register is read.
9	MATHOF	R	0h	This bit is set to 1 when an arithmetic operation causes an overflow error, indicating that current and power data may be invalid. 0h = Normal operation; no overflow 1h = Overflow error occurred Must be manually cleared by clearing the accumulators with the RSTACC bit, or by triggering another conversion.
8	RESERVED	R	0h	Reserved. Always read 0.
7	TMPOL	R	0h	This bit indicates whether the temperature measurement exceeds the threshold defined in the temperature over-limit register. 0h = Normal operation 1h = Over-temperature event detected When ALATCH = 1, this bit is cleared by reading this register.
6	SHNTOL	R	0h	This bit indicates whether the shunt voltage measurement exceeds the threshold defined in the shunt over-limit register. 0h = Normal operation 1h = Over shunt voltage event detected When ALATCH =1, this bit is cleared by reading this register.
5	SHNTUL	R	0h	This bit indicates whether the shunt voltage measurement falls below the threshold defined in the shunt under-limit register. 0h = Normal 1h = Under shunt voltage event detected When ALATCH =1, this bit is cleared by reading this register.
4	BUSOL	R	0h	This bit indicates whether the bus voltage measurement exceeds the threshold defined in the bus over-limit register. 0h = Normal operation 1h = Bus over-limit event detected When ALATCH =1, this bit is cleared by reading this register.
3	BUSUL	R	0h	This bit indicates whether the bus voltage measurement falls below the threshold defined in the bus under-limit register. 0h = Normal operation 1h = Bus under-limit event detected When ALATCH =1, this bit is cleared by reading this register.
2	POL	R	0h	This bit indicates whether the power measurement exceeds the threshold defined in the power limit register. 0h = Normal operation 1h = Power over-limit event detected When ALATCH =1, this bit is cleared by reading this register.
1	CNVRF	R	0h	This bit shows whether a conversion has been completed. 0h = Normal operation; conversion is not complete 1h = Conversion is complete When ALATCH =1, this bit is cleared by either reading this register or starting a new triggered conversion.
0	RESERVED	R	0h	Reserved. Always reads 0.

Shunt Overvoltage Threshold (SOVL) Register (Address = Ch) [reset = 7FFFh]

If negative values are entered into this register, an alarm will trigger when the shunt voltage measurement reaches 0V. When using negative values for the shunt undervoltage and overvoltage thresholds, ensure that the overvoltage threshold is set to the larger (i.e., less negative) value. Details for the SOVL register are provided in Table 16.

Table 16. SOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SOVL	R/W	7FFFh	This register sets the threshold for detecting shunt overvoltage (overcurrent protection) using a two's complement value. Conversion Factors: 5 μV/LSB when ADCRANGE = 00; 2.5μV/LSB when ADCRANGE = 01; 1.25μV/LSB when ADCRANGE = 10/11.

Shunt Undervoltage Threshold (SUVL) Register (Address = Dh) [reset = 8000h]

The SUVL register is shown in Table 17.

Table 17. SUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SUVL	R/W	8000h	This register sets the threshold for detecting shunt undervoltage (undercurrent protection) using two's complement value. Conversion Factors: 5 μV/LSB when ADCRANGE = 00; 2.5μV/LSB when ADCRANGE = 01; 1.25μV/LSB when ADCRANGE = 10/11.

Bus Overvoltage Threshold (BOVL) Register (Address = Eh) [reset = 7FFFh]

The BOVL register is shown in Table 18.

Table 18. BOVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	This register sets the threshold for detecting bus overvoltage (overvoltage protection) using an unsigned, positive value. Conversion factor: 3.75mV/LSB.

Bus Undervoltage Threshold (BUVL) Register (Address = Fh) [reset = 0h]

The BUVL register is shown in Table 19.

Table 19. BUVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BUVL	R/W	0h	This register sets the threshold for detecting bus undervoltage (undervoltage protection) using an unsigned, positive value. Conversion factor: 3.75mV/LSB.

Temperature Over-Limit Threshold (TEMP_LIMIT) Register (Address = 10h) [reset = 7FFFh]

The TEMP_LIMIT register is shown in Table 20.

Table 20. TEMP_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TOL	R/W	7FFFh	This register sets the threshold for detecting overtemperature conditions using a two's complement value. The entered value is compared directly against the reading in the DIETEMP register to determine if an overtemperature condition exists. Conversion factor: 7.8125m°C/LSB.

Power Over-Limit Threshold (PWR_LIMIT) Register (Address = 11h) [reset = FFFFh]

The PWR_LIMIT register is shown in Table 21.

Table 21. PWR_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	This register sets the threshold for detecting power over-limit measurements using an unsigned, positive value. The entered value is compared directly against the POWER register to determine if an over-power condition exists. Conversion factor: 256 × Power LSB.

Power Peak Value (PWR_PEAK) Register (Address = 20h) [reset = 0h]

The PWR_PEAK register is shown in Table 22.

Table 22. PWR_PEAK Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	PWR_PEAK	R	0h	This register records the peak power using an unsigned, positive value.

Application and Implementation

Application Information

Device Measurement Range and Resolution

The SQ52206 device provides two selectable input ranges for shunt voltage measurements. The full-scale differential input across the IN+ and IN– pins can be set to either ±163.84mV or ±40.96mV, depending on the ADCRANGE bit in the CONFIG register. The bus voltage measurement range spans from 0V to 120V, while the internal die temperature sensor covers a range of –256°C to +256°C, though the device package limits this range to–40°C to 125°C.

Table outlines the full-scale voltage ranges for shunt, bus, and temperature measurements, along with their respective step sizes.

Table 23. ADC Full Scale Values

Parameter	Full-Scale Value	Resolution
Shunt voltage	±163.84 mV (ADCRANGE = 00)	5μV/LSB
	±81.92 mV (ADCRANGE = 01)	2.5μV/LSB
	±40.96 mV (ADCRANGE = 10/11)	1.25μV/LSB
Bus voltage	0 V to 120 V	3.75mV/LSB
Temperature	–40 °C to +125 °C	7.8125 m°C/LSB

The device's shunt voltage, bus voltage, and temperature measurements can be accessed via the VSHUNT, VBUS, and DIETEMP registers, respectively. Both the VSHUNT and VBUS registers provide 16-bit digital outputs. Due to the bidirectional nature of currents in the system, the shunt voltage measurement in VSHUNT can be positive or negative, though the VBUS value is always positive. Voltage values can be calculated by multiplying the digital value by the corresponding resolution size.

The DIETEMP register also provides a 16-bit digital output, which can be converted to °C by multiplying by its resolution size. This temperature output value can be either positive or negative.

Additionally, the device offers the capability to report calculated values for current (in amperes), power (in watts), charge (in coulombs), and energy (in joules). For more details about these calculations, refer to the Current, Power, Energy, and Charge Calculations section.

Current, Power, Energy, and Charge Calculations

To obtain current measurements in amperes for the SQ52206 device, a constant conversion value must be written to the SHUNT_CAL register. This value is determined by the maximum measured current and the shunt resistance used in the application. The calculation for the SHUNT_CAL register is provided in Equation 2.

The term CURRENT_LSB represents the step size for the CURRENT register, which stores the measured current in amperes. As shown in Equation 3, CURRENT_LSB is calculated based on the maximum expected current and determines the resolution of the CURRENT register. While selecting a smaller CURRENT_LSB value results in higher resolution, it is common to choose a round-number value (up to eight times higher than the smallest possible value) to simplify CURRENT conversions.

The term RSHUNT represents the resistance of the external shunt used to generate the differential voltage across the IN+ and IN– pins. Use Equation 2 to calculate SHUNT_CAL when ADCRANGE = 0. For ADCRANGE = 01, the value of SHUNT_CAL must be multiplied by 2. For ADCRANGE = 10/11, the value of SHUNT_CAL must be multiplied by 4.

$$\text{SHUNT\_CAL} = 819.2 \times 10^{6} \times \text{CURRENT\_LSB} \times \text{RSHUNT} \tag{2}$$

Where:

- 819.2×10^6 is a fixed internal value used to ensure proper scaling is maintained.
- the value of SHUNT_CAL must be multiplied by 2 for ADCRANGE = 01.
- the value of SHUNT_CAL must be multiplied by 4 for ADCRANGE = 10/11.

$$\text{CURRENT\_LSB} = \frac{\text{Maximum Expected Current}}{2^{15}} \tag{3}$$

The current measurement is calculated based on the shunt voltage measurement and the value programmed in the SHUNT_CAL register. If the SHUNT_CAL register is set to zero, the CURRENT register will also report a value of zero.

Once the SHUNT_CAL register is programmed with the calculated value, the measured current in amperes can be read from the CURRENT register. The final current value is scaled by CURRENT_LSB, as shown in Equation 4:

$$\text{Current [A]} = \text{CURRENT\_LSB} \times \text{CURRENT} \tag{4}$$

Where:

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as a 24-bit value and converted to Watts by using Equation 5:

$$\text{Power [W]} = 0.24 \times \text{CURRENT\_LSB} \times \text{POWER} \tag{5}$$

Where:

- POWER is the value read from the POWER register.
- CURRENT_LSB is the LSB size of the current calculation, defined by Equation 3.

The ENERGY register provides a 40-bit unsigned value representing energy in Joules units. The energy in joules can be calculated using Equation 6:

$$\text{Energy [J]} = 16 \times 0.24 \times \text{CURRENT\_LSB} \times \text{ENERGY} \tag{6}$$

The CHARGE register provides a 40-bit two's complement value representing charge in Coulombs. The charge in coulombs is calculated using Equation 7:

$$\text{Charge [C]} = \text{CURRENT\_LSB} \times \text{CHARGE} \tag{7}$$

Where:

- CHARGE is the value read from the CHARGE register.
- CURRENT_LSB is the LSB size of the current calculation, defined by Equation 3.

When an overflow occurs, the ENERGY and CHARGE registers will roll over and restart from zero. These registers can also be manually reset at any time by setting the RSTACC bit in the CONFIG register.

Application Schematic

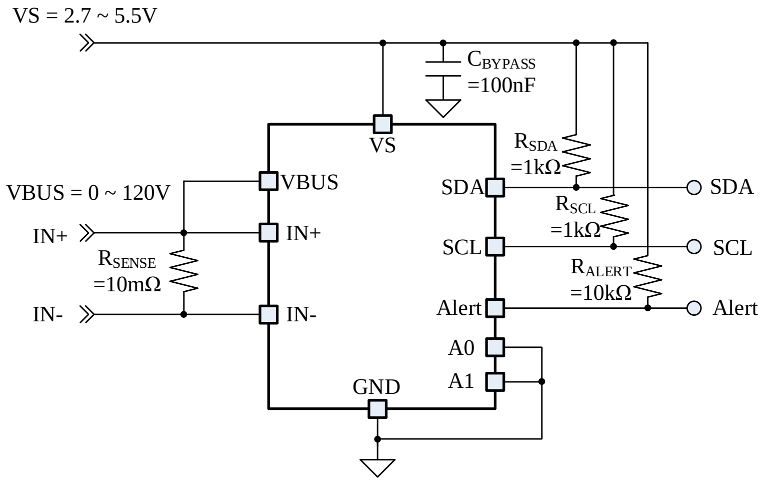


Figure 10. I^{2}C /SMBus Application Schematic

BOM List

Designator	Description	Part Number	MFR
C_{BYPASS}	100nF/50V/X7R, 0603	GCJ188R71H104KA12D	muRata
R_{SENSE}	10mΩ/1W, 1%, 2512	RL2512FK-070R01L	YAGEO
R_{SDA}, R_{SCL}	1kΩ, 1%, 0603		
R_{ALERT}	10kΩ, 1%, 0603		

Layout Design

Follow these PCB layout guidelines for optimal performance:

- Use a Kelvin connection to connect the input pins to the current-sensing resistor RSENSE. This method minimizes errors caused by parasitic resistance from poor PCB routing, ensuring only RSENSE impedance is detected between the input pins.
- Minimize the loop formed by these connections.
- Place a bypass capacitor (a 0.1μF MLCC is recommended) as close as possible to the VCC and GND pins.

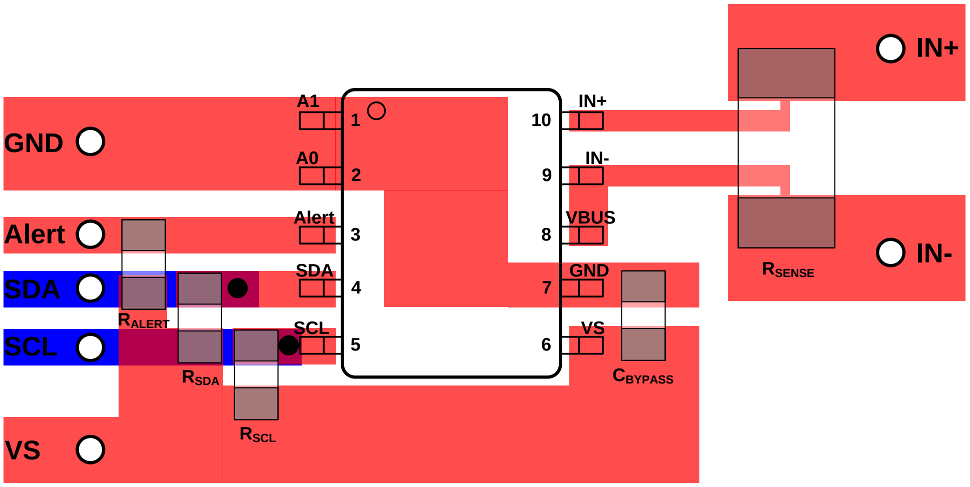
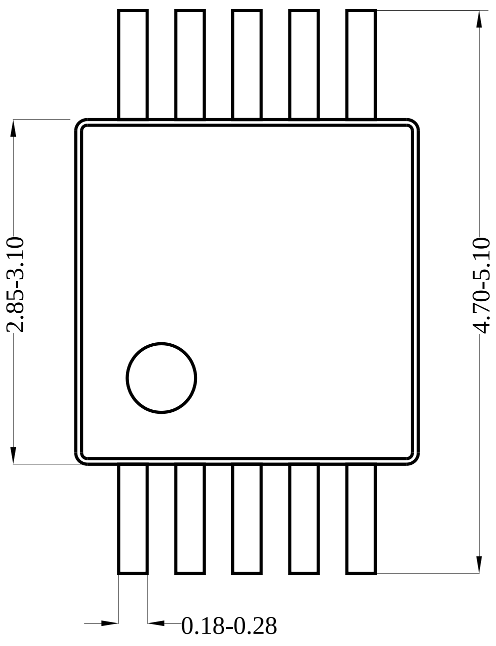
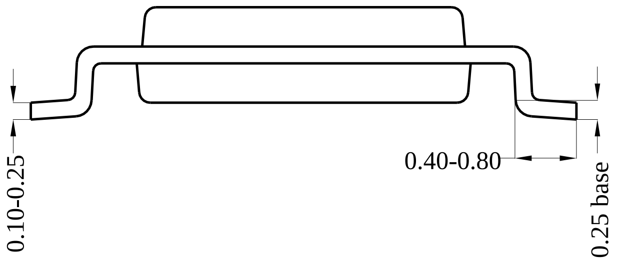


Figure 11. Suggested PCB Layout

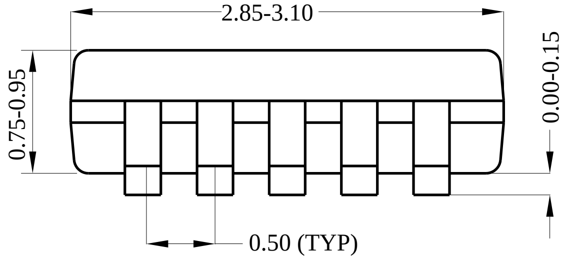
MSOP10 Package Outline & PCB Layout



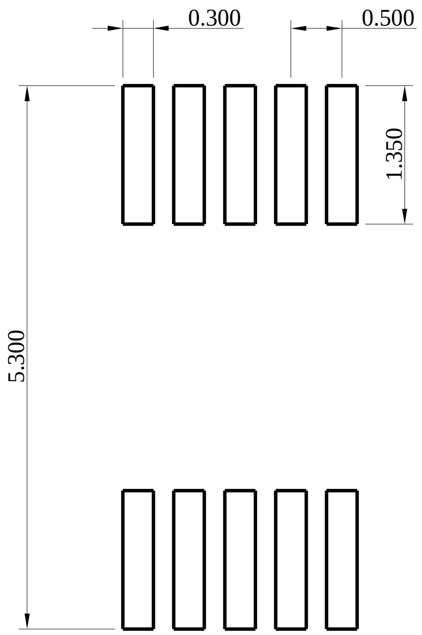
Top View



Side View



Front View



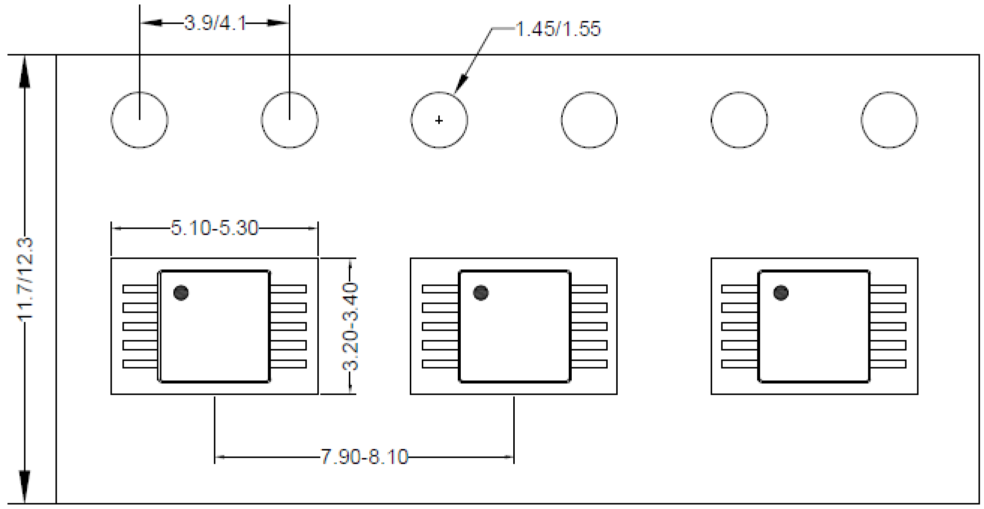
Recommended Pad Layout

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

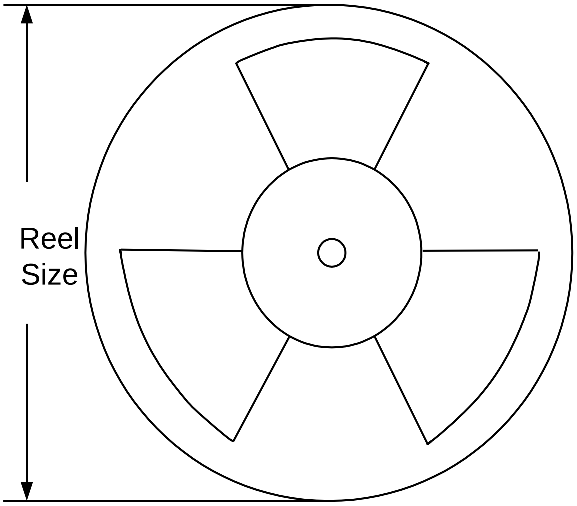
Tape Dimensions and Pin 1 Orientation

MSOP10



Direction of feed →

Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Date	**Revision**	**Change**
Mar. 31, 2025	Revision 1.0	Initial Release

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