SA59202

Multi Cell Battery Gas Gauge IC

General Description

The SA59202 is a gas gauge IC for multi-cell batteries in handheld and portable equipment. It senses battery terminal voltage, charging/discharging current by an internal 12-bit ADC. The wide input voltage range allows user with multi-cell batteries up to 25V. An accurate coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load/charger. The test results are stored in internal registers which is accessible via the I^2C Interface.

The SA59202 has programmable high and low thresholds for all measured quantities. If a programmed threshold is exceeded, the device will communicate an alert using either the alert response procedure or by setting a flag in the internal status register.

Ordering Information

SA59202 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SA59202DAA	DFN3×3-8	--

Features

- High Accuracy Coulomb Counter Measures Accumulated Battery Charge and Discharge
- Operation Voltage Range: 3.6V to 25V
- 12-bit ADC Measures Voltage and Current
- 1% Voltage, Current and Charge Accuracy
  - ±64mV Sense Voltage Range for Current ADC
  - High Side Sense for Current ADC
  - Low Value External Current Sense Resistor
- Low Quiescent Current
- Configurable Alert Output/Charge Complete Input
- I^2C Interface
- Compact DFN3×3-8 Package
- AEC-Q100 Qualified for Automotive Applications
  - Temperature Grade 2: –40°C to +105°C

Applications

- Power Tools
- Portable Equipment
- Electric and Hybrid Electric Vehicles
- Backup Battery Systems

Typical Applications

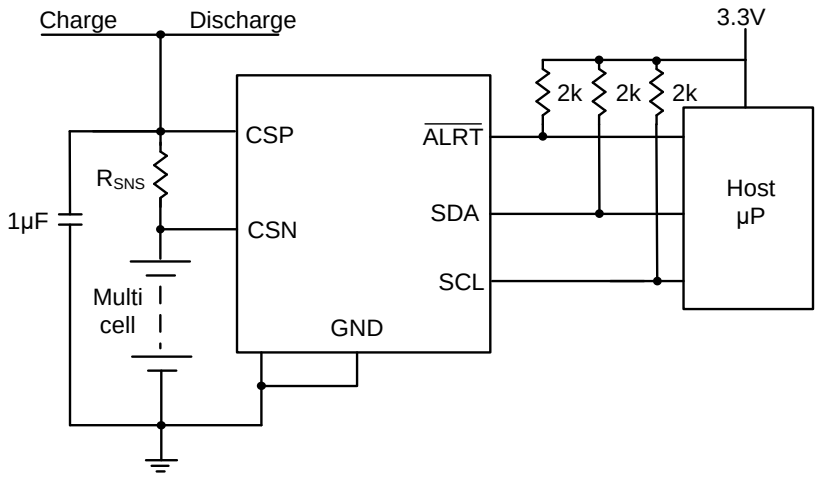
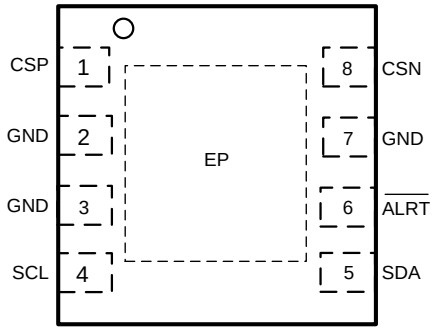


Figure 1. Typical Application Circuit

Pinout (top view)



DFN3x3-8

Top Mark: **BYQ*xyz*, (**Device code: BYQ, ***x=year code, y=week code, z= lot number code*****)**

Name	Pin Number	Description
CSP	1	Positive current sense input and power supply. Bypass with a 1μF capacitor to GND. Connect to load/charger side of the sense resistor. CSP operating range is 3.6V to 25V. CSP is also an input to the ADC during current measurement.
GND	2,3,7	Ground pin.
SCL	4	Serial clock input. 2-wire clock line. Input only.
SDA	5	Serial data input/output. 2-wire data line. Open drain output driver.
$\overline{\text{ALRT}}$	6	Alert indication or charge complete input. After power up,this pin defaults to operate as an open drain logic output. It is used to indicate alert signal by pulling to GND when any threshold registers is exceeded. When operating as a charge complete input, it connects to the charge complete output from the battery charger circuit. A low level at $\overline{\text{ALRT}}$ sets the value of the accumulated charge registers (registers C, D) to $FFFF_h$.
CSN	8	Negative current sense input. Connect CSN to the positive battery terminal side of the sense resistor. The voltage between CSN and CSP must remain within ±50mV in normal operation. CSN is also an input to the ADC during voltage and current measurement.
EP	--	Exposed pad. Connect to GND.

Block Diagram

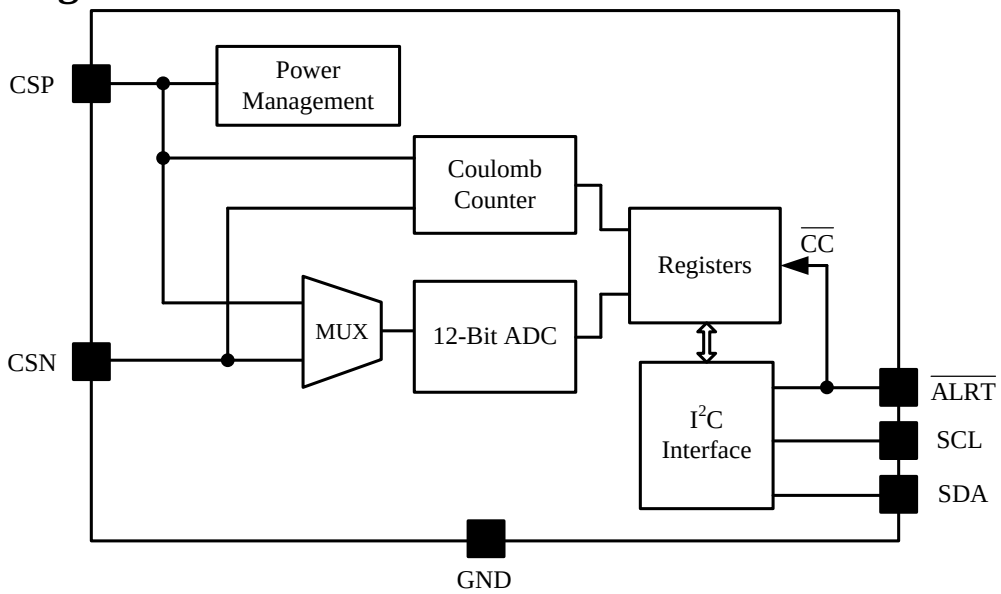


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

CSP ---------- -0.3V to 36V
CSN ---------- (-0.3V+CSP) to (0.3V+CSP)
SDA, SCL, $\overline{\text{ALRT}}$ ---------- -0.3V to 6V
Storage Temperature ---------- -65°C to +150°C
Maximum Junction Temperature (T_J) ----------150°C

Recommended Operating Conditions

CSP ----------3.6V to 25V
CSN ---------- (-50mV+CSP) to (50mV+CSP)
SDA, SCL, $\overline{\text{ALRT}}$ ---------- -0.3V to 3.3V
Operating Ambient Temperature Range (T_A) ---------- -40°C to +105°C

Electrical Characteristics

(The Δ denotes the specifications which apply over the full operating temperature range (-40°C to +105°C), otherwise specifications are at T_A = 25°C)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Power Supply							
Supply Voltage	V_{CSP}		Δ	3.6		25	V
Under Voltage Lockout Threshold	V_{UVLO}	V_{CSP} falling	Δ	3.0	3.3	3.6	V
Input Current	I_{IN_SUPPLY}	ADC on, coulomb counter on	Δ		450	600	μA
	I_{IN_SUPPLY}	ADC off, coulomb counter on	Δ		140	180	μA
	$I_{IN(SHDN)\_SUPPLY}$	Shutdown mode	Δ		15	30	μA
Current ADC							
Current ADC Conversion time	T_{COV_I}		Δ			12	ms
Current ADC Resolution			Δ	12			bits
Current Register Resolution	V_{ILSB}				31.25		uV
Current Full Scale Magnitude	V_{IFS}				±64		mV
Current Offset	V_{IOS}	CSP=CSN=12.5V			±1	±10	LSB
Current ADC Integral Nonlinearity	V_{IINL}				±1	±4	LSB
Current Gain Error	V_{IGERR}					±1	%
			Δ			±1.8	%
Voltage ADC							
Voltage ADC Conversion Time	T_{COV_V}		Δ			12	ms
Voltage ADC Resolution			Δ	12			bits
Voltage Register Resolution	V_{LSB}				6.1		mV
Voltage Full Scale Magnitude	V_{FS}				25		V
Voltage Total Unadjusted Error	TUE_V					±1	%
			Δ			±1.8	%
Coulomb Counter							
Differential Voltage Input Range	V_{DIF_IN}		Δ			±50	mV
Differential Input Resistance	R_{DIF_IN}				400		kΩ
Charge LSB	q_{LSB}	Prescale M=4096, R_{SNS}=50mΩ			0.34		mAh
Total Charge Error	E_{TC}	10mV ≤ | V_{DIF_IN} | ≤ 50mV DC				±1	%
		10mV ≤ | V_{DIF_IN} | ≤ 50mV DC -40°C ~85°C				±2.5	%
		1mV ≤ | V_{DIF_IN} | ≤ 10mV DC -40°C ~85°C				±5	%

Digital Inputs and Outputs							
Input Logic Threshold High	V_{ITH}		Δ	2.2			V
Input Logic Threshold Low	V_{ITL}		Δ			0.8	V
Low Level Output Voltage, $\overline{ALRT}$, SDA	V_{OL}	V_{CSP}≥ 5V, I=3mA	Δ			0.4	V
Input Leakage Current, $\overline{ALRT}$, SDA,SCL	I_{IN}	V_{IN}=3.3V	Δ			1	μA
Input Capacitance, $\overline{ALRT}$, SDA, SCL	C_{IN}		Δ			10	pF
Charge Complete Pulse Width	t_{PCC}			2			μs
I²C Timing Characteristics							
Maximum SCL Clock Frequency	$f_{SCL(MAX)}$		Δ	400			kHz
Bus Free Time between Stop/Start	t_{BUF}		Δ	1.3			μs
Repeated Start Set-up Time	$t_{SU,STA}$		Δ	600			ns
Hold Time(Repeated) Start Condition	$t_{HD,STA}$		Δ	600			ns
Set-up Time for Stop Condition	$t_{SU,STO}$		Δ	600			ns
Data Set-up Time Input	$t_{SU,DAT}$		Δ	100			ns
Data Hold Time Input	$t_{HD,DAT}$		Δ	50			ns
Data Hold Time Input Output	$t_{HD, DAT1/0}$		Δ	0.3		0.9	μs
Data Output Fall Time	t_{OF}	(Note 3)	Δ	20+0.1 C_B		300	ns

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: All currents into pins are positive. All voltages are referenced to GND unless otherwise specified.
Note 3: C_B is total capacitance of one bus line in pF (C_B≤400pF).

Timing Diagram

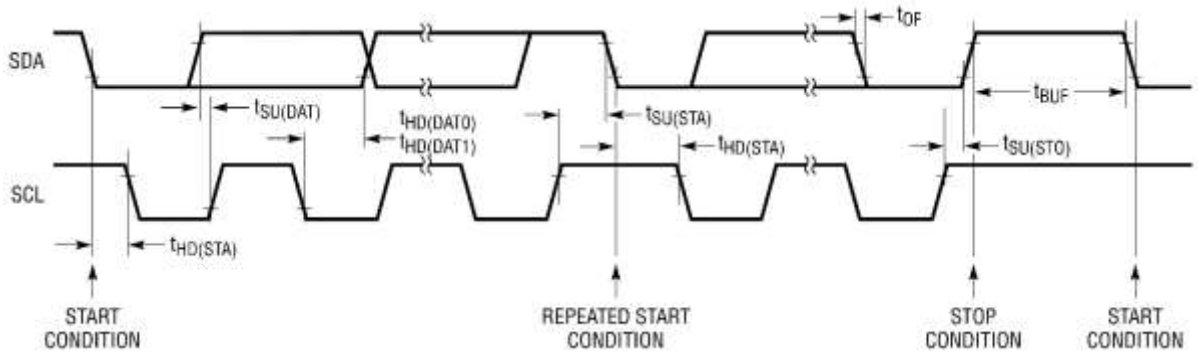
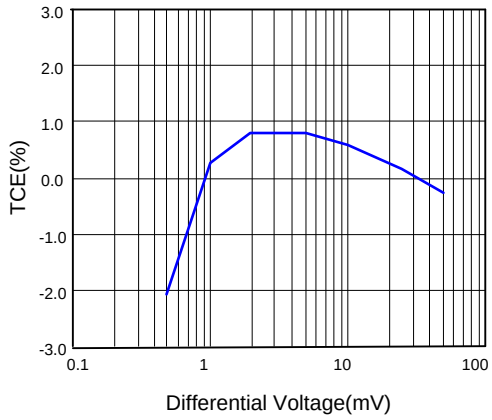


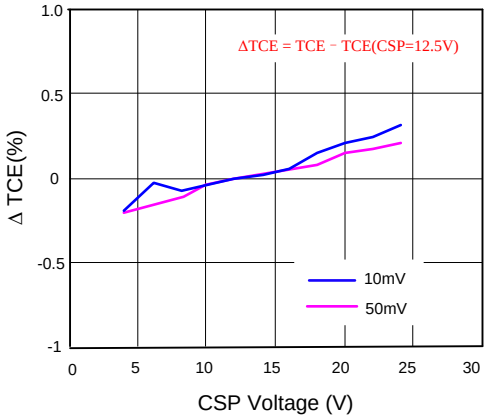
Figure 3. I²C timing diagram

Typical Performance Characteristics

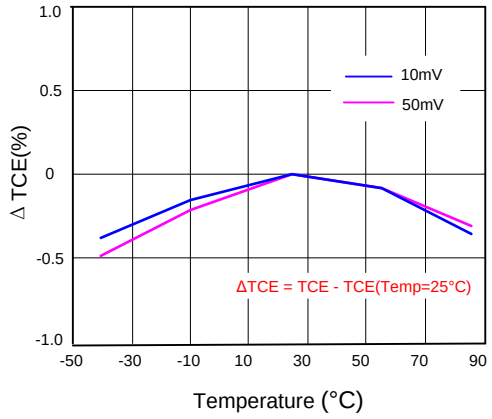
TCE vs Differential Voltage



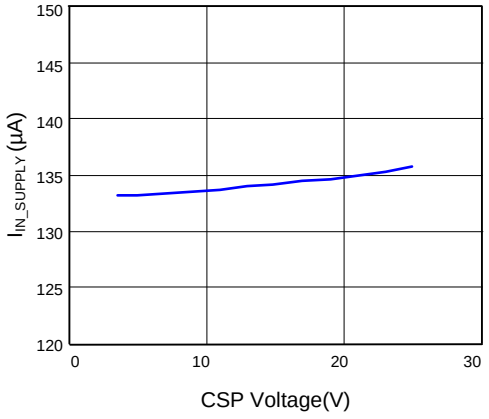
ΔTCE vs Supply Voltage



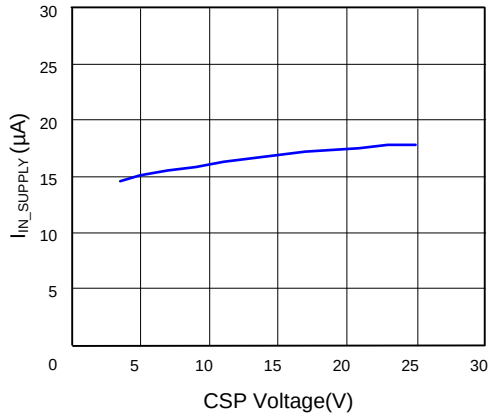
Δ TCE vs Temperature



Supply Current vs Supply Voltage



Shutdown Supply Current vs Supply Voltage



Application information

The SA59202 is a gas gauge IC for multi-cell batteries in handheld and portable equipment. It senses battery terminal voltage, charging/discharging current by an internal 12-bit ADC. The wide input voltage range allows user with multi-cell batteries up to 25V. An accurate coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load/charger. The test results are stored in internal registers which is accessible via the I^2C Interface.

Internal Registers

The SA59202 register map is shown in Table 1. The SA59202 integrates current through a sense resistor, measures battery voltage, current and stores the results in internal 16-bit registers accessible via I^2C. High and low limits can be programmed for each measured quantity. The SA59202 continuously monitors these limits and sets a flag in the status register when a limit is exceeded. If the alert mode is enabled, the $\overline{\text{ALRT}}$ pin pulls low.

Table 1 Register Map

Address	Name	Register Description	R/W	Default
00h	A	Status	R	See Table 2
01h	B	Control	R/W	3Ch
02h	C	Accumulated Charge MSB	R/W	7Fh
03h	D	Accumulated Charge LSB	R/W	FFh
04h	E	Charge Threshold High MSB	R/W	FFh
05h	F	Charge Threshold High LSB	R/W	FFh
06h	G	Charge Threshold Low MSB	R/W	00h
07h	H	Charge Threshold Low LSB	R/W	00h
08h	I	Voltage MSB	R	00h
09h	J	Voltage LSB	R	00h
0Ah	K	Voltage Threshold High MSB	R/W	FFh
0Bh	L	Voltage Threshold High LSB	R/W	FFh
0Ch	M	Voltage Threshold Low MSB	R/W	00h
0Dh	N	Voltage Threshold Low LSB	R/W	00h
0Eh	O	Current MSB	R	00h
0Fh	P	Current LSB	R	00h
10h	Q	Current Threshold High MSB	R/W	FFh
11h	R	Current Threshold High LSB	R/W	FFh
12h	S	Current Threshold Low MSB	R/W	00h
13h	T	Current Threshold Low LSB	R/W	00h

R = Read, W = Write

The status of the charge, voltage and current alerts is reported in the status register shown in **Table 2**.

Table 2 Status Register (A)

Bit	Name	Operation	Default
A[7]	Reserved		
A[6]	Current Alert	Indicates one of the current limits was exceeded	0
A[5]	Accumulated Charge Overflow/ Underflow	Indicates that the value of the ACR hit either top or bottom	0
A[4]	Reserved		0
A[3]	Charge Alert High	Indicates that the ACR value exceeded the charge threshold high limit	0
A[2]	Charge Alert Low	Indicates that the ACR value exceeded the charge threshold low limit	0
A[1]	Voltage Alert	Indicates one of the voltage limits was exceeded	0
A[0]	Under Voltage Lockout Alert	Indicates recovery from under voltage. If set to 1, a UVLO has occurred and the contents of the registers are uncertain	1

After each voltage and current conversion, the conversion result is compared to the respective threshold registers. If a value in the threshold registers is exceeded, the corresponding bit A[6] or A[1] is set.

The accumulated charge register (ACR) is compared to the charge thresholds every time the analog integrator increments or decrements the prescaler. If the ACR value exceeds the threshold register values, the corresponding bit A[3] or A[2] are set. Bit A[5] is set if the accumulated charge registers (ACR) overflows or underflows. At each overflow or underflow, the ACR rolls over and resumes integration.

The under voltage lockout (UVLO) bit of the status register A[0] is set if, during operation, the voltage on the CSP pin drops below 3.5V without reaching the POR level. The analog parts of the coulomb counter are switched off while the digital register values are retained. After recovery of the supply voltage, the coulomb counter resumes integrating with the stored value in the accumulated charge registers but it has missed any charge flowing while CSP < 3.5V.

All status register bits are cleared after being read by the host, but might be reasserted after the next voltage or current conversion or charge integration, if the corresponding alert condition is still fulfilled. Note that read operation for Status Register can not change the PIN $\overline{\text{ALRT}}$'s status.

Control Register (B)

The operation of the SA59202 is controlled by programming the control register. Table 3 shows the organization of the 8-bit control register B[7:0].

Table 3 Control Register B

BIT	NAME	OPERATION		DEFAULT
B[7:6]	ADC Mode	[11] Automatic Mode: continuously performing voltage and current conversions. [10] Scan Mode: performing voltage and current conversion every 10s [01] Manual Mode: performing single conversions of voltage and current then sleep [00] Sleep		[00]
B[5:3]	Prescaler M	Sets coulomb counter pre-scaling factor M between 1 and 4096. Default is 4096. Maximum value is limited to 4096		[111]
		B[5:3]	M	
		000	1	
		001	4	
		010	16	
		011	64	
		100	256	
		101	1024	
		110	4096	
		111	4096	
B[2:1]	$\overline{\text{ALRT}}$ configure	Configures the $\overline{\text{ALRT}}$ pin. [10] Alert Mode. Alert functionality enabled. Pin becomes logic output. [01] Charge Complete Mode. Pin becomes logic input and accepts charge complete inverted signal (e.g., from a charger) to set accumulated charge register (C,D) to FFFF'h. [00] $\overline{\text{ALRT}}$ pin disabled. [11] Not allowed.		[10]
B[0]	Shutdown	Shut down analog section to reduce I_{SUPPLY}.		[0]

Power Down B[0]

Setting B[0] to 1 shuts down the analog parts of the SA59202, reducing the current consumption to less than 15μA (typical). The circuitry managing I^2C communication remains operating and the values in the registers are retained. Note that any charge flowing while B[0] is 1 is not measured and any charge information below 1LSB of the accumulated charge register is lost.

Alert/Charge Complete Configuration B[2:1]

The $\overline{\text{ALRT}}$ pin is a dual function pin configured by the control register. By setting bits B[2:1] to [10](default), the $\overline{\text{ALRT}}$ pin is configured as an alert pin following the SMBus protocol. In this configuration, the $\overline{\text{ALRT}}$ is pulled low if one of the measured quantities(charge, voltage, current) exceeds its high or low threshold or if the value of the accumulated charge register overflows or underflows. An alert response procedure started by the master resets the alert at the $\overline{\text{ALRT}}$ pin. For further information see the Alert Response Protocol section.

Setting the control bits B[2:1] to [01] configures the $\overline{\text{ALRT}}$ pin as a digital input. In this mode, a low input on the $\overline{\text{ALRT}}$ pin indicates to the SA59202 that the battery is full and the accumulated charge register is set to its maximum, value FFFFh.

If neither the alert nor the charge complete functionality is desired, bits B[2:1] should be set to [00]. The $\overline{\text{ALRT}}$ pin is then disabled and should be tied to the supply of the I^2C bus with a 10k resistor.

Avoid setting B[2:1] to [11] as it enables the alert and the charge complete modes simultaneously.

Choosing R_{SNS}

To achieve the specified precision of the coulomb counter, the differential voltage between CSP and CSN must stay within ±50mV. With input signals up to 300mV the SA59202 will remain functional but the precision of the coulomb counter is not guaranteed.

The required value of the external sense resistor, R_{SNS}, is determined by the maximum input range of V_{SNS} and the maximum current of the system:

$$R_{SNS} \le \frac{50mV}{I_{MAX}}$$

The choice of the external sense resistor value influences the gain of the coulomb counter. A larger sense resistor gives a larger differential voltage between CSP and CSN for the same current resulting in more precise coulomb counting. The amount of charge represented by the least significant bit (q_{LSB}) of the accumulated charge (registers C, D) is equal to:

$$q_{LSB} = 0.34mAh \times \frac{50m\Omega}{R_{SNS}} \times \frac{M}{4096}$$

Note that 1mAh = 3.6C =3.6 $A \times s$ (coulomb).

Choosing R_{SNS}= $50mV / I_{MAX}$ is not sufficient in applications where the battery capacity (Q_{BAT}) is very large compared to the maximum current (I_{MAX}):

$$Q_{BAT} > I_{MAX} \times 22Hours$$

For such low current applications with a large battery, choosing R_{SNS} according to R_{SNS} = 50mV/I_{MAX} can lead to a q_{LSB} smaller than $Q_{BAT}/2^{16}$ and the 16-bit accumulated charge register may underflow before the battery is exhausted or overflow during charge. Choose, in this case, a maximum R_{SNS} of:

$$R_{SNS} \le \frac{0.34mAh \times 2^{16}}{Q_{BAT}} \times 50m\Omega$$

In an example application where the maximum current is I_{MAX} = 100mA, calculating R_{SNS} = 50mV/I_{MAX} would lead to a sense resistor of 500mΩ. This gives a q_{LSB} of 34μAh and the accumulated charge register can represent a maximum battery capacity of Q_{BAT} = 34μAh•65535 = 2228 mAh. If the battery capacity is larger, R_{SNS} must be lowered. For example, R_{SNS} should be reduced to 150mΩ if a battery with a capacity of 7200mAh is used.

Choosing Coulomb Prescaler M Config[5:3]

In these applications with a small battery but a high maximum current, q_{LSB} can get quite large with respect to the battery capacity. For example, if the battery capacity is 100mAh and the maximum current is 1A, the standard equation leads to choosing a sense resistor value of 50mΩ, resulting in:

$$q_{LSB} = 0.34mAh$$

The battery capacity then corresponds to only 294 q_{LSB} and less than 0.5% of the accumulated charge register is utilized.

To preserve digital resolution in this case, the SA59202 includes a programmable prescaler. Lowering the prescaler factor M reduces q_{LSB} to better match the accumulated charge register to the capacity of the battery. The prescaling factor M can be chosen between 1 and 4096. The charge LSB then becomes:

$$q_{LSB} = 0.34mAh \times \frac{50m\Omega}{R_{SNS}} \times \frac{M}{4096}$$

To use as much of the range of the accumulated charge register as possible the prescaler factor M should be chosen for a given battery capacity Q_{BAT} and a sense resistor R_{SNS} as:

$$M \geq 4096 \times \frac{Q_{BAT}}{2^{16} \times 0.34mAh} \times \frac{R_{SNS}}{50m\Omega}$$

M can be set to 1, 4, 16 ... 4096 by programming Config[5:3]of the control register. The default value is 4096.

In the above example of a 100mAh battery and an R_{SNS} of 50mΩ, the prescaler should be programmed to M = 64. The q_{LSB} is then 5.3125μAh and the battery capacity corresponds to roughly 18823 q_{LSB}s.

Figure 4 illustrates the best choice for prescaler value M and the sense resistor as function of the ratio between battery capacity (Q_{BAT}) and maximum current (I_{MAX}). It can be seen, that for high current applications with low battery capacity the prescaler value should be reduced, whereas in low current applications with a large battery the sense resistor should be reduced with respect to its default value of 50mV/I_{MAX}.

For example, A battery with 3500mAh capacity, I_{MAX}=2A, Qmax/Imax = 1.75h, set M=1024, R_{SNS}=25 mΩ the q_{LSB} = 0.17mAh, the full accumulated charge number is 20588LSB.

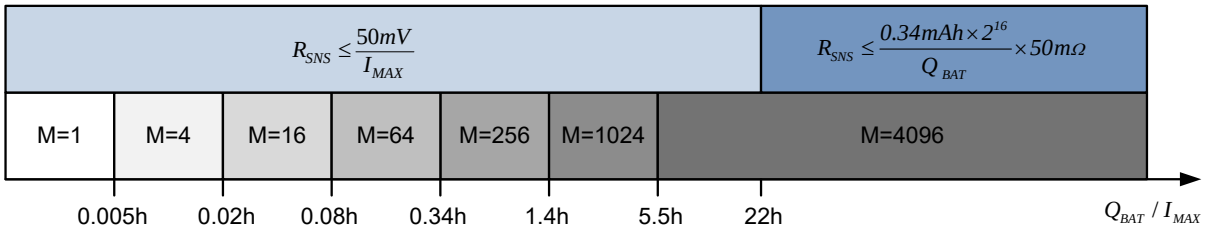


Figure 4. Choice of Sense Resistor and Prescaler as Function of Battery Capacity and Maximum Current

ADC Mode B[7:6]

The SA59202 features an ADC which measures voltage on CSN (battery voltage), voltage difference between CSP and CSN(battery current). The reference voltage and clock for the ADC are generated internally.

The ADC has four different modes of operation as shown in **Table 3**. These modes are controlled by bits B[7:6] of the control register. At power-up, bits B[7:6] are set to [00] and the ADC is in sleep mode.

- Manual Mode:

A single conversion of the three measured quantities is initiated by setting the bit B[7:6] to [01]. After two conversions (voltage and current), the ADC resets B[7:6] to [00] and goes back to sleep.

- Scan Mode:

The SA59202 is set to scan mode by setting B[7:6] to [10]. In scan mode the ADC converts voltage, current, and then sleeps for approximately ten seconds. It then reawakens automatically and repeats the two conversions. The chip remains in scan mode until reprogrammed by the host.

- Automatic Mode:

Programming B[7:6] to [11] sets the chip into automatic mode where the ADC continuously performs voltage and current conversions. The chip stays in automatic mode until reprogrammed by the host.

- Sleep Mode:

Programming B[7:6] to [00] puts the ADC to sleep. If control bits B[7:6] change within a conversion, the ADC will complete the running cycle of conversions before entering the newly selected mode.

At the end of each conversion, the corresponding registers are updated. If the converted quantity exceeds the values programmed in the threshold registers, a flag is set in the status register and the $\overline{\text{ALRT}}$ pin is pulled low (if alert mode is enabled).

The ADC conversion result can be read in Accumulated Charge Register (C, D), Voltage Registers (I,J) and Current Registers (O,P)

Alert Thresholds Registers

For each of the measured quantities (battery charge, voltage and current), the SA59202 features high and low threshold registers. At power-up, the high thresholds are set to FFFFh while the low thresholds are set to 0000h, with the effect of disabling them. All thresholds can be programmed to a desired value via I^2C. As soon as a measured quantity exceeds the high threshold or falls below the low threshold, the SA59202 sets the corresponding flag in the status register and pulls the $\overline{\text{ALRT}}$ pin low if alert mode is enabled via bits B[2:1]

- Charge Threshold Register(E, F, G, H)

The accumulated charge register (ACR) is compared to the charge thresholds every time the analog integrator increments or decrements the prescaler. If the ACR value exceeds the threshold register values, the corresponding bit A[3] or A[2] are set.

- Voltage Threshold Register (K, L, M, N)

The result of the 12-bit ADC conversion of the voltage at CSN is stored in the voltage registers (I, J). As the ADC resolution is 12 bits in voltage mode, the lowest four bits of the combined voltage registers are always zero. From the result of the 12-bit voltage registers I[7:0]J[7:0], the measured voltage can be calculated as:

$$V_{CSN} = 25V \times \frac{RESULT_h}{FFFF_h} = 25V \times \frac{RESULT_{DEC}}{65535}$$

The voltage high and low threshold values are stored in Register (K, L, M, N).

Example 1: In an application, the user wants to get an alert if the CSN voltage exceeds 20V or the CSN voltage is less than 10V. This is achieved by setting the upper threshold V_{HIGH} in register [K, L] to 20V and the lower threshold V_{LOW} in register [M, N] to 10V as following shows.

$$V_{HIGH} = \frac{20V}{25V} \times 65535 = 52428 = CCCC_h$$

$$V_{LOW} = \frac{10V}{25V} \times 65535 = 26214 = 6666_h$$

- Current Threshold Register (Q,R,S,T)

The result of the current conversion is stored in the current registers (O, P).

As the ADC resolution is 12 bits in current mode, the lowest four bits of the combined current registers are always zero.

The ADC measures battery current by converting the voltage, V_{SNS}, across the sense resistor R_{SNS}. Depending whether the battery is being charged or discharged the measured voltage drop on R_{SNS} is positive or negative. Current Registers = FFF0h corresponds to the full scale positive voltage 64mV. While Current Registers =

0x0000 corresponds to the full scale negative voltage –64mV. The battery current can be obtained from the Current Registers O[7:0]P[7:0] and the value of the chosen sense resistor R_{SNS}:

$$I_{BAT} = \frac{V_{SNS}}{R_{SNS}} = \frac{64mV}{R_{SNS}}\left(\frac{RESULT_h - 7FFF_h}{7FFF_h}\right) = \frac{64mV}{R_{SNS}}\left(\frac{RESULT_{DEC} - 32767}{32767}\right)$$

Positive current is measured when the battery is charging and the current is from CSP to CSN and negative current is measured when the battery is discharging.

Example 3: a register value of Current Registers = 0xA800 together with a sense resistor R_{SNS}= 50mΩ corresponds to a battery current:

$$I_{BAT} = \frac{V_{SNS}}{R_{SNS}} = \frac{64mV}{50m\Omega}\left(\frac{A800_h - 7FFF_h}{7FFF_h}\right) = \frac{64mV}{50m\Omega}\left(\frac{43008 - 32767}{32767}\right) \approx 400mA$$

The values in the threshold register for the current mode Q, R, S, T are also expressed in the same manner as the current conversion result. The alert after a current measurement is set if the result is higher than the value stored in the high threshold registers Q, R or lower than the value stored in the low value registers S,T.

Example 4: In an application, the user wants to get an alert if the absolute current through the sense resistor, R_{SNS}, of 50mΩ exceeds 0.5A. This is achieved by setting the upper threshold I_{HIGH} in register [Q, R] to 0.5A and the lower threshold I_{LOW} in register [S,T] to –0.5A. The formula for I_{BAT} leads to:

$$I_{HIGH(DEC)} = \left(\frac{0.5A \times 50m\Omega}{64mV} \times 32767\right) + 32767 = 45566 = B1FE_h$$

$$I_{HIGH(DEC)} = \left(\frac{-0.5A \times 50m\Omega}{64mV} \times 32767\right) + 32767 = 19967 = 4DFF_h$$

Accumulated Charge Register

The coulomb counting circuitry in the SA59202 integrates current through the sense resistor. The result of this charge integration is stored in the 16-bit accumulated charge register (registers C, D). As the SA59202 does not know the actual battery status at power-up, the accumulated charge register (ACR) is set to mid-scale (7FFFh). If the host knows the status of the battery, the accumulated charge (C[7:0]D[7:0]) can be either programmed to the correct value via I²C or it can be set after charging to FFFFh(full) by pulling the $\overline{\text{ALRT}}$ pin low if charge complete mode is enabled via bits B[2:1].

Note that before writing to the accumulated charge registers, the analog section should be temporarily shut down by setting B[0] to 1. In order to avoid a change in the accumulated charge registers between reading MSBs C[7:0] and LSBs D[7:0], it is recommended to read them sequentially as shown in Figure 5.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	02h	0		1100100	1	0	80h	0	00h	1	

Figure 5. Reading the SA59202 Accumulated Charge Registers

I²C/SMBus Interface

The SA59202 communicates with a bus master using a 2-wire interface compatible with I²C and SMBus. The 7-bit hard coded I²C address of the SA59202 is 1100100. The SA59202 is a slave only device. The serial clock line (SCL) is input only while the serial data line (SDA) is bidirectional. The device supports I²C standard and fast mode. For more details refer to the I²C Protocol section.

I²C Protocol

The SA59202 uses an I²C /SMBus-compatible 2-wire interface supporting multiple devices on a single bus. Connected devices can only pull the bus lines low and must never drive the bus high. The bus wires are externally connected to a positive supply voltage via current sources or pull-up resistors. When the bus is idle, all bus lines are high. Data on the I²C bus can be transferred at rates of up to 100kbit/s in standard mode and up to 400kbit/s in fast mode.

Each device on the I²C /SMbus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be classified as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave. The SA59202 always acts as a slave.

Figure 6 shows an overview of the data transmission on the I²C bus.

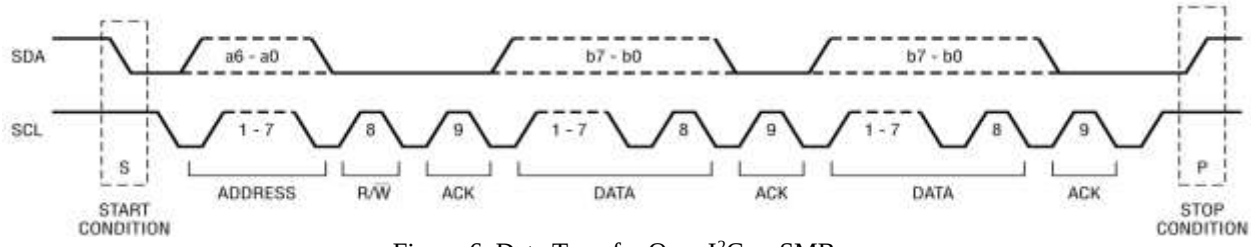


Figure 6. Data Transfer Over I²C or SMBus

Start and Stop Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START(S).

Write Protocol

The master begins a write operation with a START condition followed by the seven bit slave address 1100100 and the R/W bit set to zero, as shown in Figure 7. The SA59202 acknowledges this by pulling SDA low and the master sends a command byte which indicates which internal register the master is to write. The SA59202 acknowledges and latches the command byte into its internal register address pointer. The master delivers the data byte, the SA59202 acknowledges once more and latches the data into the desired register. The transmission is ended when the master sends a STOP condition. If the master continues by sending a second data byte instead of a stop, the SA59202 acknowledges again, increments its address pointer and latches the second data byte in the following register, as shown in Figure 8.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	P
	1100100	0	0	01h	0	FCh	0	

From Mater to Slave

From Slave to Master

A: Acknowledge(Low)

$\overline{A}$: Not Acknowledge(High)

S: Start Condition

P: Stop Condition

R: Read Bit(High)

$\overline{W}$: Write Bit(Low)

Figure 7. Writing FCh to the SA59202 Control Register (B)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	DATA	A	P
	1100100	0	0	02h	0	F0h	0	00h	0	

Figure 8. Writing F001h to the SA59202 Accumulated Charge Register (C, D)

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address 1100100 and the R/W bit set to zero, as shown in Figure 9. The SA59202 acknowledges and the master sends a command byte which indicates which internal register the master is to read. The SA59202 acknowledges and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/W bit now set to one. The SA59202 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, the SA59202 increments its address pointer and sends the contents of the following register as depicted in Figure 10.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	$\overline{A}$	P
	1100100	0	0	00h	0		1100100	1	0	01h	1	

Figure 9. Reading the SA59202 Status Register (A)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	08h	0		1100100	1	0	7Fh	0	FFh	1	

Figure 10. Reading the SA59202 Voltage Register (I, J)

Alert Response Protocol

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt (Figure 11).

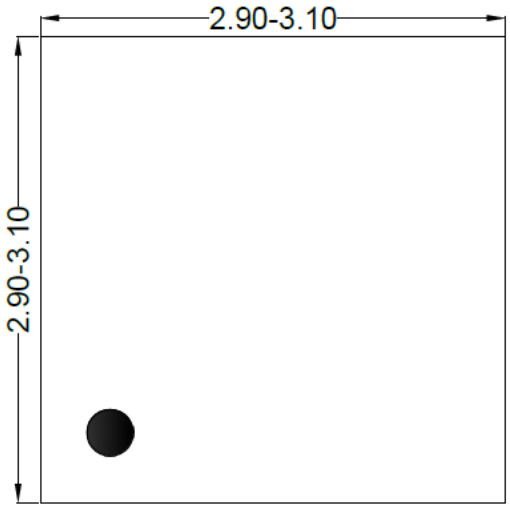
The master initiates the ARA procedure with a START condition and the special 7-bit ARA bus address (0001100) followed by the read bit(R)=1. If the SA59202 is asserting the $\overline{ALRT}$ pin in alert mode, it acknowledges and responds by sending its 7-bit bus address (1100100) and a 0. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the SA59202 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the SA59202 immediately aborts its transfer and waits for

the next ARA cycle to try again. If transfer is successfully completed, the SA59202 will stop pulling down the $\overline{\text{ALRT}}$ pin and will not respond to further ARA requests until a new Alert event occurs.

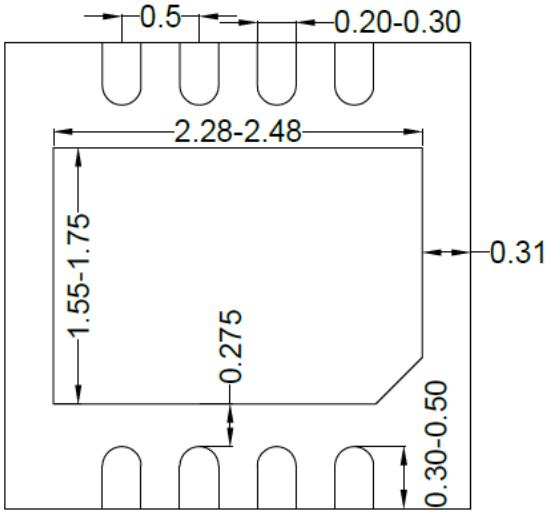
S	Alert Response Address	R	A	Device Address	$\overline{\text{A}}$	P
	0001100	1	0	11001000	1	

Figure 11. SA59202 Serial Bus SDA Alert Response Protocol

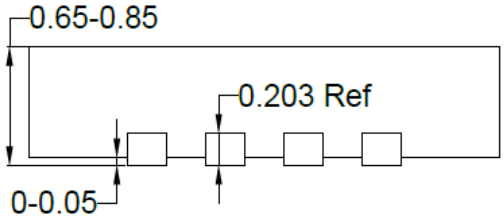
DFN3×3-8 Package Outline Drawing



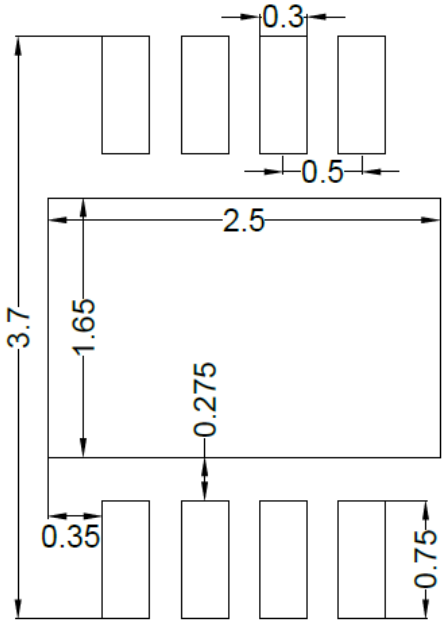
Top view



Bottom view



Front view

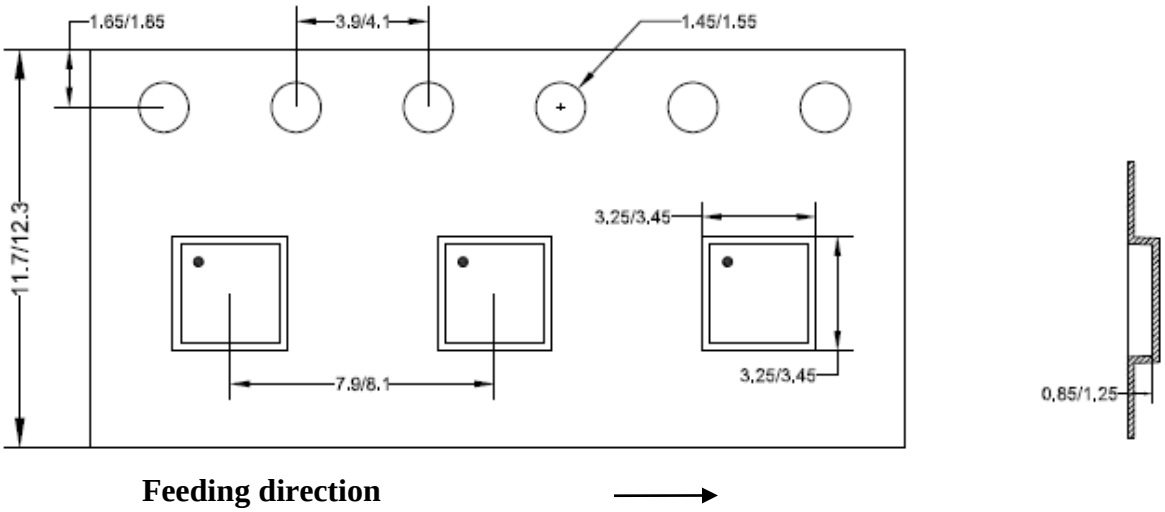


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

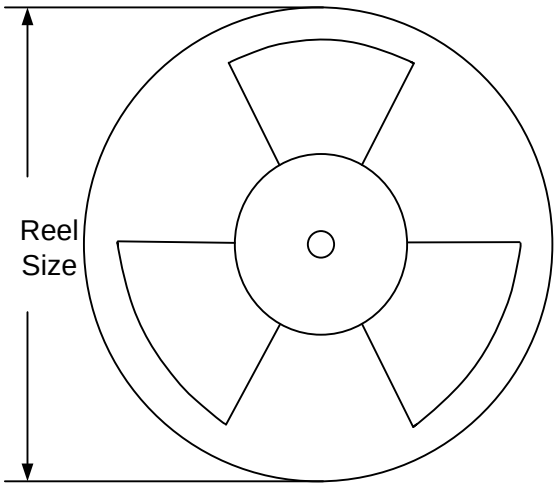
Taping & Reel Specification

1. DFN3x3 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN3x3	12	8	13"	400	400	5000

3. Others: NA

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