SY24696

Low-Power Digital Temperature Sensor with SMBus and Two-Wire Serial Interface

General Description

The SY24696 is a digital temperature sensor, it's ideal for NTC/PTC thermistor replacement where high accuracy is required. The device offers an accuracy of ±0.5°C without requiring calibration or external component signal conditioning. Device's temperature sensors are highly linear and do not require complex calculations or lookup tables to derive the temperature. The on-chip 12-bit ADC offers resolutions down to 0.0625°C.

The SY24696 features SMBus and I^2C interface compatibility, and allows up to four devices on one bus. The SY24696 also features an SMBus alert function. The device is specified to operate over supply voltages from 1.62 to 3.6V with the maximum quiescent current of 7.5μA over the full operating range. The 1.6mm×1.6mm SOT563 package is 68% smaller footprint than a SOT-23 package (and also supply other usual package).

The SY24696 is ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications. The SY24696 is specified for operation over a temperature range of –40°C to 125°C.

Ordering Information

SY24696 □(□□□)

- (□□□) — Package Code
- □ — Optional Spec Code

Ordering Number	Package type	Note
SY24696ART	SOT563	

Features

- Accuracy without Calibration:
  - 3°C (max) from –40°C to 125°C
- Low Quiescent Current:
  - 7.5μA Active (max)
  - 0.8μA Shutdown (max)
- Supply Range: 1.62 to 3.6V
- Resolution: 12 Bits
- Digital Output: SMBus, and I^2C Interface Compatibility
- SOT563 Package (1.6-mmx1.6-mm) is a 68% Smaller Footprint than SOT-23

Applications

- Portable and Battery-Powered Applications
- Power-supply Temperature Monitoring
- Computer Peripheral Thermal Protection
- Notebook Computers
- Battery Management
- Office Machines
- Thermostat Controls
- Electromechanical Device Temperatures
- General Temperature Measurements:
  - Industrial Controls
  - Test Equipment
  - Medical Instrumentations

Function Block Diagram and Application Circuit

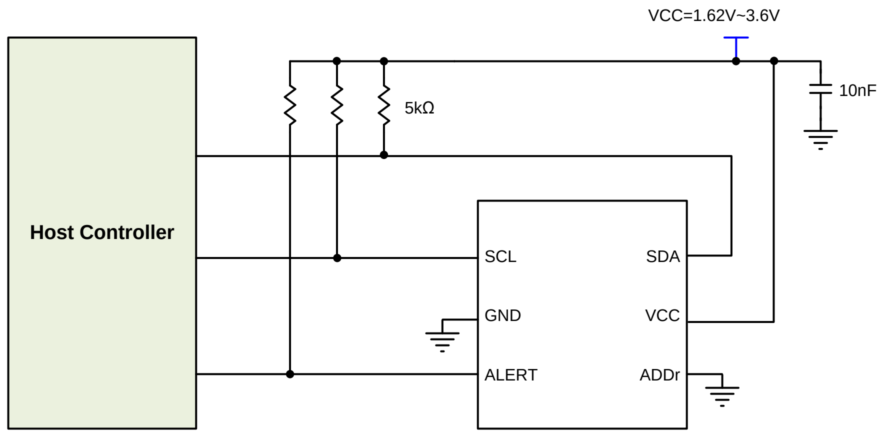
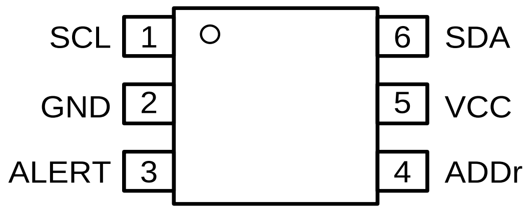


Figure 1. Simplified Application Circuit

Pinout (Top View)



SOT563

Top mark: **b8*xyz*** (Device code: **b8**, ***x=year code, y=week code, z= lot number code***)

Pin No.	Pin Name	IO type	Pin Description
1	SCL	I	Serial clock. Open-drain output; requires a pull-up resistor.
2	GND	/	Ground
3	ALERT	O	Over temperature alert. Open-drain output; requires a pull-up resistor.
4	ADDr	I	Address selects. Connect to GND or VCC
5	VCC	P	Supply voltage, 1.62 V to 3.6 V
6	SDA	I/O	Serial data. Open-drain output; requires a pull-up resistor.

Absolute Maximum Ratings (Note 1)

VCC to GND-- 4V
SCL, SDA, ADDr and ALERT --- -0.5V~4V
Operating temperature-- -55°C to 150°C
Junction temperature ---150 °C
Storage Temperature Range --- -60°C to 150°C
Package Thermal Resistance

θ_{JA}--- 265°C/W
$\theta_{JC(top)}$--38°C/W
θ_{JB}-- 55°C/W
ψ_{JT}-- 3°C/W
ψ_{JB}-- 54°C/W

ESD Susceptibility

HBM (Human Body Model) --- ±4kV
CDM (Charged-device Model) --- ±2kV

Recommended Operating Conditions

VCC to GND--- 1.62V~3.6V
Operating Free-air Temperature Range -- -40°C to 125°C

Electrical Characteristics

At T_A = 25°C and VCC = 1.62 to 3.6V, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Temperature Sense						
Temperature Sense Range			-40		125	°C
Accuracy (Temperature Error)		-25°C to +85°C		±0.5	±2	°C
		-40°C to +125°C		±0.5	±3	
PSRR				0.2	0.5	°C/V
ADC Resolution				12		Bit
Resolution				0.0625		°C
ADC Conversion Time				26	35	ms
Conversion Modes		CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		
		CR1 = 1, CR0 = 0 (default)		4		
		CR1 = 1, CR0 = 1		8		
Power Supply						
Operating Supply Range	VCC		1.62		3.6	V
Average Quiescent Current	I_Q	Serial bus inactive, CR1 = 1, CR0 = 0 (default)		6.5	7.5	µA
		Serial bus active, SCL frequency = 400 kHz		22		
		Serial bus active, SCL frequency = 3.4 MHz		103		
Shutdown Current	I_{SD}	Serial bus inactive, CR1 = 1, CR0 = 0 (default)		0.5	0.8	µA
		Serial bus active, SCL frequency = 400 kHz		16		
		Serial bus active, SCL frequency = 3.4 MHz		99		
Digital Part						
Input Capacitance				3		pF
Input Logic High, SDA, SCL	V_{IH}		0.7× VCC		3.6	V
Input Logic Low, SDA, SCL	V_{IL}		-0.5		0.3× VCC	V
Input Current, SDA, SCL, ALERT		0 < V_{IN} < 3.6 V			1	µA
Output Low Level Voltage, SDA, ALERT	V_{OL}	VCC> 2 V, I_{OL} = 3 mA	0		0.4	V
		VCC< 2 V, I_{OL} = 3 mA	0		0.2× VCC	
I^2C Timeout Time				30	40	ms
I^2C Interface- Fast Mode (Note 2)						
Clock Operation Frequency	f_{SCL}		0.001		0.4	MHz
START Condition Hold Time	$t_{HD:STA}$		600			ns
Low Period of The SCL Clock	t_{LOW}		1300			ns
High Period of The SCL Clock	t_{HIGH}		600			ns
SETUP Condition Hold Time	$t_{SU:STA}$		600			ns
DATA Hold Time (SDA Input)	$t_{HD:DAT}$		100		900	ns
DATA Setup Time (SDA Input)	$t_{SU:DAT}$		100			ns

Clock Rise Time	t_r	10%-90%			300	ns
Clock Fall Time	t_f	90%-10%			300	ns
Data Rise Time		10%-90%			300	ns
		10%-90%, SCLK ≤ 100 kHz,			1000	ns
Data Fall Time		90%-10%			300	ns
Setup Time STOP Condition	$t_{SU:STO}$		600			ns
BUS Free Time Stop to Start	t_{BUF}		600			ns
I²C Interface- High-Speed Mode (Note 2)						
Clock Operation Frequency	f_{SCL}		0.001		3.4	MHz
START Condition Hold Time	$t_{HD:STA}$		160			ns
Low Period of the SCL Clock	t_{LOW}		210			ns
High Period of the SCL Clock	t_{HIGH}		60			ns
SETUP Condition Hold Time	$t_{SU:STA}$		160			ns
DATA Hold Time (SDA Input)	$t_{HD:DAT}$		25		105	ns
DATA Setup Time (SDA Input)	$t_{SU:DAT}$		25			ns
Clock Rise Time	t_r	10%-90%			40	ns
Clock Fall Time	t_f	90%-10%			40	ns
Data Fall Time		90%-10%			80	ns
Setup Time STOP Condition	$t_{SU:STO}$		160			ns
BUS Free Time Stop to Start	t_{BUF}		160			ns

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Guaranteed by design, not subject to test.

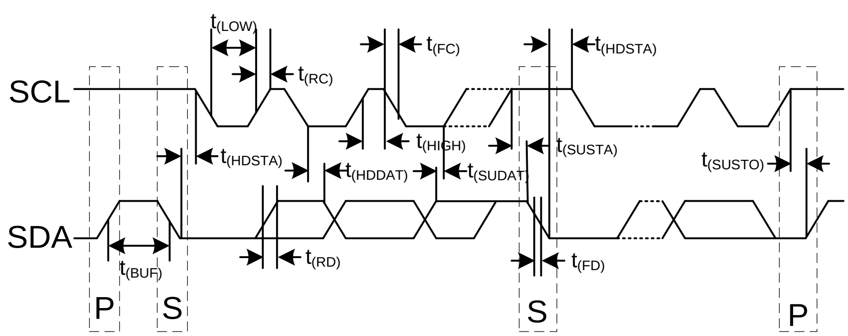


Figure 2. Two-Wire Timing Diagram

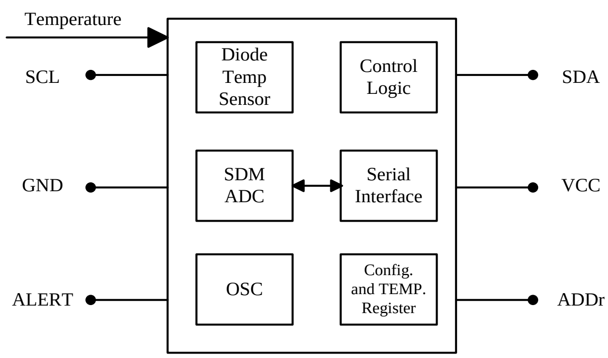
Function Description

Overview

The SY24696 is a digital temperature sensor that is optimal for thermal-management and thermal protection applications. The SY24696 is SMBus and I²C interface-compatible. The device is specified over an operating temperature range of –40°C to 125°C. The Functional Block Diagram is shown in the following figure.

The temperature sensor of the SY24696 is inside the chip. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

Functional Block Diagram



Feature Description

Digital Temperature Output

The digital outputs of each temperature measurement are stored in the read-only temperature register. The temperature register of the SY24696 is configured as a 12-bit, read-only register (configuration register EM bit = 0, see the Extended Mode (EM) section), or as a 13-bit, read-only register (configuration register EM bit = 1) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 7 and Table 8. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used for indicating temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 1 and Table 2. One LSB equals 0.0625°C. Negative numbers are represented in binary twos-complement format. Following power-up or reset, the temperature register will keep reading 0°C until the first conversion is complete. Bit D0 of byte 2 indicates normal mode (EM bit = 0) or extended mode (EM bit = 1), and can be used for distinguishing between the two temperature register data formats. The unused bits in the temperature register will always read 0.

Table 1. 12-Bit Temperature Data Format

Temperature (°C)	Digital Output (Binary)	Hex
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-55	1100 1001 0000	C90

Table 1 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:

1. Divide the temperature by the resolution
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the twos-complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

1. Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB= 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by -1 for the negative sign.

Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

Table 2. 13-Bit Temperature Data Format

Temperature (°C)	Digital Output (Binary)	Hex
150	0 1001 0110 0000	0960
128	0 1000 0000 0000	0800
127.9375	0 0111 1111 1111	07FF
100	0 0110 0100 0000	0640
80	0 0101 0000 0000	0500
75	0 0100 1011 0000	04B0
50	0 0011 0010 0000	0320
25	0 0001 1001 0000	0190
0.25	0 0000 0000 0100	0004
0	0 0000 0000 0000	0000
-0.25	1 1111 1111 1100	1FFC
-25	1 1110 0111 0000	1E70
-55	1 1100 1001 0000	1C90

Digital Temperature Output

The SY24696 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The SY24696 supports the transmission protocol for both fast (1kHz to 400kHz) and high-speed (1kHz to 3.4MHz) modes. All data bytes are transmitted MSB first.

Bus Overview

The device that initiates the transfer is called a master, and the devices controlled by the master are called slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition will be initiated, indicated by pulling the data-line (SDA) from a high to low logic level when SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed will respond to the master by generating an acknowledge and pulling SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer the SDA pin must remain stable when SCL is high, because any change in SDA pin when SCL pin is high will be interpreted as a START signal or STOP signal.

When all data have been transferred, the master will generate a STOP condition indicated by pulling SDA pin from low to high when the SCL pin is high.

Serial Bus Address

To communicate with the SY24696, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The SY24696 features an address pin to allow up to four devices to be addressed on a single bus. Table 3 describes the pin logic levels used to properly connect up to four devices.

Table 3. Address Pin and Slave Addresses

Device Two-Wire Address	A0 Pin Connection
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

Writing and Reading Operation

Accessing a particular register on the SY24696 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the SY24696 requires a value for the pointer register (see Figure 4).

When reading from the SY24696, the last value stored in the pointer register by a write operation determines register which read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/W bit low, followed by the pointer register byte. No additional data are required. The master then will generate a START condition and send the slave address byte with the R/W bit high to initiate the read command. See Figure 3 for details of this sequence.

Register bytes are sent with the most significant byte first, followed by the least significant byte

Slave Mode Operations

The SY24696 can operate as a slave receiver or slave transmitter. As a slave device, the SY24696 never drives the SCL line.

1. Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The SY24696 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register's address. The SY24696 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The SY24696 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

2. Slave Transmitter Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master terminates data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus Alert Function

The SY24696 supports the SMBus alert function. When the SY24696 operates in Interrupt Mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master will send an SMBus alert command (0001 1001) to the bus. If the ALERT pin is active, the device will acknowledge the SMBus alert command and respond by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the ALERT condition is caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. For POL = 0, the LSB is low if the temperature is greater than or equal to T_{HIGH}; this bit is high if the temperature is less than T_{LOW}. The polarity of this bit is inverted if POL = 1. See Figure 6 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines device which clears the ALERT status. The device with the lowest two-wire address wins the arbitration. If the SY24696 wins the arbitration, its ALERT pin will inactivate at the completion of the SMBus alert command. If the SY24696 loses the arbitration, its ALERT pin will remain active.

General Call

The SY24696 will respond to a two-wire general call address (000 0000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 0000 0110, the SY24696 device internal registers will be reset to power-up values. The SY24696 device does not support the general address acquire command.

High-Speed (HS) Mode

In order for the two-wire bus to operate at frequencies above 400kHz, the master device must issue an HS-Mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The SY24696 does not acknowledge this byte, but switches the input filters on SDA and SCL and the output filters on SDA to operate in HS-mode, allowing transfers of up to 3.4MHz. After the HS-Mode master code has been issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in HS-Mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the SY24696 switches the input and output filters back to fast-mode operation.

Timeout Function

The SY24696 will reset the serial interface if SCL is held low for 30ms (typ) between a start and stop condition. The SY24696 will release the SDA line if the SCL pin is pulled low and waits for a start condition from the host controller. To avoid activating the time-out function, maintaining a communication speed of at least 1kHz for SCL operating frequency is necessary.

Timing Diagrams

The SY24696 is two-wire, SMBus, and I²C-interface compatible. Figure 3, Figure 4, Figure 5, and Figure 6 list the various operations on the SY24696. Parameters for Figure 3 are defined in the Timing Requirements table. The bus definitions are defined as follows:

Acknowledge Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a not-acknowledge on the last byte that has been transmitted by the slave.

Bus Idle Both SDA and SCL line remain high.

Data Transfer The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The SY24696 can also be used for single byte updates. To update only the MS byte, terminate the communication by issuing a START or STOP communication on the bus.

Start Data Transfer A change in the state of the SDA line, from high to low, when the SCL line is high, will definesa START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

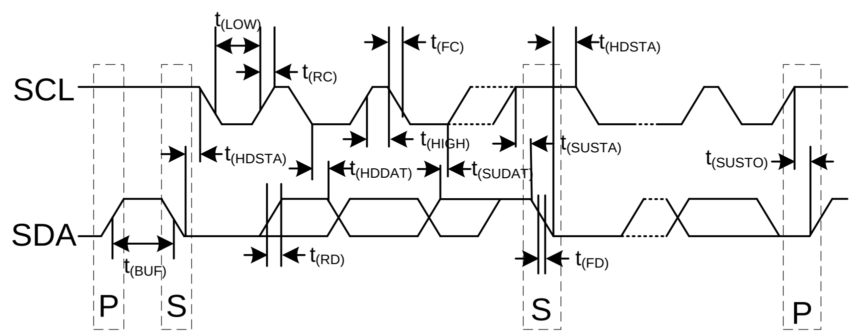
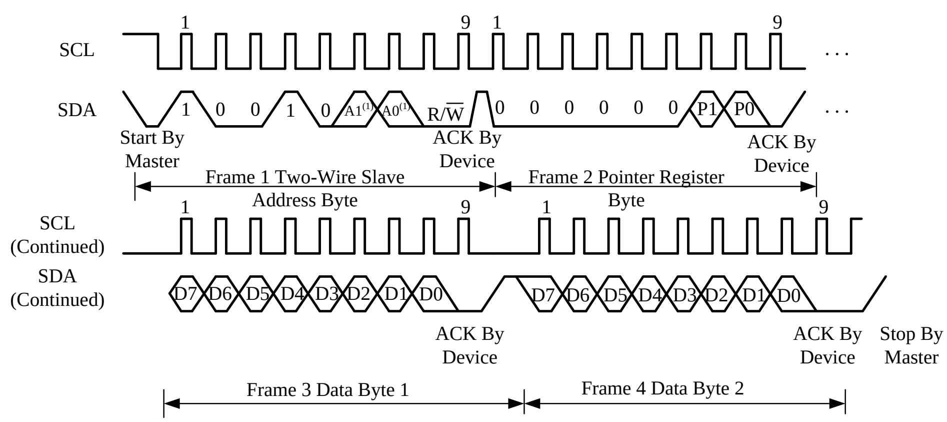
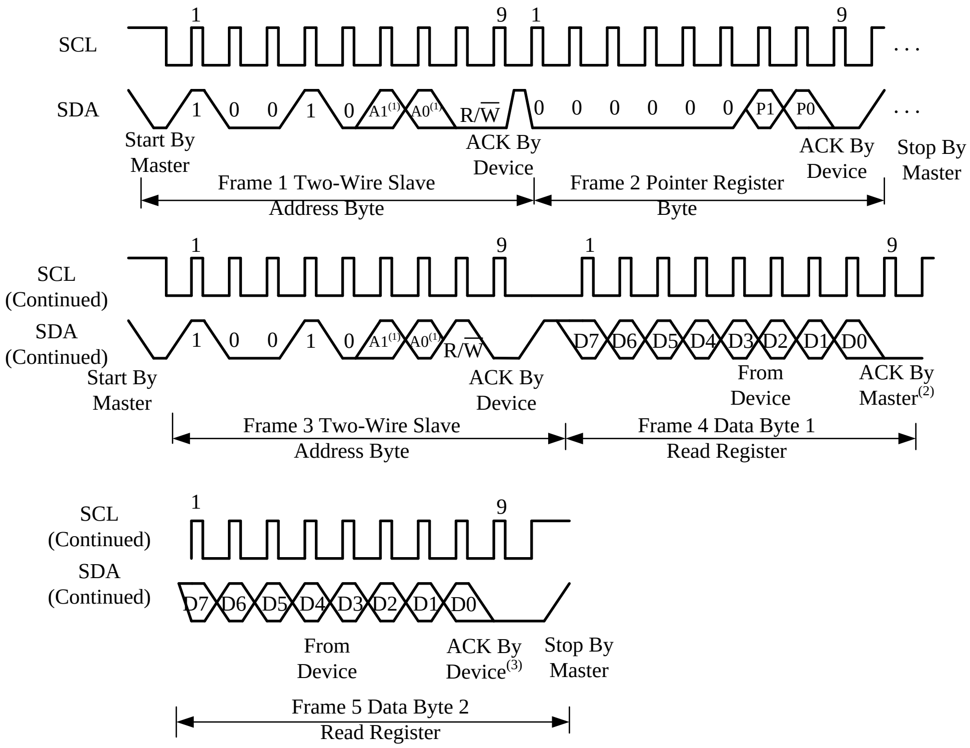


Figure 3. Two-Wire Timing Diagram



Note: (1) The value of A0 and A1 are determined by the ADDR pin.

Figure 4. Two-Wire Timing Diagram for Write Word Format

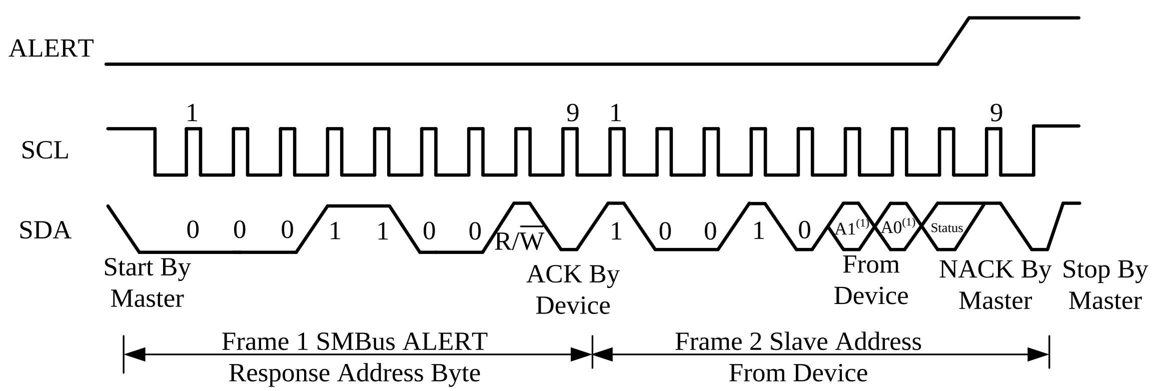


Note: (1) The value of A0 and A1 are determined by the ADDR pin.

(2) Master should leave SDA high to terminate a single-byte read operation.

(3) Master should leave SDA high to terminate a two-byte read operation

Figure 5. Two-Wire Timing Diagram for Read Word Format



Note: (1) The value of A0 and A1 are determined by the ADDR pin

Figure 6. Timing Diagram for SMBus Alert

Device Functional Modes

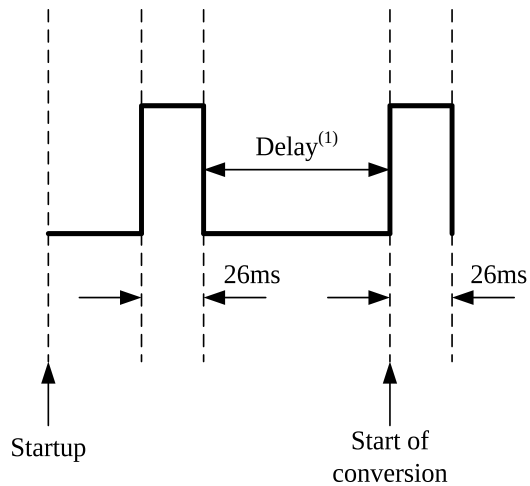
Continuous-Conversion Mode

The default mode of the SY24696 is continuous conversion mode. During continuous-conversion mode, the ADC performs continuous temperature conversions and stores each results to the temperature register, overwriting the result from the previous conversion. The conversion rate bits, CR1 and CR0, configure the SY24696 for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. The SY24696 has a typical conversion time of 26ms. To achieve different conversion rates, the SY24696 makes a conversion and then powers down to wait for the appropriate delay set by CR1 and CR0. Table 4 lists the settings for CR1 and CR0.

Table 4. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25 Hz
0	1	1 Hz
1	0	4 Hz (default)
1	1	8 Hz

After power-up or general-call reset, the SY24696 will start a conversion after a short time, as shown in Figure 7. The first result is available after 26ms (typical). The active quiescent current during conversion is 30μA (typical at +25°C). The quiescent current during delay is 3.5μA (typical at +25°C).



(1) Delay is set by CR1 and CR0.

Figure 7. Conversion Start

Extended Mode (EM)

The Extended-Mode bit configures the device for Normal mode operation (EM = 0) or Extended mode operation (EM = 1). In Normal mode, the Temperature Register and high- and low-limit registers use a 12-bit data format.

Extended mode (EM = 1) allows measurement of temperatures above 128°C by configuring the Temperature Register, and high- and low-limit registers for 13-bit data format.

Shutdown Mode (SD)

The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5μA. Shutdown mode will enable when the SD bit is 1; the device will shut down when current conversion is completed. When SD is equal to 0, the device will maintain a continuous conversion state.

One-Shot/Conversion Ready (OS)

The SY24696 features a one-shot temperature measurement mode. When the device is in Shutdown Mode, writing a 1 to the OS bit will start a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. After the conversion, the OS bit will read 1. This feature will reduce power consumption in the SY24696 when continuous temperature monitoring is not required.

As a result of the short conversion time, the SY24696 achieves a higher conversion rate. A single conversion typically takes 26ms and a read can take place in less than 20μs. When using One-Shot Mode, 30 or more conversions per second will be possible.

Thermostat Mode (TM)

The thermostat-mode bit indicates to the device whether to operate in comparator mode (TM = 0) or Interrupt mode (TM = 1).

1. Comparator Mode (TM = 0)

In Comparator mode (TM = 0), the Alert pin will be activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and remains active until the temperature falls below the value in the $T_{(LOW)}$ register. For more information on the comparator mode, see the High- and Low-Limit Registers section.

2. Interrupt Mode (TM = 1)

In Interrupt mode (TM = 1), the Alert pin will be activated when the temperature exceeds $T_{(HIGH)}$ or goes below $T_{(LOW)}$ registers. The Alert pin will be cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the High- and Low-Limit Registers section.

Programming

Pointer Register

Figure 8 illustrates the internal register structure of the SY24696. The 8-bit Pointer Register of the device is used for addressing a given data register. The Pointer Register uses the two least-significant bytes (LSBs) (see Table 14 and Table 15) to identify which of the data registers must respond to a read or write command. Table 5 identifies the bits of the Pointer Register byte. During a write command, P2 through P7 must always be '0'. Table 6 describes the pointer address of the registers available in the SY24696. The power-up reset value of P1 and P0 is 00. By default, the SY24696 reads the temperature on power up.

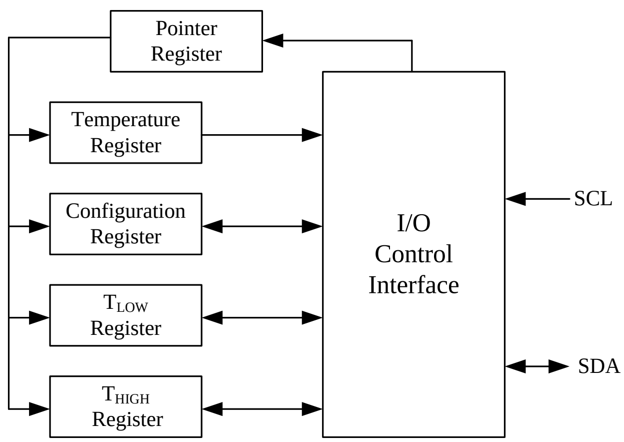


Figure 8. Internal Register Structure

Table 5. Point Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 6. Point Addresses

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

Temperature Register

The Temperature Register of the SY24696 is configured as a 12-bit, read-only register (Configuration Register EM bit = 0, see the Extended Mode section), or as a 13-bit, read-only register (Configuration Register EM bit = 1) that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 7 and Table 8. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits (13 bits in Extended mode) are used for indicating temperature. The least significant byte does not have to be read if that information is not needed.

Table 7. Byte 1 of Temperature Register [1]

D7	D6	D5	D4	D3	D2	D1	D0
T11 （T12）	T10 (T11)	T9 (T10)	T8 (T9)	T7 (T8)	T6 (T7)	T5 (T6)	T4 (T5)

(1) Extended mode 13-bit configuration shown in parenthesis.

Table 8. Byte 2 of Temperature Register [1]

D7	D6	D5	D4	D3	D2	D1	D0
T3 （T4）	T2 (T3)	T1 (T2)	T0 (T1)	0 (T0)	0 (0)	0 (0)	0 (1)

(1) Extended mode 13-bit configuration shown in parenthesis.

Configuration Register

The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. Table 9 and Table 10 list the format and the power-up or reset value of the configuration register. All registers are updated byte by byte.

Table 9. Byte 1 of Configuration and Power-Up or Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
OS 0	R1 1	R0 1	F1 0	F0 0	POL 0	TM 0	SD 0

Table 10. Byte 2 of Configuration and Power-Up or Reset Format

D7	D6	D5	D4	D3	D2	D1	D0
CR1 1	CR0 0	AL 1	EM 0	0 0	0 0	0 0	0 0

1. Shutdown Mode (SD)

The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5μA. Shutdown mode will enable when the SD bit is 1; the device will shut down when current conversion is completed. When SD is equal to 0, the device will maintain a continuous conversion state

2. Thermostat Mode (TM)

The Thermostat mode bit indicates to the device whether to operate in Comparator mode (TM = 0) or Interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the High- and Low-Limit Registers section

3. Polarity (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin will become active low. When the POL bit is set to 1, the ALERT pin will become active high and the state of the ALERT pin will be inverted. The operation of the ALERT pin in various modes is illustrated in Figure 9.

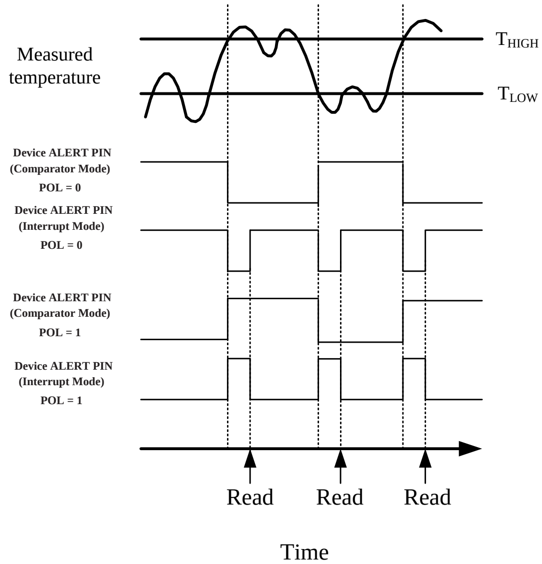


Figure 9. Output Transfer Function Diagrams

4. Fault Queue (F1/F0)

A fault condition will exist when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 11 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the High- and Low-Limit Registers section.

Table 11. SY24696 Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

5. Converter Resolution (R1/R0)

The converter resolution bits, R1 and R0, are read-only bits. The SY24696 converter resolution is set at device start-up to 11 which sets the temperature register to a 12 bit-resolution.

6. One-Shot (OS)

When the device is in Shutdown Mode, writing a 1 to the OS bit will start a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. For more information on the one-shot conversion mode, see the One-Shot/Conversion Ready (OS) section

7. EM Bit

The Extended-Mode bit configures the device for Normal Mode operation (EM = 0) or Extended Mode operation (EM = 1). In normal mode, the temperature register, high-limit register, and low-limit register use a 12-bit data format. For more information on the extended mode, see the Extended Mode (EM) section.

8. Alert (AL Bit)

The AL bit is a read-only function. Reading the AL bit provides information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. When the POL bit equals 0, the AL bit will read as 1 until the temperature equals or exceed $T_{(HIGH)}$ for the programmed number of consecutive faults, causing the AL bit to read as 0.

The AL bit will continue to read as 0 until the temperature falls below $T_{(LOW)}$ for the programmed number of consecutive faults.

9. Conversion Rate (CR)

The conversion rate bits, CR1 and CR0, configure the SY24696 for conversion rates of 0.25Hz, 1Hz, 4Hz, or 8Hz. The default rate is 4Hz. For more information on the conversion rate bits, see Table 4.

High- and Low-Limit Registers

The temperature limits are stored in the $T_{(LOW)}$ and $T_{(HIGH)}$ registers in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or an interrupt, and is set by the TM bit in the configuration register.

In Comparator mode (TM = 0), the ALERT pin will become active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated TLOW value for the same number of faults.

In Interrupt mode (TM = 1), the ALERT pin will become active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions (as shown in Table 4). The ALERT pin will remain active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response address. The ALERT pin will also be cleared if the device is placed in Shutdown mode. When the ALERT pin is cleared, it will become active again only when temperature falls below T_{LOW}, and will remain active until cleared by a read operation of any register or a successful response to the SMBus Alert Response address. When the ALERT pin is cleared, the above cycle will repeat, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This action also clears the state of the internal registers in the device, returning the device to Comparator mode (TM = 0).

Both operational modes are represented in Figure 9. Table 12 through Table 15 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = +80°C and T_{LOW} = +75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register

Table 12. Byte 1 Temperature Register $_{HIGH}$ (1)

D7	D6	D5	D4	D3	D2	D1	D0
H11 (H12)	H10 (H11)	H9 (H10)	H8 (H9)	H7 (H8)	H6 (H7)	H5 (H6)	H4 (H5)

(1) Extended mode 13-bit configuration shown in parenthesis.

Table 13. Byte 2 Temperature Register $_{HIGH}$

D7	D6	D5	D4	D3	D2	D1	D0
H3 (H4)	H2 (H3)	H1 (H2)	H0 (H1)	0 (H0)	0 (0)	0 (0)	0 (0)

Table 14. Byte 1 Temperature Register $_{LOW}$ (1)

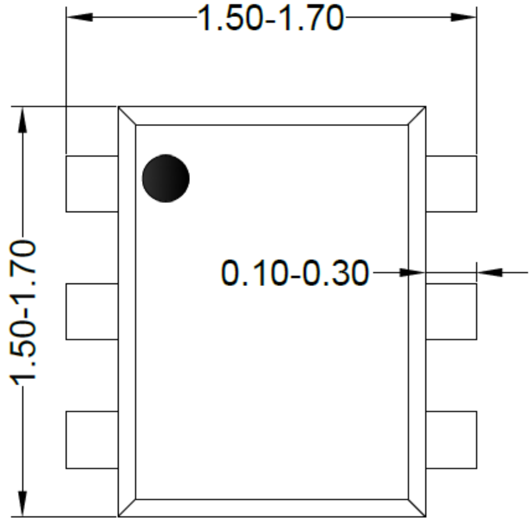
D7	D6	D5	D4	D3	D2	D1	D0
L11 (L12)	L10 (L11)	L9 (L10)	L8 (L9)	L7 (L8)	L6 (L7)	L5 (L6)	L4 (L5)

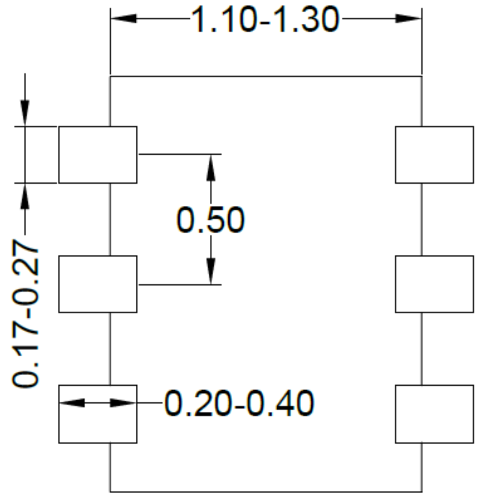
(1) Extended mode 13-bit configuration shown in parenthesis.

Table 15. Byte 2 Temperature Register $_{LOW}$

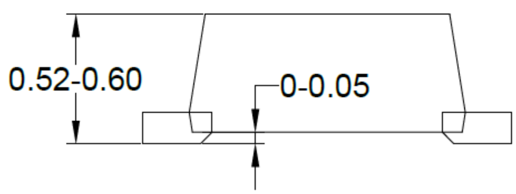
D7	D6	D5	D4	D3	D2	D1	D0
L3 (L4)	L2 (L3)	L1 (L2)	L0 (L1)	0 (L0)	0 (0)	0 (0)	0 (0)

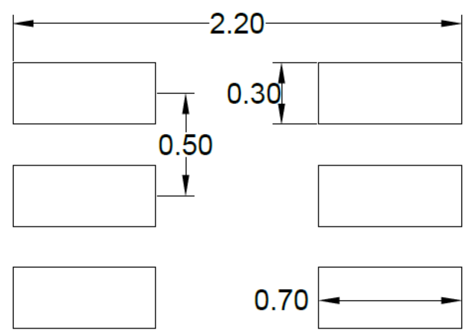
SOT563 Package Outline Drawing





Top view **Bottom view**





Side View

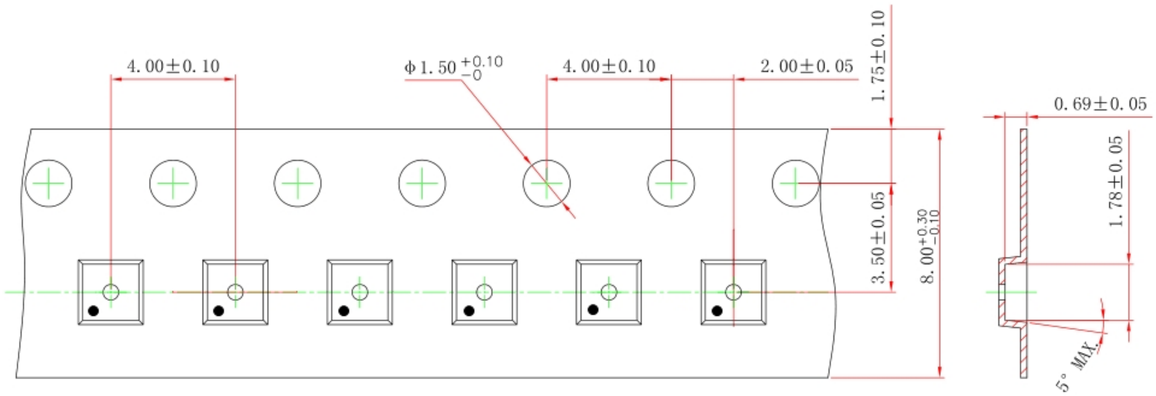
Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

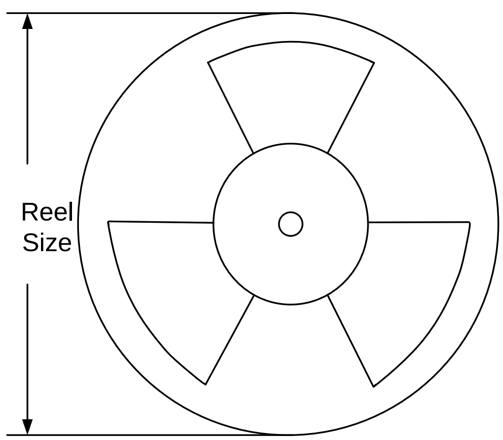
1. Taping Orientation

SOT563



Feeding Direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SOT563	8	4	7"	280	160	5000

3. Others: NA

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