# SY205279

## Low Capacitance TVS Protection

## General Description

The SY205279 is a low-capacitance, bi-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 15pF, the SY205279 is designed to protect parasitic-sensitive systems against overvoltage and overcurrent transient events. It complies with IEC 61000-4-2 (ESD), (±30kV air, ±30kV contact discharge), and IEC 61000-4-5 (Surge) (7A, 8/20μs) standards.

Each SY205279 device can protect one line. It is available in a compact DFN0.6×0.3-2 or DFN1.0×0.6-2 or SOD-523 package.

## Features

- Operating Voltage: 5V and Below
- Transient Protection for High-Speed Data Lines
  - IEC61000-4-2 (ESD) ±30kV (Air) ±30kV (Contact)
  - IEC61000-4-5 (Surge) 7A (8/20μs)
- Low Capacitance: 15pF(Typical)
- Low Leakage Current: 0.1μA at $V_{RWM}$ (Max)
- Low Clamping Voltage

## Applications

- Portable Electronics
- Desktops, Servers and Notebooks
- Smart Phones
- MP3 Ports
- Digital Camera Ports

## Mechanical Characteristics

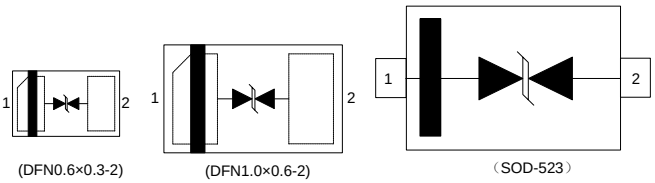
- DFN0.6×0.3-2/DFN1.0×0.6-2/SOD-523 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

## Circuit Diagram

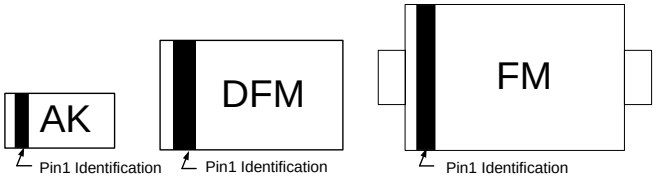
## Ordering Information

| Part Number | Package Type | Top Mark |
|---|---|---|
| SY205279DXD | DFN0.6×0.3-2 | AK |
| SY205279DWD | DFN1.0×0.6-2 | DFM |
| SY205279ANO | SOD-523 | FM |

## Pinout (Top View)




## Marking Codes




*Notes: "AK", "DF" and "F" are the device code, fixed.*
*"M" is the date code.*

## Pin Descriptions

| Device Pins | Name | Description |
|---|---|---|
| 1 | Input/Output | IO |
| 2 | Input/Output | IO |

| **Absolute Maximum Ratings**(Note 1) | | | | |
|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** |
| Maximum Peak Pulse Current (8/20μs) | $I_{PP}$ | | 7 | A |
| Maximum Peak Pulse Power (8/20μs) | $P_{PK}$ | | 65 | W |
| ESD per IEC 61000-4-2 (Air)<br>ESD per IEC 61000-4-2 (Contact) | $V_{ESD}$ | -30<br>-30 | 30<br>30 | kV |
| Junction Temperature | $T_J$ | -40 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -55 | +150 | °C |

| **Electrical Characteristics** (IO Referenced to IO, $T_A$ = 25°C, Note 4) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Min** | **Typ** | **Max** | **Unit** |
| Nominal Reverse Working Voltage | $V_{RWM}$ | | -5.0 | | 5.0 | V |
| Reverse Leakage Current at $V_{RWM}$ | $I_R$ | $V_{RWM}$ = 5V, $T_A$ = 25°C | | 0.01 | 0.1 | μA |
| Reverse Breakdown Voltage at $I_T$ | $V_{BR}$ | $I_t$=1mA | 5.4 | | 8 | V |
| Clamping Voltage at $I_{PP}$ (Note 5) | $V_C$ | $I_{PP}$ = 7A, $t_p$ = 8/20μs | | 9 | 15 | V |
| Clamping Voltage at $I_{PP}$ (Note 5) | $V_C$ | $I_{PP}$ = 16A, $t_p$ = 10/100ns | | 7.5 | | V |
| Dynamic Resistance (Note 2, 5) | $R_{DYN}$ | $t_p$ = 10/100ns | | 0.09 | | Ω |
| Parasitic Capacitance (Note 5) | $C_{ESD}$ | $V_R$ = 0V, f = 1MHz | | 15 | 20 | pF |

**Note 1:** Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended

periods may affect device reliability.

**Note 2:** $R_{DYN}$ calculated based on $I_{PP}$=8A to $I_{PP}$=16A, $t_p$ = 10/100ns.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

**Note 5:** Guaranteed by design or statistical correlation and not production tested.

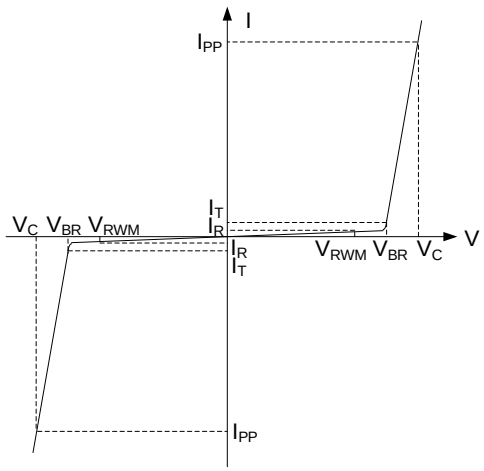
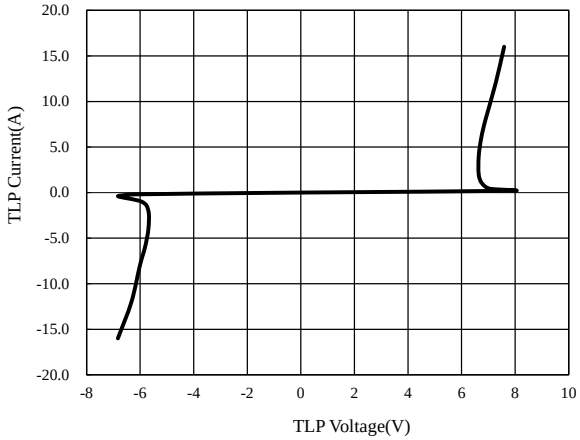


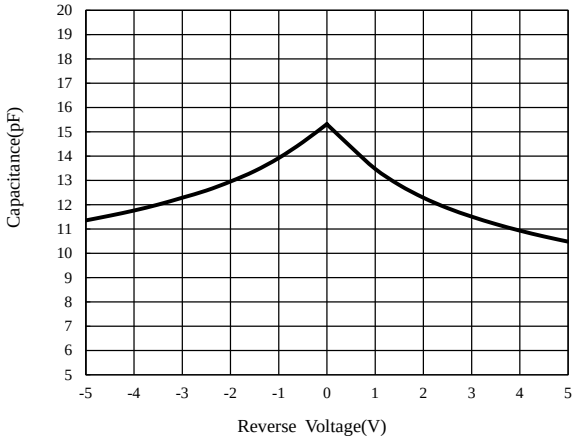

*Figure 1. Bi-Directional TVS*

## Typical Performance Characteristics, Between IO1 and IO2

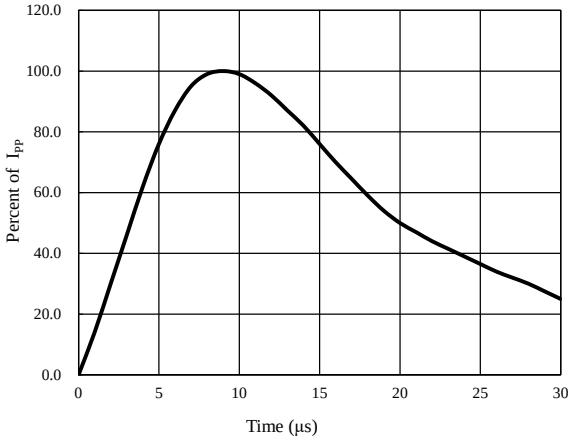
TLP Testing



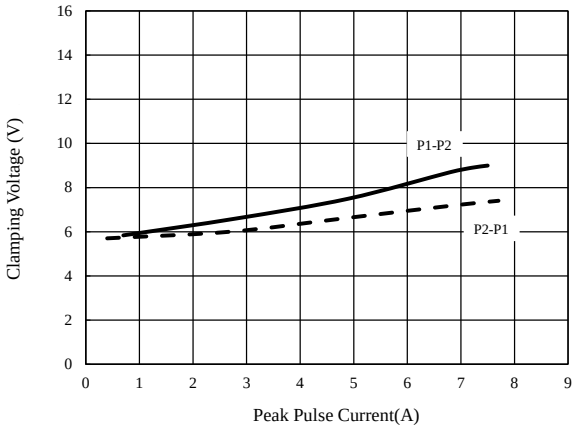

Capacitance vs. Voltage




Pulse Waveform




Clamping Voltage vs. Peak Pulse Current

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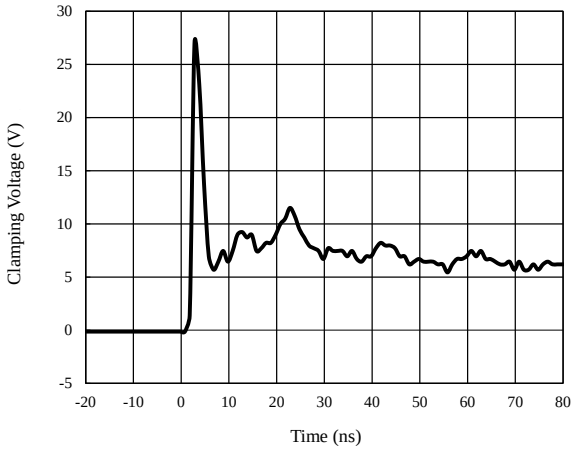
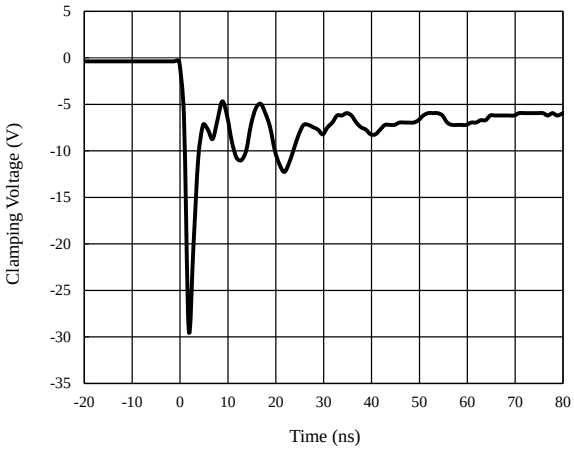
ESD Clamping
(+8kV Contact per IEC 61000-4-2)




ESD Clamping
(-8kV Contact per IEC 61000-4-2)



# Application Information

## PCB Pin Connections

The SY205279 is designed to protect one bi-directional data or power line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The SY205279 pin connections are shown in Figure 2. The protected line connects to one of the pins, while the other is connected to GND, which should connect to a ground plane on the board. All path lengths connected to the pins of SY205279 should be as short as possible to minimize parasitic inductance.

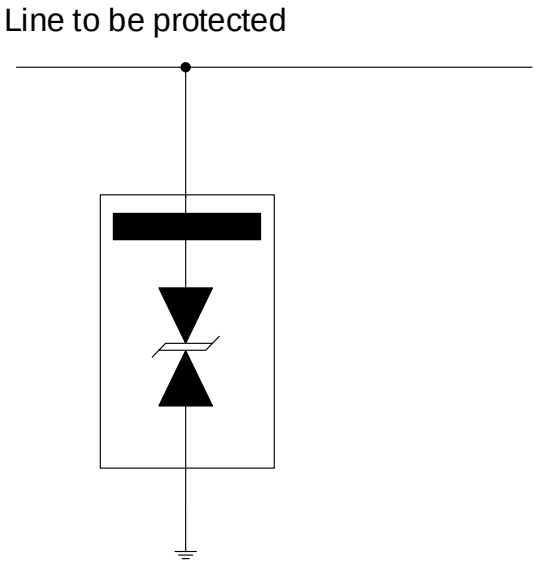


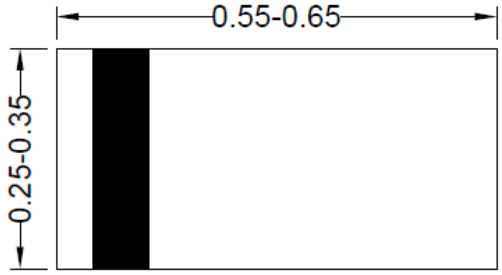

*Figure 2 ESD/Surge Protection Circuit*

# PCB Layout Guidelines

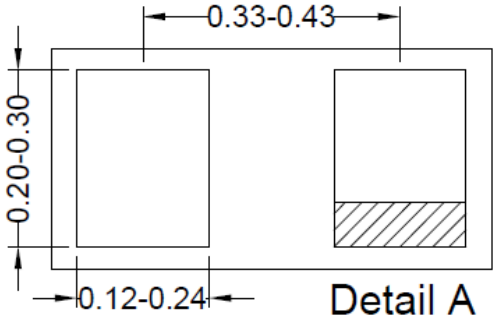
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place the SY205279 as close to the connectors or terminal ports as possible.
- Use a large via to connect the SY205279 pin to the ground.
- Avoid running signals near board edges.
- The SY205279 should be placed near the protected line.
- The distance between the SY205279 ground pin to the board ground rail should be as short as possible to reduce the ESD transient return path to ground.

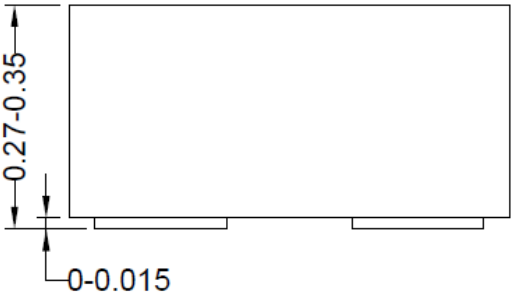
## DFN0.6×0.3-2 Package Outline



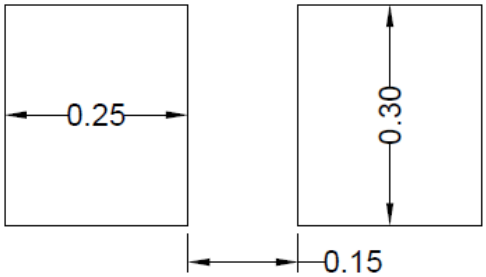

**Top View**



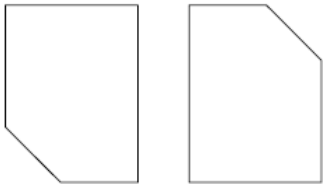

**Bottom View**




**Front View**



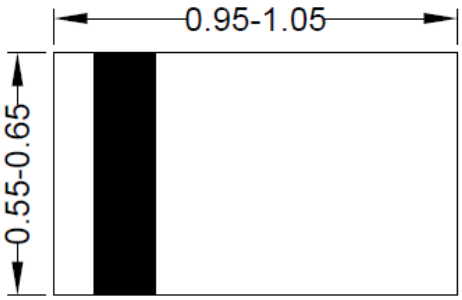

**Recommended PCB Layout**
**(Reference only)**



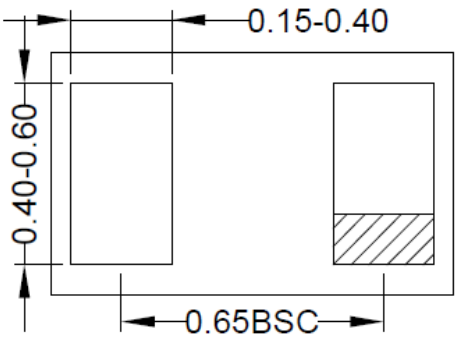
**Detail A**
**Pin1 Identifier: Two Options**

*Notes: All dimensions are in millimeters and exclude mold flash and metal burr.*

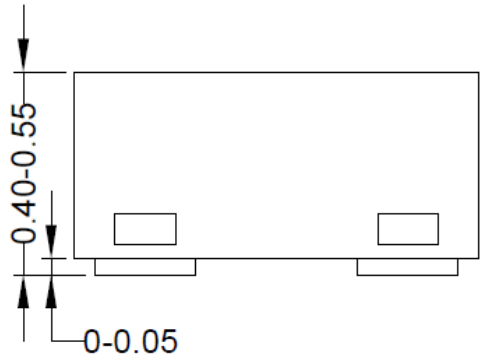
## DFN1.0×0.6-2 Package Outline



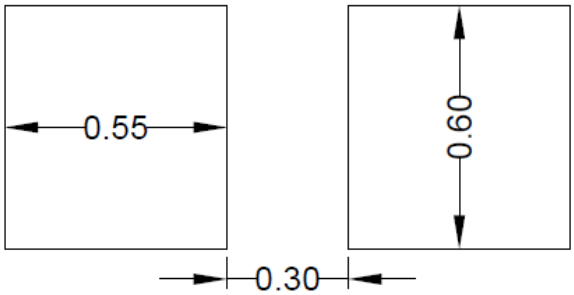

**Top View**




**Bottom View**




**Front View**

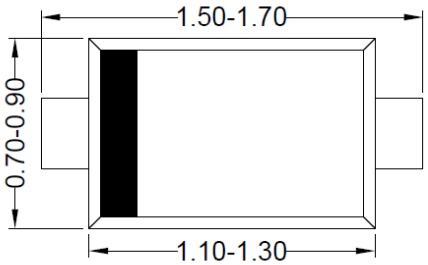



**Recommended PCB Layout**
**(Reference only)**

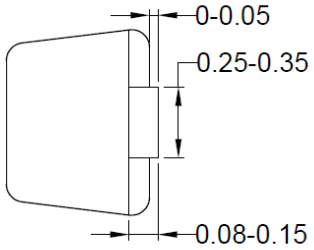
**Detail A**
**Pin1 Identifier: Three Options**

*Note: All dimensions are in millimeters and exclude mold flash and metal burr.*

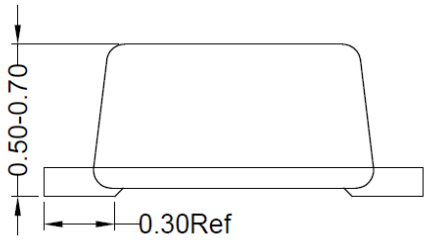
## SOD-523 Package Outline



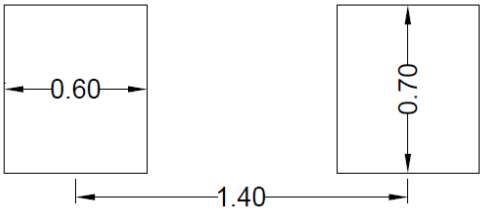

**Top View**




**Side View A**




**Side View B**



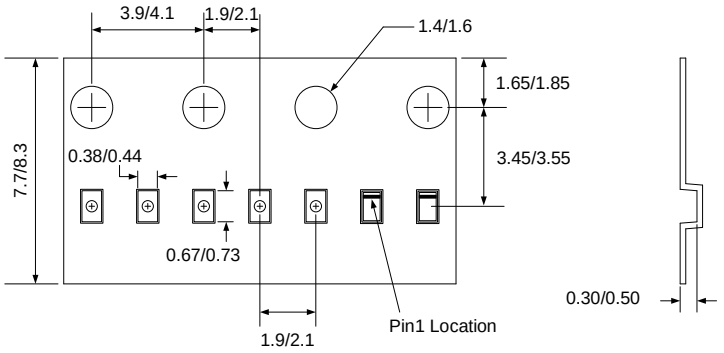

**Recommended PCB Layout (Reference only)**

*Note: All dimensions are in millimeters and exclude mold flash and metal burr*

# Tape and Reel Information

## Tape Dimensions and Pin 1 Orientation

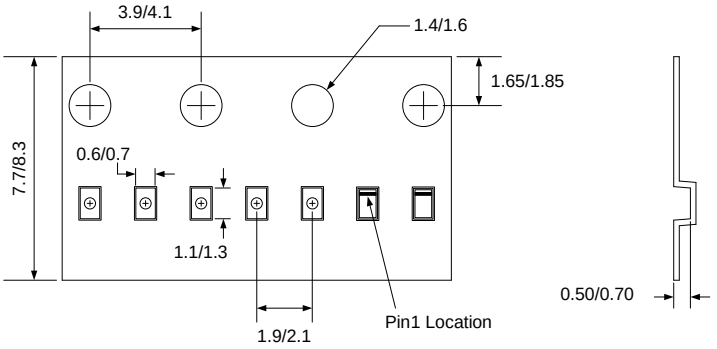
DFN0.6×0.3-2




*Dimensions In mm*

**Feeding direction**

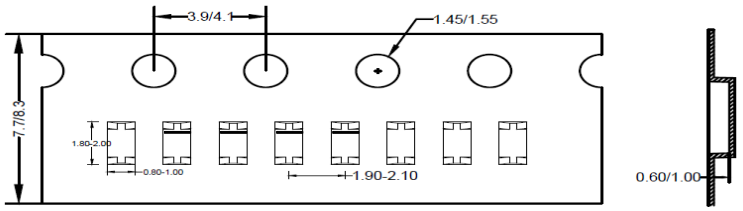
DFN1.0×0.6-2




*Dimensions In mm*

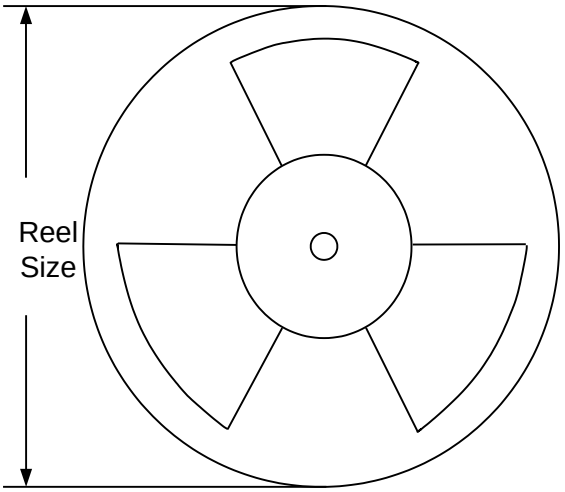
**Feeding direction**

SOD-523




**Feeding direction**

## Reel Dimensions




| Package Type | Tape Width (mm) | Pocket Pitch(mm) | Reel Size (Inch) | Qty per Reel (pcs) |
|---|---|---|---|---|
| DFN0.6×0.3-2 | 8 | 2 | 7" | 10000 |
| DFN1.0×0.6-2 | 8 | 2 | 7" | 10000 |
| SOD-523 | 8 | 2 | 7" | 8000 |

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

| Revision Number | Revision Date | Description | Pages changed |
|---|---|---|---|
| 1.0 | Nov.14,2024 | Initial Release | |
| 1.0 | Mar.17,2025 | SY205279ANO related information added | |

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