SYT16S03DVC

Ultra-Low Capacitance TVS Protection

Features

- Transient protection for high-speed data lines
  IEC 61000-4-2 (ESD) ±15kV (Air)
  ±15kV (Contact)
  IEC 61000-4-5 (Surge) 3A (8/20μs)
- For 3.3V and below operating voltage
- Ultra-small package (2.5mm*1.0mm*0.55mm)
- Protects four data lines
- Ultra Low capacitance: 0.25pF for each channel
- Low leakage current: 0.1μA @ V_{RWM} (Max.)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge
- Pb free & RoHS Compliant

Description

SYT16S03DVC is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.25pF only, SYT16S03DVC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) (±15kV air, ±15kV contact discharge), IEC 61000-4-5 (Surge) (3A, 8/20μs), etc.

SYT16S03DVC uses small DFN2.5*1.0-10 package. Each SYT16S03DVC device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SYT16S03DVC ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the SYT16S03DVC guarantees a minimum stress on the protected IC.

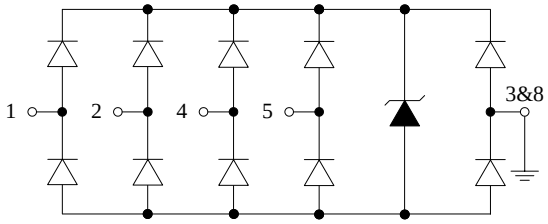
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB2.0, 3.0 and 3.1
- Display Ports
- HDMI 1.3, 1.4, 2.0 and 2.1.
- Digital Visual Interfaces (DVI)

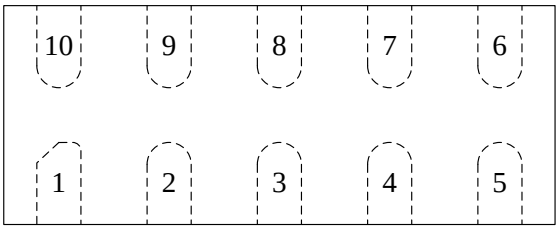
Mechanical Characteristics

- DFN2.5*1.0-10 package
- Flammability Rating: UL 94V-0
- Marking: Part number, Date
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



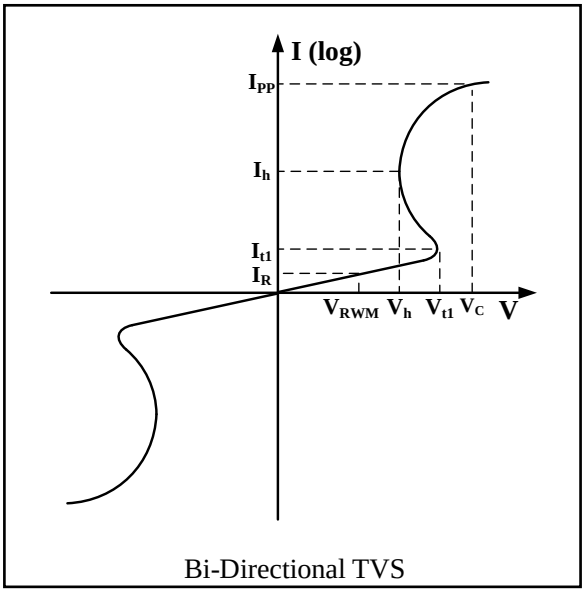
DFN2.5*1.0-10
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (8/20μs)	3	A
P_{PK}	Peak Pulse Power (8/20μs)	50	Watts
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±15 ±15	kV
T_{OPT}	Operating Temperature	-40/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25°C)

Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{t1}	Reverse Triggering Voltage @ I_{t1}
I_{t1}	Test Current for Reverse Triggering
V_h	Holding Voltage @ I_h
I_h	Test Current for Holding Voltage
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency



Bi-Directional TVS

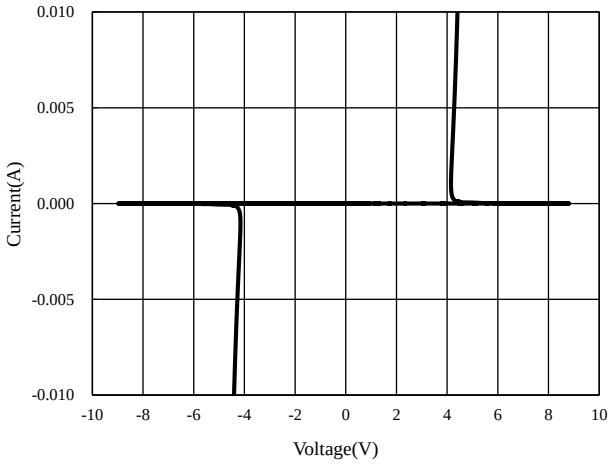
Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				3.3	V
I_R	V_{RWM} = 3.3V, T = 25°C Between I/O and GND		0.01	0.1	μA
V_h	I_h = 1mA Between I/O and GND	3.7			V
V_C[1]	I_{PP} = 3A, t_p = 8/20μs Between I/O and GND			11	V
V_C[1]	I_{PP} = 16A, t_p = 10/100ns Between I/O and GND		10		V
R_{DYN}[1,2]	t_p = 10/100ns Between I/O and GND		0.3		Ω
C_{ESD}[1]	V_R = 3.3V, f = 1MHz Between Any Pins		0.25	0.30	pF

NOTES

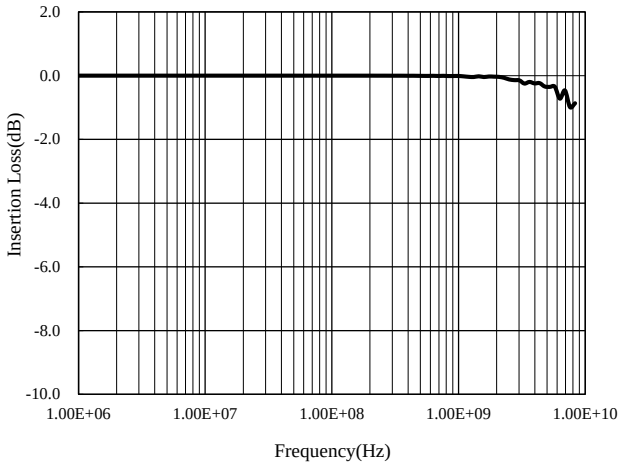
[1]Guaranteed by design and not subject to production test.

[2]R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

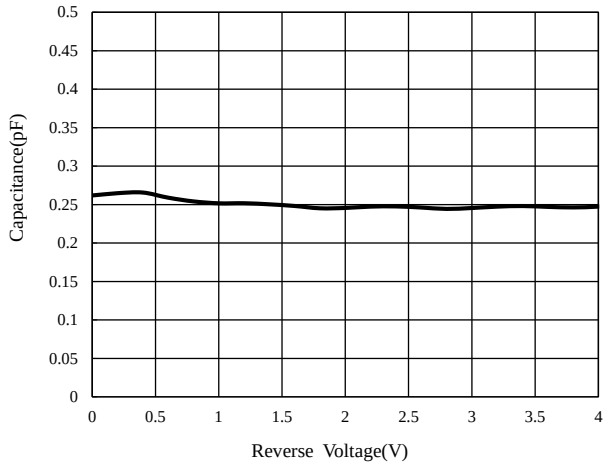
Current Sweeping of I/O to GND



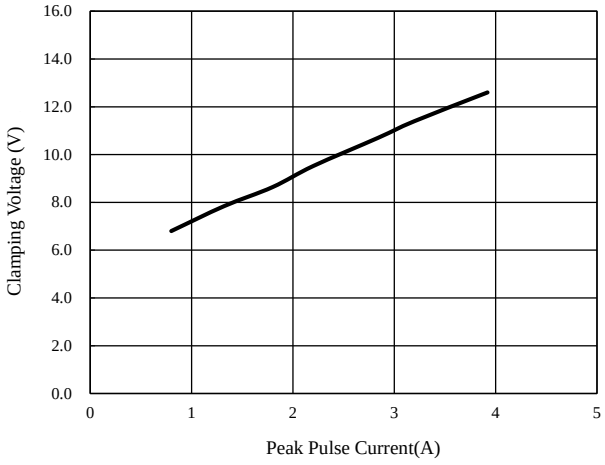
Insertion Loss S21 of I/O to GND



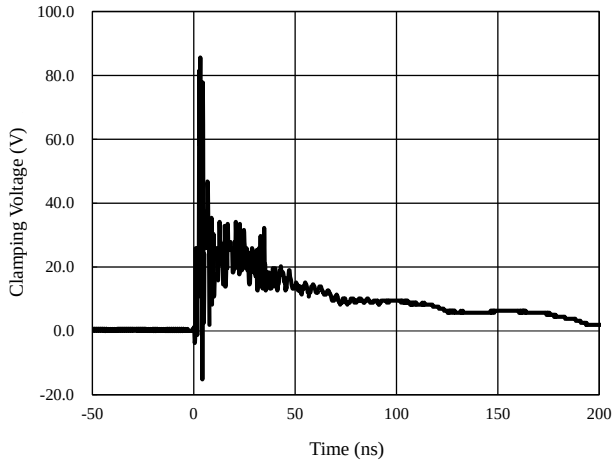
Capacitance vs. Voltage of I/O to GND



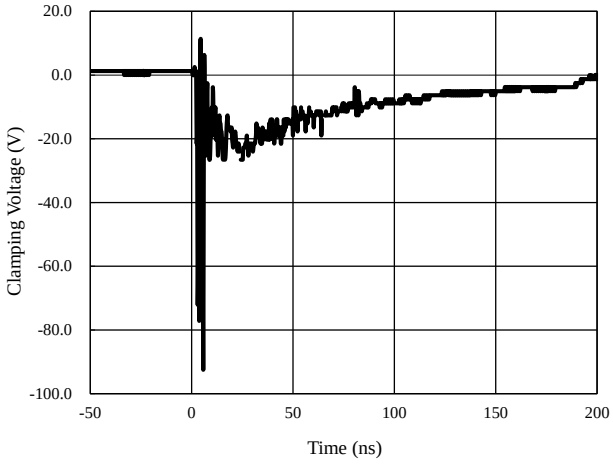
Clamping Voltage vs. Peak Pulse Current (8/20μs)



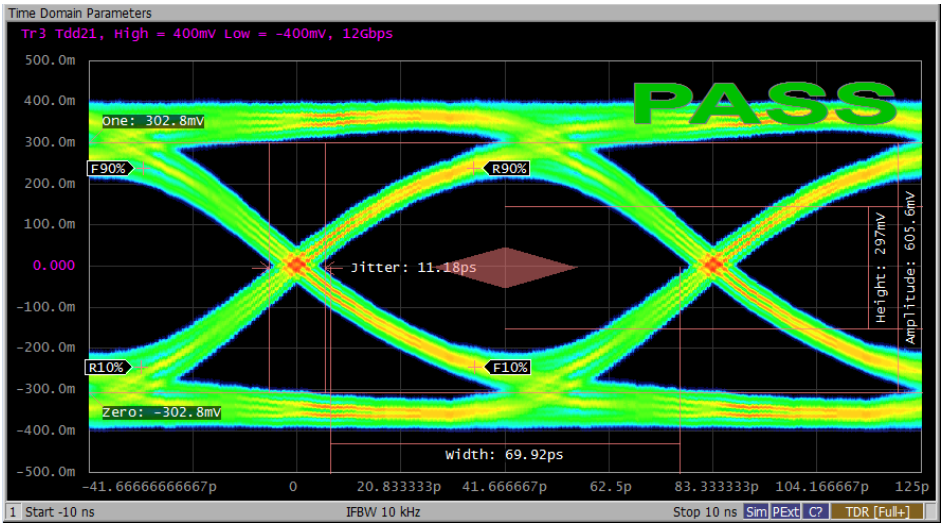
ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)

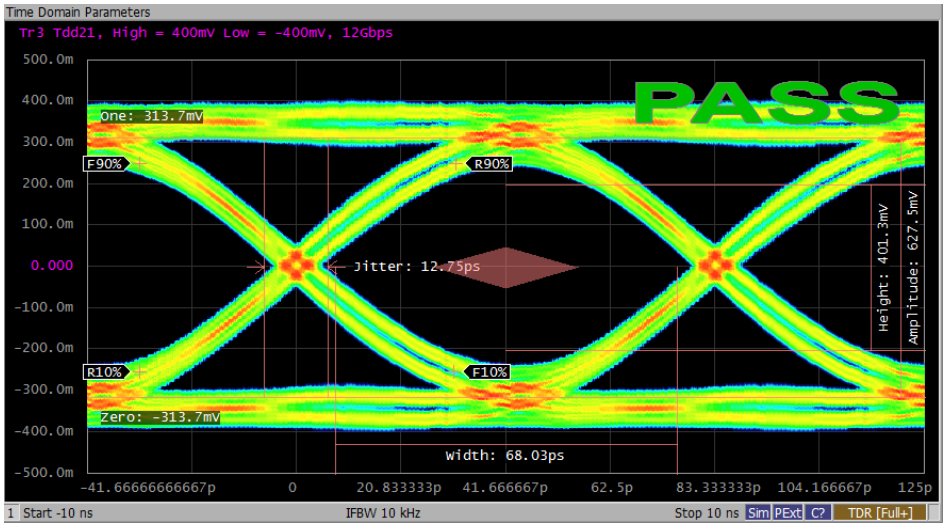


Eye Diagram Measurement For HDMI2.1



Data rate 12Gb/s

HDMI2.1 Eye Diagram without SYT16S03DVC



Data rate 12Gb/s

HDMI2.1 Eye Diagram with SYT16S03DVC

Application Information

Pin Connection in PCB

SYT16S03DVC provides ESD protection for four data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, could connect to SYT16S03DVC four I/O pins directly. Pin 3&8 of SYT16S03DVC is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

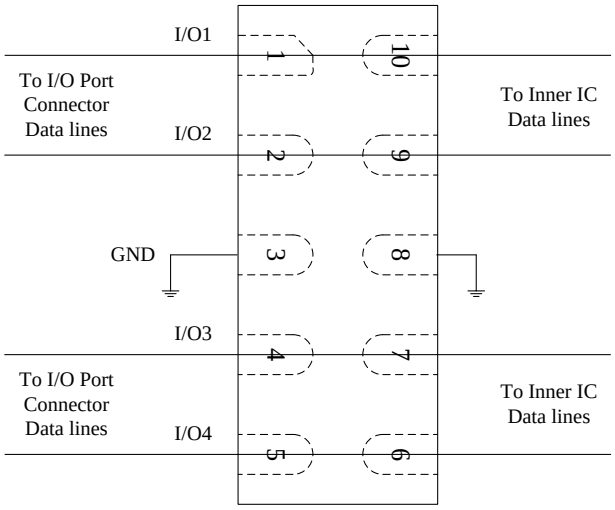


Figure 1 SYT16S03DVC pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- SYT16S03DVC GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting SYT16S03DVC GND pins to the PCB GND should be wide.
- Place SYT16S03DVC as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

Application Information

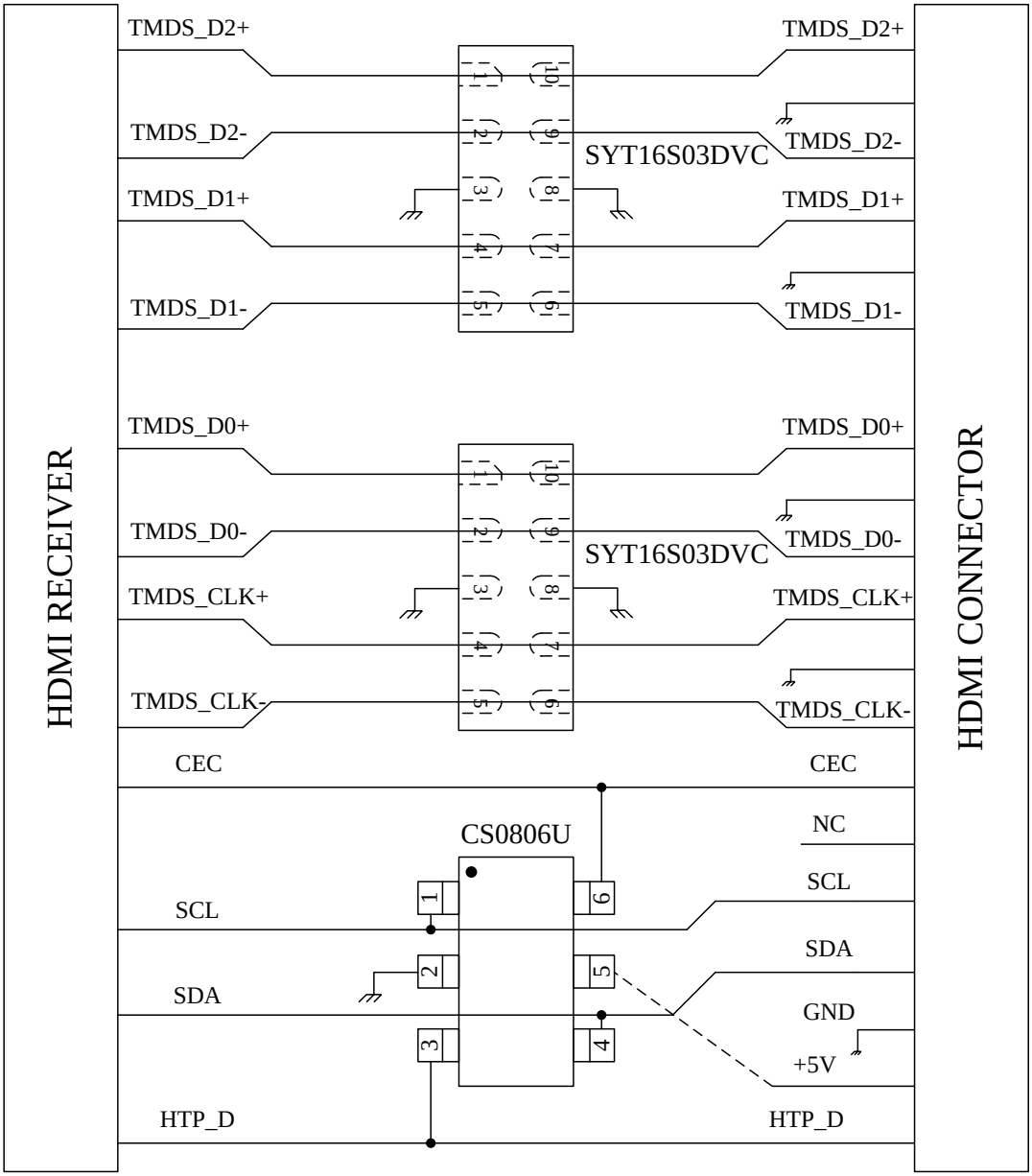
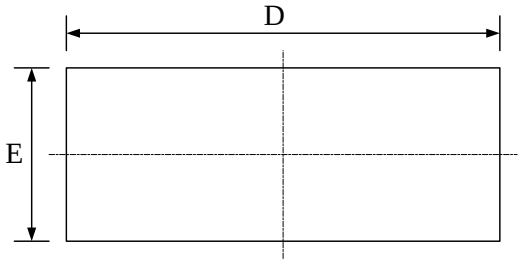


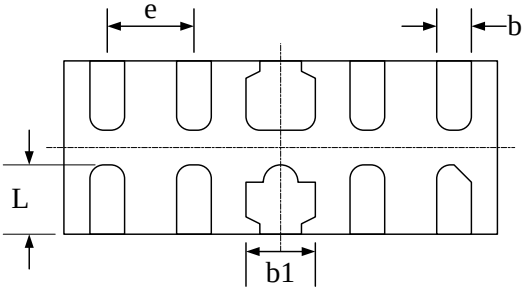
Figure 2 Layout Top View for HDMI Interface with SYT16S03DVC & CS0806U

Package Outline

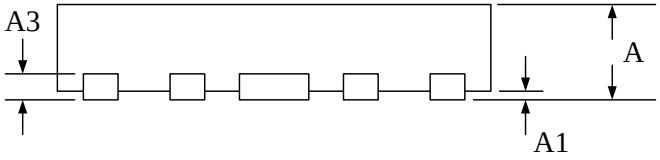
- DFN2.5*1.0-10 package



TOP VIEW



BOTTOM VIEW



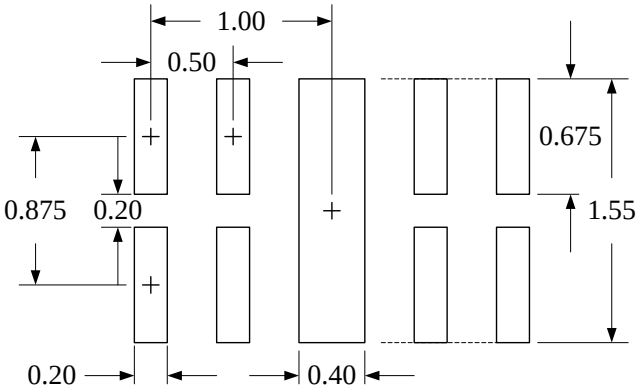
SIDE VIEW

Package Dimensions

Symbol	Dimensions (mm)	
	Minimum	Maximum
A	0.450	0.650
A1	0.000	0.050
A3	0.15REF.	
b	0.150	0.250
b1	0.350	0.450
D	2.450	2.550
E	0.950	1.050
e	0.500 BSC	
L	0.300	0.400

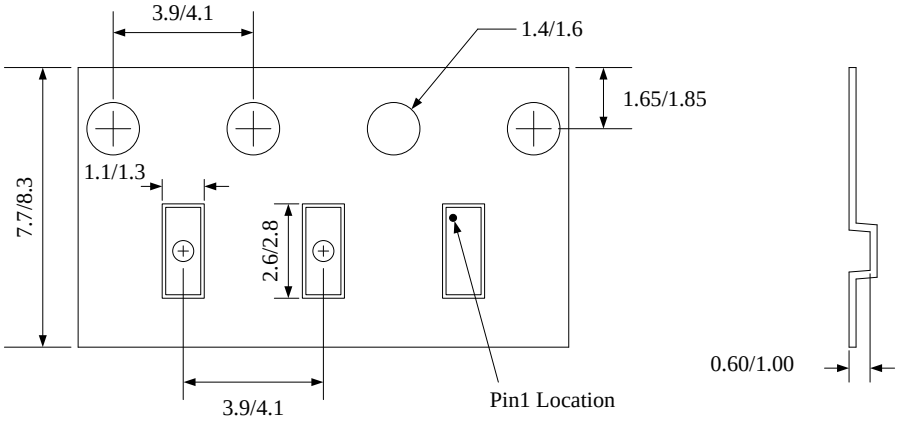
Notes: All dimension in millimeter and exclude mold flash & metal burr.

PCB Layout Pattern



Notes: All dimension in millimeter

Tape and Reel Specification



Dimensions In mm

Feeding direction →

Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
DFN2.5*1.0-10	8	4	7"	400	400	3000

Marking Codes

Note:

(1) "Ym" is the part number of SYT16S03DVC, fixed.
(2) "Y" is year code, from 0 to 9, for 2015 "Y" is 5.
(3) "W" is date code. "W" is the assembly week in a year, from 1 to 0, A to Z.
(4) "A" is the production lot number, from A to Z.

Ordering Information

Part Number	Quantity Per Reel	Reel Size
SYT16S03DVC	3,000	7 Inch

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	June. 15, 2017	Initial Release	
1.0	June. 15, 2018	Production Release	

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