

### General Description

The SYT21N03DWD is a single-line, Bi-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for various applications. The SYT21N03DWD is designed to protect sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other overcurrent transient events. It complies with IEC 61000-4-2 (ESD) ( $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge), and IEC 61000-4-5 (Surge) 28A (8/20 $\mu\text{s}$ ) standards.

The SYT21N03DWD is available in a DFN1.0x0.6-2L package.

### Features

- Operating Voltage: 3.3V and Below
- Transient Protection for A Single Line
  - IEC61000-4-2 (ESD)  $\pm 30\text{kV}$  (Air)  $\pm 30\text{kV}$  (Contact)
  - IEC61000-4-5 (Surge) 28A (8/20 $\mu\text{s}$ )
- Low Capacitance: 45pF (Typical)
- Low Leakage Current: 0.01 $\mu\text{A}$  at  $V_{\text{RWM}}$  (Typical)
- Low Clamping Voltage

### Applications

- Portable Electronics
- Desktops, Servers and Notebooks
- Cellular Phones
- Digital Camera Ports

### Mechanical Characteristics

- DFN1.0x0.6-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

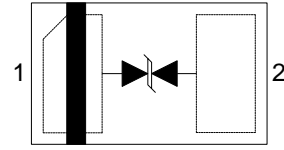
### Circuit Diagram



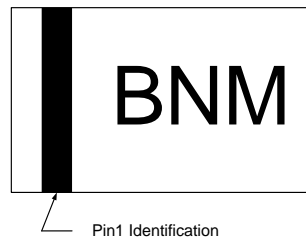
## Ordering Information

## Pinout (Top View)

Part Number	Package Type	Top Mark
SYT21N03DWD	DFN1.0x0.6-2	BNM



## Marking Codes



Notes: "BN" is the device code, fixed.

"M" is the date code.

Absolute Maximum Ratings (Note 1)				
Parameter	Symbol	Min	Max	Unit
Peak Pulse Current (8/20 $\mu$ s)	$I_{PP}$		28	A
Peak Pulse Power (8/20 $\mu$ s)	$P_{PK}$		190	W
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	-30	30	kV
ESD per IEC 61000-4-2 (Contact)		-30	30	
Junction Temperature	$T_J$	-40	+125	$^{\circ}$ C
Storage Temperature	$T_{STG}$	-55	+150	$^{\circ}$ C

Electrical Characteristics(Between IO1 and IO2, $T_A = 25^{\circ}$ C, Note 4)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	$V_{RWM}$				3.3	V
Reverse Leakage Current at $V_{RWM}$	$I_R$	$V_{RWM} = 3.3V, T_A = 25^{\circ}$ C		0.01	0.1	$\mu$ A
Reverse Breakdown Voltage at $I_T$	$V_{BR}$	$I_T = 1mA$	3.3			V
Dynamic Resistance (Note 2, 5)	$R_{DYN}$	$t_p = 10/100ns$		0.08		$\Omega$
Clamping Voltage at $I_{PP}$ (Note 5)	$V_C$	$I_{PP} = 28A, t_p = 8/20\mu s$		7		V
Clamping Voltage at $I_{PP}$ (Note 5)	$V_C$	$I_{PP} = 16A, t_p = 10/100ns$		4.9	5.5	V
Parasitic Capacitance (Note 5)	$C_{ESD}$	$V_R = 0V, f = 1MHz$		45	55	pF

**Note 1:** Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $R_{DYN}$  calculated based on  $I_{PP}=8A$  to  $I_{PP}=16A, t_p = 10/100ns$ .

**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that  $T_A \cong T_J = 25^{\circ}$ C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage

range(s) are guaranteed by design, test, or statistical correlation.

**Note 5:** Guaranteed by design or statistical correlation and not production tested.

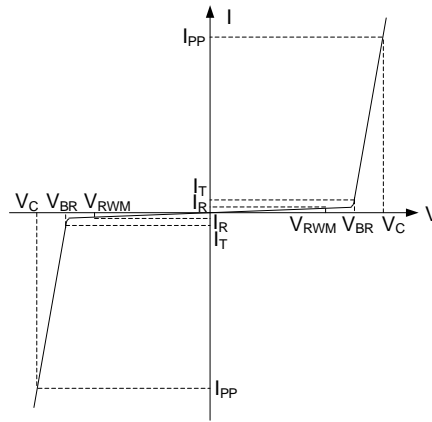
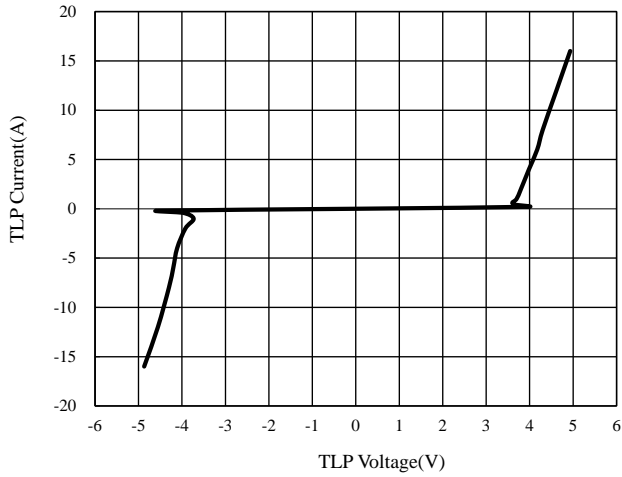


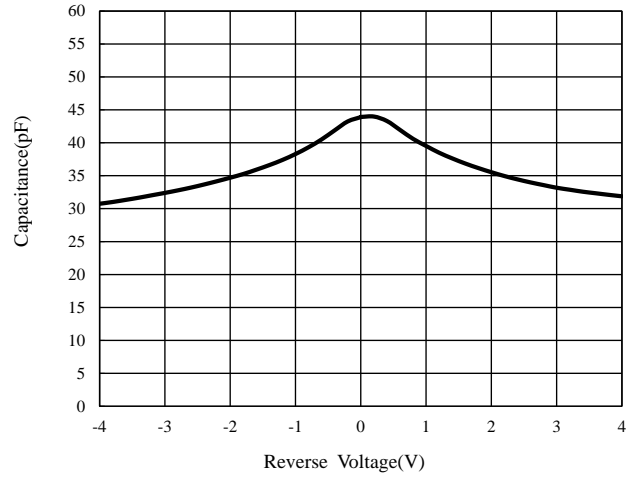
Figure 1. Bi-Directional TVS

## Typical Performance Characteristics, Between IO1 and IO2

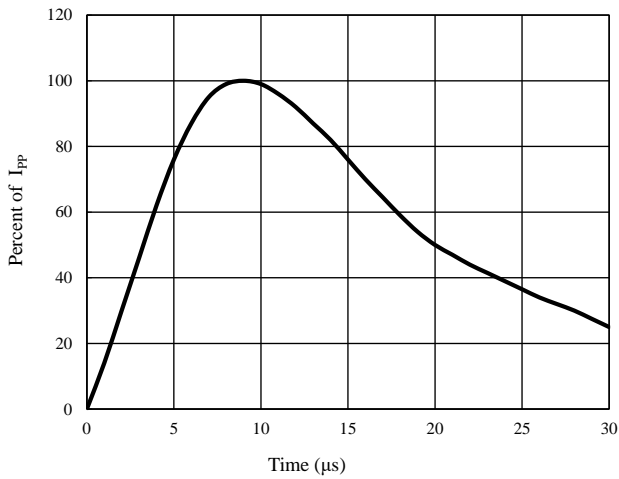
TLP Testing



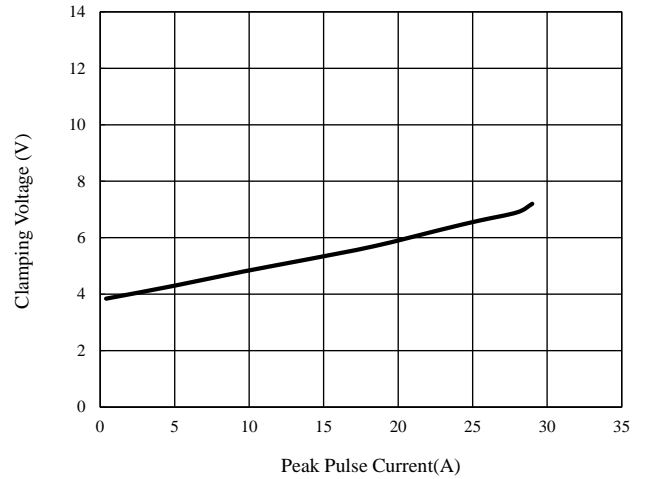
Capacitance vs. Voltage



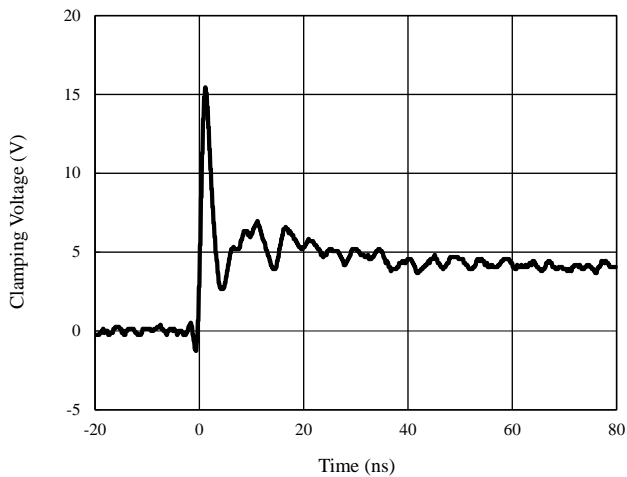
Pulse Waveform



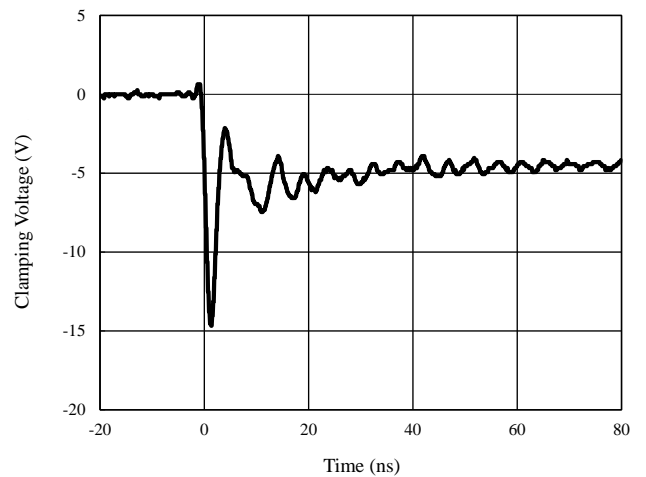
Clamping Voltage vs. Peak Pulse Current



ESD Clamping  
(+8kV Contact per IEC 61000-4-2)



ESD Clamping  
(-8kV Contact per IEC 61000-4-2)



## Application Information

### PCB Pin Connections

The SYT21N03DWD protects one Bi-directional data or power line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The SYT21N03DWD pin connections are shown in Figure 2. The protected line connects to one of the pins, while the other is connected to GND, which should connect to a ground plane on the board. All path lengths connected to the pins of the SYT21N03DWD should be as short as possible to minimize parasitic inductance.

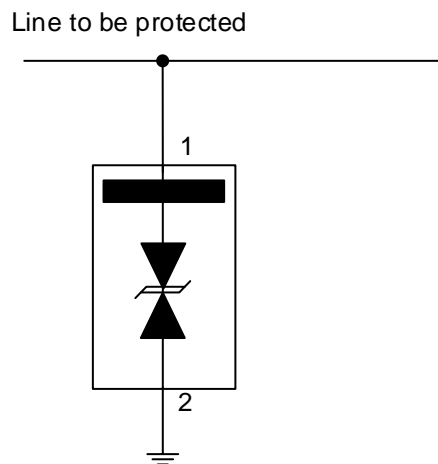


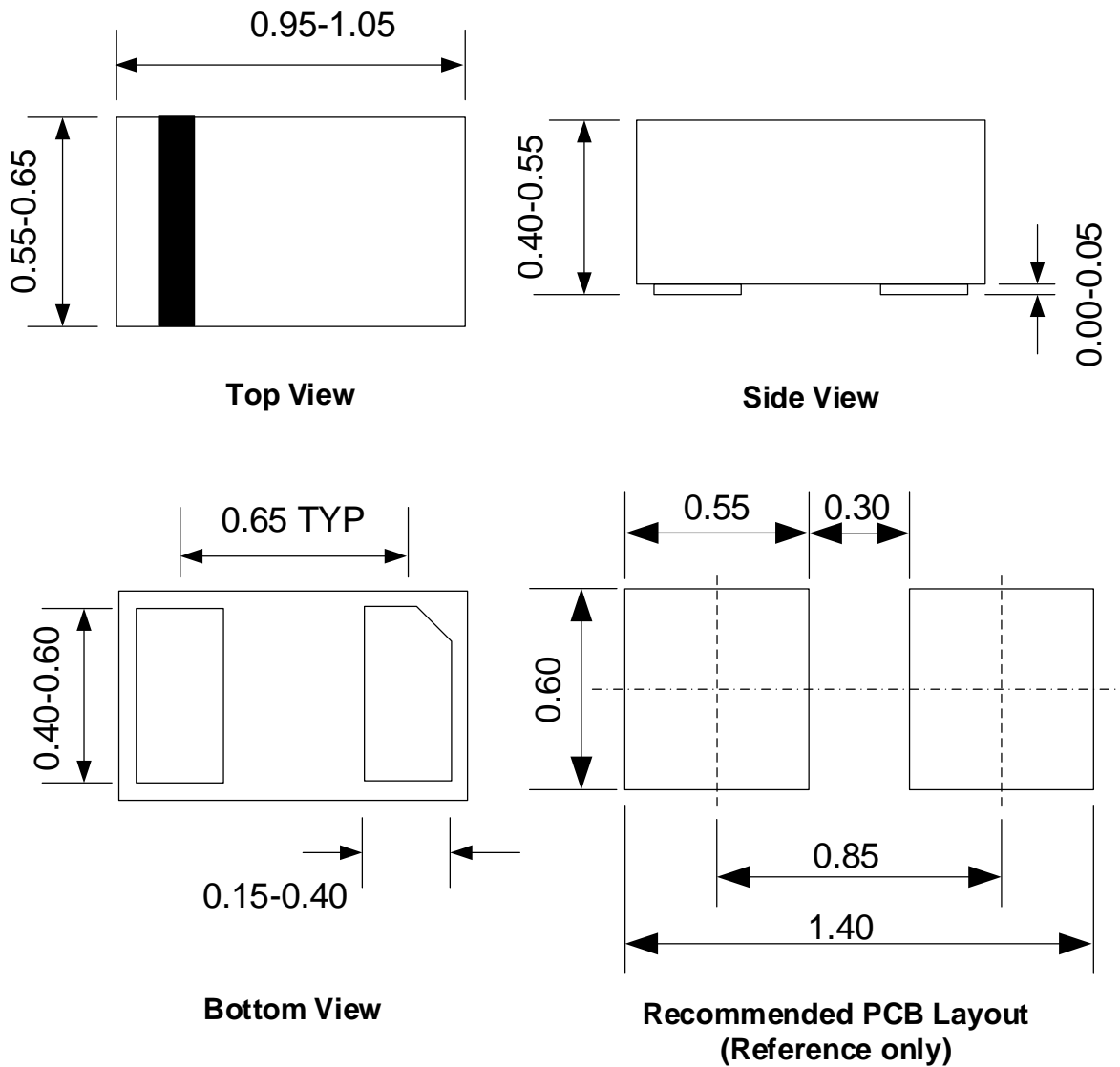
Figure 2. ESD/Surge Protection

## PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SYT21N03DWD as close to the connector or terminal ports as possible.
- Use a large via to connect the SYT21N03DWD pin to the ground.
- Avoid running signals near board edges.
- The SYT21N03DWD should be placed near the protected line.
- The distance between the SYT21N03DWD ground pin and the GND reference path should be as short as possible.

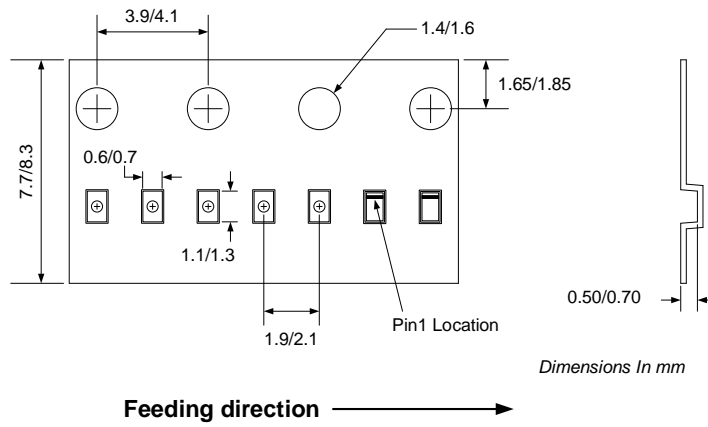
## DFN1.0x0.6-2 Package Outline



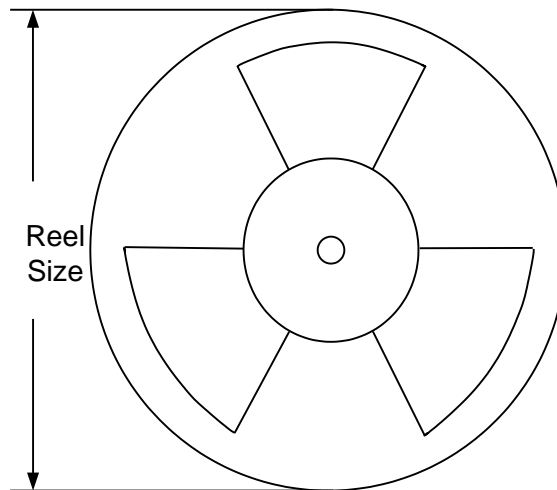
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

## Tape and Reel Information

### Tape Dimensions and Pin 1 Orientation



### Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.0×0.6-2	8	2	7"	10000



## Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	May.06, 2025	Initial Release	

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