



SYS42V04SLD

Single Line TVS Diode for ESD Protection

General Description

The SYS42V04SLD is a single-line, uni-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for various applications. The SYS42V04SLD is designed to protect sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other overcurrent transient events. It complies with IEC 61000-4-2 (ESD) ($\pm 30\text{kV}$ air, $\pm 30\text{kV}$ contact discharge), and IEC 61000-4-5 (surge) 170A (8/20 μs) standards.

The SYS42V04SLD is available in a DFN1.6 \times 1.0-2L package.

Features

- Operating Voltage: 4.8V and Below
- Transient Protection for a Single Line
 - IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (Air) $\pm 30\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 170A (8/20 μs)
- Low Capacitance: 1000pF (Typical)
- Low Leakage Current: 10 μA at V_{RWM} (Typical)
- Low Clamping Voltage

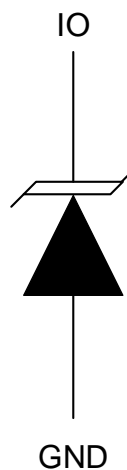
Applications

- VBUS and VBAT Lines
- Desktops, Servers, and Notebooks
- Smartphones
- Microprocessor-Based Equipment
- Portable Instrumentation

Mechanical Characteristics

- DFN1.6 \times 1.0-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

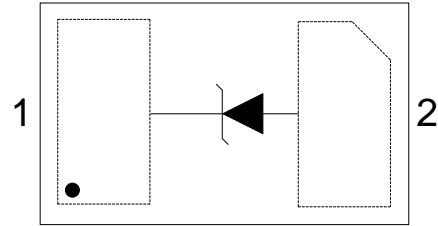
Circuit Diagram



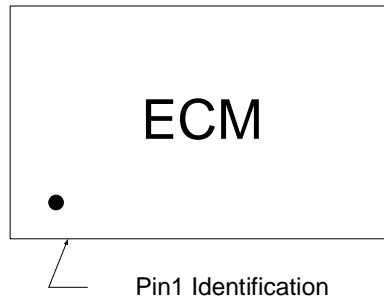
Ordering Information

Part Number	Package Type	Top Mark
SYS42V04SLD	DFN1.6x1.0-2	ECM

Pinout (Top View)



Marking Codes



Notes: “EC” is the device code, fixed.

“M” is the date code.

Absolute Maximum Ratings(Note 1)				
Parameter	Symbol	Min	Max	Unit
Peak Pulse Current (8/20 μ s)	I_{PP}		170	A
Peak Pulse Power (8/20 μ s)	P_{PK}		1600	W
ESD per IEC 61000-4-2 (Air)	V_{ESD}	-30	30	kV
ESD per IEC 61000-4-2 (Contact)		-30	30	
Junction Temperature	T_J	-45	+125	$^{\circ}$ C
Storage Temperature	T_{STG}	-55	+150	$^{\circ}$ C

Electrical Characteristics (From IO to GND, $T_A = 25^{\circ}$ C, Note 4)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	V_{RWM}				4.8	V
Reverse Leakage Current at V_{RWM}	I_R	$V_{RWM} = 4.5V, T_A = 25^{\circ}C$			20	μ A
Reverse Breakdown Voltage at I_T	V_{BR}	$I_T = 1mA$	5.1		7	V
Forward Voltage at I_F	V_F	$I_F = 1mA$	0.55		0.85	V
Dynamic Resistance (Note 2, 5)	R_{DYN}	$t_p = 10/100ns$		0.01		Ω
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 170A, t_p = 8/20\mu s$		9.5		V
Clamping Voltage at I_{PP} (Note 5)	V_C	$I_{PP} = 16A, t_p = 10/100ns$		5		V
Parasitic Capacitance (Note 5)	C_{ESD}	$V_R = 0V, f = 1MHz$		1000	1200	pF

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may

affect device reliability.

Note 2: R_{DYN} calculated based on $I_{PP}=8A$ to $I_{PP}=16A$, $t_p = 10/100ns$.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ C$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

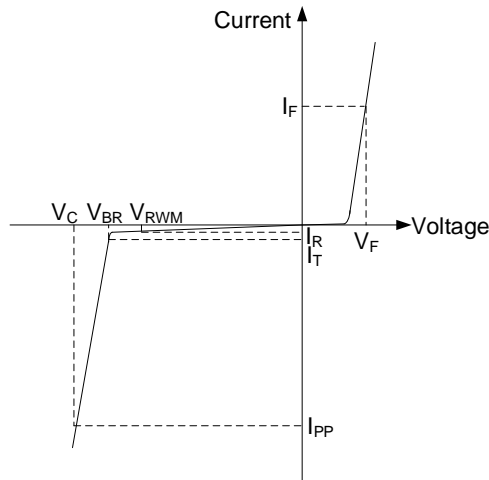
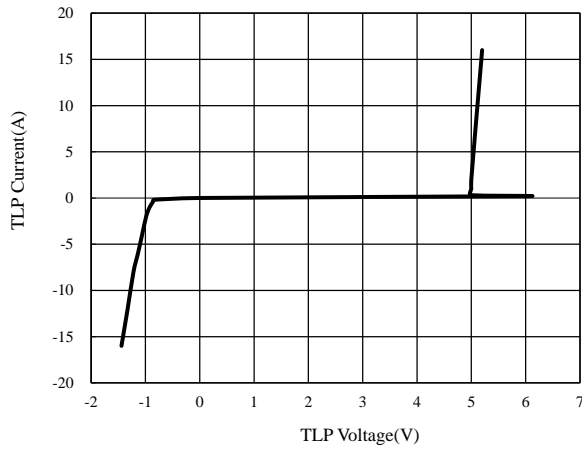


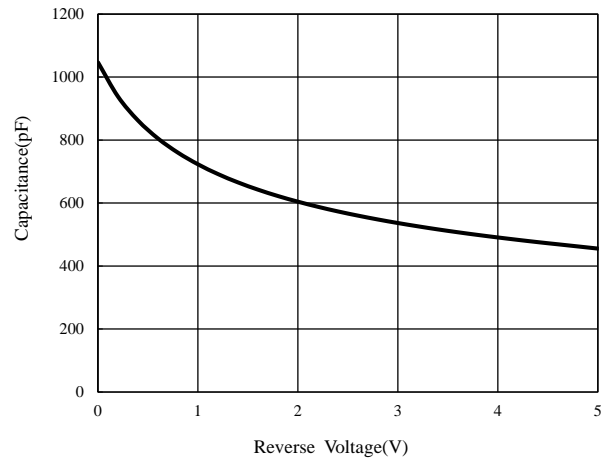
Figure 1. Uni-Directional TVS

Typical Performance Characteristics, From IO to GND

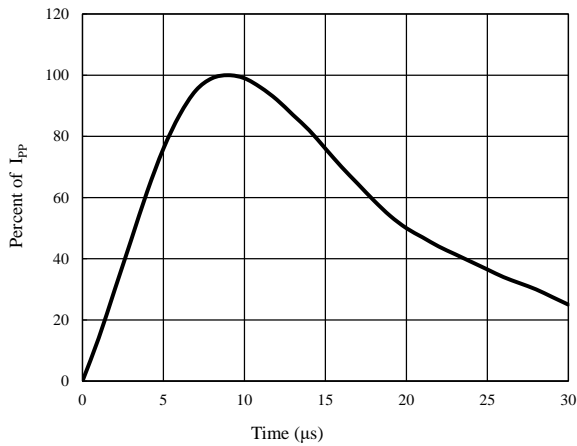
TLP Testing



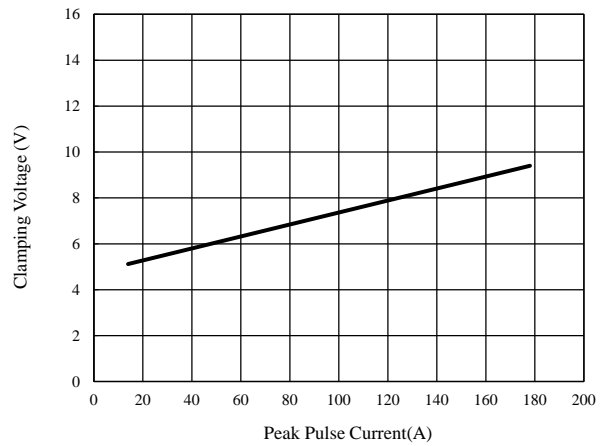
Capacitance vs. Voltage



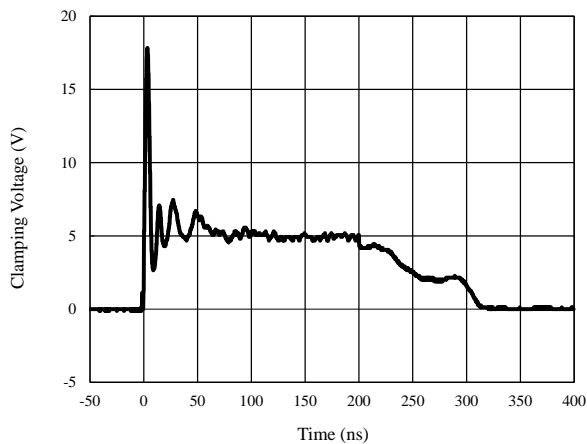
Pulse Waveform



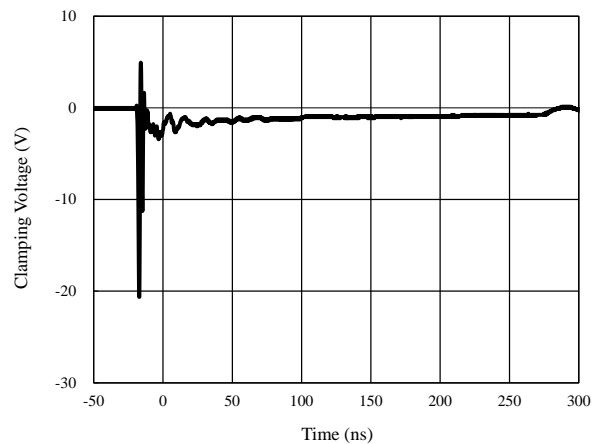
Clamping Voltage vs. Peak Pulse Current



ESD Clamping (+8kV Contact per IEC 61000-4-2)



ESD Clamping (-8kV Contact per IEC 61000-4-2)



Application Information

PCB Pin Connections

The SYS42V04SLD protects one uni-directional data or power line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The SYS42V04SLD pin connections are shown in Figure 2. The protected line connects to one of the pins, while the other is connected to GND, which should connect to a ground plane on the board. All path lengths connected to the pins of the SYS42V04SLD should be as short as possible to minimize parasitic inductance.

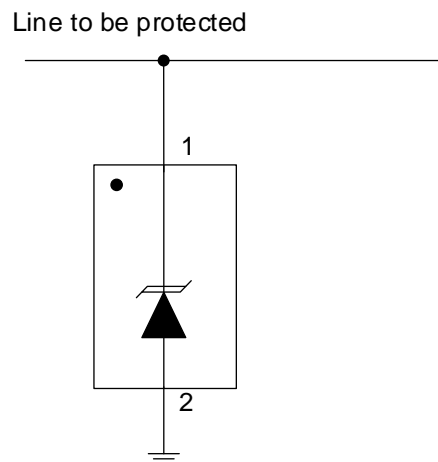


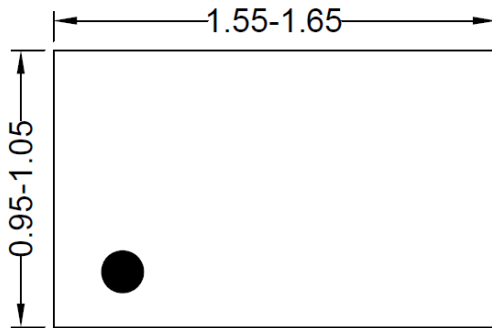
Figure 2. ESD/Surge Protection Circuit

PCB Layout Guidelines

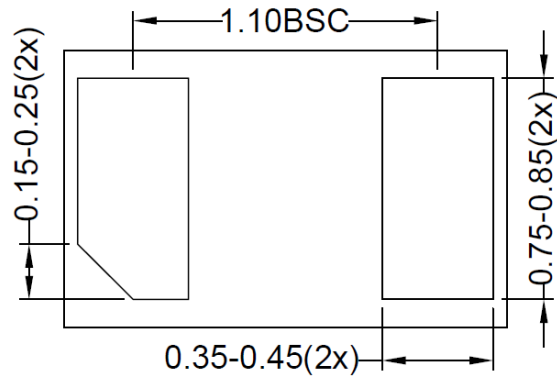
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place the SYS42V04SLD as close to the connector or terminal ports as possible.
- Use a large via to connect the SYS42V04SLD pin to the ground.
- Avoid running signals near board edges.
- The SYS42V04SLD should be placed near the protected line.
- The distance between the SYS42V04SLD ground pin and the GND reference path should be as short as possible.

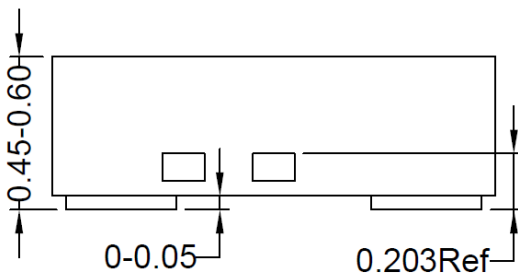
DFN1.6x1.0-2 Package Outline



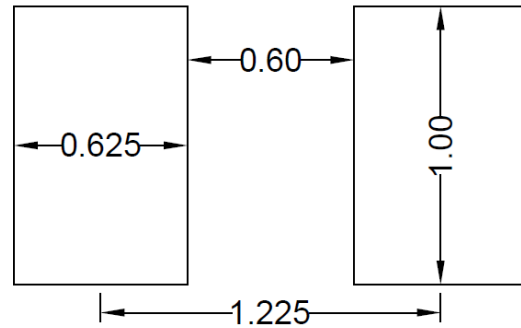
Top View



Bottom View



Front View

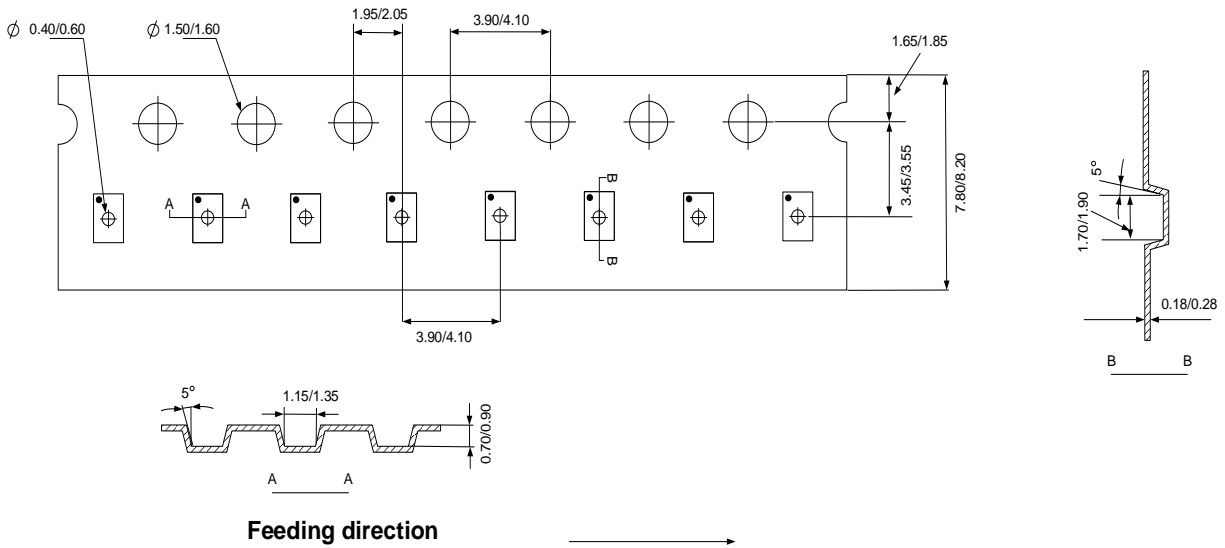


**Recommended PCB Layout
(Reference only)**

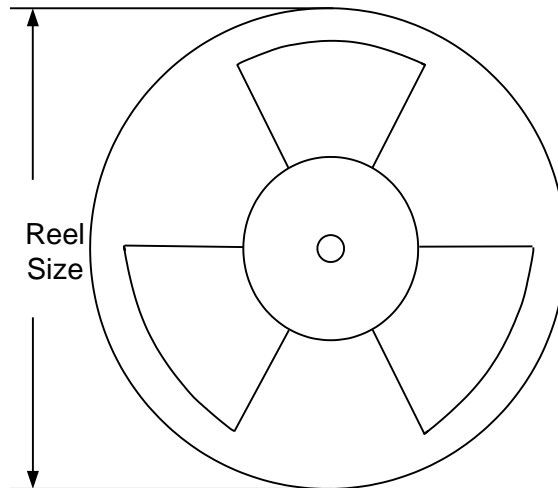
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.6x1.0-2	8	4	7"	3000



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Dec. 23, 2024	Initial Release	



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