SA52270L

40V 12A H-bridge Automotive Motor Driver

General Description

The SA52270L is a 12A H-bridge motor driver designed for automotive applications. The highly integrated H-bridge driver block comprises two MOSFET half-bridges with internal logic control, gate drivers, and full protection features.

The device includes multiple protection features including short-circuit protection, overvoltage clamp and thermal shutdown are provided for reliable system operation.

The device is available in a compact SOP16 package.

Features

- Operating Voltage Range: 4V to 28V
- Output Current: 12A
- Undervoltage Lockout
- Overvoltage Clamp
- Thermal Shutdown
- Cross-Conduction Protection
- Current Limit
- Protection Against Loss of Ground and Loss of VCC
- Output Short Circuit Protection
- Low Power Standby Mode
- PWM Operating Mode
- Current Sense Output
- Diagnostic Function
- SOP16 Package
- AECQ100 Qualified

Applications

- Automotive Motor Drivers
- DC Brushed Motor Drivers

Typical Application

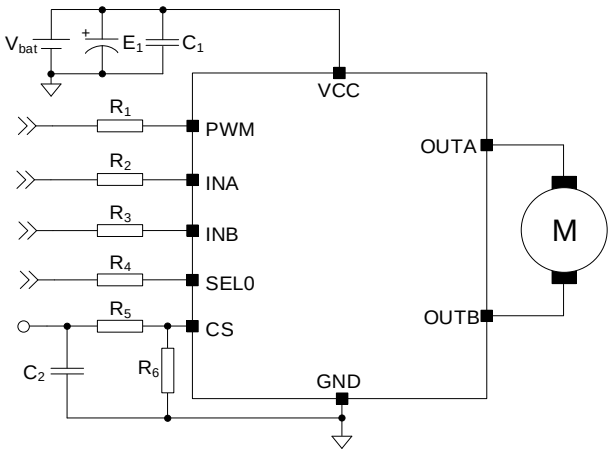


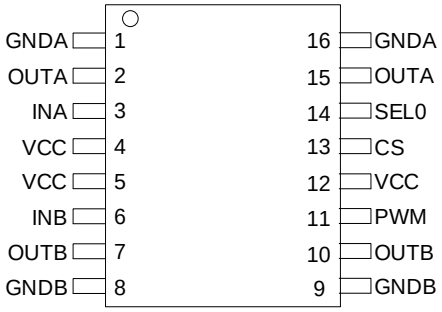
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SA52270LFFP	SOP16 RoHS Compliant and Halogen Free	***KFHxyz***

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin No.	Pin Name	Pin Description
1,16	GNDA	Return path of half-bridge A.
2,15	OUTA	Source of high-side switch A / drain of low-side switch A.
3	INA	OUTA control input.
4,5,12	VCC	Power supply voltage.
6	INB	OUTB control input.
7,10	OUTB	Source of high-side switch B / drain of low-side switch B.
8,9	GNDB	Return path of half-bridge B.
11	PWM	PWM control of the low-side power MOSFET.
13	CS	Analog sense output and fault diagnostic output.
14	SEL0	Combined with INA, INB configures the CS information to the output.

Block Diagram

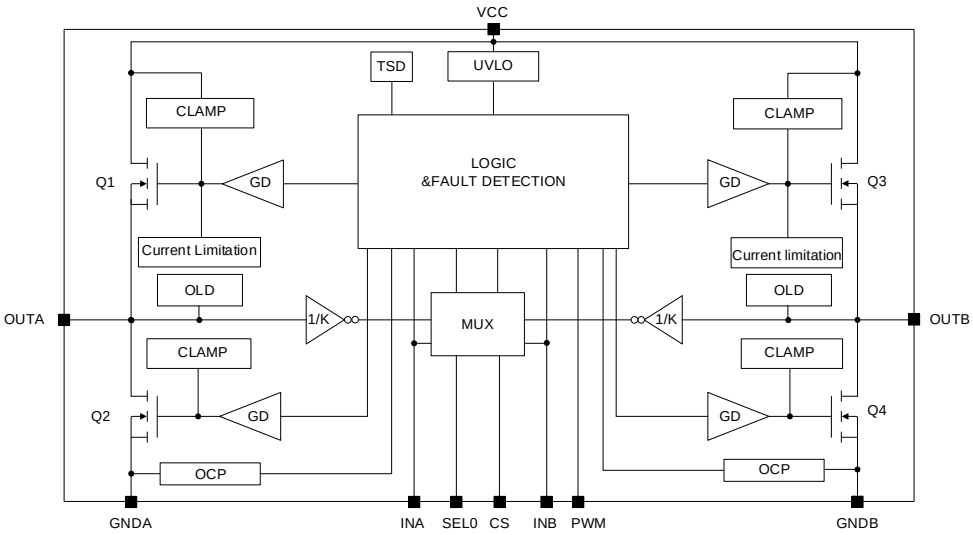


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

All voltages are referenced to GND unless otherwise noted.

Parameter		Min.	Max.	Unit
VCC		-0.3	38	V
OUTA, OUTB		-0.3	38	V
$I_{reverse}$			12	A
I_{CS}		-20	10	mA
$I_{INX,PWM,SEL0}$		-1	10	mA
Junction Temperature (T_J)		-40	150	°C
Storage Temperature		-55	150	°C
Electrostatic Discharge	HBM (Human Body Model) INX, PWM, SEL0, CS	2		kV
	HBM (Human Body Model) VCC, OUTA, OUT	4		
	CDM (Charge Device Model)	1		

Thermal Information (Note 2)

Parameter	Value	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	55	°C/W
θ_{JC} Junction-to-case Thermal Resistance	17	

Recommended Operating Conditions

All voltages are referenced to GND unless otherwise noted.

Parameter(Note 3)	Min.	Max.	Unit
VCC	4	28	V
OUTA, OUTB	-0.1	28	V
INA, INB, SEL0, PWM	-0.1	5	V
Junction Temperature (T_J)	-40	150	°C

Electrical Characteristics

(-40°C ≤T_A ≤ 125°C, VCC=7V to 28V, unless otherwise specified) (Note 3)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply Current	Quiescent VCC Supply Current	I_{QVCC}	INA=INB=0, SEL0=PWM=0, T_A=25°C, VCC=13V			1	μA
			INA=INB=0, SEL0=PWM=0, T_A=85°C, VCC=13V(Note 4)			1	μA
			INA=INB=0, SEL0=PWM=0, T_A=125°C, VCC=13V			8	μA
	Operation VCC Supply Current	I_{OPVCC}	INA or INB=5V, PWM=0V or 5V, SEL0=x		3.5	6	mA
	Off State VCC Supply Current	I_{OFFVCC}	INA=INB=0, SEL0=5V, PWM=0		2	4	mA
Power MOSFETs	High Side Power MOSFETs Turn-on Resistance	R_{ONHS}	I_{OUT}=3.5A, T_A=25°C		40		mΩ
			I_{OUT}=3.5A			85	mΩ
	Low Side Power MOSFETs Turn-on Resistance	R_{ONLS}	I_{OUT}=-3.5A, T_A=25°C		20		mΩ
			I_{OUT}=-3.5A			60	mΩ
	Off-state Output Current of One Leg	I_{LKOFF}	INA=INB=0V, PWM=0V, VCC=13V, T_A=25°C	-0.2		1	μA
			INA=INB=0V, PWM=0V, VCC=13V, T_A=125°C	-0.2		3.5	μA
	Free-wheeling Diode Forward Voltage	V_f	I_{OUT}=-3.5A, T_A=125℃		0.7	0.9	V
Input Signal (INA, INB, SEL0, PWM)	Logic “1” Input Voltage	V_{IH}		2.1			V
	Logic “0” Input Voltage	V_{IL}				0.9	V
	Input Voltage Hysteresis	V_{IHYS}		0.2			V
	High Level Logic Bias Current	I_{INH}	V_{IN}=2.1V			10	μA
	Low Level Logic Bias Current	I_{INL}	V_{IN}=0.9V	1			μA
	Input Clamp Voltage	V_{ICL}	I_{IN}=1mA	6.1		8.3	V
			I_{IN}=-1mA		-0.7		V
Thermal Shutdown	High Side Thermal Shutdown Threshold	T_{SD_HS}		150	170	190	°C
	High Side Thermal Shutdown Hysteresis	T_{SDHYS_HS}			7		°C
	High Side Thermal Shutdown Reset Threshold	T_{SD_HSRST}		135			°C
	Low Side Thermal Shutdown Threshold	T_{SD_LS}		150	170	190	°C
Under Voltage Lock Out	VCC under Voltage Rising Threshold	VCC_{UVON}			4	5	V
	VCC under Voltage Hysteresis	VCC_{UVHYS}			0.5		V
Open Load Detection	Off-state Open Load Detection Threshold	V_{OL}	INA=INB=0V, PWM=0V, SEL0=5V for OUTA; SEL0=0 and within t_{DSTB} for OUTB	2	3	4	V
	Off-state Output Sink Current	$I_{L\ (off2)}$	INA=INB=0V, V_{OUT}=V_{OL}, PWM=0V, SEL0=5V for OUTA; SEL0=0V for OUTB	-135		-15	μA
Current Protection	High Side Current Limitation	I_{LIM_HS}		12	22	30	A
	Low Side Shutdown Current	I_{SD_LS}		14	22	30	A
	Time to Shutdown for the Low Side	t_{SD_LS}	INA=5V, INB=0V, PWM=5V		5		μs
Voltage Clamp	High Side Clamp Voltage (VCC to OUTA =0 or OUTB=0)	V_{CLPHS}	I_{OUT}=100mA, t_{clamp}=1ms	38	46		V
	Low Side Clamp Voltage (OUTA =VCC or OUTB=VCC to GND)	V_{CLPLS}	I_{OUT}=100mA, t_{clamp}=1ms	38	46		V
	Total Clamp Voltage (VCC to GND)	V_{CLP}	I_{OUT}=100mA, t_{clamp}=1ms	38	46	52	V
Current Sense	Multi-sense Clamp Voltage	V_{CS_CL}	VCC=18V, I_{SENSE}=-5mA		15.3		V
			VCC=18V, I_{SENSE}= 5mA	-17.3		-13.3	V
	I_{OUT}/I_{SENSE}	K_0	I_{OUT}=0.1A, V_{SENSE}=0.5V	420			
	I_{OUT}/I_{SENSE}	K_1	I_{OUT}=0.2A, V_{SENSE}=0.5V	710	1190	1670	
	I_{OUT}/I_{SENSE}	K_2	I_{OUT}=3.5A, V_{SENSE}=4V	980	1120	1247	
	I_{OUT}/I_{SENSE}	K_3	I_{OUT}=5.5A, V_{SENSE}=4V (Note 4)	990	1120	1235	
	Analog Sense Current Drift	DK_0/K_0	I_{OUT}=0.1A, V_{SENSE}=0.5V (Note 4)	-25		25	%
	Analog Sense Current Drift	DK_1/K_1	I_{OUT}=0.2A, V_{SENSE}=0.5V (Note 4)	-21		21	%
	Analog Sense Current Drift	DK_2/K_2	I_{OUT}=3.5A, V_{SENSE}=4V (Note 4)	-6		6	%
	Analog Sense Current Drift	DK_3/K_3	I_{OUT}=5.5A, V_{SENSE}=4V (Note 4)	-6		6	%
	Max Analog Sense Output Voltage	V_{SENSE}	VCC=7V, SEL0=5V, INA=5V, PWM=0V, I_{OUT}=2A, R_{SENSE}=10kΩ, T_A=125°C	5			V
	Current Sense Saturation Current	I_{SENSE_SAT}	VCC=13V, INA=5V, INB=0V, V_{SENSE} =4V, SEL0=5V, T_A=125°C	5.8			mA

	Output Saturation Current	I_{OUT_SAT}	VCC=13V, INA=5V, INB=0V, V_{SENSE} =4V, SEL0=5V, T_A=125°C (Note 4)	7			A
	VCC Output Voltage for CS Shutdown	V_{OUT_SD}	INA=5V, INB=0V, SEL0=5V, R_{SENSE}=2.7kΩ, I_{OUT}=3.5A (Note 4)		3		V
	CS Leakage Current	I_{SENSE_LK}	I_{OUTA}=0A, V_{SENSE}=0V, INx=0V, SEL0=0 (Standby)	-0.2		0.5	μA
			I_{OUTA}=0A, V_{SENSE}=0V, INx=0V, SEL0=5V (No Standby)	-0.2		0.5	μA
			I_{OUTA}=0A, INx=5V, PWM=5V	-0.2		15	μA
	CS Output Voltage in Fault Condition	V_{SENSEH}	VCC=13V, R_{SENSE}=1kΩ, For example: OUTA in open load, INA=0V, I_{OUTA}=0A, OUTA=4V, SEL0=5V	5		7	V
	CS Output Current in Fault Condition	I_{SENSEH}	VCC=13V, V_{SENSE}=V_{SENSEH}	7	20	30	mA

Timing

(-40°C ≤T_A ≤ 125°C, VCC=13V, R_{LOAD}=3.7Ω, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM Frequency	f				20	kHz
HS Turn-on Delay Time	$t_{d(on)\_HS}$	Input rise time <1μs, INx to OUTx rise edge 90%		25		μs
HS Turn-off Delay Time	$t_{d(off)\_HS}$	Input rise time <1μs, INx to OUTx fall edge 10%		15		μs
HS Rise Time	t_{r_HS}	OUTx edge 10%-80%		10		μs
HS Fall Time	t_{f_HS}	OUTx edge 90%-20%		0.6		μs
LS Turn-on Delay Time	$t_{d(on)\_LS}$	Input rise time <1μs, INx to OUTx fall edge 90%		0.4		μs
LS Turn-off Delay Time	$t_{d(off)\_LS}$	Input rise time <1μs, INx to OUTx rise edge 10%		2		μs
LS Rise Time	t_{r_LS}	OUTx edge 10%-80%		0.7	1.5	μs
LS Fall Time	t_{f_LS}	OUTx edge 90%-20%		0.2	0.6	μs
Low-side Turn-on Delay Time	t_{cross}	Input rise time <1μs	40	140	350	μs
Off-state Diagnostic Delay Time from Falling Edge of INPUT	t_{DIADLF}	INA=5V to 0V; INB=0; SEL0=5V; PWM=0V; I_{OUT}=0A; OUTA=4V	40	140	350	μs
Off-state Diagnostic Delay Time from Rising Edge of V_{OUT}	t_{DIADLR}	INA=INB=0V; PWM=0V; OUTx=0V to 4V; SEL0=5V for OUTA; SEL0=0V and within t_{DSTB} for OUTB		5	30	μs
Input Reset Time for High Side Fault Unlatch	$t_{LT\_RS\_HS}$	V_{INx}=5V to 0V; HSx faulting	3	10	20	μs
Input Reset Time for Low Side Fault Unlatch	$t_{LT\_RS\_LS}$	V_{INx}=0V to 5V; LSx faulting	3	10	20	μs
Standby Mode Blanking Time	t_{DSTB}	VCC=13V, INA=INB=PWM=0V, SEL0 from 5V to 0V	0.2	1	1.8	ms

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy evaluation board.

Note 3: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 4: Guaranteed by design or statistical correlation and not production tested.

Switching Timing

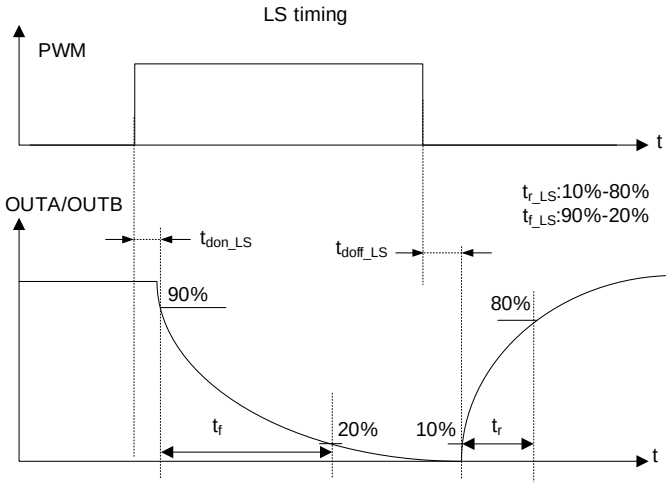


Figure 3. Definition of the LS Switching Timing (INA=INB=0)

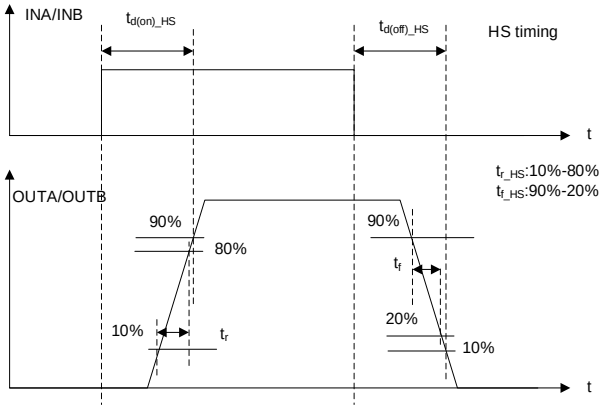


Figure 4. Definition of the HS Switching Timing

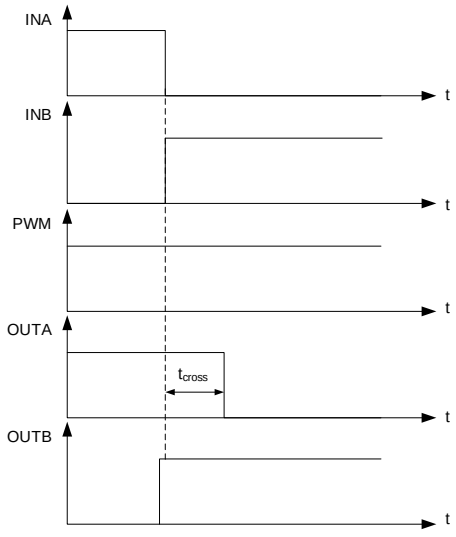


Figure 5. t_{cross} (Cross-conduction Definition)

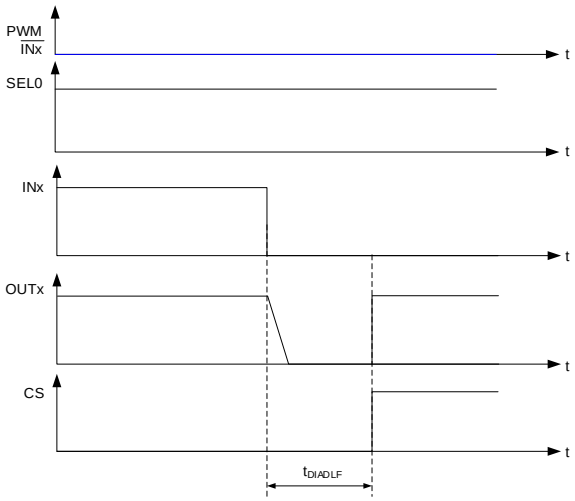


Figure 6. t_{DIADLF} (Off-state Diagnostic Delay Time from Falling Edge of INPUT)

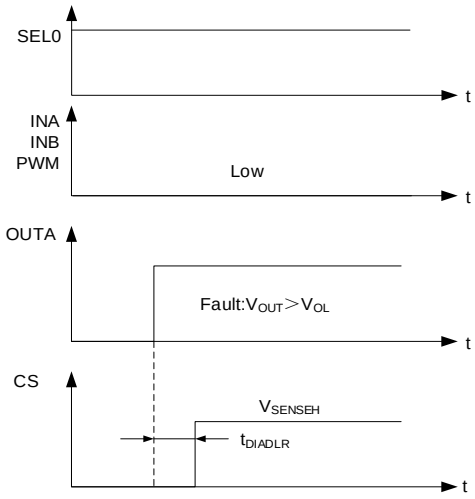


Figure 7. t_{DIADLR} (Off-state Diagnostic Delay Time from Rising Edge of OUTA/B)

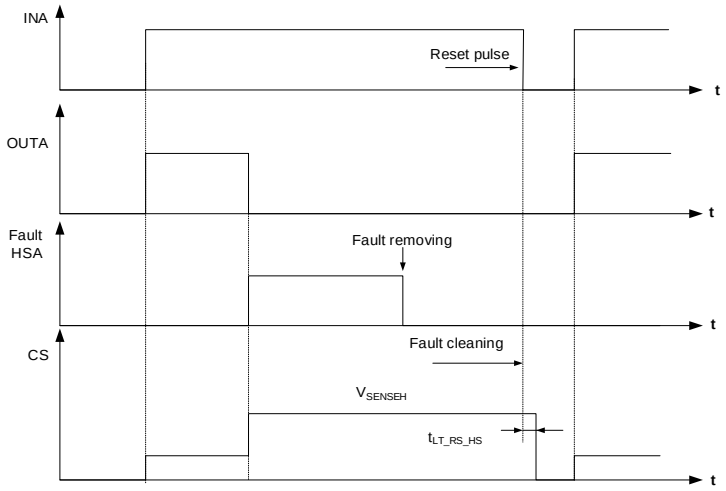


Figure 8. $t_{LT\_RS\_HS}$ (Input Reset Time for High Side Fault Unlatched)

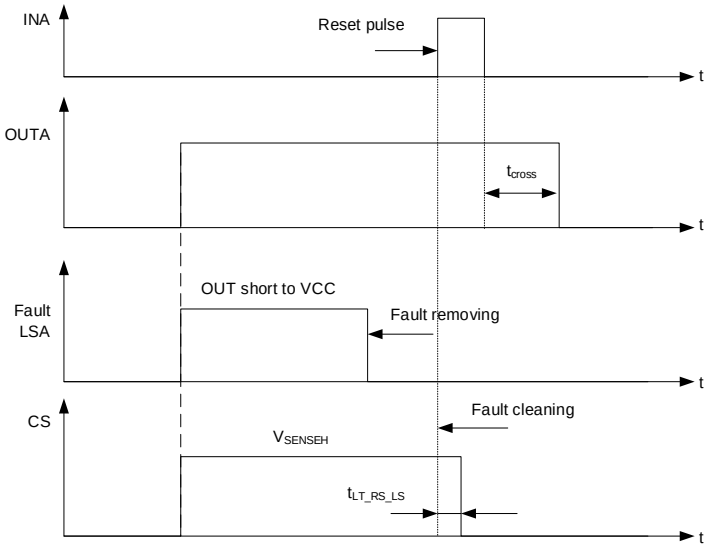
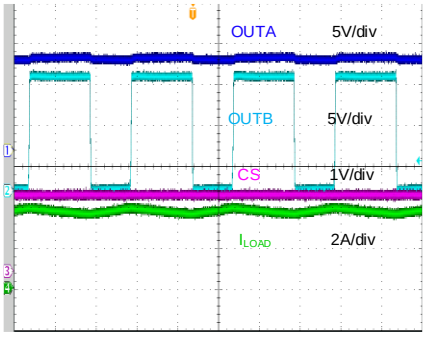


Figure 9. $t_{LT\_RS\_LS}$ (Input Reset Time for Low Side Fault Unlatched)

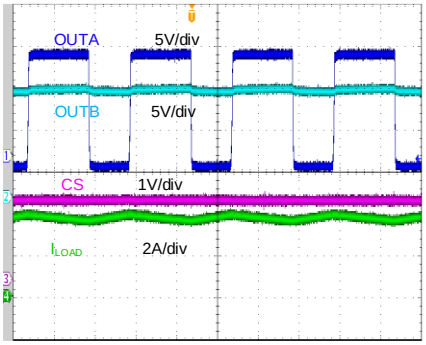
Typical Performance Characteristics

Forward OUTA→OUTB
(VCC=13V I_{LOAD}=4A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



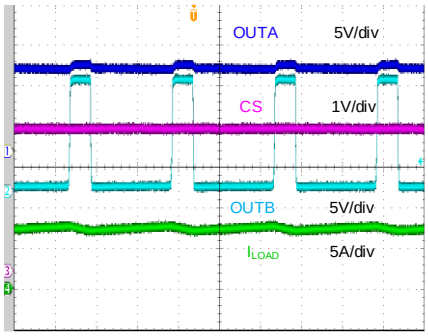
Time (20μs/div)

Reverse OUTB→OUTA
(VCC=13V I_{LOAD}=4A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



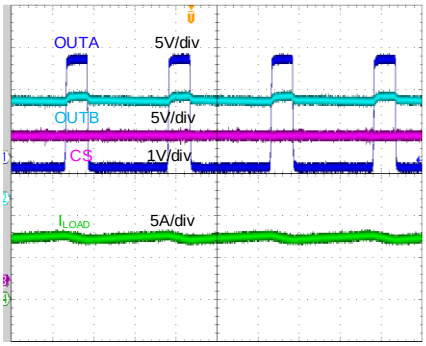
Time (20μs/div)

Forward OUTA→OUTB
(VCC=13V I_{LOAD}=8A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



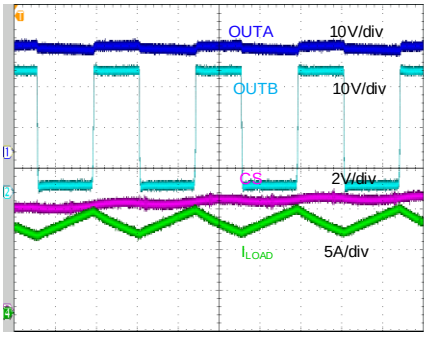
Time (20μs/div)

Reverse OUTB→OUTA
(VCC=13V I_{LOAD}=8A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



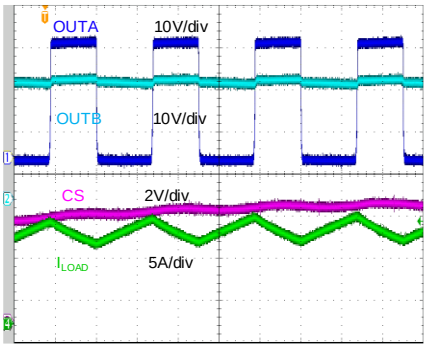
Time (20μs/div)

Forward OUTA→OUTB
(VCC=28V I_{LOAD}=12A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



Time (20μs/div)

Reverse OUTB→OUTA
(VCC=28V I_{LOAD}=12A
CH1:OUTA CH2:OUTB CH3:CS CH4:I_{LOAD})



Time (20μs/div)

Functional Description

Logic Truth Table

The output state is dependent on the INA, INB, SEL0, and PWM states.

Table 1. Truth Table in Normal Operating Conditions

INA	INB	SEL0	PWM	CS	HSA	LSA	HSB	LSB
1	1	1	x	Current Monitoring HSA	ON	OFF	ON	OFF
		0		Current Monitoring HSB				
1	0	1	1	Current Monitoring HSA	ON	OFF	OFF	ON
			0		ON	OFF	OFF	OFF
1	0	0	1	Hi-Z	ON	OFF	OFF	ON
			0		ON	OFF	OFF	OFF
0	1	1	1	Hi-Z	OFF	ON	ON	OFF
			0		OFF	OFF	ON	OFF
0	1	0	1	Current Monitoring HSB	OFF	ON	ON	OFF
			0		OFF	OFF	ON	OFF
0	0	1	1	Hi-Z	OFF	ON	OFF	ON
		0						
0	0	1	0	Refer to table 3	OFF	OFF	OFF	OFF
		0			OFF	OFF	OFF	OFF

Table 2. OUTA Fault Conditions Truth Table

Digital Input Pins				CS	Comment
INA	INB	PWM	SEL0		
0	0	1	0	V_{SENSEH}	LSB protection triggered; LSB latched off
0	0	1	1	V_{SENSEH}	LSA protection triggered; LSA latched off
0	1	x	0	V_{SENSEH}	HSB protection triggered; HSB latched off
0	1	1	1	V_{SENSEH}	LSA protection triggered; LSA latched off
1	0	1	0	V_{SENSEH}	LSB protection triggered; LSB latched off
1	0	x	1	V_{SENSEH}	HSA protection triggered; HSA latched off
1	1	x	1	Hi-Z	HSB protection triggered; HSB latched off
1	1	x	0	Hi-Z	HSA protection triggered; HSA latched off

Table 3. Truth Table in Off-State

INA	INB	SEL0	PWM	OUTA	OUTB	CS
0	0	1	0	$V_{OUTA}>V_{OL}$	x	V_{SENSEH}
				$V_{OUTA}<V_{OL}$	x	Hi-Z
		0		x	$V_{OUTB}>V_{OL}$	V_{SENSEH}
				x	$V_{OUTB}<V_{OL}$	Hi-Z

Typical Application Waveforms

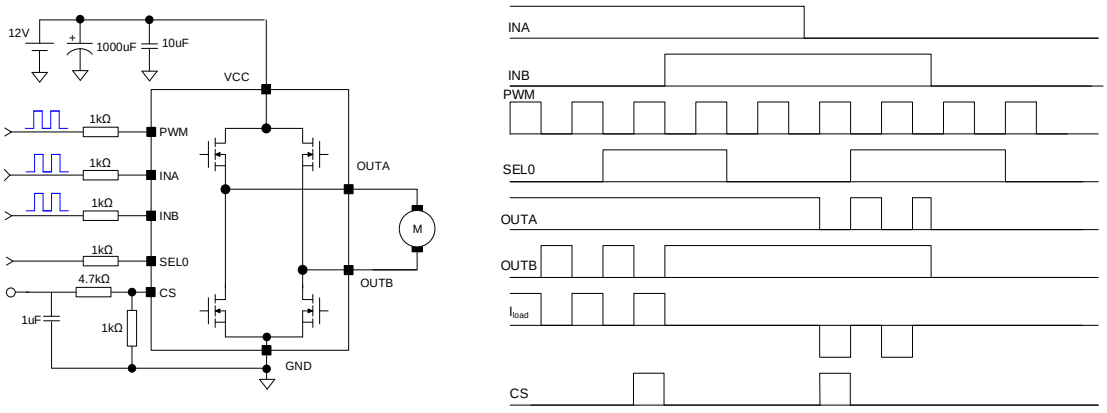
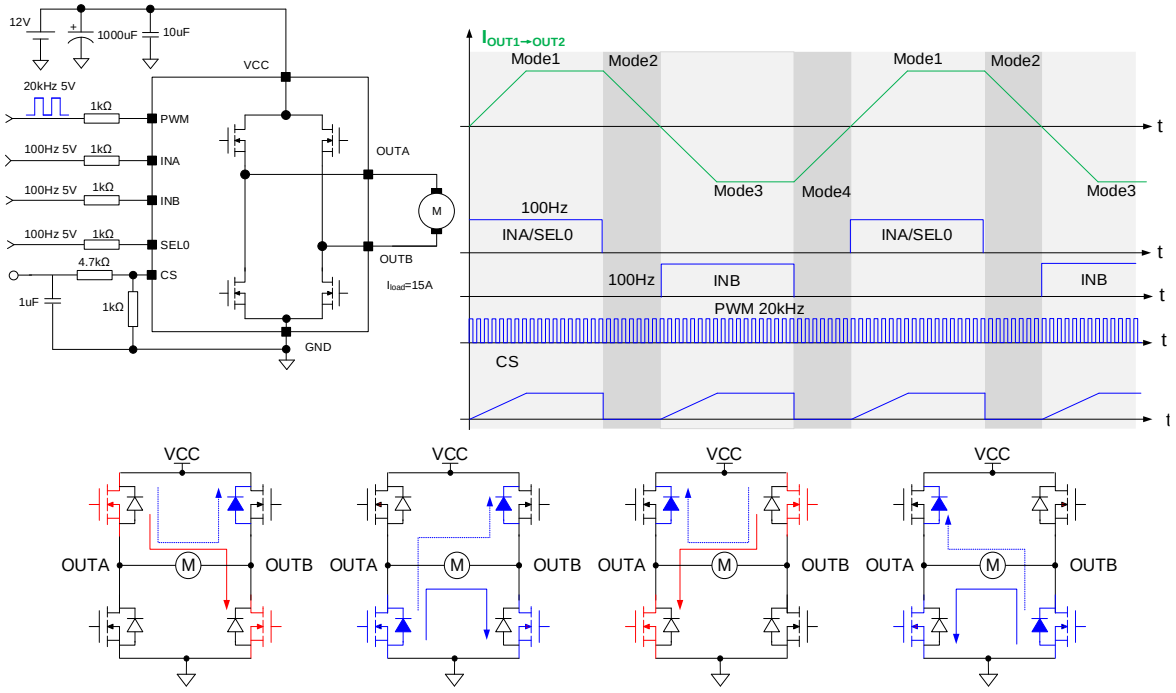


Figure 10. Typical Waveform



(a) Mode1 *(b) Mode2* *(c) Mode3* *(d) Mode4*

Figure 11. Typical Application: Waveforms in Normal Operation

Table 4. Normal Operation Truth Table

Mode	INA	INB	PWM	SEL0	CS	Function
1	High	Low	20kHz	High	Current Monitoring HSA	Forward
2	Low	Low		Low	Hi-Z	Coast
3	Low	High		Low	Current Monitoring HSB	Reverse
4	Low	Low		Low	Hi-Z	Coast

Power on

When VCC is powered on with a fast slope rate (less than 10V/μs) and exceeds the UVLO threshold (VCC_{UVON}), OUTA and OUTB are pulled up to VCC (activating HSx) after a delay of approximately 25μs. Conversely, if VCC powers on with a slow

slope rate (1V/ms) and surpasses the UVLO threshold (VCC_{UVON}), OUTA and OUTB are pulled up to VCC (activating HSx) with a shorter delay of about 1μs.

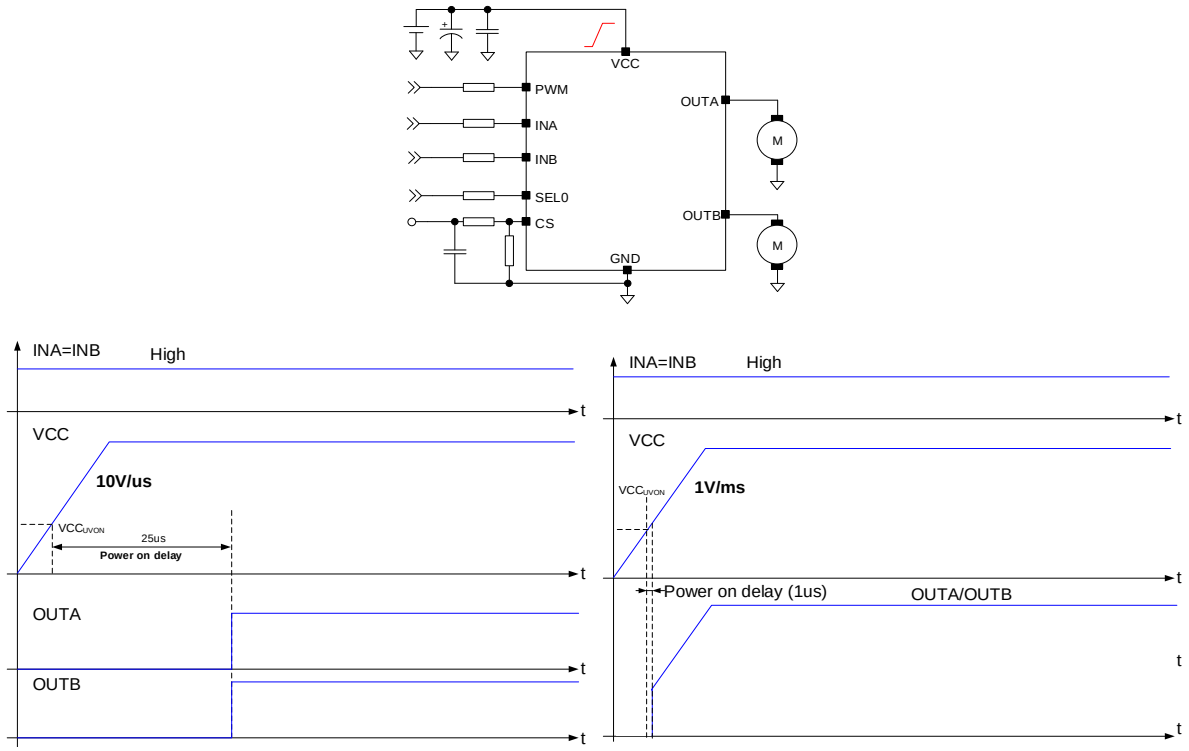


Figure 12. Power On Waveforms with Different Slope Rates

Standby Mode

To initiate standby mode, all logic pins (INA, INB, SEL0, PWM) must be set to low for a minimum duration of t_{DSTB}, starting when the last input pin is switched to low. In this mode, the device achieves low power dissipation (less than 8μA). Exiting standby mode requires setting any one of the logic pins (INA, INB, SEL0, PWM) from low to high. Normal operation resumes after a brief delay.

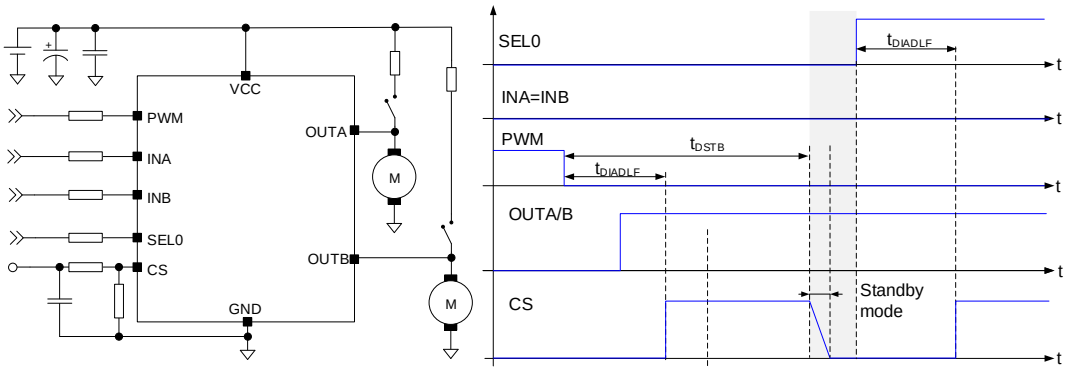


Figure 13. Standby Mode Waveform

Table 5. Truth Table in Standby Mode

INA	INB	PWM	SEL0	Enter Standby
H→L	L	L	L	t_{DSTB}
L	H→L	L	L	
L	L	H→L	L	
L	L	L	H→L	

CS Output

Current during Normal Operation

During normal operation, the current is proportional to the load current flowing through the activated high side, which is selected by SEL0. This relationship follows a known ratio, denoted as K, and is indicated on the CS pin. This current can be converted into a voltage with an external resistor. This conversion allows continuous load monitoring and abnormal condition detection.

Diagnostics Output during Fault Conditions

During fault conditions, the CS output can be used as the diagnostics output. In this state the pin is pulled up to V_{SENSEH} and can drive a maximum current I_{SENSEH} with a typical value of 20mA. This occurs in the following scenarios:

a. During a fault condition on the active high side (in the ON state) triggered by overtemperature protection. In this case the CS output, when selected by SEL0, reflects the high side fault state.

b. During a fault condition on the active low side (also in the ON state), initiated by overcurrent shutdown or overtemperature protection. In this case, the CS output selected by SEL0 corresponds to the same leg (of the high side) where the low side is in a fault state.

c. During Open Load (OL) detection in the OFF state (INA=INB=PWM=L), as selected by SEL0. Special attention must be paid to the H-bridge, particularly for OUTB (SEL0=L). Here, the fixed voltage is available only before the device enters standby mode after t_{DSTB}, as all control signals are set to low. In standby mode, CS will pull down within 47μs (CS fall edge time is 47μs).

Diagnostic Flag Under Normal Operation

The device delivers a fixed voltage (V_{SENSEH}) in the following configuration: when the full bridge is in the OFF state (with the load connected between OUTA and OUTB, and OUTA and OUTB, INA=INB=PWM=0). This is achieved by activating an external pull-up resistor on the leg opposite to the one monitored by the CS output. Specifically, the pull-up should be on OUTB when SEL0=1, and on OUTA when SEL0=0. Special attention is required when the external pull-up is applied on OUTA with SEL0=0, as the device will enter standby mode after the elapsed time of t_{DSTB}.

Normal Operation (SEL0=1/0, Corresponding to OUTA/OUTB)

The current provided by CS output can be estimated using the following equation:

$$I_{SENSE} = \frac{I_{OUT}}{K} \quad (1)$$

The voltage developed across a current sense resistor R_{SENSE}, connected to this pin becomes:

$$V_{SENSE} = R_{SENSE} I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K} \quad (2)$$

Where:

V_{SENSE} is the voltage measured on the R_{SENSE} resistor; I_{SENSE} is the current provided from the CS pin in the current output mode; I_{OUT} is the current flowing in the selected high side. K factor represents the ratio between the Power MOSFET and Sense FET and can be selected from the EC table based on the current range.

Current Sense in Overload Condition (Failure Flag Indication)

Faults resulting from overtemperature and open load in the OFF state are signaled by the CS pin being pulled up to V_{SENSEH}, which is sourced from the internal LDO.

The conditions that trigger the CS pin to switch to V_{SENSEH} include:

- **Overtemperature Protection:** When the current flows in the active high side, it triggers overtemperature protection if the junction temperature exceeds the specified limit.
- **Short-Circuit to Ground:** This occurs when the CS output, is selected to an OUT with the active high side selected by SEL0.
- **Active Low Side Output:** Overcurrent protection is triggered when the current in the active low side output exceeds the cut-off current protection threshold ($I_{OUT} > I_{SD\_LS}$) or the junction temperature surpasses the overtemperature shutdown threshold. For SEL0=H, the CS output represents an LSA fault; for SEL0=L, it represents an LSB fault.

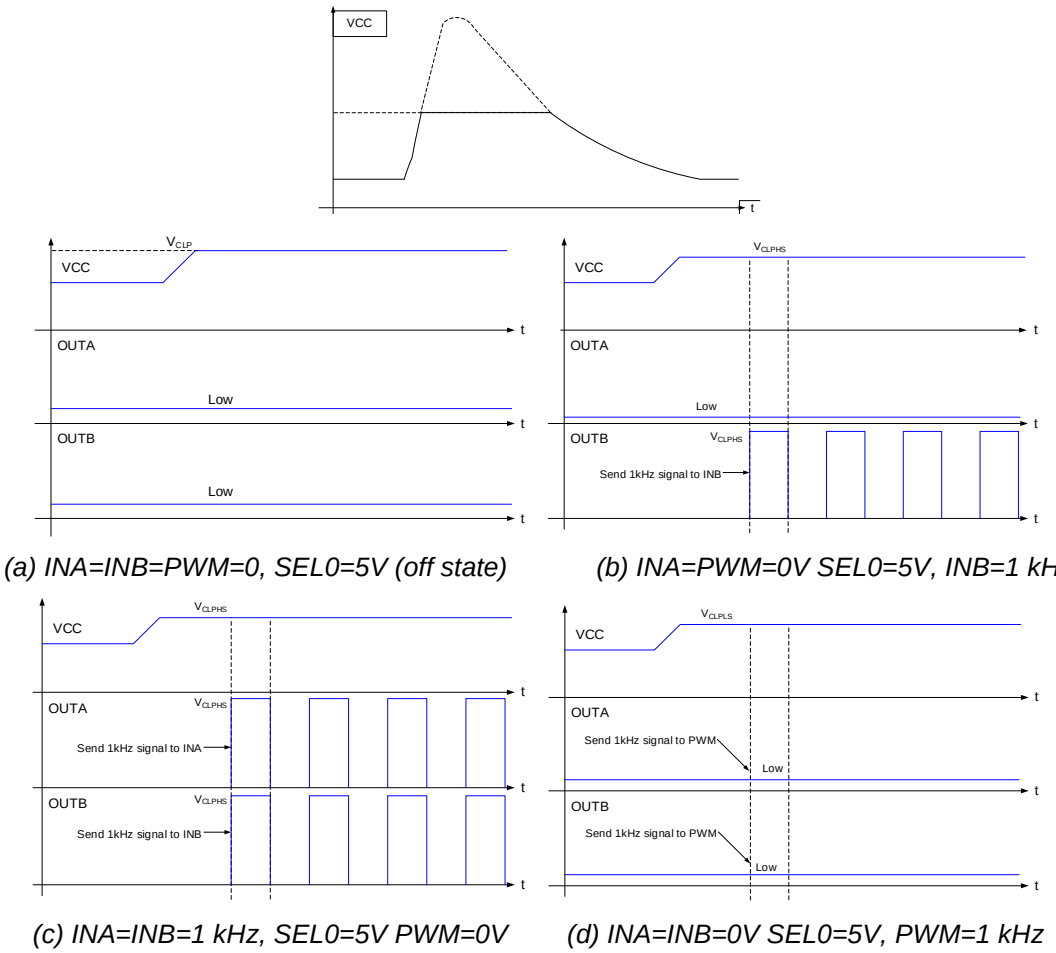
- **OFF State Voltage Conditions:** If the voltage on the OUT pin in the OFF state (INA=INB=PWM=L) exceeds the VOL threshold, such as in a short-circuit to VCC scenario, the CS output is enabled and selected by SEL0 corresponding to the output voltage. Special attention is needed for the H-bridge, particularly for OUTB (SEL0=L). In this case, the fixed voltage is only available until the device enters standby mode after t_{DSTB}, as all control signals are set to low. During these events, the CS output is controlled to drive a voltage level of V_{SENSEH} (as specified in the datasheet) across the external sense resistor.

Note: When HSx is operating in current limit mode, the drain-source voltage of HSx changes rapidly, and the voltage range exceeds the common input voltage range of the current sense operational amplifier, causing it to stop operating. In practical terms, when the output voltage drops to less than approximately 3V (as detailed under V_{OUT_SD} in the EC table, and guaranteed by design), the CS pin ceases to source current. Subsequently, the CS pin is pulled down by the CS pin pull-down resistor until the activation of the first thermal protection.

Protection Circuits

Overvoltage Clamp

When a voltage transient on VCC exceeds V_{CLP} (V_{CLPHS}/V_{CLPLS}), the Low-Side (LS) MOSFET is forced to operate in the linear region, while the High-Side (HS) is compelled to operate in the saturation region. As a result, the HS component experiences the highest level of power dissipation. In the case of negative transients across the device supply pin terminals, most of the current flows through the Power MOSFET body diodes. This current is not limited by anything except the intrinsic resistance of the pulse generator. External circuitry is typically used to protect the device against such events.



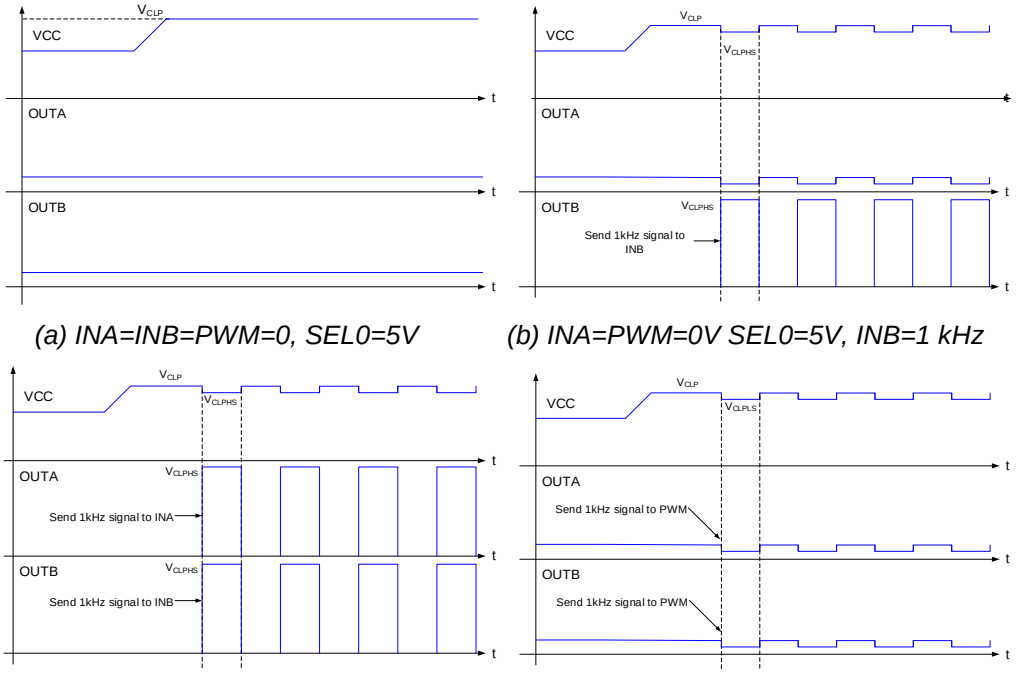
(a) INA=INB=PWM=0, SEL0=5V (off state)

(b) INA=PWM=0V SEL0=5V, INB=1 kHz

(c) INA=INB=1 kHz, SEL0=5V PWM=0V

(d) INA=INB=0V SEL0=5V, PWM=1 kHz

Figure 14. Over Voltage Clamp Protection Ideal Waveform



(a) INA=INB=PWM=0, SEL0=5V

(b) INA=PWM=0V SEL0=5V, INB=1 kHz

(c) INA=INB=1 kHz, SEL0=5V PWM=0V

(d) INA=INB=0V SEL0=5V, PWM=1 kHz

Figure 15. Over Voltage Clamp Protection Practical Waveform

Undervoltage Protection

If the voltage on the VCC pin drops below the undervoltage lockout (UVLO) threshold voltage during the UVLO filter time t_{UVLO_filter} (approximately 5μs), all circuitry within the device is disabled, and the internal logic is reset. Normal operation will resume once the VCC voltage exceeds the UVLO threshold after a delay of approximately 1μs (t_{UVLO_delay}).

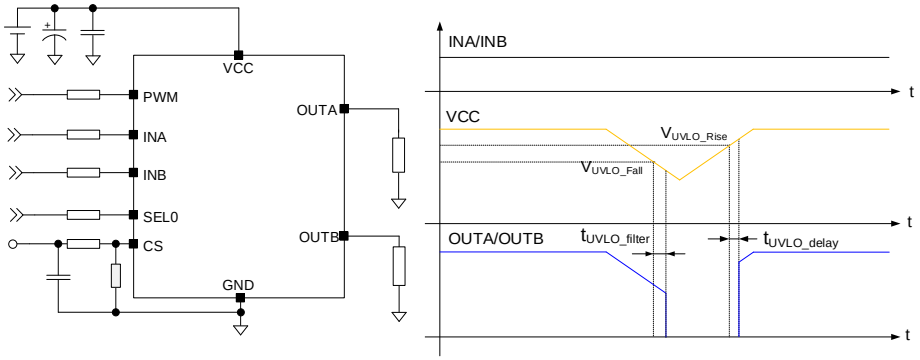


Figure 16. UVLO Protection

Loss of GND Connection

When GND disconnection protection is activated, the device ceases normal operation (such as motor rotation control) and ensures a safe operating state without motor activation. In the event of a GND connection loss, the I_{OPVCC} (as detailed in the datasheet) will flow through the ESD components of PWM, INA, INB, and SEL0. Subsequently, the device generates an I_{GND_loss} of approximately 10mA using an internal Power MOSFET. The device monitors the voltage across the logic pins (PWM, INA, INB, SEL0) relative to GND. The device enters standby mode if a fault is detected, and the internal Power MOSFET is switched off. The device resumes normal operation once GND is reconnected.

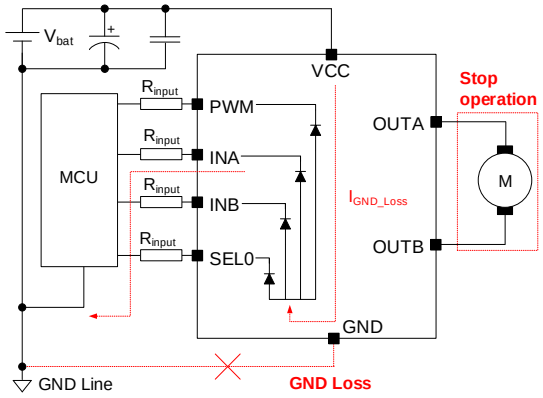


Figure 17. GND Loss Schematic

A series resistor with the value R_{input} is recommended on all the control inputs with a minimum value calculated using the following equations:

$$V_{MCU} - {}^{1}/_{3} \times I_{GND_{loss}} \times R_{input} - V_{ESD} \leq V_{IL} \quad (3)$$

$$R_{input} \geq (V_{MCU} - V_{IL} - V_{ESD}) \times {}^{3}/_{I_{GND\_loss}} \quad (4)$$

VCC Power Loss

When a VCC disconnection occurs, the voltage at the device's VCC begins to decline, as the energy stored in the bulk capacitor is consumed to power the motor. This process continues until the bulk capacitor is fully discharged, leading to a drop in the VCC voltage below the undervoltage lockout (UVLO) threshold.

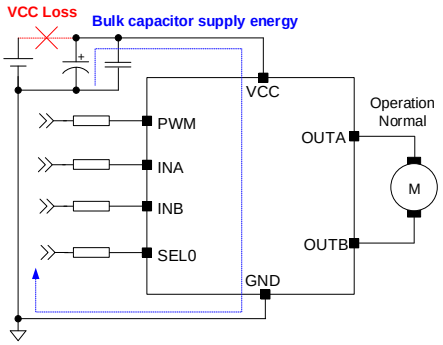


Figure 18. VCC Loss Schematic

Short-circuit Protection

Short to VCC Protection (LS)

The LS is equipped with dual protection mechanisms for OUTx shorts to VCC, which vary depending on whether the short-circuit is hard or resistive (refer to Figure 19)

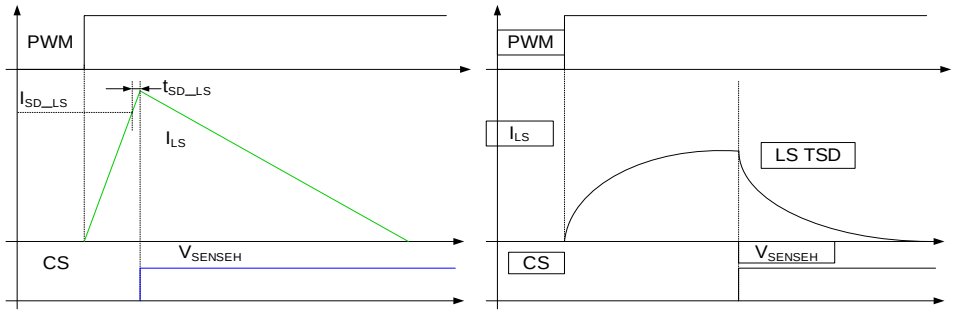
Hard Short-circuit

In the event of a hard short-circuit to VCC (characterized by low parasitic resistance), the device will turn off if the current through the LS as it goes above I_{SD_LS}. This shutdown occurs after a predefined filtering time (t_{SD_LS}) and results in a latched state (see Figure 19. (a)). Under this fault condition, the CS pin is pulled up to V_{SENSEH}. To reset the device after fault removal, a short high-level pulse must be sent to the INx corresponding to the faulty OUTx (refer to Figure 9).

Resistive Short-circuit

During a resistive short-circuit, the current through the LS does not reach I_{SD_LS}, but the temperature may rise to the LS thermal shutdown threshold (T_{SD_LS}). This leads to the device switching off and latching (see Figure 19. (b)). The CS pin

being pulled up to V_{SENSEH} indicating the fault condition. Once the fault is cleared, the device can be restarted by sending a short, high-level pulse to the Inx input where the fault occurred (refer to Figure 9).



(a) Hard Short-circuit *(b) Resistive Short-circuit*

Figure 19. Short to VCC Protection

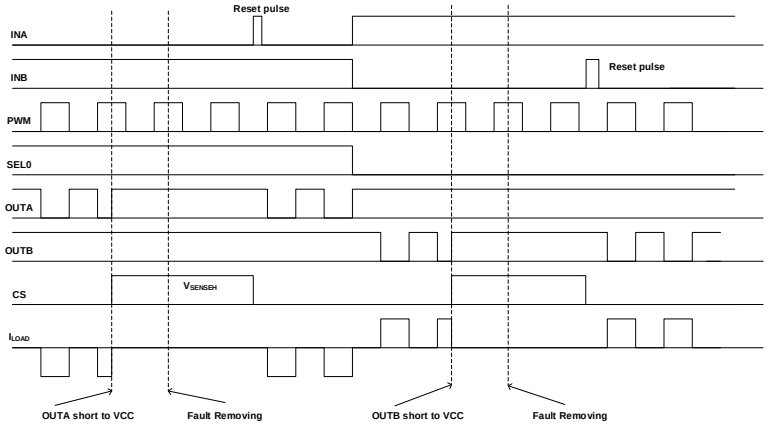


Figure 20. OUTx Short to VCC and Fault Clearing

Short to GND Protection

In the event of an output short to GND, the High-Side (HS) switch enters the saturation region once the current limit threshold (I_{LIM_HS}) is reached. This transition occurs after a specific filter time, denoted as $t_{LIM\_HS\_filter}$, which corresponds to the response time of the operational amplifier. Approximately 10μs after reaching this state, the HS driver is immediately disabled, and the CS pin is pulled up to V_{SENSEH}.

To reset the device following the removal of this fault, a short low-level pulse should be sent to the INx input corresponding to the faulty OUTx (as shown in Figure 8).

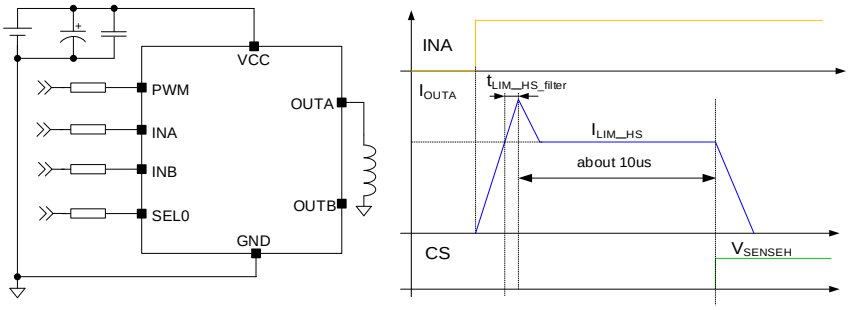


Figure 21. HSA Short Protection

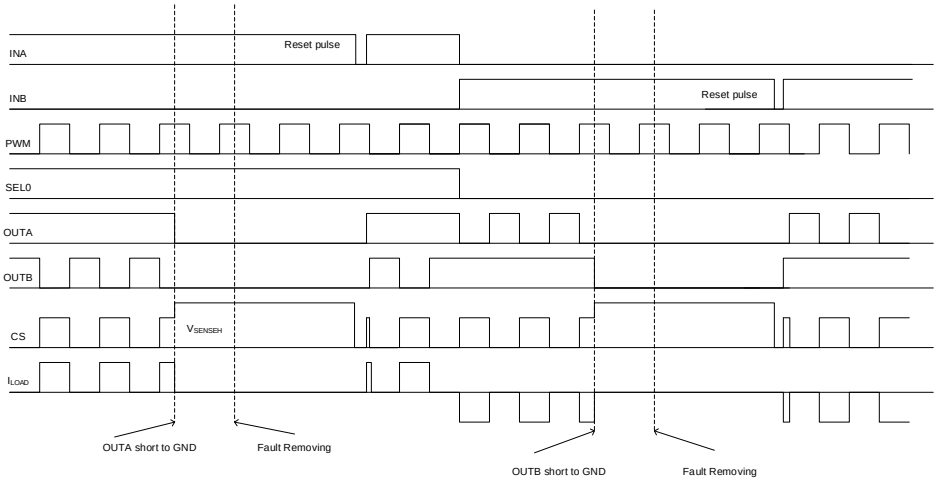


Figure 22. OUT Short to GND and Fault Clearing

Shoot-through Protection

The design prohibits the simultaneous activation of both Power MOSFETs in the same half-bridge, as this would result in a 'shoot-through' event. Considering that the turn-off process for the HS MOSFET is slower than the turn-on process for the LS MOSFET, a delay time (t_{cross}) is incorporated. This delay ensures that the LS MOSFET turns on only after the HS MOSFET has fully turned off. Consequently, the duration of t_{cross} is set to be longer than the HS turn-off time (as shown in Figure 23)

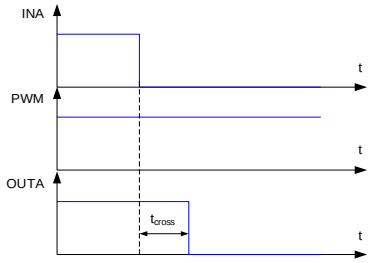
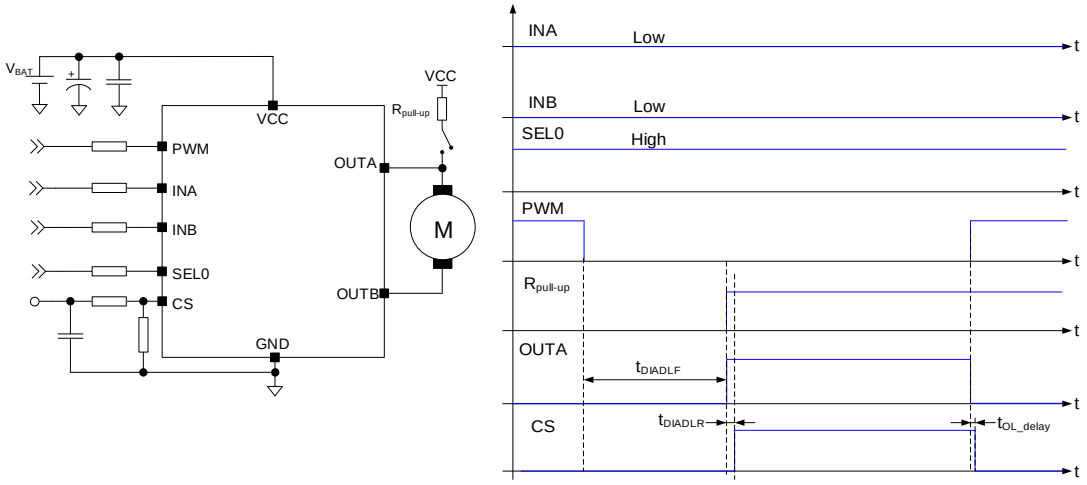


Figure 23. Anti-Shoot-through

Open Load Detection in Off-State (OL)

In off-state (INA=INB=PWM=Low, SEL0=H), open load detection of the device is active after t_{DIADLF} filtering time. When the OUTA voltage exceeds the open load detection threshold, CS is pulled up to V_{SENSEH} after a specific filtering time (t_{DIADLR}). SEL0 can be set low, and the open load detection on OUTB can also be performed (within t_{staby} for OUTB). OUTx needs a pull-up resistor $R_{pull-up}$ in normal applications (Figure 24). When the OUTx voltage falls below the threshold, or the device is out of the off-state, operation resumes after the t_{OL_delay} delay time (about 3μs).



(a) OL Configuration *(b) OL Waveform*

Figure 24. Open Load Detection Configuration

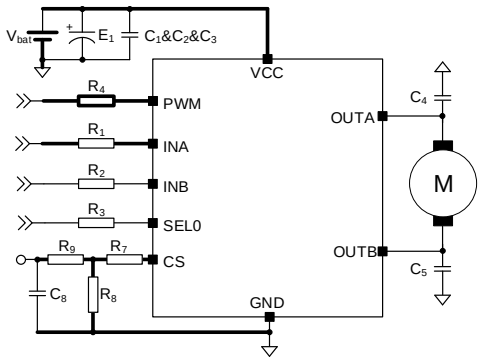
The optimal pull up resistor Rpull-up connected to Vbat supply can be estimated using the following equation.

$$R_{\text{pull-up}} \leq \frac{V_{BAT}-V_{OL\_MAX}}{-2*I_{L(off2)\_MIN}} \quad (5)$$

Thermal Shutdown Protection (TSD)

If the temperature of any Power MOSFET reaches approximately 170°C, its corresponding gate driver is disabled, and the CS pin is pulled up to V_{SENSEH}. This state is maintained until the temperature falls back to a safe level. Similarly, if the controller die temperature exceeds approximately 170°C, all Power MOSFET gate drivers are disabled. In this scenario, the CS pin is also pulled up to V_{SENSEH}, remaining in that state until the temperature decreases to a safe threshold. It's important to note that any occurrence of the device approaching thermal shutdown suggests potential issues, such as excessive power dissipation, inadequate heatsinking, or an overly high ambient temperature.

Application Example



Reference Designator	Description	Package Info	Note
C1 C2 C3	10μF/50V	1206	
C4 C5	100nF/50V	0603	
E1	100uF/E_{cap}/50V		
C8	1μF/16V	0805	
R1 R2 R3 R4	1kΩ/1%	0603	
R7 R8	270Ω/1%	1206	
R9	4.7kΩ/1%	1206	

PCB Guide

An optimal PCB floor plan is important to minimize current loop areas and arrange the power components so that the current flows smoothly, avoiding sharp corners and narrow paths. This layout recommendation helps reduce parasitic capacitance and inductance, therefore, eliminating ground bounce. All filtering capacitors (mainly C1&C2&C3 (VCC)) must be placed as close as possible to the device terminals to keep the parasitic inductance of the PCB traces as low as possible. To improve noise immunity, place the terminals of the filtering capacitors (VCC) on the same layer as the device. If GND and VCC areas are not on the same layer, use multiple vias for the connection. Place a capacitor between OUT and GND. A multilayer PCB is recommended for improved heat dissipation. For improved thermal and electrical conduction, a 2 ounce or higher copper thickness may be used instead of the standard 1 ounce.

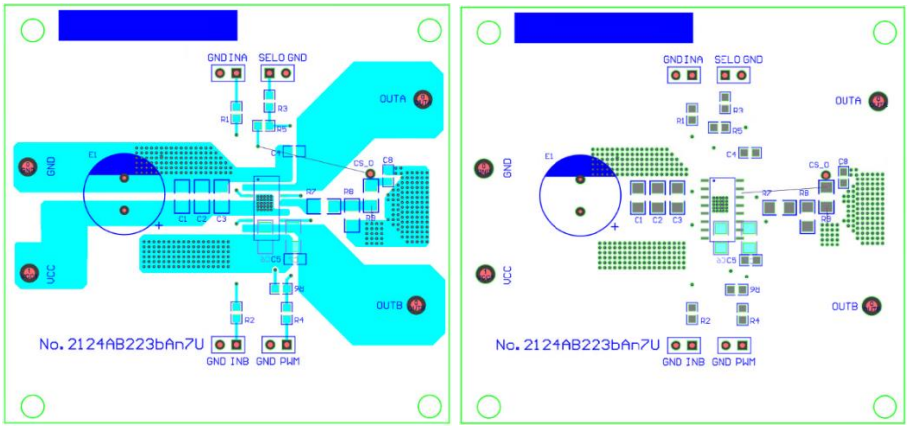
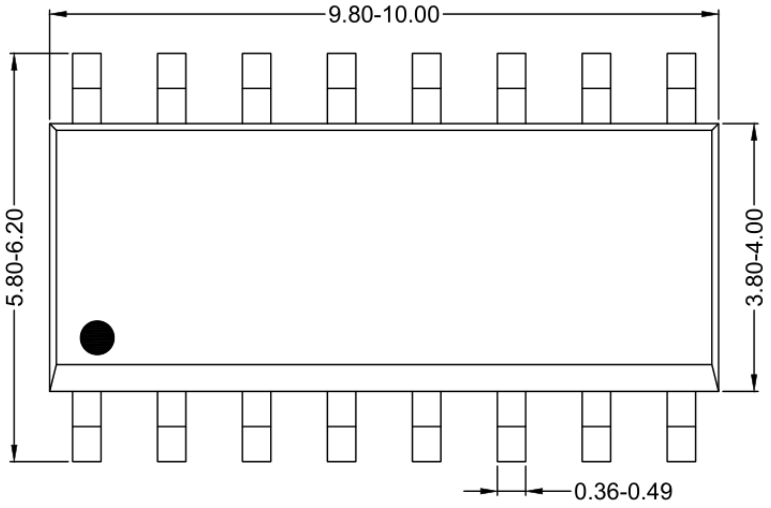
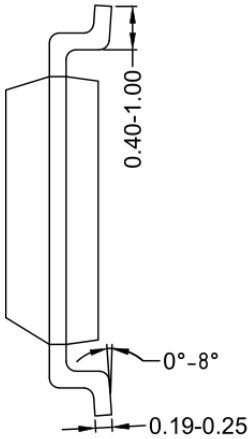


Figure 25. Top Layer *Top Silkscreen*

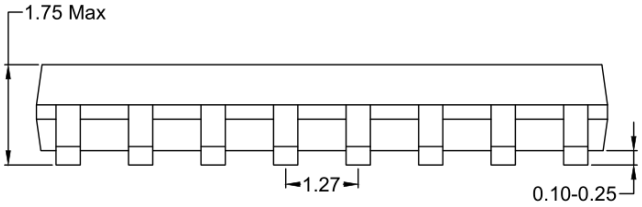
SOP16 Package Outline



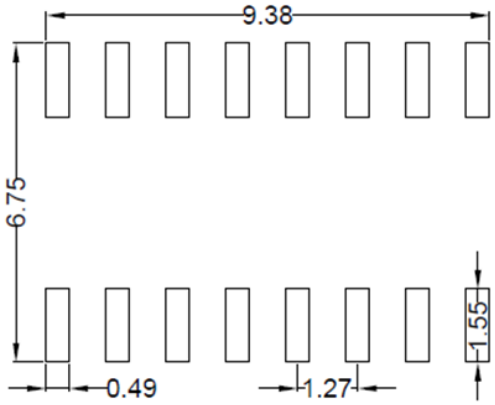
Top View



Side View



Front View

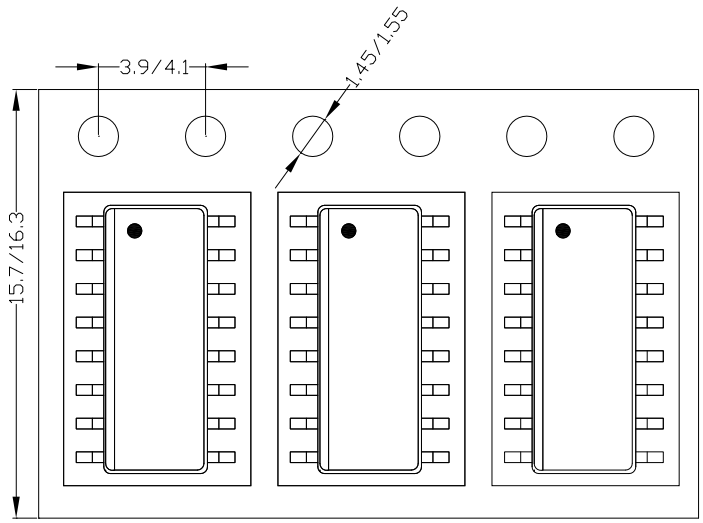


Recommended PCB Layout
(Reference only)

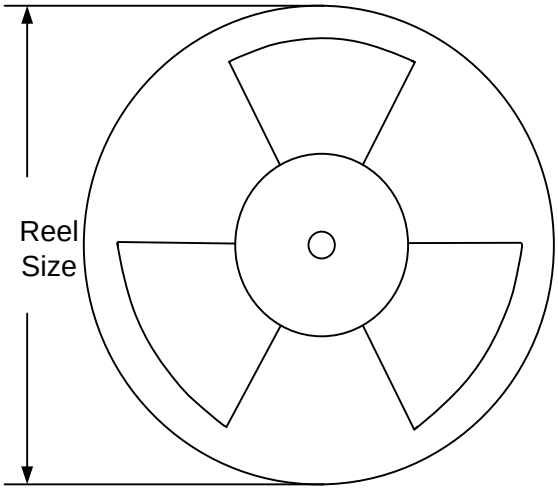
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel (pcs)
SOP16 & SOP16E	16	8	13"	400	400	2500

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Jan.03, 2025	Initial Release	

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