

General Description

The SA52128B is an eight half-bridge motor driver solution for automotive, industrial, and other mechatronic applications. The half-bridges are fully controllable, facilitating forward, reverse, coasting, and braking motor operations. All the functions are programmable via a serial peripheral interface (SPI).

The device includes protection features such as overcurrent protection, open load detection, undervoltage lockout, overvoltage lockout, and thermal shutdown for reliable operation. The open-drain nFAULT output pin can be used to notify the system in the event of a fault. The device is available in a TSSOP24E package with an exposed pad to enhance thermal dissipation.

Features

- 8 Half-Bridge Outputs
- Operating Voltage: 4.5V to 32V
- Compatible with a 5V/3.3V System
- Up to 1A Output Current for Each Output
- Low-Power Sleep Mode
- SPI Up to 5MHz
- Daisy Chain Functionality
- PWM Capable Output for Frequencies of 80Hz, 100Hz, 200Hz and 2kHz with an 8-Bit Duty Cycle Resolution
- Integrated Protection Features:
 - Overcurrent Protection
 - Short-Circuit Protection
 - Open Load Detection
 - Undervoltage Lockout
 - Overvoltage Protection
 - Thermal Shutdown
- nFAULT Pin Output
- TSSOP24E Package
- MSL Rating: MSL3
- AEC-Q100 Qualified

Applications

- Automotive
- HVAC
- DC Brushed Motor Drivers
- LEDs

Typical Application

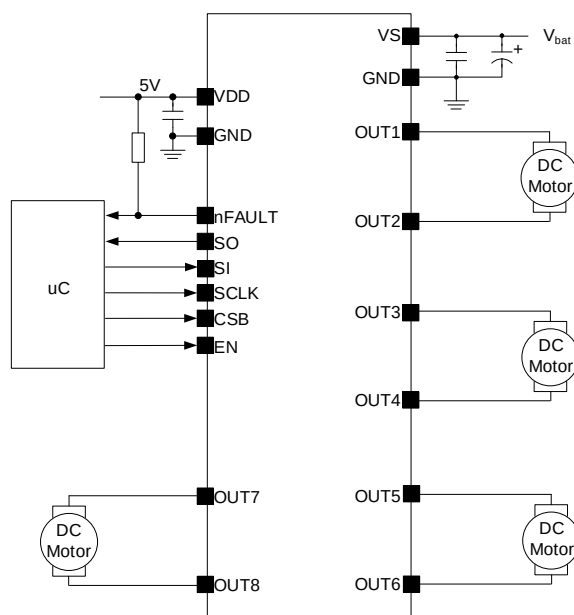


Figure 1. Typical Application Circuit

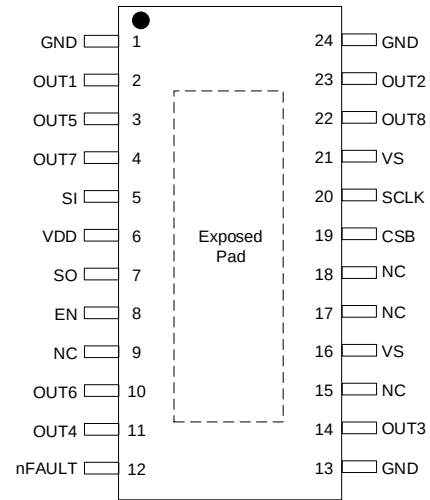
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA52128BHHP	TSSOP24E RoHS Compliant and Halogen Free	LKFxyz

Device code: LKF

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Name	Pin No.	Pin Description
GND	1,13,24	Ground.
OUT1	2	Half-bridge output 1
OUT5	3	Half-bridge output 5.
OUT7	4	Half-bridge output 7.
SI	5	16-bit SPI data input.
VDD	6	Power supply for internal logic. It is recommended to choose 1nF and 100nF low-ESR ceramic bypass capacitor to filter out high-frequency noise.
SO	7	16-bit SPI data output.
EN	8	Drive enable pin. Logic high enables the IC. Internal pull-down.
NC	9,15,17,18	Not connected.
OUT6	10	Half-bridge output 6.
OUT4	11	Half-bridge output 4.
nFAULT	12	Fault indicator output. Open-drain. This pin is pulled low during a fault condition and requires an external pull-up resistor for operation.
OUT3	14	Half-bridge output 3.
VS	16,21	Main power supply. It is recommended to use at least 10μF capacitance to maintain a stable motor supply voltage, and choose 1nF and 100nF low-ESR ceramic bypass capacitor to filter out high-frequency noise.
CSB	19	Chip select bar. Active low serial port operation. Internal pull-up.
SCLK	20	SPI clock input.
OUT8	22	Half-bridge output 8.
OUT2	23	Half-bridge output 2.
Exposed Pad	-	Exposed Pad. It is recommended to connect the pad to GND for heat dissipation.

Block Diagram

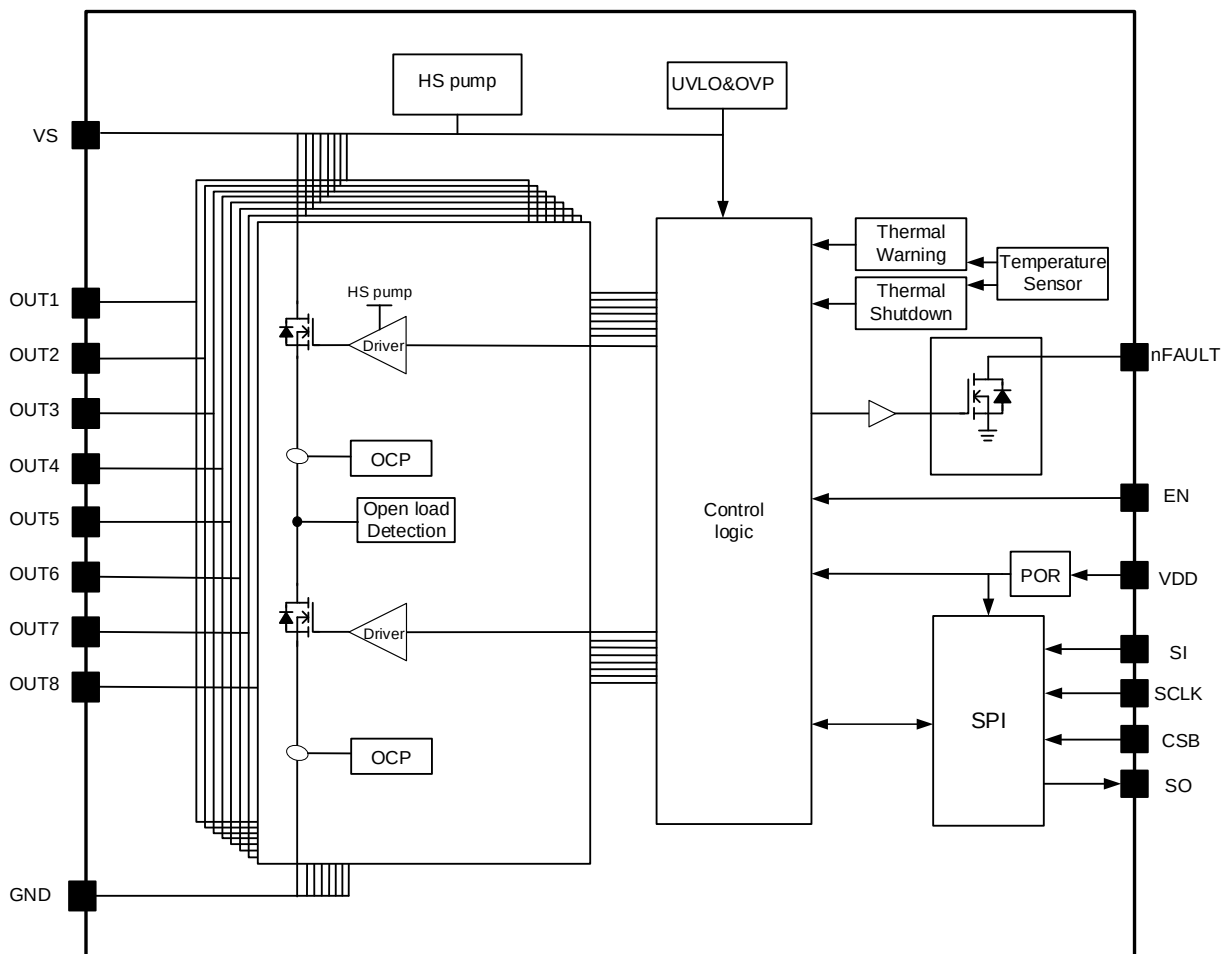


Figure 2. SA52128B Function Block Diagram

Absolute Maximum Ratings (Note 1)

Parameter		Min	Max	Unit
VS (DC)		-0.3	40	V
OUTx (DC)		-0.3	VS+0.7	V
Digital Pin (SI, SCLK, CSB, SO, EN, nFAULT)		-0.3	VDD+0.3	V
VDD		-0.3	5.75	V
Continuous Supply Current (VS pins) (Note 2)		0	6	A
Continuous Sink Current (GND pins) (Note 2)		0	6	A
Junction Temperature (T _J)		-40	150	°C
Storage Temperature		-65	150	°C
Electrostatic Discharge	HBM (Human Body Model) VS and OUTx pins	4k		V
	HBM (Human Body Model) all other pins	2k		
	CDM (Charge Device Model)	500		
	CDM (Charge Device Model) corner pins	750		

Thermal Information

Parameter(Note 3)	Typ.	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance (TSSOP24E)	34	°C/W
$\theta_{JC TOP}$ Junction-to-Case Thermal Resistance (TSSOP24E)	19	

Recommended Operating Conditions

Parameter(Note 4)	Min	Max	Unit
VS	4.5	32	V
VDD	3.15	5.5	V
Digital Pins	0	5.5	V
nFAULT Pullup Voltage	0	5.5	V
nFAULT Input Current	0	5	mA
Operating Temperature (T _A)	-40	125	°C
Junction Temperature (T _J)	-40	150	°C

Electrical Characteristics

(-40°C ≤ T_A ≤ 125°C, 4.5V ≤ V_S ≤ 32V, 3.15V ≤ V_{DD} ≤ 5.5V, EN=VDD, unless otherwise specified)(Note 2)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies	VS Sleep Mode Current	I _{VS_sleep}	VS =40V, EN=L, T _A =25°C		0	1	μA
			VS =40V, EN=L, T _A =125°C			2	μA
	VS Standby Mode Current	I _{VS_standby}	VS=13.5V, EN=H, Driver=OFF, T _A =25°C		0.8	1.6	mA
			VS=13.5V, EN=H, Driver=OFF, T _A =125°C			1.6	mA
	VS Operating Mode Current	I _{VS}	VS=13.5V, EN=H, All High-side MOSFETs=ON, T _A =25°C		3.3	5	mA
			VS=13.5V, EN=H, All High-side MOSFETs=ON, T _A =125°C			5	mA
	VS Undervoltage Lockout Voltage	V _{UVLO_FALL}	VS falling	3.7		4.3	V
		V _{UVLO_RISE}	VS rising	4		4.5	V
		V _{UVLO_HYS}			250		mV
	VS Undervoltage Lockout Deglitch Time	t _{UVLO}			10		μs
	VS Overvoltage Protection	V _{OVP}	VS rising, EXT_OVP=0b	21		25	V
			VS falling, EXT_OVP=0b	20		24	V
			VS rising, EXT_OVP=1b	32.7		35.5	V
			VS falling, EXT_OVP=1b	31.7		34.5	V
		V _{OVP_HYS}	Rising to falling hysteresis, EXT_OVP=0b		1		V
			Rising to falling hysteresis, EXT_OVP=1b		1		V
	VS Overvoltage Protection Deglitch Time	t _{OVP}			10		μs
	VDD Power On Reset Threshold	V _{POR_ON}	Supply rising	2.75		2.95	V
	VDD Power Off Reset Threshold	V _{POR_OFF}	Supply falling	2.6		2.8	V
	Logic Undervoltage Hysteresis	V _{POR_HYS}	Rising to falling hysteresis		150		mV
	VDD Operating Supply Current	I _{VDD}	VS =13.5V, VDD=3.3V, EN=H, All Low-side MOSFETs=ON, SPI=ON, T _A =25°C		2	5	mA
			VS =13.5V, VDD=3.3V, EN=H, All Low-side MOSFETs=ON, SPI=ON, T _A =125°C			5	mA
	VDD Standby Mode Current	I _{VDD_Standby}	VS=13.5V, VDD=3.3V, EN=H, SPI=OFF, T _A =25°C		1	2.5	mA
			VS=13.5V, VDD=3.3V, EN=H, SPI=OFF, T _A =125°C			2.5	mA
	VDD Sleep Mode Current	I _{VDD_SLEEP}	VS=13.5V, VDD=5V, EN=L, T _A =25°C		0	1.7	μA
			VS=13.5V, VDD=5V, EN=L, T _A =125°C			2	μA
Logic Level Input (EN, SI, SCLK, CSB)	Input Low Voltage	V _{IL}		0		0.3* VDD	V
	Input High Voltage	V _{IH}		0.7* VDD		VDD	V
	Input Logic Hysteresis	V _{HYS}		200			mV
	Input Low Current	I _{IL}	V _{IN} =0V, (SI, SCLK, EN)	-1		1	μA
			V _{IN} =0V, VDD=5V, (CSB)		45	65	μA
	Input High Current	I _{IH}	V _{IN} =5V, (SI, SCLK, EN)		45	65	μA
Open-Drain Output (nFAULT)	Input Capacitance	C _{CAPINX}	(Note 5)			15	pF
	Output Low Voltage	V _{OL}	I _{sink} =5mA	0		0.2	V
	Output High Current	I _{OH}	V _{OD} =5V	-1		1	μA
	Output Capacitance	C _{OD}	(Note 5)			15	pF
Push-Pull Output (SO)	Output Low Voltage	V _{OL}	I _{out} =-5mA	0		0.2	V
	Output High Voltage	V _{OH}	I _{out} =5mA	VDD -0.6		VDD	V
	Output Capacitance	C _{OD}	(Note 5)			30	pF
	Output Low Current	I _{OL}	V _{SO} =0V	-1		1	μA
	Output High Current	I _{OH}	V _{SO} =VDD	-1		1	μA

Power MOSFETs	High Side MOSFETs on Resistance	R _{DS(on)}	I _{OUT} =-500mA, VS=13.5V, T _A =25°C		0.75	1.1	Ω
			I _{OUT} =-500mA, VS=13.5V, T _A =125°C			1.5	
	Low Side MOSFETs on Resistance		I _{OUT} =500mA, VS=13.5V, T _A =25°C		0.75	1.1	Ω
			I _{OUT} =500mA, VS=13.5V, T _A =125°C			1.5	
	Output Rise and Fall Time (HS and LS)	SR _{rise and fall}	VS =13.5V, 10%-90%, R _{LOAD} =27Ω, HB _X _SR=0b		1		V/μs
			VS =13.5V, 10%-90%, R _{LOAD} =27Ω, HB _X _SR=1b		3.2		V/μs
	Output Dead Time (H to L / L to H)	t _{DEAD}	VS =13.5V, SR=0, HS/LS driver OFF to LS/HS driver ON	8	20	32	μs
			VS =13.5V, SR=1, HS/LS driver OFF to LS/HS driver ON	2	5	15	μs
	Propagation Delay (HS and LS ON/OFF)	t _{PD}	High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=0	5	12	25	μs
			High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=1	3	6	12	μs
	Source Leakage Current	I _{source_LC}	OUTx=0V, EN=H	-25	-10		μA
			OUTx=0V, EN=L	-2			μA
PWM Mode	PWM Switching Frequency	f _{PWM}	PWM_CHx_FREQ=00b	72	80	88	Hz
			PWM_CHx_FREQ=01b	90	100	110	Hz
			PWM_CHx_FREQ=10b	180	200	220	Hz
			PWM_CHx_FREQ=11b	1800	2000	2200	Hz
Protections	Thermal Warning Temperature	T _{WARN}		120	140	170	°C
	Thermal Warning Hysteresis	T _{WARN_HYS}			20		°C
	Thermal Shutdown Temperature	T _{SD}		150	165	200	°C
	Thermal Shutdown Hysteresis	T _{HYS}			20		°C
	Over Current Shutdown (Source)	I _{OCSO}	VDD=5V, VS=13.5V	-2.2	-1.5	-1.1	A
	Over Current Shutdown (Sink)	I _{OCSI}	VDD=5V, VS=13.5V	1.1	1.5	2.2	A
	Over Current Shutdown Delay Time	t _{OC}	OCP_DEG=000b	6	10	14	μs
			OCP_DEG=001b	2.6	5	7.9	μs
			OCP_DEG=010b	0.4	2.5	5.9	μs
			OCP_DEG=011b	0.1	1	3.4	μs
			OCP_DEG=110b	18.5	30	41.5	μs
			OCP_DEG=111b	8.4	20	31.6	μs
	Open Load Detection Current	I _{OLD}	High-side or Low-side	2	9	18	mA
	Open Load Detection Current in Low Current OLD Mode	I _{OLD_LOW}	Low-side	0.5	1.2	2	mA
	Open Load Detection Delay Time	t _{OL}	Active OLD (Continuous Mode)	2.2	3	3.8	ms
			Active OLD (PWM Mode)	150	200	300	μs

Serial Peripheral Interface

($-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $4.5\text{V} \leq V_S \leq 32\text{V}$, $3.15\text{V} \leq V_{DD} \leq 5.5\text{V}$, $\text{EN} = V_{DD}$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}				5	MHz
SCLK High Time	t_{CLKH}	(Note 5)	100			ns
SCLK Low Time	t_{CLKL}	(Note 5)	100			ns
SI Setup Time	$t_{\text{SU_SI}}$	(Note 5)	40			ns
SI Hold Time	$t_{\text{HD_SI}}$	(Note 5)	60			ns
SO Output Data Delay Time	$t_{\text{DLY_SO}}$	SCLK high to SO valid (Note 5)			60	ns
CSB Setup Time	$t_{\text{SU_CSB}}$	(Note 5)	100			ns
CSB Hold Time	$t_{\text{HD_CSB}}$	(Note 5)	100			ns
CSB Disable Delay Time	$t_{\text{DIS_CSB}}$	CSB high to SO High-Z (Note 5)		30		ns
CSB Minimum High Time before Active Low	$t_{\text{HI_CSB}}$	(Note 5)	600			ns
EN Low Valid Time	t_{ENL}	$V_{DD} = 5\text{V}$, EN going low 50% to OUTx turning off 50% (Note 5)			30	μs
EN High to SPI Valid	$t_{\text{ENH_SPIV}}$	(Note 5)			200	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J = 25^{\circ}\text{C}$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 3: θ_{JA} is measured with natural convection at $T_A = 25^{\circ}\text{C}$ on a four-layer Silergy evaluation board.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Guaranteed by design or statistical correlation and not production tested.

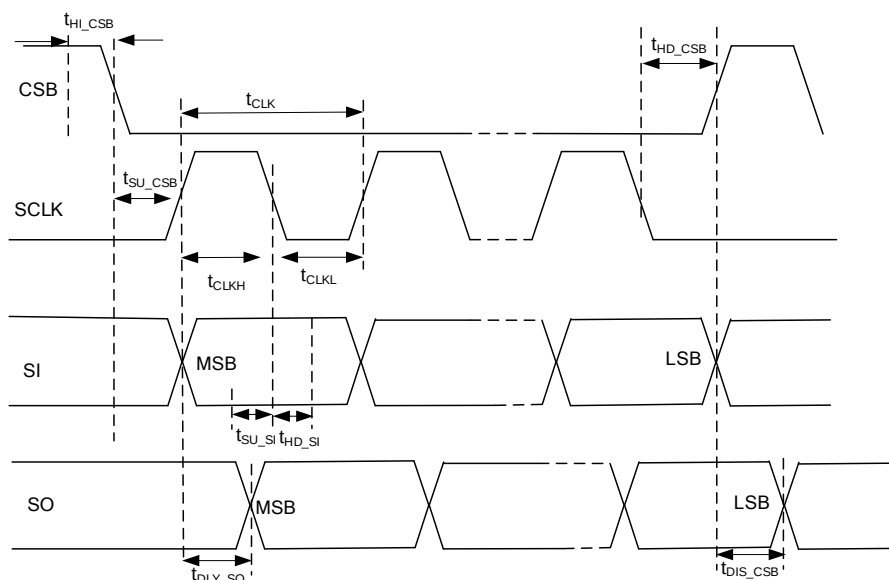
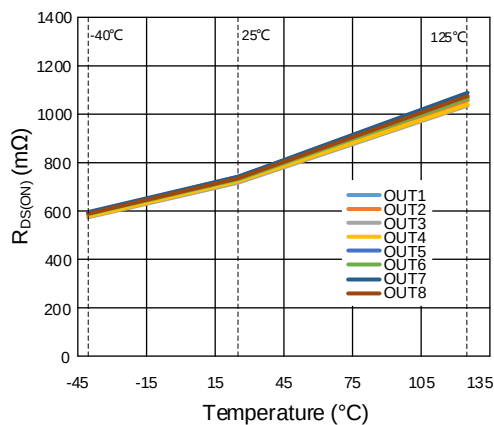


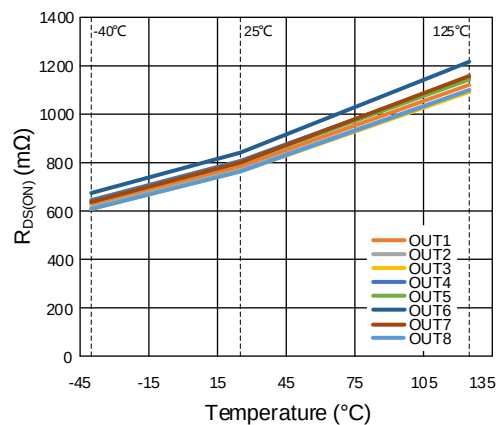
Figure 3. SPI Timing

Typical Performance Characteristics

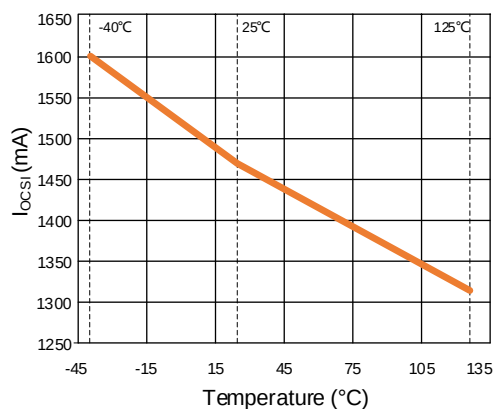
High Side MOSFETs on Resistance



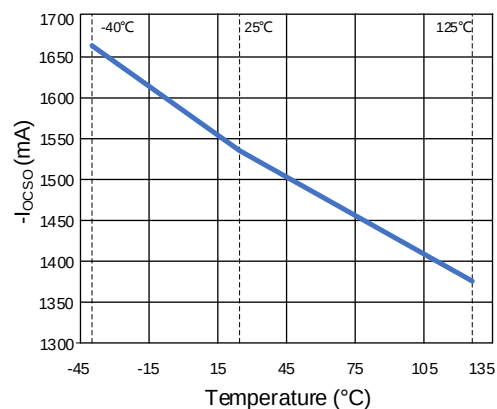
Low Side MOSFETs on Resistance



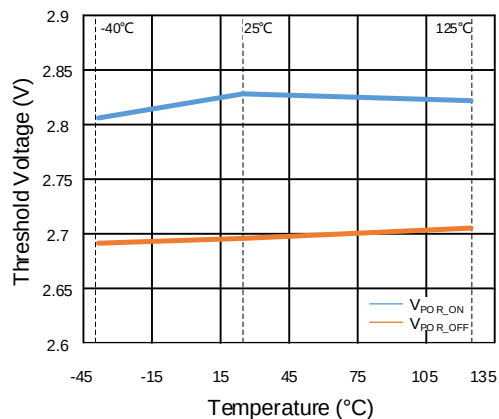
Low Side MOSFETs Over Current Limit
($V_S=13.5V$)



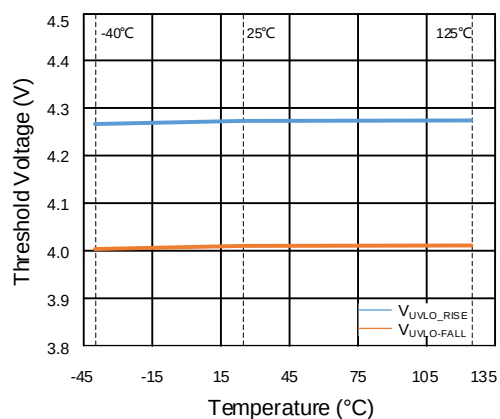
High Side MOSFETs Over Current Limit
($V_S=13.5V$)



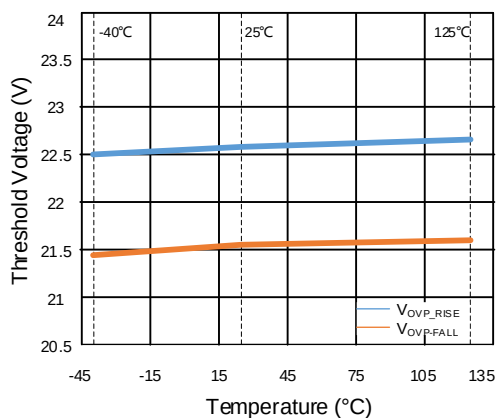
VDD Power On Reset and Power Off Reset
($V_S=13.5V$)



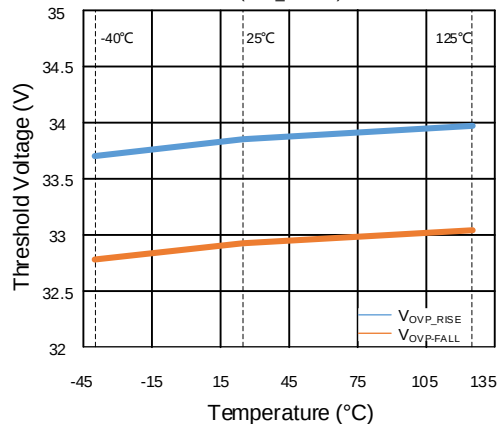
VS Undervoltage Lockout Voltage
($V_{DD}=5V$)



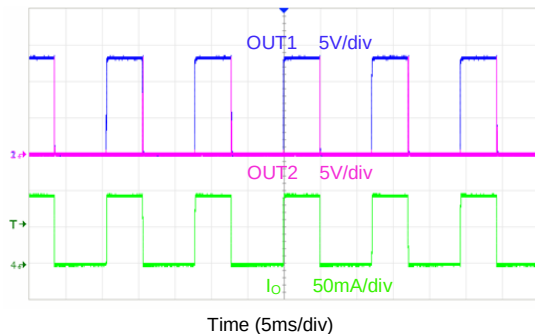
VS Overvoltage Protection Voltage
(EXT_OVP=0)



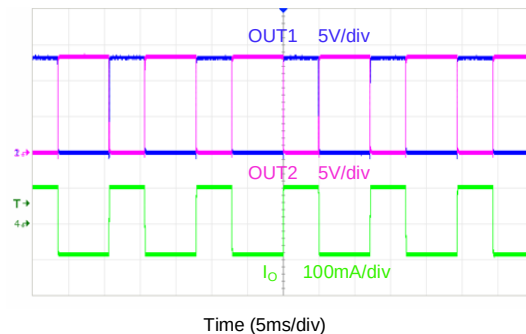
VS Overvoltage Protection Voltage
(EXT_OVP=1)



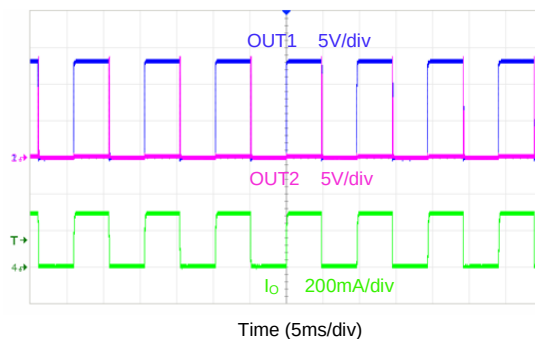
Passive Free-wheeling
(VS=13.5V I_o =100mA Duty=40% Frequency=80Hz)



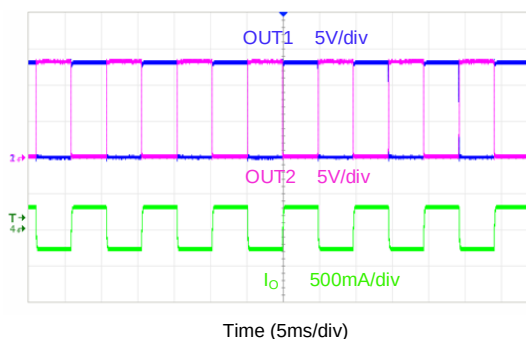
Active Free-wheeling
(VS=13.5V I_o =100mA Duty=40% Frequency=80Hz)

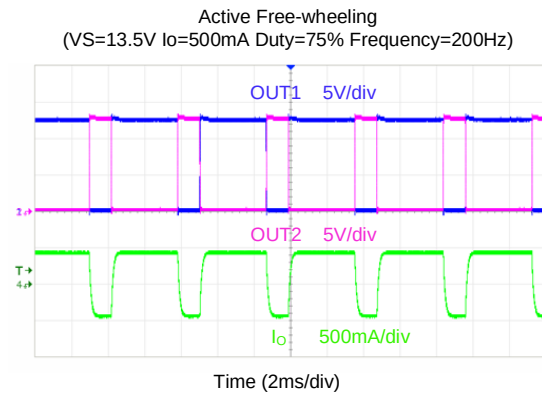
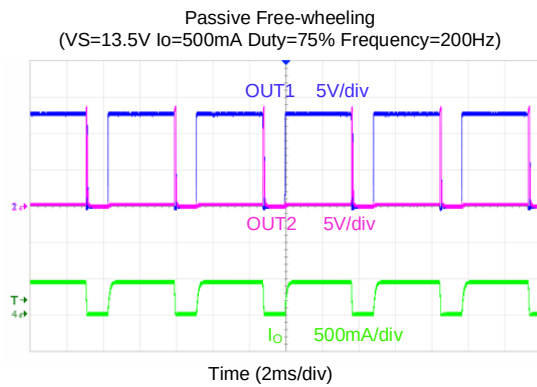


Passive Free-wheeling
(VS=13.5V I_o =300mA Duty=50% Frequency=100Hz)



Active Free-wheeling
(VS=13.5V I_o =300mA Duty=50% Frequency=100Hz)





Detailed Description

The SA52128B is an eight half-bridge motor driver for automotive, industrial, and other mechatronic applications. It can be configured as four independent H-bridges. Each half-bridge is designed to support up to 1A current.

To reduce the impact of electromagnetic interference (EMI) generated by the device, a spread spectrum clocking technique for the oscillator and charge pump is designed.

The device supports a standard 16-bit, 5MHz serial peripheral interface (SPI). It also features daisy-chain functionality, allowing the connection of multiple devices using a single CSB line.

Power Supply

VS supplies power to the MOSFETs, while VDD powers the logic circuits. Once VS is powered up, the drivers can be activated. Initially, all drivers are set to an off condition and maintain this state regardless of the VDD status. Powering up VDD results in a reset of all internal logic, and all internal registers are cleared upon VDD Power-On Reset (POR).

Driving Control

The device can be configured as an H-bridge, high-side driver, or low-side driver. The half-bridge outputs are designed to drive motor or LED loads. The half-bridge drivers can be programmed for continuous load driving (without PWM) or in chopping mode (with PWM). They also support parallel operation, which can be used for driving high-current loads.

Continuous Mode (Without PWM)

The half-bridge drivers can be programmed to drive loads continuously (without PWM). A controller can set the high-side enable bits (HBx_HS_EN) and low-side enable bits (HBx_LS_EN) in operation control registers (OP_CTRL_1, OP_CTRL_2) to switch the high-side or low-side individually.

Additionally, the device remains in Hi-Z mode if a particular half-bridge's high-side and low-side switches are simultaneously set high. This configuration is illustrated in Figures 4 and 5, which depict OUT1 and OUT2 driving a DC brush motor. In this setup, the motor operates in the forward direction when the high-side MOSFET of OUT1 and the low-side MOSFET of OUT2 are activated, allowing the motor current to flow from OUT1 to OUT2. Conversely, activating the high-side MOSFET of OUT2 and the low-side MOSFET of OUT1 will reverse the motor's direction, causing the motor current to flow from OUT2 to OUT1.

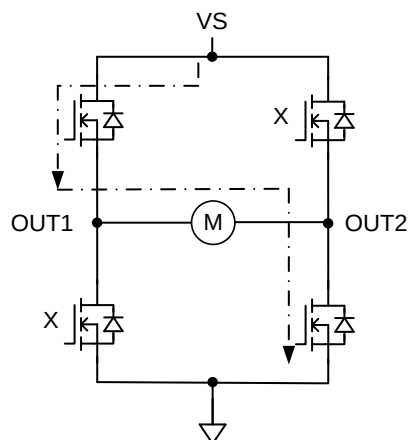


Figure 4. Continuous Mode (Forward)

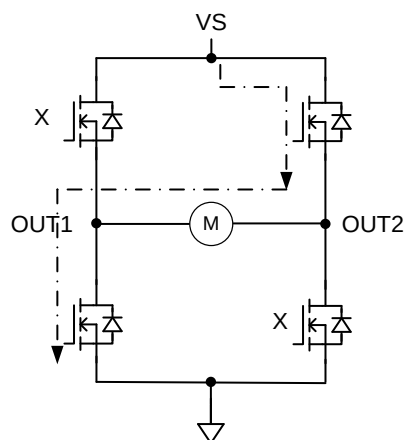


Figure 5. Continuous Mode (Reverse)

If the motor initially operates in either the forward or reverse direction, and then both the high-side and low-side switches are turned off, the H-bridge will enter coast mode. Due to the inductive energy, current will continue to flow in the motor, taking a path through the body diodes of the MOSFETs, as illustrated in Figures 6 and 7.

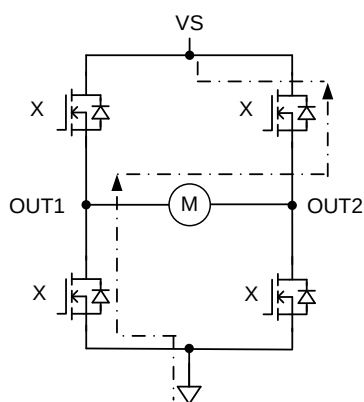


Figure 6. Coast-From Forward

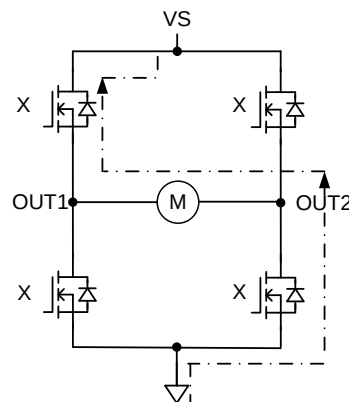


Figure 7. Coast-From Reverse

If the motor initially operates in either the forward or reverse direction, and then either the high-side or low-side switch is activated, the H-bridge will operate in brake mode. In the case of low-side braking, both low-side MOSFETs of the driver are turned on. Similarly, for high-side braking, both high-side MOSFETs are activated. These configurations are illustrated in Figures 8 and 9.

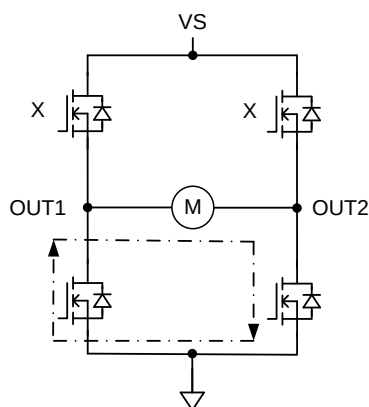


Figure 8. Brake-Low-Side

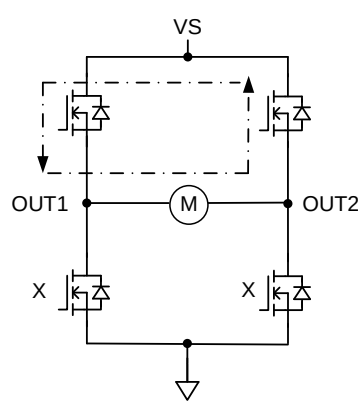


Figure 9. Brake-High-Side

Chopping Mode (With PWM)

Each half-bridge of the device can be configured for PWM mode, making it suitable for driving inductive loads such as DC brush motors. The device features eight distinct PWM channels, each with its own duty cycle settings using 8-bit resolution. It offers four selectable PWM frequencies, 80 Hz, 100 Hz, 200 Hz, and 2 kHz, for various application requirements.

The PWM chopping mode operation is performed through the following steps:

1. PWM Configuration

The half-bridge can be configured for continuous or chopping mode (PWM mode) through the PWM control register (PWM_CTRL_1). The HBx_PWM bit must be set to 1 to enable PWM switching mode. If it is not set, the half-bridge will operate in continuous mode. Additionally, setting the PWM_CHx_DIS bit in the PWM control register (PWM_CTRL_2) activates the PWM generator.

2. Free-Wheeling Mode (Synchronous Rectification) Disable/Enable

The device allows the selection of the synchronous rectification mode by setting the HBx_FW bit in the free-wheeling control registers (FW_CTRL_1). As illustrated in Figure 10, when the HBx_FW is disabled, the current flows through the high-side diode during the PWM off time. Conversely, enabling the HBx_FW bit opens the MOSFET to create an alternative current path. Figure 11 provides an example of synchronous rectification, demonstrating how the high-side

MOSFET of the OUT2 half-bridge is turned on while the low-side MOSFET of the same half-bridge is turned off during a PWM cycle.

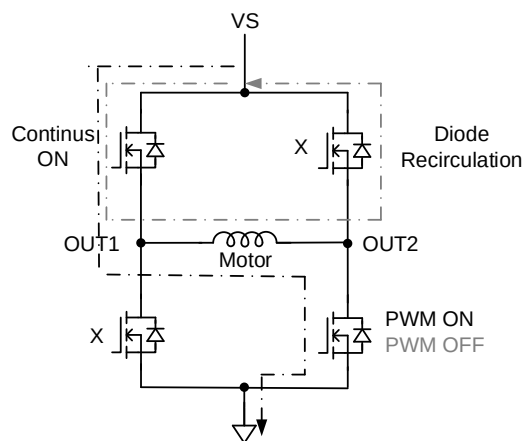


Figure 10. PWM Mode (Synchronous Rectification = OFF)

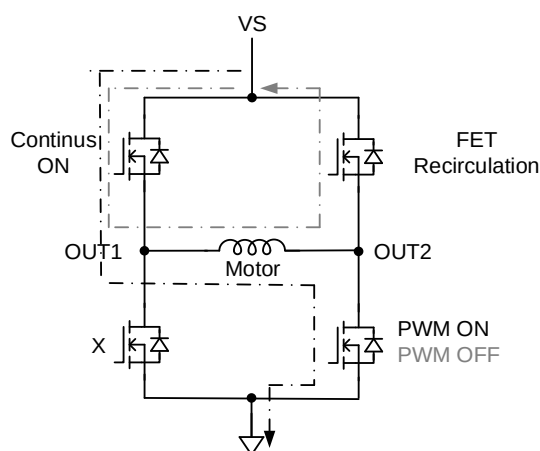


Figure 11. PWM Mode (Synchronous Rectification = ON)

3. PWM Channels Mapping

By configuring the PWM map control registers (PWM_MAP_CTRL_x), any OUTx half-bridge output can be mapped to any of the eight available PWM generators. The HBx_PWM_MAP bits are used to map these eight channels, as detailed in Table 1.

Table 1. PWM Mapping

HBx_PWM_MAP BITS	PWM CHANNEL
HBx_PWM_MAP=000b	Channel 1 selected for OUTx
HBx_PWM_MAP=001b	Channel 2 selected for OUTx
HBx_PWM_MAP=010b	Channel 3 selected for OUTx
HBx_PWM_MAP=011b	Channel 4 selected for OUTx
HBx_PWM_MAP=100b	Channel 5 selected for OUTx
HBx_PWM_MAP=101b	Channel 6 selected for OUTx
HBx_PWM_MAP=110b	Channel 7 selected for OUTx
HBx_PWM_MAP=111b	Channel 8 selected for OUTx

PWM Channels Configuration (PWM Frequency and PWM Duty)

Each PWM generator can be independently configured with a different frequency and duty cycle. The PWM frequency for each channel is determined by the PWM frequency control register (PWM_FREQ_CTRL_x), as shown in Table 2. The PWM duty cycle is managed using the PWM_DUTY_CHx bit in the PWM control register (PWM_DUTY_CTRL_x), as shown in Table 3.

Table 2. PWM Frequency

PWM_CHx_FREQ BITS	PWM FREQUENCY
PWM_CHx_FREQ=00b	80Hz
PWM_CHx_FREQ=01b	100Hz
PWM_CHx_FREQ=10b	200Hz
PWM_CHx_FREQ=11b	2000Hz

Table 3. PWM Duty Control Channelx Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CHx	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxx) × 1/255

Half-Bridge Enable

Following the initial four configuration steps, the final step involves enabling either the high-side or low-side MOSFETs. Once the half-bridge is configured for PWM generation, activation is achieved by enabling one of these switches. Specifically, the HBx_HS_EN bit in the operation control registers (OP_CTRL_1, OP_CTRL_2) is used to enable the high-side, while the HBx_LS_EN bit enables the low-side.

Protection Circuits

The device includes embedded protection functions: undervoltage, overvoltage, overcurrent, power-on reset, open load, thermal warning and thermal shutdown.

Undervoltage Lockout (UVLO)

When the voltage VS drops below the switch-off voltage threshold, V_{UVLO_FALL} , all output stages switch off. The configuration information remains intact and uncorrupted. The VS undervoltage error bit is latched high in the device status register (IC_STAT), and the nFAULT pin is driven low. If VS rises again and reaches the switch-on voltage V_{UVLO_RISE} , the power stages will be reactivated, and the nFAULT pin is set to high impedance. The UVLO error bit remains set until manually cleared through the CLR_FLT bit.

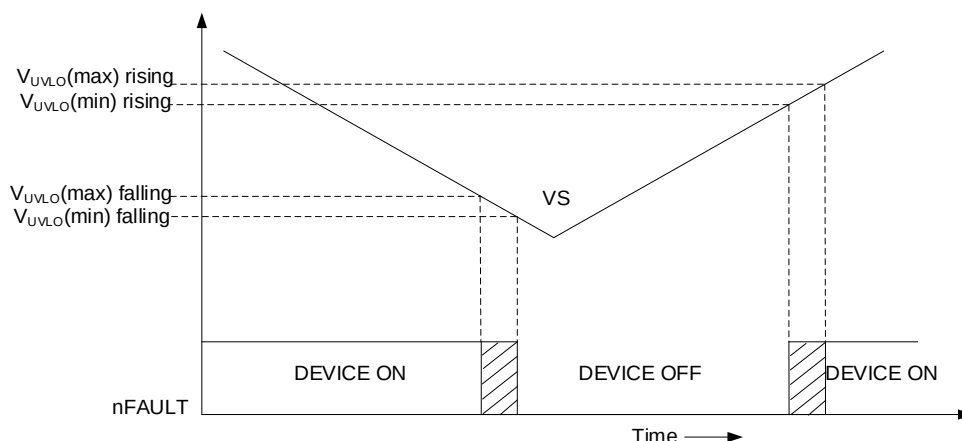


Figure 12. VS UVLO Operation

Overvoltage Protection (OVP)

If the supply voltage V_S exceeds the overvoltage voltage threshold, V_{OVP} , all output stages are automatically deactivated. Simultaneously, the V_S overvoltage error bit is latched high in the device status register (IC_STAT), and the nFAULT pin is driven low. If V_S falls below the threshold ($V_{OVP} - V_{OVP_HYS}$), the power stages are enabled, and the nFAULT pin is set to high-impedance. The OVP error bit remains set until cleared using an SPI command through the CLR_FLT bit. Additionally, the device supports an extended overvoltage operation, supporting a higher overvoltage range of up to 32.7V, by enabling the EXT_OVP bit in the configuration register (CONFIG_CTRL).

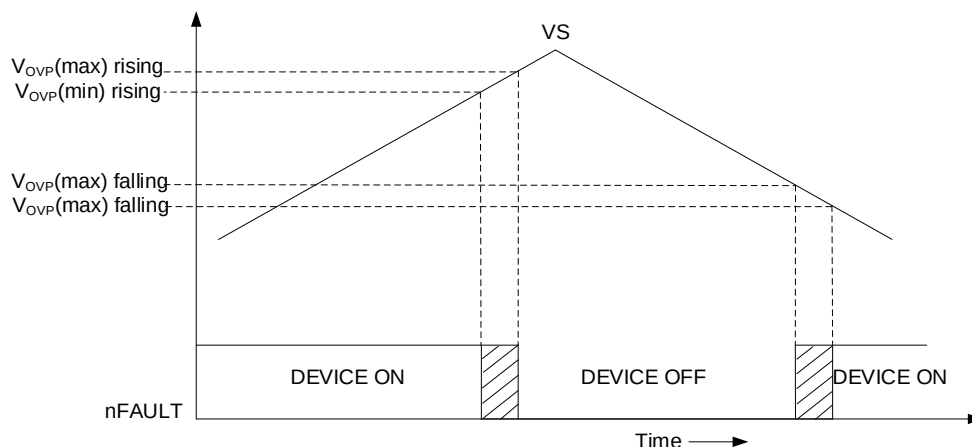


Figure 13. VS OVP Operation

VDD Power-On Reset (POR)

If the VDD logic supply decreases below the undervoltage threshold, V_{POR_OFF} , the SPI interfaces will no longer function, and the device will enter reset mode. The digital block will be initialized, and the output stages will switch to a high-impedance state. The undervoltage reset is released once the VDD voltage level exceeds the undervoltage threshold, V_{POR_ON} . This reset event is reported in the CONFIG_CTRL register by the NPOR bit. The NPOR error bit remains reset and latched low until it is cleared through the CLR_FLT bit.

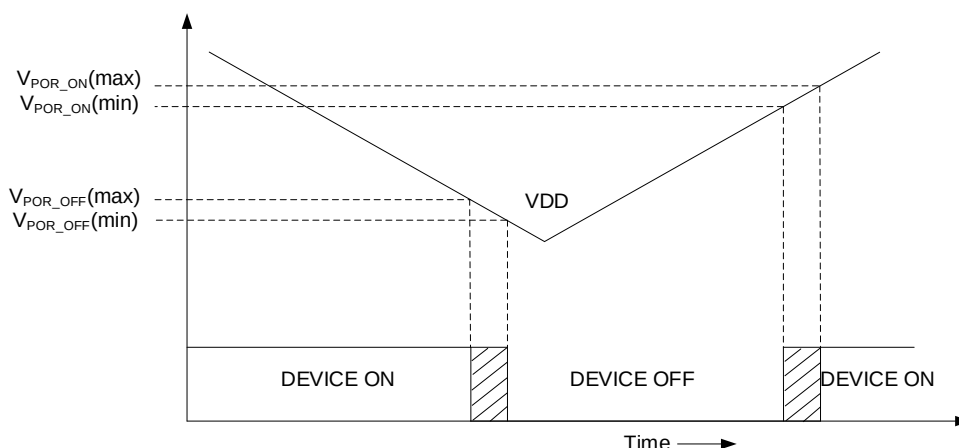


Figure 14. VDD POR Operation

Overcurrent Protection (OCP)

The device features overcurrent protection, actively monitoring the current in both the high-side and low-side drivers. If the current exceeds the overcurrent shutdown detection threshold, the affected high-side (HS) or low-side (LS) driver is immediately latched off. Simultaneously, the corresponding error bit—either HBx_HS_OCP or HBx_LS_OCP—is set and

latched after the specified shutdown time, t_{OC} . To restore normal functionality of the power switch after an overcurrent condition has been resolved, or to check if the fault persists, the user can disable the OCP fault indication on the nFAULT pin by activating the OCP_REP bit in the CONFIG_CTRL register.

Notes:

1. For $20V < V_S < 25V$, the OCP deglitch filter time must be limited to $10\mu s$ (Default Value, OCP_DEG = 000b).
2. For $V_S > 25V$, the OCP deglitch filter time must be limited to $1\mu s$ (Lowest Value, OCP_DEG = 011b).

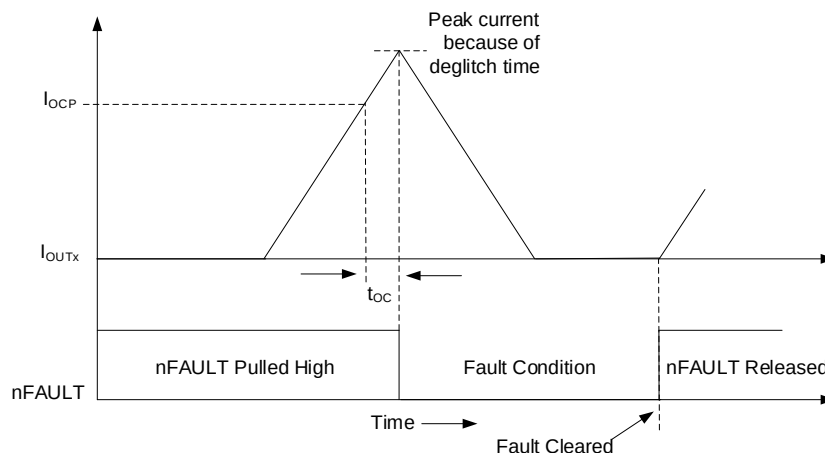


Figure 15. Over Current Protection

Open Load Detection (OLD)

The open-load detection (OLD) function is used to detect a proper load connection. The device supports active OLD and low-current OLD:

Active OLD

Active OLD can identify an open-load condition on the OUTx pins during load operation. As depicted in Figure 16, if the motor current (I_{OUTx}) falls below the open-load current threshold (I_{OLD}) and the fault condition persists for longer than the open-load deglitch time (t_{OL}), the device will recognize this as an active open-load fault. Under these circumstances, the nFAULT pin will be driven low. Once the open-load condition is resolved and the CLR_FLT bit is set to 1, the nFAULT pin is released.

The controller can determine the presence of an open-load condition by reading the device registers. The OLD bit in the device status register (IC_STAT) and either the HBx_HS_OLD or HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1 to indicate an open-load fault.

Two OLD control registers (OLD_CTRL_1 and OLD_CTRL_2) are used to configure the OLD function. The HBx_OLD_DIS bit in the OLD_CTRL_1 register allows the user to disable OLD on the OUTx pins, although OLD is enabled by default on the device. The OLD_REP bit in the OLD_CTRL_2 register determines whether a fault is reported on the nFAULT pin. The OLD_OP bit sets the device's response to an active OLD fault: if OLD_OP = 0, the OUTx pins switch to the Hi-Z state, stopping the output drive. Otherwise, the OUTx pins maintain their previous state and do not respond to the OLD fault.

Low-Current OLD

The device also incorporates a low-current open-load detection (OLD) mode, which operates similarly to the active open-load detection. The primary distinction between the low-current open-load and the active open-load is the current detection threshold, which is approximately ten times lower in the low-current open-load mode. This mode functions only with the low-side MOSFET. Activating the low-current OLD mode simultaneously deactivates the high-side OLD for the respective half-bridge.

As illustrated in Figure 17, if the motor current (I_{OUTX}) drops below the low-current open-load threshold (I_{OLD_LOW}) and the fault condition persists longer than the open-load deglitch filter time (t_{OL}), the device detects a low-current open-load fault. In this event, the nFAULT pin will be driven low. The fault condition can be cleared, and the nFAULT pin released, by resolving the open-load condition and setting the CLR_FLT bit to high.

The host controller can also read the register to determine whether an open-load condition exists. The OLD bit in the device status register (IC_STAT) and the HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1 to indicate a low-current open-load fault.

Notes: The following limitations apply when low-current OLD detection is enabled:

3. The corresponding over-current threshold for the low-side MOSFET is also reduced by a factor of 10 (~170 mA typ.).
4. The $R_{DS(on)}$ of the low-side MOSFET will increase by a factor of 10 (~7.5Ω typical), requiring thermal performance monitoring.

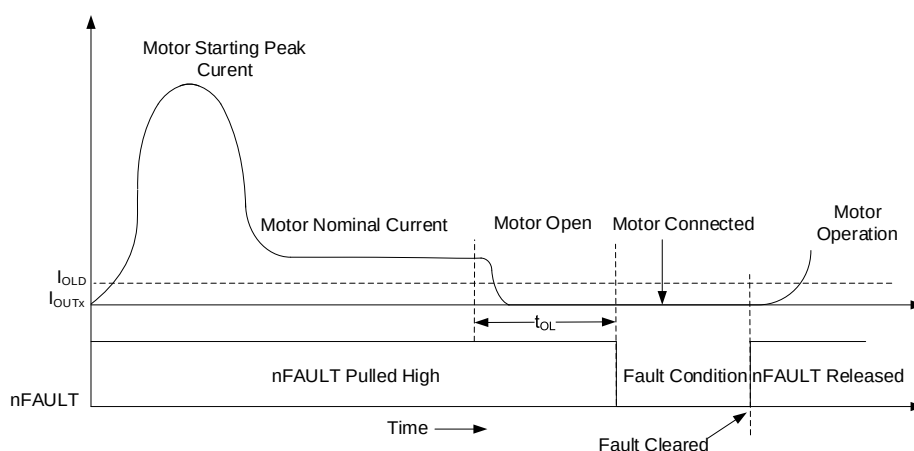


Figure 16. Active Open-Load Detection

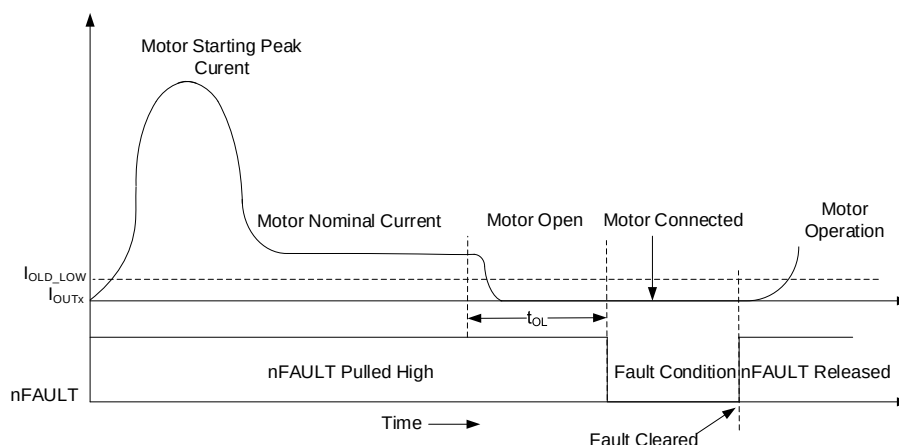


Figure 17. Low-Current OLD

Thermal Warning (OTW)

The device provides overtemperature warning and shutdown protection. If one or more temperature sensors reach the warning threshold, the temperature pre-warning bit, OTW, is set in the device status (IC_STAT) register. This bit is latched and can only be cleared through the SPI, while the output stages remain active. The reporting of OTW on the nFAULT pin can be enabled by setting the overtemperature warning reporting (OTW_REP) bit in the configuration control

(CONFIG_CTRL) register. The nFAULT pin is released when the die temperature falls below the $T_{WARN}-T_{WARN_HYS}$ threshold.

Thermal Shutdown (TSD)

If one or more temperature sensors reach the shutdown temperature threshold, all outputs are latched off, and the nFAULT pin is driven low. The OTSD bit is set in the device status (IC_STAT) register. All outputs will be activated, and the nFAULT pin will be released when the die temperature decreases below the thermal shutdown threshold ($T_{SD}-T_{HYS}$). The OTSD bit remains latched high, indicating a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

Programming Configuration

The device can be controlled using a standard 16-bit SPI interface, with data communication initiated by clocking in the Most Significant Bit (MSB) first. The SPI interface operates as a synchronous serial interface, allowing for address and data transfer at bit rates of up to 5MHz. It is configured for 8-bit byte transfers, making it compatible with a standard SPI bus. Communication over the SPI utilizes four pins: SCLK (synchronous clock), CSB (chip select, active low), SI (data input to the device for write operations), and SO (data output from the device for read operations), as shown in Figure 18.

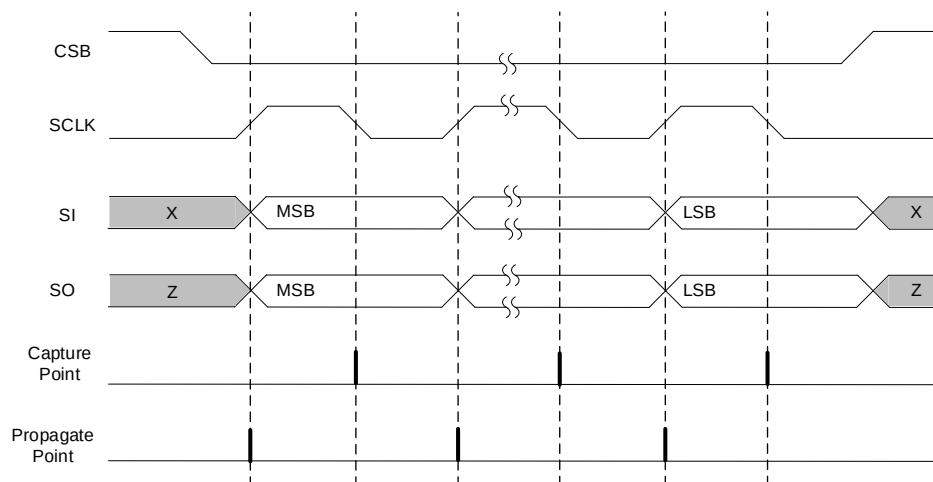


Figure 18. SPI Data Frame

A valid frame on the SPI interface must adhere to the following conditions:

1. When the CSB pin is set to high, the device disregards any signals on the SCLK and SI pins, and the SO pin enters a high impedance (Hi-Z) state.
2. Data is captured on the falling edge of SCLK, and data is propagated on the rising edge of SCLK.
3. The most significant bit (MSB) is always shifted in and out first.
4. A complete transaction requires a full sequence of 16 SCLK cycles.
5. The data word transmitted to the SI pin must consist of exactly 16 bits.
6. For write commands, the current data in the register being written to is shifted out on the SO pin, following the 8-bit command data.

SPI Format

Each SPI communication sequence with the device begins with an address byte, followed by a data byte. The device's SPI functionality includes 1 Read/Write (R/W) bit at bit position 14, six address bits, and eight data bits. The control registers are READ/WRITE registers. To set the control register to READ, bit 14 in the address byte must be set to '1'; otherwise, it should be set to '0' for WRITE. As the microcontroller transmits the address byte via the SI pin, the device's Status Register data is simultaneously shifted out through the SO pin. The subsequent data byte, consisting of bits 7 to 0, is used to configure the half-bridges or retrieve the device's status information. The mapping of the SPI Registers is shown in Table 6.

Table 4. SI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. SO Output Data Word Format

			Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OTSD	OLD	OCP	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

Daisy Chain

The device is designed to support daisy-chain operation with other devices that utilize the same SPI protocol, as demonstrated in Figure 19. In this setup, the controller's output (MO) is connected to the serial input (SI) of the first target device. The serial output (SO) of this device is then connected to the SI of the next target, forming a chain. The SO of the last target in the chain is linked to the controller's input (MI), thereby completing the SPI communication loop.

In a daisy-chain configuration, a single chip select (CSB) and a clock signal (SCLK) are distributed in parallel across all target devices. These connections allow the microcontroller to efficiently control and access the SPI devices. Figure 20 illustrates the topology and corresponding waveforms when three devices are interconnected in a series configuration.

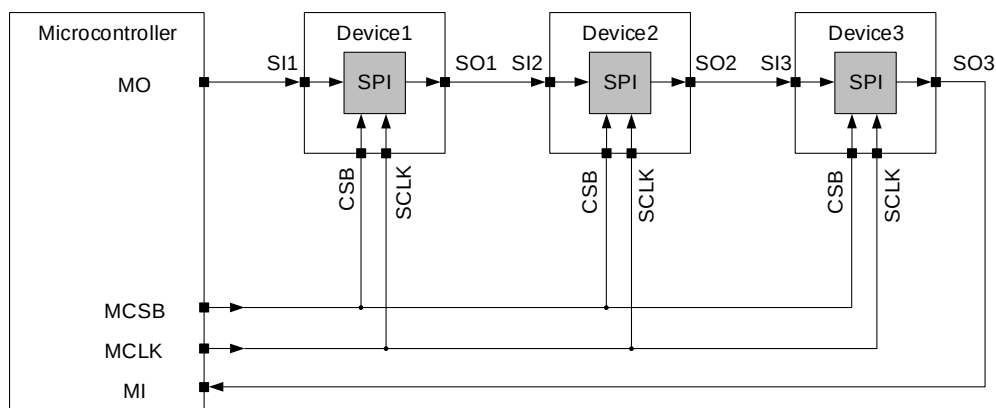


Figure 19. SPI Daisy Chain

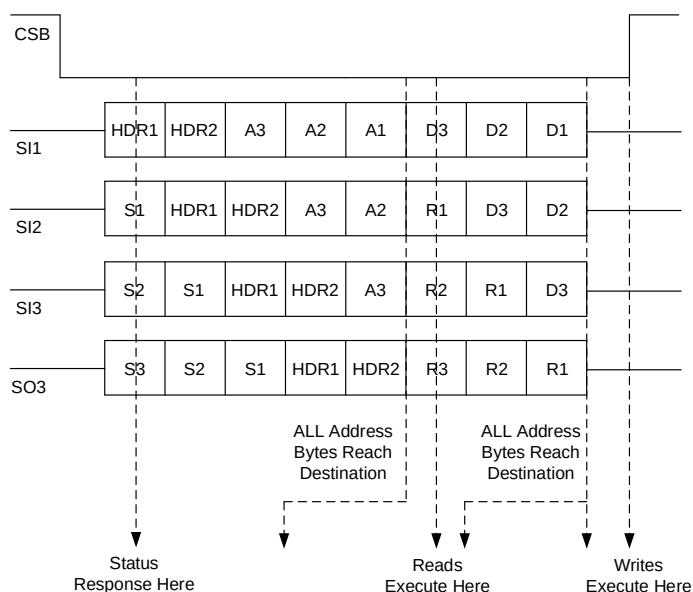


Figure 20. Daisy Chain SPI Operation

In the daisy-chain configuration depicted above, the first device in the chain receives data from the controller in the following format, as shown in SI1 of Figure 20:

1. 2 bytes of Header
2. 3 bytes of Address
3. 3 bytes of Data

Once the data has been transmitted through the chain, the controller receives it back in the format illustrated in SO3 of Figure 20:

1. 3 bytes of Status
2. 2 bytes of Header (which should be identical to the information sent by the controller)
3. 3 bytes of Report

The two header bytes carry critical information, including the number of devices in the chain and a global clear fault command. The N5 to N0 bits in Header1 indicate that up to 63 ($2^6 - 1$) devices can be connected in series using daisy-chain connection. The CLR bit in Header2 is a global clear fault command that resets the fault registers of all devices in the chain. Both header bytes must start with 1 and 0.

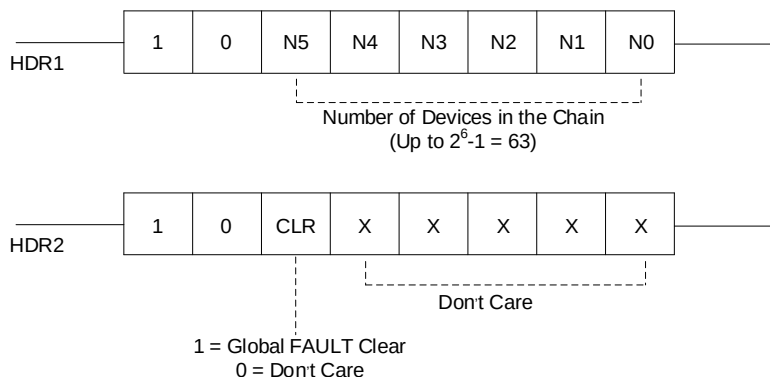


Figure 21. Header Bits

All devices in the configuration will relay their fault status through the status byte, as shown in Figure 22. This feature facilitates convenient and efficient monitoring of controller fault status, enhancing the overall functionality of the device.

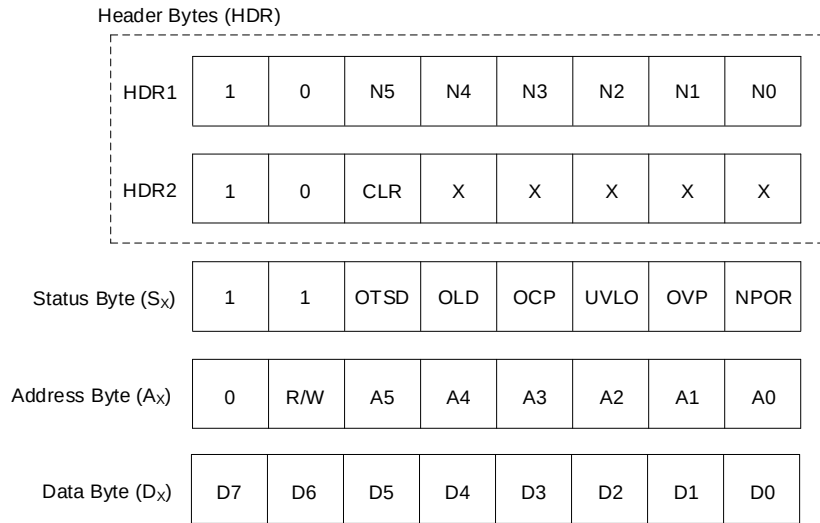


Figure 22. Daisy Chain Read Registers

The device can determine its position in the chain by counting the number of status bytes that follow the header byte. As illustrated in Figure 20, device 2 identifies its position by recognizing one status byte (S1) following the header, while device 3 identifies two status bytes (S1, S2) after the header. Once the device determines its position and the total number of devices connected in the chain, each device can load the relevant address and data bytes into its buffer, effectively bypassing irrelevant bits. This method ensures efficient operation, even in a chain comprising up to 63 devices.

Table 6. SA52128B Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
CONFIG_CTRL	Reserved		IC_ID		OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	R/W	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	R/W	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	R/W	09h
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	R/W	0Bh
PWM_CTRL_2	PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	R/W	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	R/W	0Dh
PWM_MAP_CTRL_1	Reserved			HB2_PWM_MAP			HB1_PWM_MAP		R/W	0Fh
PWM_MAP_CTRL_2	Reserved			HB4_PWM_MAP			HB3_PWM_MAP		R/W	10h
PWM_MAP_CTRL_3	Reserved			HB6_PWM_MAP			HB5_PWM_MAP		R/W	11h
PWM_MAP_CTRL_4	Reserved			HB8_PWM_MAP			HB7_PWM_MAP		R/W	12h
PWM_FREQ_CTRL_1	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		R/W	13h
PWM_FREQ_CTRL_2	PWM_CH8_FREQ		PWM_CH7_FREQ		PWM_CH6_FREQ		PWM_CH5_FREQ		R/W	14h
PWM_DUTY_CTRL_1				PWM_DUTY_CH1					R/W	15h
PWM_DUTY_CTRL_2				PWM_DUTY_CH2					R/W	16h
PWM_DUTY_CTRL_3				PWM_DUTY_CH3					R/W	17h
PWM_DUTY_CTRL_4				PWM_DUTY_CH4					R/W	18h
PWM_DUTY_CTRL_5				PWM_DUTY_CH5					R/W	19h
PWM_DUTY_CTRL_6				PWM_DUTY_CH6					R/W	1Ah
PWM_DUTY_CTRL_7				PWM_DUTY_CH7					R/W	1Bh
PWM_DUTY_CTRL_8				PWM_DUTY_CH8					R/W	1Ch
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	R/W	1Dh
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	R/W	1Fh
OLD_CTRL_2	OLD_REP	OLD_OP				Reserved			R/W	20h
OLD_CTRL_3		OCP_DEG				Reserved			R/W	21h
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	R/W	22h

SPI Status Registers

The read-only status registers are used to report warning and fault conditions.

IC_STAT

IC_Status Register (Address =0x00) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	OTSD	OTW	OLD	OCF	UVLO	OVP	NPOR
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
Reserved	D7	R	Reserved. Always reads as '0'
OTSD	D6	R	Temperature shutdown error detection 0 _B Junction temperature below temperature shutdown threshold 1 _B Junction temperature has reached temperature shutdown threshold
OTW	D5	R	Temperature pre-warning error detection 0 _B Junction temperature below temperature pre-warning threshold 1 _B Junction temperature has reached temperature pre-warning threshold.
OLD	D4	R	Open Load error detection 0 _B No Open Load 1 _B Open load
OCF	D3	R	Over current error detection 0 _B No Over current 1 _B Over current
UVLO	D2	R	VS Undervoltage error detection 0 _B No undervoltage on VS detected 1 _B Undervoltage on VS detected
OVP	D1	R	VS Overvoltage error detection 0 _B No overvoltage on VS detected 1 _B Overvoltage on VS detected
NPOR	D0	R	Not Power on Reset (NPOR) detection 0 _B POR on EN or VDD supply rail 1 _B No POR

OCP_STAT_1

Overcurrent Error Status of Half-Bridge Outputs 1-4 (Address =0x01) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB4_HS_OC	D7	R	High-side (HS) switch of half-bridge 4 overcurrent detection 0 _B No error on HS4 switch 1 _B Overcurrent detected on HS4 switch
HB4_LS_OC	D6	R	Low-side (LS) switch of half-bridge 4 overcurrent detection 0 _B No error on LS4 switch 1 _B Overcurrent detected on LS4 switch
HB3_HS_OC	D5	R	High-side (HS) switch of half-bridge 3 overcurrent detection 0 _B No error on HS3 switch 1 _B Overcurrent detected on HS3 switch
HB3_LS_OC	D4	R	Low-side (LS) switch of half-bridge 3 overcurrent detection 0 _B No error on LS3 switch 1 _B Overcurrent detected on LS3 switch
HB2_HS_OC	D3	R	High-side (HS) switch of half-bridge 2 overcurrent detection 0 _B No error on HS2 switch 1 _B Overcurrent detected on HS2 switch
HB2_LS_OC	D2	R	Low-side (LS) switch of half-bridge 2 overcurrent detection 0 _B No error on LS2 switch 1 _B Overcurrent detected on LS2 switch
HB1_HS_OC	D1	R	High-side (HS) switch of half-bridge 1 overcurrent detection 0 _B No error on HS1 switch 1 _B Overcurrent detected on HS1 switch
HB1_LS_OC	D0	R	Low-side (LS) switch of half-bridge 1 overcurrent detection 0 _B No error on LS1 switch 1 _B Overcurrent detected on LS1 switch

OCP_STAT_2

Overcurrent Error Status of Half-Bridge Outputs 5-8 (Address =0x02) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OC	HB8_LS_OC	HB7_HS_OC	HB7_LS_OC	HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB8_HS_OC	D7	R	High-side (HS) switch of half-bridge 8 overcurrent detection 0 _B No error on HS8 switch 1 _B Overcurrent detected on HS8 switch
HB8_LS_OC	D6	R	Low-side (LS) switch of half-bridge 8 overcurrent detection 0 _B No error on LS8 switch 1 _B Overcurrent detected on LS8 switch
HB7_HS_OC	D5	R	High-side (HS) switch of half-bridge 7 overcurrent detection 0 _B No error on HS7 switch 1 _B Overcurrent detected on HS7 switch
HB7_LS_OC	D4	R	Low-side (LS) switch of half-bridge 7 overcurrent detection 0 _B No error on LS7 switch 1 _B Overcurrent detected on LS7 switch
HB6_HS_OC	D3	R	High-side (HS) switch of half-bridge 6 overcurrent detection 0 _B No error on HS6 switch 1 _B Overcurrent detected on HS6 switch
HB6_LS_OC	D2	R	Low-side (LS) switch of half-bridge 6 overcurrent detection 0 _B No error on LS6 switch 1 _B Overcurrent detected on LS6 switch
HB5_HS_OC	D1	R	High-side (HS) switch of half-bridge 5 overcurrent detection 0 _B No error on HS5 switch 1 _B Overcurrent detected on HS5 switch
HB5_LS_OC	D0	R	Low-side (LS) switch of half-bridge 5 overcurrent detection 0 _B No error on LS5 switch 1 _B Overcurrent detected on LS5 switch

OLD_STAT_1

Open Load Error Status of Half-Bridge Outputs 1-4 (Address =0x04) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OL	HB4_LS_OL	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB4_HS_OL	D7	R	High-side (HS) switch of half-bridge 4 open load detection 0 _B No error on HS4 switch (default value) 1 _B Open load detected on HS4 switch
HB4_LS_OL	D6	R	Low-side (LS) switch of half-bridge 4 open load detection 0 _B No error on LS4 switch (default value) 1 _B Open load detected on LS4 switch
HB3_HS_OL	D5	R	High-side (HS) switch of half-bridge 3 open load detection 0 _B No error on HS3 switch (default value) 1 _B Open load detected on HS3 switch
HB3_LS_OL	D4	R	Low-side (LS) switch of half-bridge 3 open load detection 0 _B No error on LS3 switch (default value) 1 _B Open load detected on LS3 switch
HB2_HS_OL	D3	R	High-side (HS) switch of half-bridge 2 open load detection 0 _B No error on HS2 switch (default value) 1 _B Open load detected on HS2 switch
HB2_LS_OL	D2	R	Low-side (LS) switch of half-bridge 2 open load detection 0 _B No error on LS2 switch (default value) 1 _B Open load detected on LS2 switch
HB1_HS_OL	D1	R	High-side (HS) switch of half-bridge 1 open load detection 0 _B No error on HS1 switch (default value) 1 _B Open load detected on HS1 switch
HB1_LS_OL	D0	R	Low-side (LS) switch of half-bridge 1 open load detection 0 _B No error on LS1 switch (default value) 1 _B Open load detected on LS1 switch

OLD_STAT_2

Open Load Error Status of Half-Bridge Outputs 5-8 (Address =0x05) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OL	HB8_LS_OL	HB7_HS_OL	HB7_LS_OL	HB6_HS_OL	HB6_LS_OL	HB5_HS_OL	HB5_LS_OL
R	R	R	R	R	R	R	R

Field	Bits	Type	Description
HB8_HS_OL	D7	R	High-side (HS) switch of half-bridge 8 open load detection 0 _B No error on HS8 switch 1 _B Open load detected on HS8 switch
HB8_LS_OL	D6	R	Low-side (LS) switch of half-bridge 8 open load detection 0 _B No error on LS8 switch 1 _B Open load detected on LS8 switch
HB7_HS_OL	D5	R	High-side (HS) switch of half-bridge 7 open load detection 0 _B No error on HS7 switch 1 _B Open load detected on HS7 switch
HB7_LS_OL	D4	R	Low-side (LS) switch of half-bridge 7 open load detection 0 _B No error on LS7 switch 1 _B Open load detected on LS7 switch
HB6_HS_OL	D3	R	High-side (HS) switch of half-bridge 6 open load detection 0 _B No error on HS6 switch 1 _B Open load detected on HS6 switch
HB6_LS_OL	D2	R	Low-side (LS) switch of half-bridge 6 open load detection 0 _B No error on LS6 switch 1 _B Open load detected on LS6 switch
HB5_HS_OL	D1	R	High-side (HS) switch of half-bridge 5 open load detection 0 _B No error on HS5 switch 1 _B Open load detected on HS5 switch
HB5_LS_OL	D0	R	Low-side (LS) switch of half-bridge 5 open load detection 0 _B No error on LS5 switch 1 _B Open load detected on LS5 switch

SPI Control Registers

The control registers are used to configure the device. The control registers have both read and write capabilities.

CONFIG_CTRL

Configuration Register (Address =0x07) [reset =0x20]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	IC_ID			OCP_REG	OTW_REG	EXT_OVP	CLR_FLT
R	R	R	R	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7	R	Reserved. Always reads as '0'
IC_ID	D6	R	Reserved. Always reads as '0'
	D5	R	Reserved. Always reads as '1'
	D4	R	Reserved. Always reads as '0'
OCP_REG	D3	R/W	0 _B Overcurrent condition is reported in nFAULT pin 1 _B Overcurrent condition warning is not reported in nFAULT pin
OTW_REG	D2	R/W	0 _B Overtemperature warning is not reported in nFAULT pin 1 _B Overtemperature warning is reported in nFAULT pin
EXT_OVP	D1	R/W	0 _B Overvoltage protection threshold is at 21V min. 1 _B Overvoltage protection threshold is at 32.7V min.
CLR_FLT	D0	R/W	0 _B Faults not cleared 1 _B Clear all faults

OP_CTRL_1

Half-Bridge Output Control 1(Address =0x08) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB4_HS_EN	D7	R/W	Half-bridge output 4 High side switch enable 0 _B HS4 OFF 1 _B HS4 ON
HB4_LS_EN	D6	R/W	Half-bridge output 4 Low side switch enable 0 _B LS4 OFF 1 _B LS4 ON
HB3_HS_EN	D5	R/W	Half-bridge output 3 High side switch enable 0 _B HS3 OFF 1 _B HS3 ON
HB3_LS_EN	D4	R/W	Half-bridge output 3 Low side switch enable 0 _B LS3 OFF 1 _B LS3 ON
HB2_HS_EN	D3	R/W	Half-bridge output 2 High side switch enable 0 _B HS2 OFF 1 _B HS2 ON
HB2_LS_EN	D2	R/W	Half-bridge output 2 Low side switch enable 0 _B LS2 OFF 1 _B LS2 ON
HB1_HS_EN	D1	R/W	Half-bridge output 1 High side switch enable 0 _B HS1 OFF 1 _B HS1 ON
HB1_LS_EN	D0	R/W	Half-bridge output 1 Low side switch enable 0 _B LS1 OFF 1 _B LS1 ON

OP_CTRL_2

Half-Bridge Output Control 2 (Address =0x09) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_HS_EN	D7	R/W	Half-bridge output 8 High side switch enable 0 _B HS8 OFF 1 _B HS8 ON
HB8_LS_EN	D6	R/W	Half-bridge output 8 Low side switch enable 0 _B LS8 OFF 1 _B LS8 ON
HB7_HS_EN	D5	R/W	Half-bridge output 7 High side switch enable 0 _B HS7 OFF 1 _B HS7 ON
HB7_LS_EN	D4	R/W	Half-bridge output 7 Low side switch enable 0 _B LS7 OFF 1 _B LS7 ON
HB6_HS_EN	D3	R/W	Half-bridge output 6 High side switch enable 0 _B HS6 OFF 1 _B HS6 ON
HB6_LS_EN	D2	R/W	Half-bridge output 6 Low side switch enable 0 _B LS6 OFF 1 _B LS6 ON
HB5_HS_EN	D1	R/W	Half-bridge output 5 High side switch enable 0 _B HS5 OFF 1 _B HS5 ON
HB5_LS_EN	D0	R/W	Half-bridge output 5 Low side switch enable 0 _B LS5 OFF 1 _B LS5 ON

PWM_CTRL_1

Half-Bridge PWM Control 1 (Address =0x0B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_PWM	D7	R/W	0 _B Half-bridge 8 is operating in continuous mode 1 _B Half-bridge 8 is operating in PWM mode
HB7_PWM	D6	R/W	0 _B Half-bridge 7 is operating in continuous mode 1 _B Half-bridge 7 is operating in PWM mode
HB6_PWM	D5	R/W	0 _B Half-bridge 6 is operating in continuous mode 1 _B Half-bridge 6 is operating in PWM mode
HB5_PWM	D4	R/W	0 _B Half-bridge 5 is operating in continuous mode 1 _B Half-bridge 5 is operating in PWM mode
HB4_PWM	D3	R/W	0 _B Half-bridge 4 is operating in continuous mode 1 _B Half-bridge 4 is operating in PWM mode
HB3_PWM	D2	R/W	0 _B Half-bridge 3 is operating in continuous mode 1 _B Half-bridge 3 is operating in PWM mode
HB2_PWM	D1	R/W	0 _B Half-bridge 2 is operating in continuous mode 1 _B Half-bridge 2 is operating in PWM mode
HB1_PWM	D0	R/W	0 _B Half-bridge 1 is operating in continuous mode 1 _B Half-bridge 1 is operating in PWM mode

PWM_CTRL_2

Half-Bridge PWM Control 2 (Address =0x0C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH8_DIS	D7	R/W	0 _B PWM Generator-8 is enabled 1 _B PWM Generator-8 is disabled
PWM_CH7_DIS	D6	R/W	0 _B PWM Generator-7 is enabled 1 _B PWM Generator-7 is disabled
PWM_CH6_DIS	D5	R/W	0 _B PWM Generator-6 is enabled 1 _B PWM Generator-6 is disabled
PWM_CH5_DIS	D4	R/W	0 _B PWM Generator-5 is enabled 1 _B PWM Generator-5 is disabled

PWM_CH4_DIS	D3	R/W	0 _B PWM Generator-4 is enabled 1 _B PWM Generator-4 is disabled
PWM_CH3_DIS	D2	R/W	0 _B PWM Generator-3 is enabled 1 _B PWM Generator-3 is disabled
PWM_CH2_DIS	D1	R/W	0 _B PWM Generator-2 is enabled 1 _B PWM Generator-2 is disabled
PWM_CH1_DIS	D0	R/W	0 _B PWM Generator-1 is enabled 1 _B PWM Generator-1 is disabled

FW_CTRL_1

Free-Wheeling Configuration 1 (Address =0x0D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
FW_HB8	FW_HB7	FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
FW_HB8	D7	R/W	HB8 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB7	D6	R/W	HB7 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB6	D5	R/W	HB6 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB5	D4	R/W	HB5 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB4	D3	R/W	HB4 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB3	D2	R/W	HB3 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB2	D1	R/W	HB2 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling
FW_HB1	D0	R/W	HB1 free-wheeling configuration 0 _B Passive free-wheeling 1 _B Active free-wheeling

PWM_MAP_CTRL_1

Half-Bridge Output PWM Map Control 1 (Address =0x0F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB2_PWM_MAP		HB1_PWM_MAP			
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7:D6	R	Reserved. Always reads as '0'
HB2_PWM_MAP	D5:D3	R/W	Half-bridge output 2 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8
HB1_PWM_MAP	D2:D0	R/W	Half-bridge output 1 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7

			111 _B PWM control with PWM Channel 8
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PWM_MAP_CTRL_2

Half-Bridge Output PWM Map Control 2 (Address =0x10) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB4_PWM_MAP			HB3_PWM_MAP		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7:D6	R	Reserved. Always reads as '0'
HB4_PWM_MAP	D5:D3	R/W	Half-bridge output 4 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8
HB3_PWM_MAP	D2:D0	R/W	Half-bridge output 3 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8

PWM_MAP_CTRL_3

Half-Bridge Output PWM Map Control 3 (Address =0x11) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB6_PWM_MAP			HB5_PWM_MAP		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7:D6	R	Reserved. Always reads as '0'
HB6_PWM_MAP	D5:D3	R/W	Half-bridge output 6 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8
HB5_PWM_MAP	D2:D0	R/W	Half-bridge output 5 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8

PWM_MAP_CTRL_4

Half-Bridge Output PWM Map Control 4 (Address =0x12) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HB8_PWM_MAP			HB7_PWM_MAP		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
Reserved	D7:D6	R	Reserved. Always reads as '0'
HB8_PWM_MAP	D5:D3	R/W	Half-bridge output 8 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8
HB7_PWM_MAP	D2:D0	R/W	Half-bridge output 7 mode select 000 _B PWM control with PWM Channel 1 001 _B PWM control with PWM Channel 2 010 _B PWM control with PWM Channel 3 011 _B PWM control with PWM Channel 4 100 _B PWM control with PWM Channel 5 101 _B PWM control with PWM Channel 6 110 _B PWM control with PWM Channel 7 111 _B PWM control with PWM Channel 8

PWM_FREQ_CTRL_1

PWM Channel Frequency Select 1 (Address =0x13) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_FREQ	PWM_CH3_FREQ	PWM_CH2_FREQ	PWM_CH1_FREQ				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH4_FREQ	D7:D6	R/W	PWM Channel 4 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz
PWM_CH3_FREQ	D5:D4	R/W	PWM Channel 3 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz
PWM_CH2_FREQ	D3:D2	R/W	PWM Channel 2 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz
PWM_CH1_FREQ	D1:D0	R/W	PWM Channel 1 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz

PWM_FREQ_CTRL_2

PWM Channel Frequency Select 2 (Address =0x14) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH8_FREQ	PWM_CH7_FREQ	PWM_CH6_FREQ	PWM_CH5_FREQ				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_CH8_FREQ	D7:D6	R/W	PWM Channel 8 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz
PWM_CH7_FREQ	D5:D4	R/W	PWM Channel 7 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz

PWM_CH6_FREQ	D3:D2	R/W	PWM Channel 6 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz
PWM_CH5_FREQ	D1:D0	R/W	PWM Channel 5 frequency select 00 _B PWM frequency: 80Hz 01 _B PWM frequency: 100Hz 10 _B PWM frequency: 200Hz 11 _B PWM frequency: 2000Hz

PWM_DUTY_CTRL_1

PWM Channel 1 Duty Cycle Configuration (Address =0x15) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH1	D7:D0	R/W	PWM Channel 1 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_2

PWM Channel 2 Duty Cycle Configuration (Address =0x16) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH2	D7:D0	R/W	PWM Channel 2 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_3

PWM Channel 3 Duty Cycle Configuration (Address =0x17) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH3	D7:D0	R/W	PWM Channel 3 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_4

PWM Channel 4 Duty Cycle Configuration (Address =0x18) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH4							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH4	D7:D0	R/W	PWM Channel 4 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_5

PWM Channel 5 Duty Cycle Configuration (Address =0x19) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH5							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH5	D7:D0	R/W	PWM Channel 5 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_6

PWM Channel 6 Duty Cycle Configuration (Address =0x1A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH6							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH6	D7:D0	R/W	PWM Channel 6 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_7

PWM Channel 7 Duty Cycle Configuration (Address =0x1B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH7							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH7	D7:D0	R/W	PWM Channel 7 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

PWM_DUTY_CTRL_8

PWM Channel 8 Duty Cycle Configuration (Address =0x1C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH8							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
PWM_DUTY_CH8	D7:D0	R/W	PWM Channel 8 Duty-Cycle configuration 0000 0000 _B 100% OFF xxxx xxxx _B parts of 255 ON 1111 1111 _B 100% ON

SR_CTRL_1

The Slew Rate Configuration 1 (Address =0x1D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_SR	D7	R/W	HB8 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs
HB7_SR	D6	R/W	HB7 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs
HB6_SR	D5	R/W	HB6 slew rate configuration

			0 _B 1V/μs 1 _B 3.2V/μs
HB5_SR	D4	R/W	HB5 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs
HB4_SR	D3	R/W	HB4 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs
HB3_SR	D2	R/W	HB3 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs
HB2_SR	D1	R/W	HB2 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs
HB1_SR	D0	R/W	HB1 slew rate configuration 0 _B 1V/μs 1 _B 3.2V/μs

OLD_CTRL_1

The Open Load Detection Control 1 (Address =0x1F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_OLD_DIS	D7	R/W	HB8 open load detection configuration 0 _B Open-load detection on half-bridge 8 is enabled 1 _B Open-load detection on half-bridge 8 is disabled
HB7_OLD_DIS	D6	R/W	HB7 open load detection configuration 0 _B Open-load detection on half-bridge 7 is enabled 1 _B Open-load detection on half-bridge 7 is disabled
HB6_OLD_DIS	D5	R/W	HB6 open load detection configuration 0 _B Open-load detection on half-bridge 6 is enabled 1 _B Open-load detection on half-bridge 6 is disabled
HB5_OLD_DIS	D4	R/W	HB5 open load detection configuration 0 _B Open-load detection on half-bridge 5 is enabled 1 _B Open-load detection on half-bridge 5 is disabled
HB4_OLD_DIS	D3	R/W	HB4 open load detection configuration 0 _B Open-load detection on half-bridge 4 is enabled 1 _B Open-load detection on half-bridge 4 is disabled
HB3_OLD_DIS	D2	R/W	HB3 open load detection configuration 0 _B Open-load detection on half-bridge 3 is enabled 1 _B Open-load detection on half-bridge 3 is disabled
HB2_OLD_DIS	D1	R/W	HB2 open load detection configuration 0 _B Open-load detection on half-bridge 2 is enabled 1 _B Open-load detection on half-bridge 2 is disabled
HB1_OLD_DIS	D0	R/W	HB1 open load detection configuration 0 _B Open-load detection on half-bridge 1 is enabled 1 _B Open-load detection on half-bridge 1 is disabled

OLD_CTRL_2

The Open Load Detection Control 2 (Address =0x20) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OLD_REP	OLD_OP						
R/W	R/W	R	R	R	R	R	R

Field	Bits	Type	Description
OLD_REP	D7	R/W	0 _B Report on nFAULT pin during OLD condition 1 _B No report on nFAULT pin during OLD condition
OLD_OP	D6	R/W	0 _B Half-bridges are not active after OLD condition detection 1 _B Half-bridges are active after OLD condition detection
Reserved	D5:D0	R	Reserved. Always reads as '0'

OLD_CTRL_3

The Open Load Detection Control 3 (Address =0x21) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OCP_DEG			Reserved				
R/W	R/W	R/W	R	R	R	R	R

Field	Bits	Type	Description
OCP_DEG	D7:D5	R/W	000 _B OCP deglitch time is 10μs 001 _B OCP deglitch time is 5μs 010 _B OCP deglitch time is 2.5μs 011 _B OCP deglitch time is 1μs 110 _B OCP deglitch time is 30μs 111 _B OCP deglitch time is 20μs
Reserved	D4:D0	R	Reserved. Always reads as '0'

OLD_CTRL_4

The Open Load Detection Control 4 (Address =0x22) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Field	Bits	Type	Description
HB8_LOLD_EN	D7	R/W	HB8 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 8 is disabled 1 _B Low-current OLD detection on half-bridge 8 is enabled
HB7_LOLD_EN	D6	R/W	HB7 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 7 is disabled 1 _B Low-current OLD detection on half-bridge 7 is enabled
HB6_LOLD_EN	D5	R/W	HB6 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 6 is disabled 1 _B Low-current OLD detection on half-bridge 6 is enabled
HB5_LOLD_EN	D4	R/W	HB5 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 5 is disabled 1 _B Low-current OLD detection on half-bridge 5 is enabled
HB4_LOLD_EN	D3	R/W	HB4 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 4 is disabled 1 _B Low-current OLD detection on half-bridge 4 is enabled
HB3_LOLD_EN	D2	R/W	HB3 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 3 is disabled 1 _B Low-current OLD detection on half-bridge 3 is enabled
HB2_LOLD_EN	D1	R/W	HB2 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 2 is disabled 1 _B Low-current OLD detection on half-bridge 2 is enabled
HB1_LOLD_EN	D0	R/W	HB1 low-current OLD detection configuration 0 _B Low-current OLD detection on half-bridge 1 is disabled 1 _B Low-current OLD detection on half-bridge 1 is enabled

Application information

The SA52128B is an eight half-bridge motor driver solution for automotive, industrial, and other mechatronic applications. The half-bridges are fully controllable to achieve a forward, reverse, coasting, and braking motor operation. All functions can be programmed through the serial peripheral interface (SPI).

Design Specification

Input Voltage	Logic Voltage (VDD/EN)	DC Output Maximum Current	PWM Output	Duty Cycle
4.5-32V	3.3-5V	1A per channel	80/100/200/2000Hz	0%~100%

Schematic

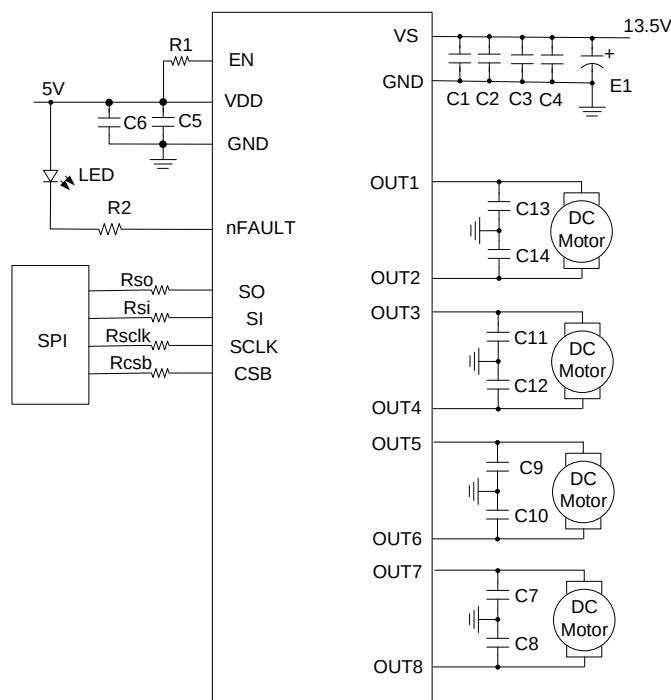


Figure 23. Typical Application Schematic

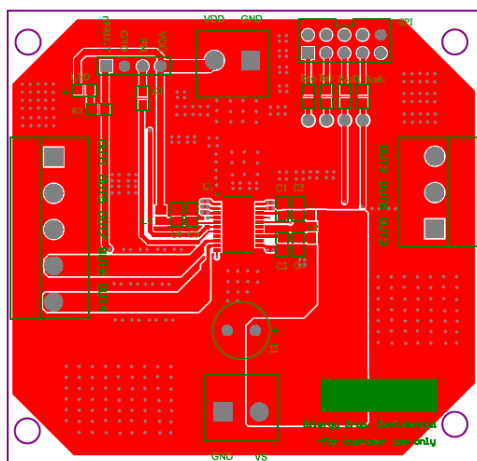
BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	TSSOP24E	SA52128BHHP	Silergy
Rso, Rsclk, Rsi, Rcsb, R1	100Ω, 5%, 0603	RC0603JR-07100RL	YAGEO
R2	10kΩ, 5%, 0603	RC0603JR-0710KRL	YAGEO
E1	100uF/ 50V/E-CAP	ERS1HM101F12OT	AISHI
C1, C2,	1nF/50V	C1608NP01H102J	TDK
C3, C4	100nF/50V	C1608X7R1H104K	TDK
C5	1nF/25V	C1608X7R1E102J	TDK
C6	100nF/25V	C1608X7R1E104K	TDK
C7-C14	10nF/50V	C1608NP01H103J	TDK
LED	Green, 0603	XL-1608UGC-04	XINGLIGHT

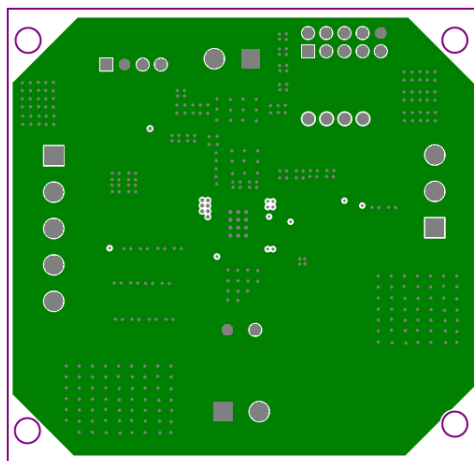
Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

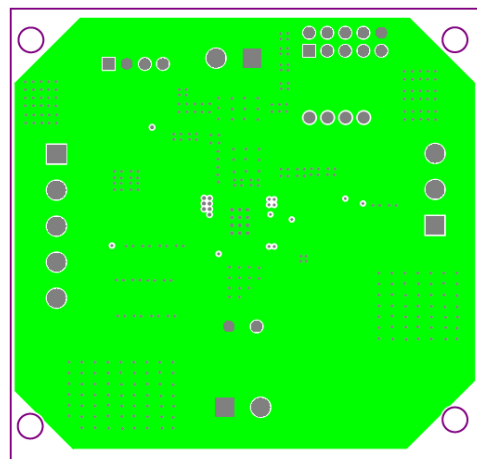
1. Place the large electrolytic capacitors (E1) between VS and GND. It is recommended to use at least 10 μ F capacitance to maintain a stable motor supply voltage.
2. Place the input capacitors (C1, C2, C3, C4, C5, C6) as close as possible to the VS/VDD and GND pins, minimizing the loop formed by these connections. Avoid using direct vias in the power trace between the input capacitors and VS/VDD, GND to reduce parasitic inductances. It is recommended to choose 100pF~1nF for C1/C2, and 100nF~1 μ F for C3/ C4.
3. It is recommended to choose 100pF~1nF for C5, and 100nF~1 μ F for C6.
4. Keep the high current traces (VS, GND, and OUTx traces) as short and wide as possible.
5. Connect the exposed GND pad to a large copper area and place several GND vias to an internal GND plane or the bottom of the board for heat sinking and noise reduction. Maximize the GND copper area to improve power dissipation.



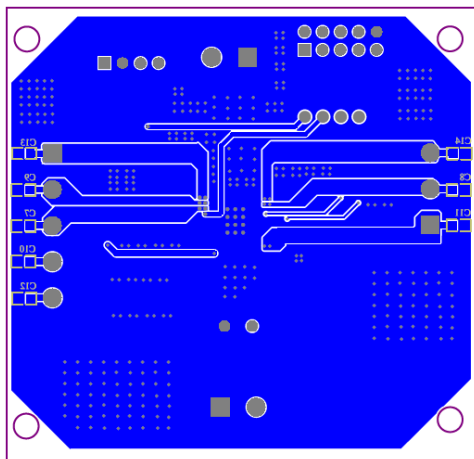
(a) Top Layer



(b) Sig1 Layer



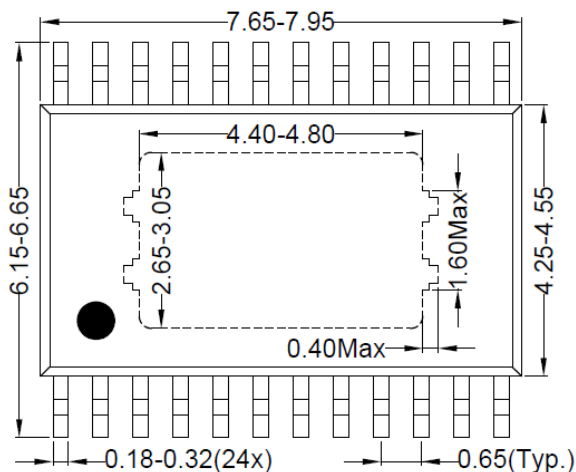
(c) Sig2 Layer



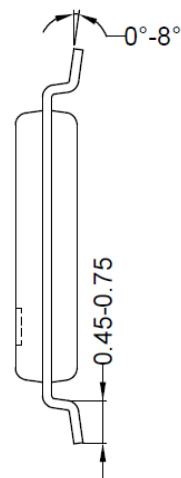
(d) Bottom Layer

Figure 24. PCB Layout Example

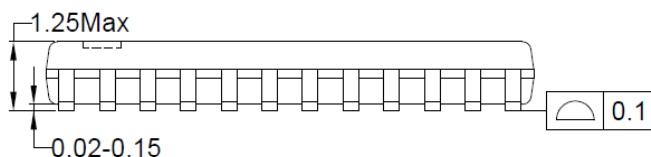
TSSOP24E Package Outline Drawing



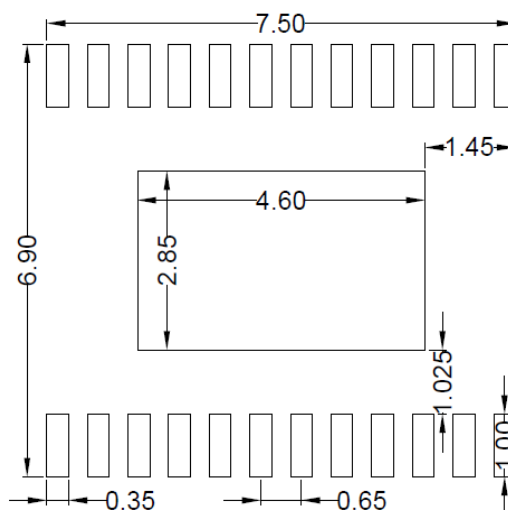
Top View



Side View



Front View

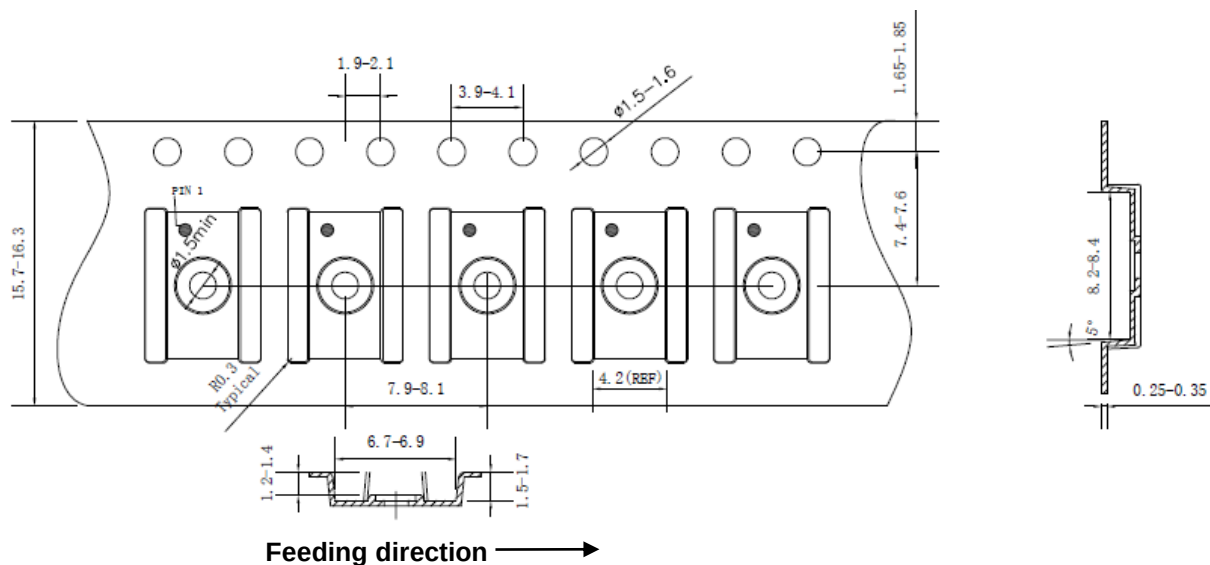


**Recommended PCB Layout
(Reference Only)**

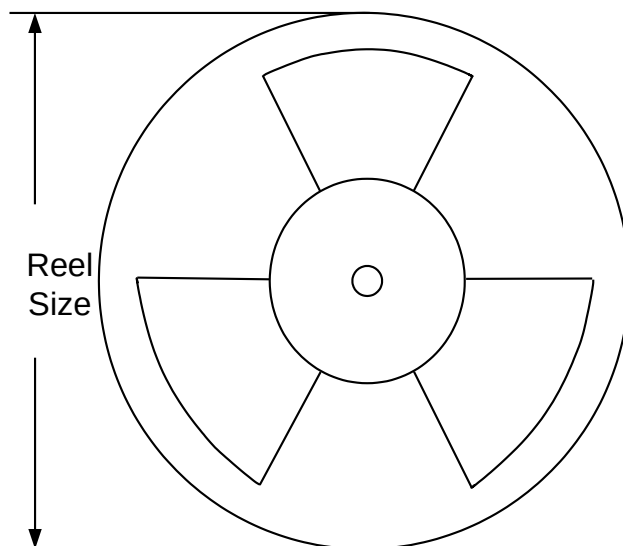
Note: All dimensions are in millimeters and exclude mold flash & metal burr.

Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
TSSOP24E	16	8	13"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Sept. 03, 2025	Initial Release	

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