

### General Description

The SY82852G high-efficiency 3.3V fixed output synchronous buck converter operates over a wide input voltage range of 4.5V to 30V, and can deliver an output current up to 0.6A. It integrates a top MOSFET and a bottom MOSFET with very low  $R_{DS(ON)}$  to minimize conduction loss. The 1100kHz pseudo-constant switching frequency enables using small external inductor and capacitor values.

The SY82852G uses constant on-time and ripple-based control strategy to achieve fast transient response for applications with variable duty cycle, and uses FCCM (Forced Continuous Conduction Mode) light load operation mode. It also provides cycle-by-cycle current limit protection and over temperature protection.

Only the input and output capacitors, inductor need to be selected for the targeted application specifications.

The SY82852G is available in a compact SOT23-6 package.

### Features

- Low  $R_{DS(ON)}$  for Internal MOSFETs: 160mΩ Top, 120mΩ Bottom
- Wide Input Voltage Range: 4.5V ~ 30V
- Up to 0.6A Output Current Capability
- Fixed 3.3V Output Voltage
- Precise EN Threshold
- FCCM Light Load Operation Mode for Small Ripple
- Internal Soft-Start Limits the Inrush Current
- Support Smooth Startup with Pre-Bias Output
- 1100kHz Switching Frequency Minimize the External Components
- Constant On-Time and Advanced Ripple-Based Mode Control Strategy
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection
- Auto Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package SOT23-6
- Moisture Sensitivity Level (MSL): 1

### Applications

- LCD-TV/Net-TV/3D-TV
- Set Top Box
- Notebook
- High Power AP

### Typical Application

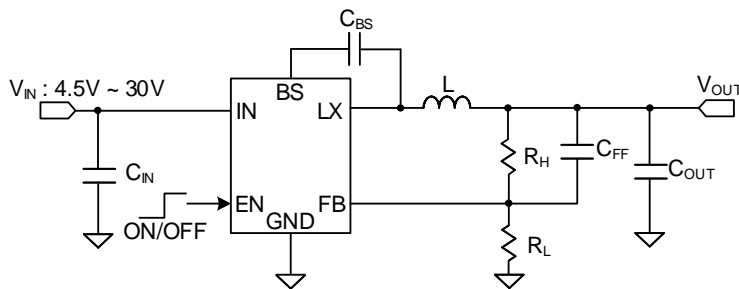


Figure1. Schematic Diagram

Inductor and COUT Selectin Table

V <sub>OUT</sub> [V]	L[μH]	C <sub>OUT</sub> [μF]			
		10	22	32	44
3.3	4.7	√	√	√	√
	6.8	√	☆	√	

Note: '☆' means recommended for most applications.

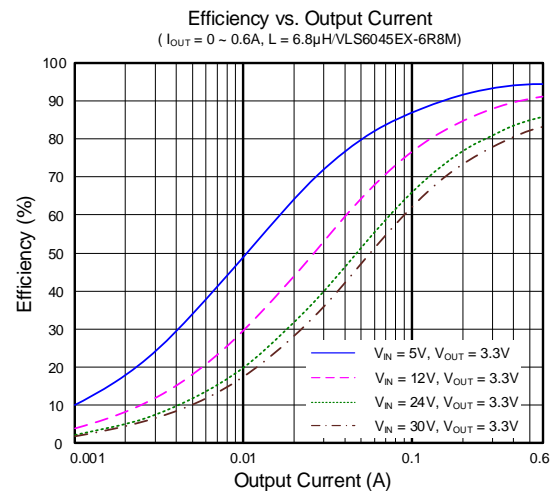


Figure2. Efficiency vs. Output Current

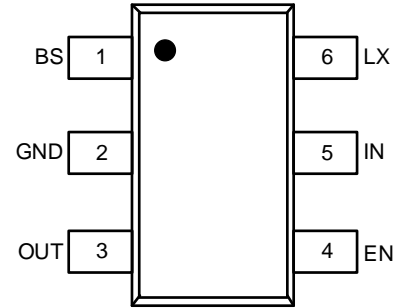


## Ordering Information

Ordering Part Number	Package Type	Top Mark
SY82852GABT	SOT23-6 RoHS Compliant and Halogen Free	HEQxyz

*x = year code, y = week code, z = lot number code*

## Pinout (top view)



## Pin Description

Pin Number	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1 $\mu$ F ceramic capacitor between the BS and the LX pin.
2	GND	Ground pin.
3	OUT	Output feedback pin. Connect this pin to the output capacitor of buck converter.
4	EN	Enable pin. Pull this pin higher than EN rising threshold to turn on the device and pull this pin lower than EN falling threshold to turn off the device. Do not leave this pin floating.
5	IN	Input pin. Decouple this pin from the GND pin with at least a 2.2 $\mu$ F ceramic capacitor.
6	LX	Inductor pin. Connect this pin to the switching node of inductor.



Block Diagram

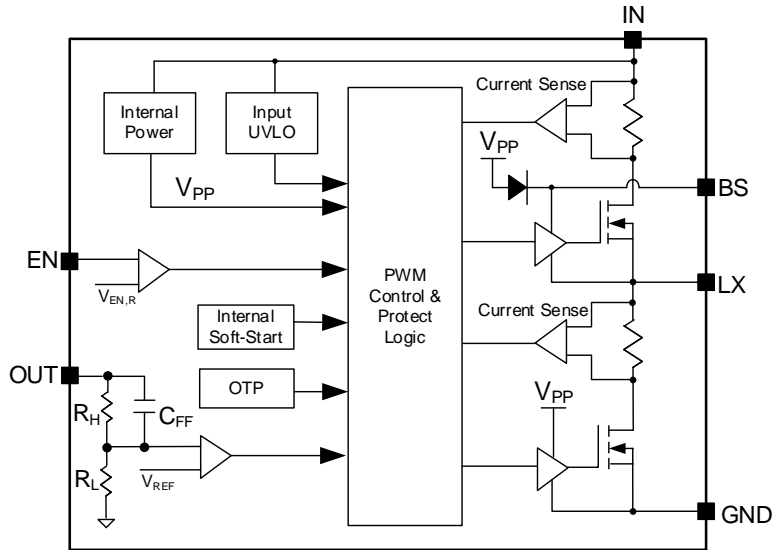


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	32	V
EN, LX	-0.3	IN + 0.3	
OUT, BS-LX	-0.3	4	
LX, 10ns Duration	- 5	IN + 3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
$\theta_{JA}$ Junction-to-Ambient Thermal Resistance	55	°C/W
$\theta_{JC}$ Junction-to-Case Thermal Resistance	6.5	
$P_D$ Power Dissipation $T_A = 25^\circ\text{C}$	1.8	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4.5	30	V
Output Current		0.6	A
Ambient Temperature	-40	85	°C
Junction Temperature Operating	-40	125	



## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 6.8\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_J = 25^\circ C$ ,  $I_{OUT} = 0.6A$  unless otherwise specified (note4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	$V_{IN}$	4.5		30	V
	UVLO Threshold	$V_{UVLO}$	$V_{IN}$ rising		4.45	
	UVLO Hysteresis	$V_{HYS}$		0.3		
	Shutdown Current	$I_{SHDN}$	EN = 0V		9.6	13
Output (OUT)	Voltage Set-point	$V_{SET}$	CCM	3.3		V
	Turn On Delay Time	$t_{ON,DLY}$	from EN high to LX start switching(Note 5)	200		$\mu s$
	Soft-Start Time	tss	$V_{OUT}$ from 0 to 100% $V_{SET}$	1.8		ms
	UVP Threshold	$V_{UVP}$		33		% $V_{SET}$
	UVP Delay Time	$t_{UVP,DLY}$		200		$\mu s$
	UVP Hiccup On-Time	$t_{UVP,ON}$		2		ms
	UVP Hiccup Off-Time	$t_{UVP,OFF}$		15		
Enable (EN)	Rising Threshold	$V_{EN,R}$	1.1	1.23	1.36	V
	Falling Threshold	$V_{EN,F}$	0.95	1.1	1.22	
	Input Current	$I_{EN}$	$V_{EN} = 3.3V$	-1	0	1
MOSFET	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$		160		$m\Omega$
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$		120		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$		1.2		A
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$		0.8		
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$	$T_J = 25^\circ C$	0.5		
$T_J = -40^\circ C \sim 125^\circ C$			0.45		1	
Frequency	Switching Frequency	fsw	$I_{OUT} = 0.6A$		1100	kHz
	Minimum On-Time	$t_{ON,MIN}$		50		ns
	Minimum Off-Time	$t_{OFF,MIN}$		100		
OTP	Temperature	$T_{OTP}$	(Note 5)	150		$^\circ C$
	Temperature Hysteresis	$T_{HYS}$	(Note 5)	15		

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a 6cmx6cm size, two-layer Silergy Evaluation Board with 2-oz copper. Pin 6 of SOT23-6 package is the case position for  $\theta_{JC}$  measurement.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

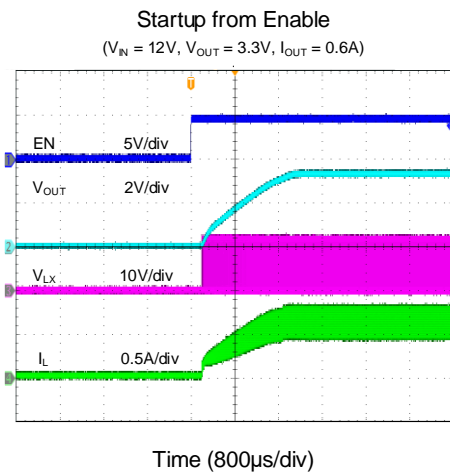
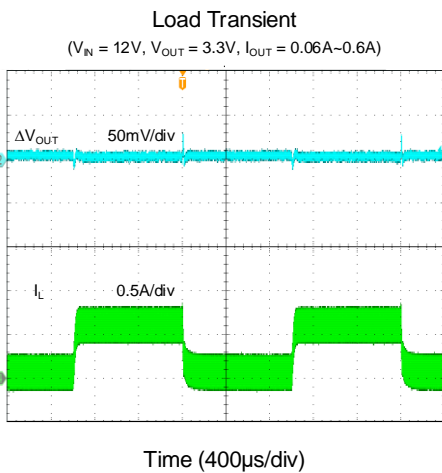
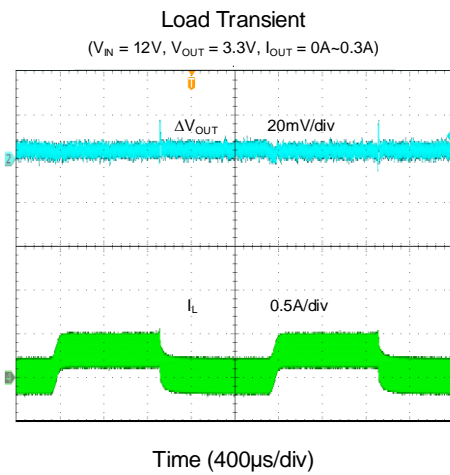
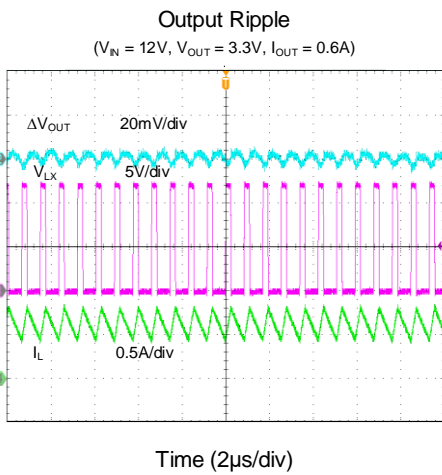
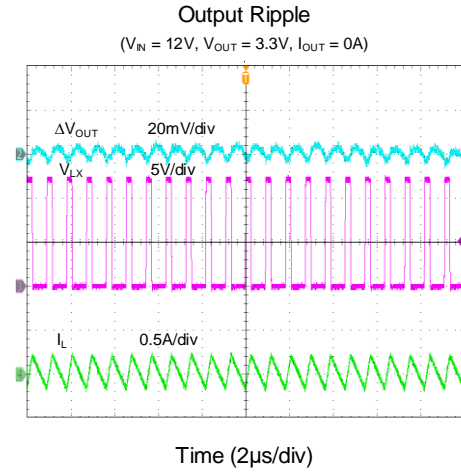
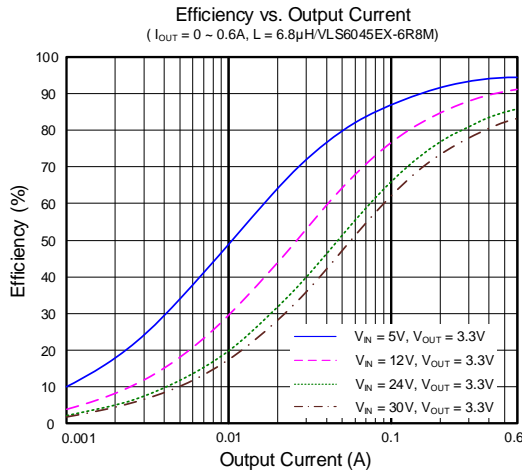
**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that  $T_A \cong T_J = 25^\circ C$ . Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

**Note 5:** Guaranteed by design or statistical correlation and not production tested.

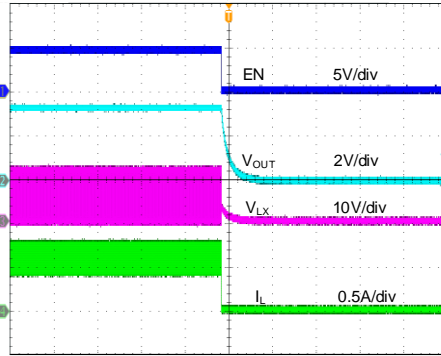


## Typical Performance Characteristics

( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 3.3\text{V}$ ,  $L = 6.8\mu\text{H}$ ,  $C_{OUT} = 22\mu\text{F}$ , unless otherwise noted)

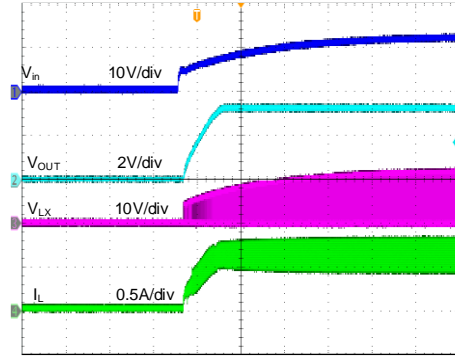


**Shutdown from Enable**  
 $(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.6A)$



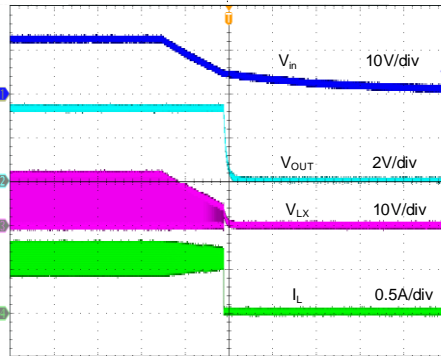
Time (800 $\mu$ s/div)

**Startup from  $V_{IN}$**   
 $(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.6A)$



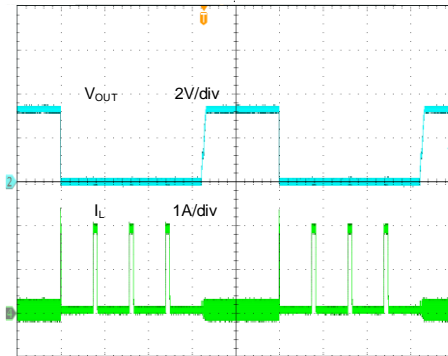
Time (2ms/div)

**Shutdown from  $V_{IN}$**   
 $(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.6A)$



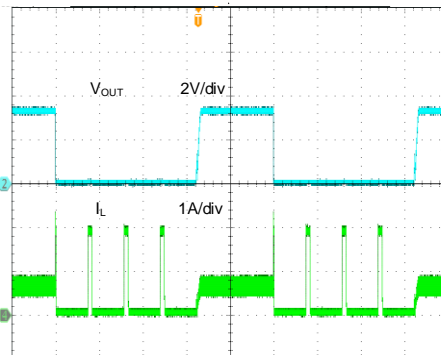
Time (2ms/div)

**Short Circuit Protection**  
 $(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A\text{-short})$



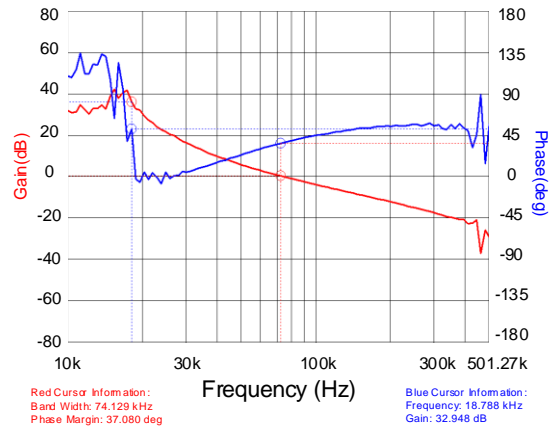
Time (20ms/div)

**Short Circuit Protection**  
 $(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.6A\text{-short})$



Time (20ms/div)

**Bode Plot**  
 $(V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0.6A)$





## Detailed Description

### General Description

The SY82852G high efficiency 1100kHz synchronous buck converter operates over a wide input voltage range of 4.5V to 30V, and can deliver an output current up to 0.6A. It integrates a top MOSFET and a bottom MOSFET with very low  $R_{DS(ON)}$  to minimize conduction loss. The 1100kHz pseudo-constant switching frequency allows small external inductor and capacitor values.

The SY82852G also provides cycle-by-cycle current limit protection, output under voltage protection and over temperature protection.

### Constant On-Time and Ripple-Based Control Strategy

The SY82852G uses instant PWM architecture to achieve fast transient response for applications with high step-down ratios, and high efficiency at light loads. It uses a constant on-time and ripple-based control strategy in which a virtual replica of the inductor current signal is synthesized internally and combined with the feedback voltage. When the sum voltage is lower than the reference voltage, the bottom MOSFET turns off and the top MOSFET turns on for a fixed period of time (Constant  $t_{ON}$ ).  $t_{ON}$  is internally calculated according to the input voltage, output voltage, and desired switching frequency ( $f_{sw}$ ):

$$t_{ON} = \frac{V_{OUT} / V_{IN}}{f_{SW}}$$

The top MOSFET turns off after a period of  $t_{ON}$ .

### Minimum and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

The device can support a maximum duty cycle of up to 74% across the entire operating temperature range of -40°C ~ 125°C.

### Light Load Operation

The device uses forced continuous conduction mode (FCCM) under light load condition. Under light load conditions, the bottom MOSFET still turns on even when the inductor current crosses zero. Current flow will continue until the next  $t_{ON}$  cycle. The device always operates under continuous conditions mode and keeps fairly constant switching frequency over all the output current range.

### Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection. The SY82852G remains in a low current state and all LX node switching actions are inhibited until  $V_{IN}$  exceeds its rising threshold. At that time, if EN is enabled, the device will startup. If  $V_{IN}$  falls below  $V_{IN,UVLO}$  less than the input UVLO hysteresis, the LX node switching actions will again be suppressed.

### Precise EN Threshold

The EN pin uses precise rising and falling thresholds to provide programmable ON/OFF control. The device will be turned on when the EN pin voltage exceeds the rising threshold. The device will be turned off while the EN pin voltage falls below the falling threshold. Increasing the input UVLO threshold is possible using an external resistor divider as shown below:

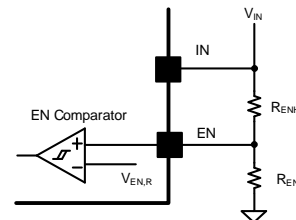


Figure4. Enable Control

It is not recommended to connect EN pin to the  $V_{IN}$  or another voltage source directly. A resistor with a value between 1kΩ and 1MΩ is recommended if the EN pin is pulled high.

### Soft-Start and Startup with Pre-Biased Output

The device incorporates an internal soft-start circuit to ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1.8ms, which avoids high current flow and transients during startup.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage  $V_{SS}$  exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

### External Bootstrap Capacitor

The external bootstrap capacitor provides the gate driver voltage for the N-channel top MOSFET. A 0.1μF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

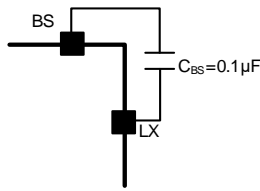


Figure5. Bootstrap Capacitor Connection

## Fault Protection Modes

### Cycle-by-Cycle Current Limit Protection

If the top MOSFET current exceeds the top current limit threshold, it will turn off and the bottom MOSFET will turn on. If the bottom MOSFET current exceeds the bottom current limit threshold, it will stay on until the current decreases below its current limit threshold. As a result, both inductor peak and valley currents are limited.

### Output Under Voltage Protection (UVP)

With output current increasing, as soon as the bottom MOSFET current exceeds its current limit threshold, the top MOSFET will not be allowed to turn on any more. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 33% of the regulated level, the output under voltage protection will be activated and the device will operate in hiccup mode. The hiccup on-time is 2ms, and the hiccup off-time is 15ms. If the hard short condition is removed, the device will return to normal operation.

### Over Temperature Protection (OTP)

The device includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature is reduced by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

## Application Information

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

### Input Capacitor C<sub>IN</sub>

For the best performance, select a typical X5R or better grade ceramic capacitor with a 50V rating, and at least 10µF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C<sub>IN</sub> and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of

the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for most applications.

### Output Inductor L

Consider the following when choosing this inductor:

- 1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT} (1 - V_{OUT} / V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 0.4}$$

Where, f<sub>sw</sub> is the switching frequency and I<sub>OUT,MAX</sub> is

the maximum load current.

The SY82852G has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- For FCCM mode converter, in order to avoid the Reverse Current Limit (0.5A min) being triggered at open load condition, when choosing the inductance, we have to make sure the 1/2 inductor ripple current ( $\Delta I$ ) is smaller than the Reverse Current Limit threshold. Otherwise the output voltage will be charged to higher value. The 1/2 inductor ripple current is calculated as:

$$\frac{1}{2} \Delta I = \frac{V_{OUT}(V_{IN} - V_{OUT})}{2 \times L \times f_{SW} \times V_{IN}} \leq 0.5$$

Where  $f_{sw}$  is the switching frequency and 0.5 is Bottom FET Reverse Current Limit. So the inductance can be calculated as:

$$L \geq \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW}}$$

- The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor

with DCR less than 50m $\Omega$  to achieve good overall efficiency.

### Output Capacitor $C_{OUT}$

Select the output capacitor  $C_{OUT}$  to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting  $C_{OUT}$ . For the best performance, use a X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10 $\mu$ F.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple ( $\Delta I_L$ ) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.



Application Schematic (V<sub>OUT</sub>=3.3V)

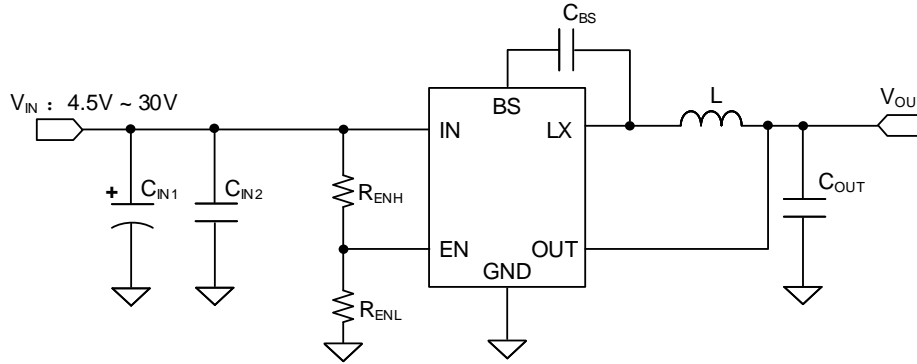


Figure6. Schematic Diagram

BOM List

Reference Designator	Description	Part Number	Manufacturer
C <sub>IN1</sub>	47µF/50V Electrolytic Capacitor		
C <sub>IN2</sub>	10µF/50V//X5R, 1206	GRM31CR61H106KA12L	Murata
C <sub>OUT</sub>	22µF/16V//X5R, 1206	GRM31CR61C226ME15L	Murata
C <sub>BS</sub>	0.1µF/50V//X5R, 0603	GRM188R61H104KA93D	Murata
L	6.8µH/inductor,4.7A	VLS6045EX-6R8M	TDK
R <sub>ENH</sub>	10kΩ, 1%, 0603		
R <sub>ENL</sub>	1MΩ, 1%, 0603		



## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

**Input Capacitors:** Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND pins using a wide copper area.

**Output Capacitors:** Connect the  $C_{OUT}$  negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.

**LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

**BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and  $C_{BS}$ ) as short as possible.

**EN Signal:** It is not recommended to connect EN pin directly to  $V_{IN}$  or another voltage source. A resistor in a range of  $1k\Omega$  to  $1M\Omega$  should be used if EN pin is pulled high.

**GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.

**PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if possible. Connect the ground pad to a large copper area to enhance thermal performance.

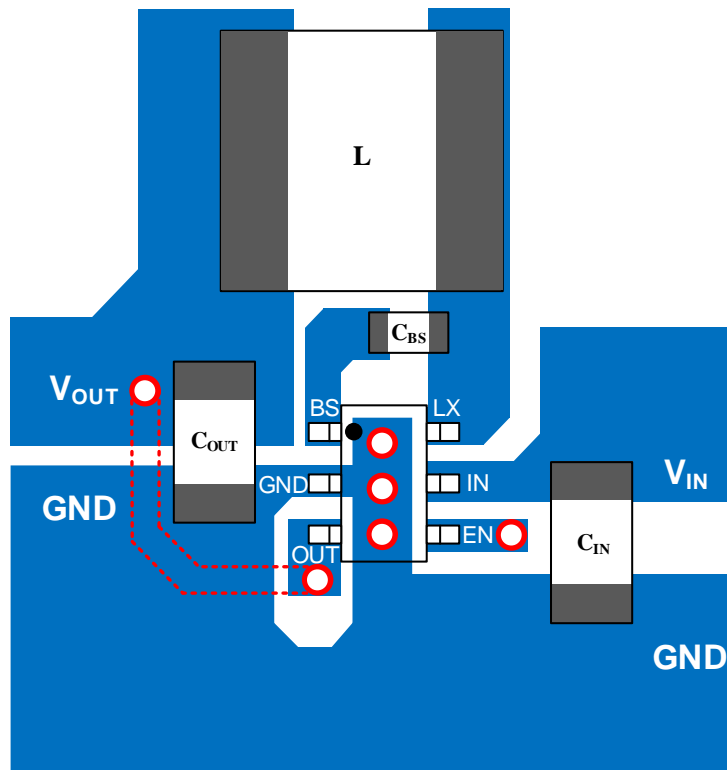
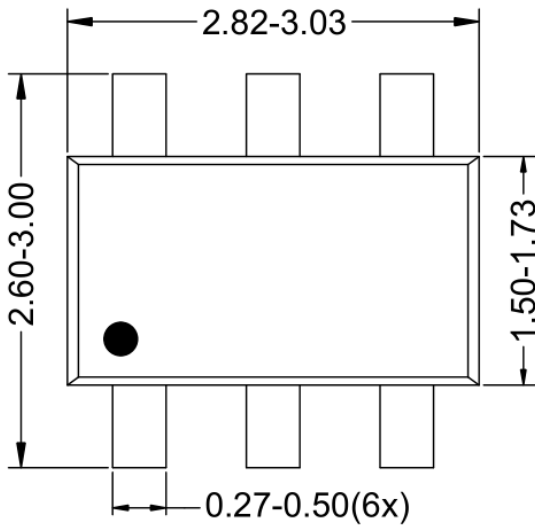
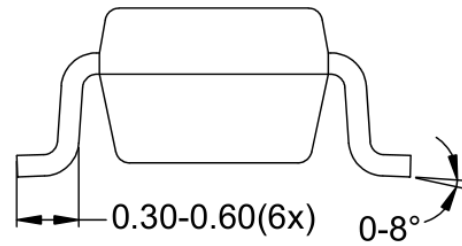


Figure 7. Suggested PCB Layout

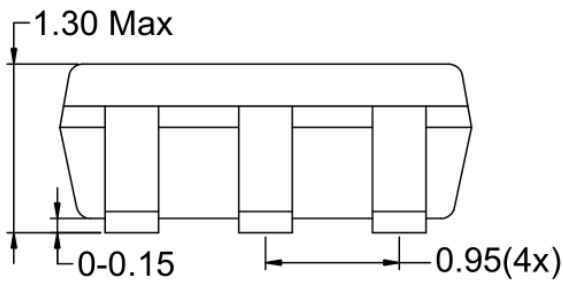
## SOT23-6 Package Outline & PCB layout



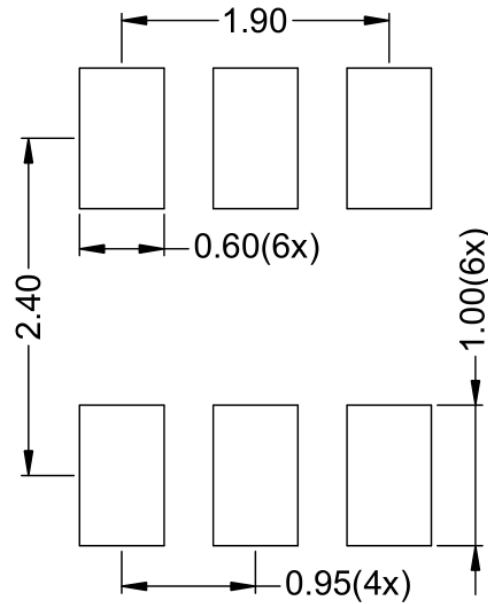
**Top View**



**Side View**



**Front View**

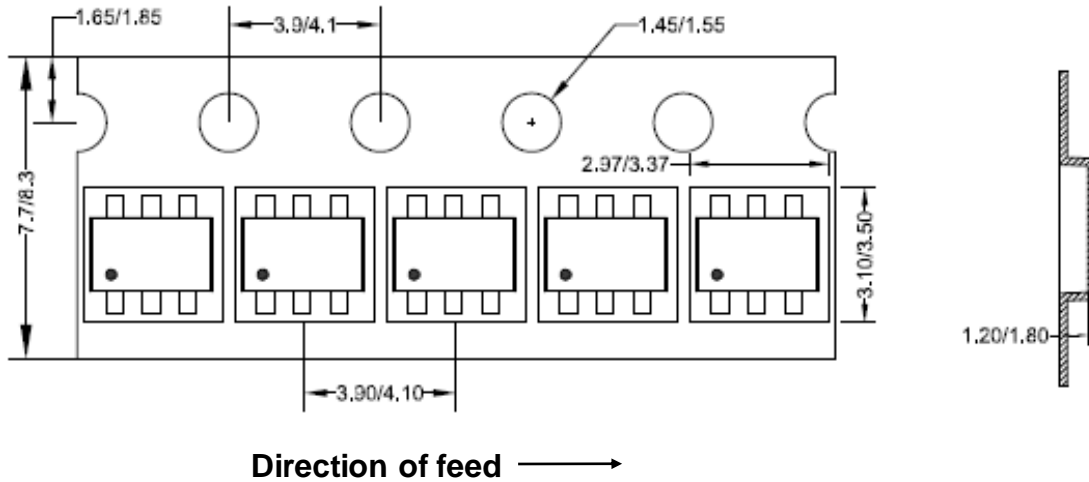


**Recommended PCB Layout**

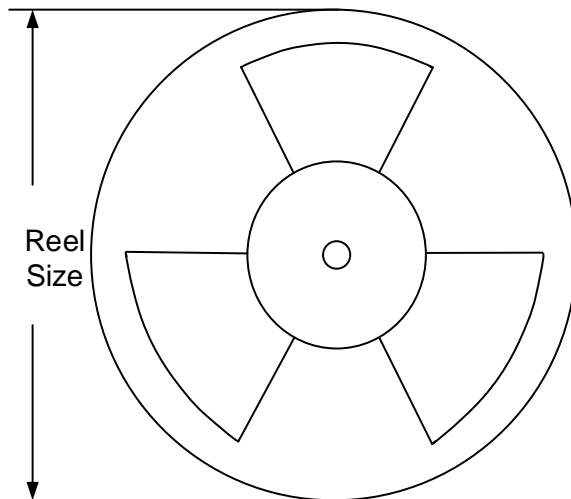
**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Taping & Reel Specification

### 1. Taping orientation for package



### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7	280	160	3000



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## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Sep.17,2025	1.0	Initial Release	-

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